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[Continued on next page]

(54) **Title**: LEADFRAME FOR ELECTRONIC SYSTEM HAVING VERTICALLY STACKED CHIPS AND COMPONENTS

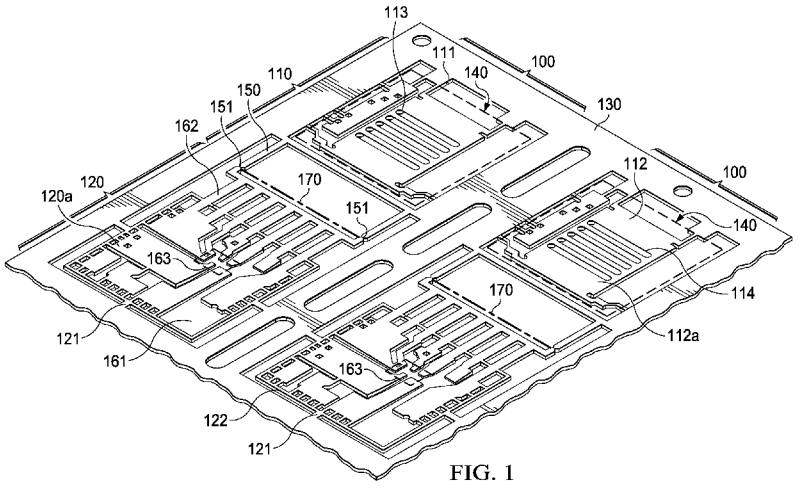

FIG. 1

(57) **Abstract**: In described examples, a leadframe (100) for electronic systems includes a first sub-leadframe (110) connected by links (150) to a second sub-leadframe (120). The first and second sub-leadframes (110, 120) are connected by tiebars (111, 121) to a frame (130). Each link (150) has a neck (151) suitable for bending the link (150). The necks (151) are arrayed in a line (170) operable as an axis for bending the second sub-leadframe (120) towards the first sub-leadframe (110), with the necks (151) being operable as rotation pivots.

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— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

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— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

LEADFRAME FOR ELECTRONIC SYSTEM HAVING VERTICALLY STACKED CHIPS AND COMPONENTS

[0001] This relates generally to semiconductor devices and processes, and more particularly to a structure and fabrication method of packaged electronic systems having multiple leadframes, vertically stacked by folding, together with semiconductor chips and passive components.

BACKGROUND

[0002] Driven by the desire to reduce the board area needed to assemble a semiconductor device into electronic products such as hand-held telephones, today's semiconductor devices often use vertically stacked chips inside the packages. These chip stacks frequently include chips of significantly different sizes, assembled mostly by wire bonding techniques on interposers commonly made of rigid materials such as ceramics or fiber-enforced plastics such as FR-4 and others.

[0003] In applications where a whole system is to be encapsulated into a package, it is desirable to add passive components (such as capacitors, resistors and inductors) to the stacked chips and incorporate the components into the package without unduly complicating the vertical stack. A frequently practiced solution for this integration, especially in power and converter systems, is the use of a first and a second metallic leadframe as a means for providing simultaneously the benefit for a significantly higher number of inputs/outputs, for freedom of choosing chips of different sizes and rerouting needs, for higher reliability based on reduced stress on the contact joints and on low-k dielectrics in the chips, and on reduced package warpage, and for reduced package thickness due to avoidance of wire bonding.

[0004] When the assembly of the system involves two leadframes sequentially, the process flow needs to pay attention to careful alignment of the second leadframe with the first leadframe – a process which involves a lot of manual handling and control of coplanarity. As an example, in some devices the first leadframe for signal connection involves a high number of leads connected to the chip terminals by a dense array of bonding wires; the signal connections are aligned along two opposite sides of the semiconductor chip. Also, the power supply is provided by a second leadframe involving a low number of leads, but requiring broad geometry. The power leads are preferably attached by solder balls to the chip and require carful positioning

along the remaining two chip sides.

SUMMARY

[0005] In described examples, a first sub-leadframe is connected by links to a second sub-leadframe, so that each link has a neck suitable for bending the link. The necks of adjacent links are arrayed in a line operable as an axis for bending the second sub-leadframe towards the first sub-leadframe, with the necks being operable as rotation pivots.

[0006] For packaged electronic systems, the first sub-leadframe may include a pad suitable as substrate of an electronic system. The pad may have through-holes extending into grooves across the pad surface. In an encapsulation process, packaging material can be pressed through the through-holes and grooves to fill the space between the first and the folded second sub-leadframe with insulating material.

[0007] The second sub-leadframe may include leads having wide portions in an area approximately matching the area of the pad, and narrow portions outside the matched area. In the assembly process flow of an electronic system, the second sub-leadframe is folded at the bendable necks so that the second sub-leadframe is rotated around the axis until the second sub-leadframe is aligned on top of the first sub-leadframe and spaced form the first sub=leadframe by a gap. One or more semiconductor chips are disposed between the leads and the pad; and one or more passive components can be attached to the surface of the leads facing away from the chips.

[0008] The folded sub-leadframes, together with the attached passive components, can be encapsulated in a packaging compound.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. 1 illustrates a perspective view of multiple leadframes, each having a first and a second sub-leadframe connected by links having a neck suitable for bending the link according to example embodiments.

[0010] FIG. 2 shows a top view of a leadframe strip including multiple leadframes with first and second sub-leadframes.

[0011] FIG. 3 depicts a perspective view of a leadframe in the process of attaching a semiconductor chip onto the leads of the second sub-leadframe.

[0012] FIG. 4 illustrates the process of folding the second sub-leadframe at the bendable necks to rotate the second sub-leadframe around the axis formed by the aligned necks, until the second

sub-leadframe is on top of the first sub-leadframe and spaced from it by a gap.

[0013] FIG. 5 shows the process of attaching passive components to the second sub-leadframe on the surface facing away from the first sub-leadframe.

[0014] FIG. 6 depicts the process of encapsulating the folded sub-leadframes together with the attached passive components in a packaging compound.

[0015] FIG. 7A illustrates a perspective top view of a discrete packaged system after the processes of trimming the first and second sub-leadframes and forming the un-encapsulated leads.

[0016] FIG. 7B depicts a perspective bottom view of a discrete packaged system.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0017] In conventional semiconductor manufacturing, the advantage of using two leadframes on semiconductor devices with needs for high density stacking is frequently offset by the disadvantage of excessive manual handling, difficult alignments, and hard-to-control coplanarity. Difficulties of achieving compactness and avoiding misalignment and solder reflow limitations are compiled when passive components have to be merged in close proximity to active chips.

[0018] In example embodiments, the problems of assembling two separate leadframes with the associate mating process are solved by a methodology for constructing and processing a single leadframe, which combines both leadframes in an arrangement, so that the second leadframe can be rotated and effortlessly aligned relative to the first leadframe.

[0019] FIG. 1 shows an example embodiment of a leadframe 100. For cost-effective manufacturing and enabling batch-processing, it is practical to start with a leadframe strip 200 as shown in FIG. 2, which includes multiple leadframes 100. Leadframe strip 200 is stamped or etched from a flat sheet of metal selected from a group including copper, copper alloys, aluminum, iron-nickel alloys, and Kovar™. When the metal sheet is made of copper, the preferred thickness of the sheet is between 100 and 300 μm. For some applications, the sheet may be thicker or thinner. The metal sheet has a first surface and an opposite second surface. In FIGs. 1 and 2, the first surface is depicted and the opposite second surface is nor shown. The metallurgical preparation of the second surface may be the same as the first surface, or it may be different. As an example, one surface, or at least a portion of the surface, may be prepared for facilitating solder attachment; or may be prepared for enhancing adhesion to polymeric compounds.

[0020] Generally, leadframe 100 is intended for an electronic system. The system may include at least one active semiconductor chip and one or more passive components. Consequently, the leadframe feature include elements for assembling and supporting semiconductor chips and for assembling and supporting component, as well as interconnecting leads within the leadframe and to external parts, and supporting rails for stability and handling.

[0021] Referring now to the embodiment of FIG. 1, each leadframe 100 includes two sub-leadframes 110 and 120. Herein, sub-leadframe 110 is called first sub-leadframe, and sub-leadframe 120 is called second sub-leadframe. FIG. 1 indicates that first sub-leadframe 110 and second sub-leadframe 120 are connected by tiebars 111 and 121, respectively, to frame 130. Especially tiebars 121 are mechanically weak to allow an easy trimming process. Also, sub-leadframe 120 is surrounded by dambars 122 for encapsulation control. For explanatory purpose, FIG. 1 includes the outline of the encapsulating package of the finished product.

[0022] As FIG. 1 illustrates, first sub-leadframe 110 is connected to second sub-leadframe 120 by a couple of links 150; in other embodiments, there may be more than two links. Each link 150 has a narrow neck 151, which is suitable for allowing easy bending of the link. The necks of adjacent links are arrayed in a line 170, which is operable as the axis for bending the second sub-leadframe 120 towards the first sub-leadframe 110 in the assembly process described below, so the necks 151 operate as rotation pivots.

[0023] For the electronic system realized by the example embodiment of FIG. 1, first sub-leadframe 110 includes a pad 112 suitable as substrate of the electronic system. FIG. 1 shows the first surfaced 112a of pad 112. For the purposes of electrically grounding the system and of dissipating the operational heat, pad 112 is preferably intended to be exposed from the encapsulating package. Consequently, second surface 112b (not shown in FIG. 1) has a metallurgical configuration to enhance solderability, such as a surface layer of nickel followed by a layer of palladium (and a layer of gold).

[0024] In FIG. 1, pad 112 further includes through-holes 113, which extend into elongated grooves 114 across first surface 112a. The through-holes and the grooves are suitable for channeling a viscous encapsulation compound. In the encapsulation process (see below), the semi-liquid encapsulation compound is pressured from surface 112b through the holes 113 to surface 112a, where the compound can form an insulating layer between the folded first and second sub-leadframes.

[0025] For the electronic system realized in the example embodiment of FIG. 1, second sub-leadframe 120 includes a set of leads, which have wide portions 161 in an area outlined by dashed lines 140, and narrow portions 162 outside the matched area. The area of the wide portion 161 may substantially coincide with the area of pad 112 of the first sub-leadframe. It may be advantageous for the assembly of some embodiments, when some spots 163 of the wide lead portions 161 have recesses relative to first surface 120a; such recesses may facilitate the attachment of semiconductor chip terminals, preferably with the help of solder balls. Sometimes these recesses 163 are referred to as first recesses. Also, the wide portions of some leads may have recesses relative to the second surface (not shown in FIG. 1; see however FIGs. 4 and 5); such recess may facilitate the attachment of passive components. Sometimes these recesses are referred to as second recesses. Furthermore, it may be advantageous for assembling electronic systems when the first and the second recesses of the wide lead portions have a metallurgical configuration suitable for solder attachment.

[0026] Another embodiment is a method for assembling an electronic system. The method starts by the process of providing a leadframe strip, such as example strip 200 of FIG. 2. The strip has a first surface 200a and an opposite second surface (not shown in FIG. 2). The strip includes multiple assembly sites 201. Each site 201 includes a leadframe 230, which holds a pair of sub-leadframes 210 and 220 by tiebars 211 and 221, respectively.

[0027] First sub-leadframe 210 is connected by links 250 to second sub-leadframe 220. Each link 250 of the pair has a neck 251 suitable for bending the link. The necks 251 of adjacent links are arrayed in a line 270 operable as the axis for bending the second sub-leadframe 220 towards the first sub-leadframe 210 with the necks 251 operable as rotation pivots.

[0028] The example leadframes depicted in strip 200 of FIG. 2 are for an example electronic system analogous to the system described in FIG. 1. Thus, the structure of the first sub-leadframe 210 includes a pad 212 suitable as substrate of the electronic system. As mentioned above, it may be advantageous for many systems that pad 212 includes through-holes, which extend into elongated grooves across the first surface of the pad. These through-holes and the grooves are suitable for channeling a viscous encapsulation compound so that an insulating layer between the folded first and second sub-leadframes can be formed.

[0029] The second sub-leadframe 220 includes leads with wide portions 261 of various configurations in an area approximately matching the area of pad 212, and narrow portions 262

outside the matched area; after the packaging process, the narrow lead portions are operable to connect the packaged system to external parts.

[0030] The next process is indicated in FIG. 3. A semiconductor chip 301 with terminals is selected. The terminals are connected to the first surface of spots of leads 261, which belong to the wide portion of the leads. These spots may have a suitable recess or a specific metallurgy, such as an enhanced affinity to solder attachment (such as thin layers of nickel and palladium), which facilitates the connection to the chip terminals.

[0031] In the next process, shown in FIG. 4, the tiebars 221, which connect sub-leadframe 220 to frame 230, are trimmed so that sub-leadframe 230 becomes movable. Then, the second sub-leadframe 220 is folded at the bendable necks 251 to rotate the second sub-leadframe around the axis constituted by the line 270 running through the necks of adjacent links, until second sub-leadframe 220 is aligned on top of first sub-leadframe 210. In this aligned position, second sub-leadframe 220 is spaced from first sub-leadframe 210 by a gap, while the side of semiconductor chip 301 opposite the attached chip terminals touches the first surface of pad 212. In FIG. 4, the second surface of sub-leadframe 220 is visible and is therefore obscuring the view of the gap and chip 301 disposed between the first and second sub-leadframes.

[0032] FIG. 5 illustrates the next process of attaching one or more discrete components 500 onto the second surface 220b of the second sub-leadframe. The attachment process can be facilitated when the second surface 220b has recesses for the components, and when the recesses further have a surface metallurgy enhancing solder adhesion. For copper leadframes, an example is offered by thin layers of nickel, palladium, and gold.

[0033] The next procedure, shown in FIG. 6, is the process of encapsulating the folded sub-leadframes 210 and 220 together with the attached passive components in a packaging compound 600. However, the narrow portions 262 of the leads are left un-encapsulated. A preferred process is the transfer molding of an epoxy-based polymeric packaging compound. During the encapsulation process, the packaging compound propagates through any through-hole and groove of the pad to fill the gap between the first and the second sub-leadframe. In this process, an insulating layer ios formed between the first and second sub-leadframe, except for the chip disposed between the first and second sub-leadframe.

[0034] In the next process, depicted in FIGs. 7A and 7B, the first and second sub-leadframes are trimmed, and concurrently the un-encapsulated leads are formed. Subsequently, the strip is

singulated into discrete packaged electronic systems. FIG. 7A shows a discrete packaged system in perspective top view, and FIG. 7B in perspective bottom view, displaying the second surface of the pad 212 of the first sub-leadframe. Preferably, the second pad surface has a metallurgical configuration for facilitating solder attachment to boards and external parts.

[0035] Another embodiment is a packaged electronic system based on a metallic leadframe. An example embodiment includes a vertical stack, which includes a second sub-leadframe aligned over and insulated from a first sub-leadframe, at least one semiconductor chip disposed between the first and second sub-leadframe, and one or more on top of the second sub-leadframe. In this example system, the first sub-leadframe has a pad suitable to operate as the substrate of the system; as the system substrate, the second surface of the pad preferably has the metallurgical configuration to be solderable to external boards. The second sub-leadframe has leads with narrow and wide portions. Preferably, the wide portions have first recesses facing the pad and second recesses facing away from the pad. The recesses preferably have a metallurgical configuration to be solderable. Other systems may use flat leads shaped like in QFN (quad flat no-lead) and SON (small outline no-lead) devices.

[0036] The at least one chip of the example system is disposed in the space between the first recesses and the pad. The remainder of the space between first and second sub-leadframe is filled with insulating material. A preferred method of filling the space uses multiple holes through the pad to allow ingress of insulating compound during the encapsulation process; the holes feed into an array of grooves across the pad surface so that the compound can spread from the grooves to fill the available space. Discrete components are attached to the second recesses. Topping the vertical stack, the components are in close proximity to the chips, minimizing parasitic resistances and inductances, and they top the second sub-leadframe. The components may include resistors, capacitors and inductances.

[0037] Example embodiments apply to active semiconductor devices with low and high pin counts, such as transistors and integrated circuits, and to combinations of active and passive components on a leadframe pad. Further, example embodiments apply to silicon-based semiconductor devices, and to devices using gallium arsenide, gallium nitride, silicon germanium, and any other semiconductor material employed in industry.

[0038] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A leadframe for electronic systems comprising:

a first sub-leadframe connected by links to a second sub-leadframe, the first and second sub-leadframe connected by tiebars to a frame; and

each link having a neck suitable for bending the link, the necks arrayed in a line operable as the axis for bending the second sub-leadframe towards the first sub-leadframe with the necks operable as rotation pivots.

2. The leadframe of claim 1 wherein the first and second sub-leadframes and the frame are cut from a flat metal sheet having a first surface and an opposite second surface.

3. The leadframe of claim 2 wherein the first sub-leadframe includes a pad suitable as substrate of the electronic system.

4. The leadframe of claim 3 wherein the pad further includes through-holes extending into elongated grooves across the first surface, the through-holes and the grooves suitable for channeling a viscous encapsulation compound.

5. The leadframe of claim 3 wherein the second sub-leadframe includes a set of leads having wide portions in an area approximately matching the area of the pad, and narrow portions outside the matched area.

6. The leadframe of claim 5 wherein the wide portions of the leads have first recesses in the first surface and second recesses in the second surface.

7. The leadframe of claim 6 wherein the first and the second recesses of the leads have a metallurgical configuration suitable for solder attachment.

8. A packaged electronic system comprising:

a vertical stack including a second sub-leadframe aligned over and insulated from a first sub-leadframe, the first sub-leadframe having a pad suitable as substrate of the system, and the second sub-leadframe having leads with narrow and wide portions, the wide portions having first recesses facing the pad, and second recesses facing away from the pad;

a semiconductor chip disposed between the first recesses and the pad;

discrete components attached to the second recesses, topping the second sub-leadframe; and

the vertical stack including the first sub-leadframe, the chip, the second sub-leadframe,

and the components encapsulated in a packaging compound, leaving the leads un-encapsulated.

9. The system of claim 8 wherein the discrete components include passive components such as capacitors, resistors and inductances.

10. The system of claim 8 wherein the insulation between the first and second sub-leadframe derives from packaging compound channeled between the first and second sub-leadframes during the encapsulation process.

11. A method for assembling an electronic system comprising:

providing a leadframe strip having a first and a second surface and a plurality of assembly sites, each site including a leadframe with a pair of a first sub-leadframe connected by links to a second sub-leadframe, the pair connected by tiebars to the frame; each link of the pair having a neck suitable for bending the link, and the necks arrayed in a line operable as the axis for bending the second sub-leadframe towards the first sub-leadframe with the necks operable as rotation pivots; the first sub-leadframe including a pad suitable as substrate of the electronic system; and the second sub-leadframe including leads having wide portions in an area approximately matching the area of the pad, and narrow portions outside the matched area;

attaching the terminals of a semiconductor chip to the first surface of the wide portions of the second sub-leadframe;

trimming the tie-bars to the frame of the second sub-leadframe;

folding the second sub-leadframe at the bendable necks to rotate the second sub-leadframe around the axis until the second sub-leadframe is aligned on top of the first sub-leadframe and spaced from the first sub-leadframe by a gap while the semiconductor chip touches the first surface of the pad; and

attaching discrete components onto the second surface of the second sub-leadframe.

12. The method of claim 11 wherein the pair of sub-leadframes and the frame are made of a flat metal sheet.

13. The method of claim 12 wherein the pad of the first sub-leadframe includes through-holes extending into elongated grooves across the pad surface, the through-holes and the grooves suitable for channeling a viscous encapsulation compound.

14. The method of claim 13 further including the process of encapsulating the folded sub-leadframes together with the attached passive components in a packaging compound, leaving the narrow portions of the leads un-encapsulated.

15. The method of claim 14 wherein the packaging compound propagates through the through-holes and grooves to fill the gap, forming an insulating layer between the first and second sub-leadframe.

16. The method of claim 13 further including the process of trimming the first and second sub-leadframes, the process of forming the un-encapsulated leads, and the process of singulating the strip into discrete packaged electronic systems.

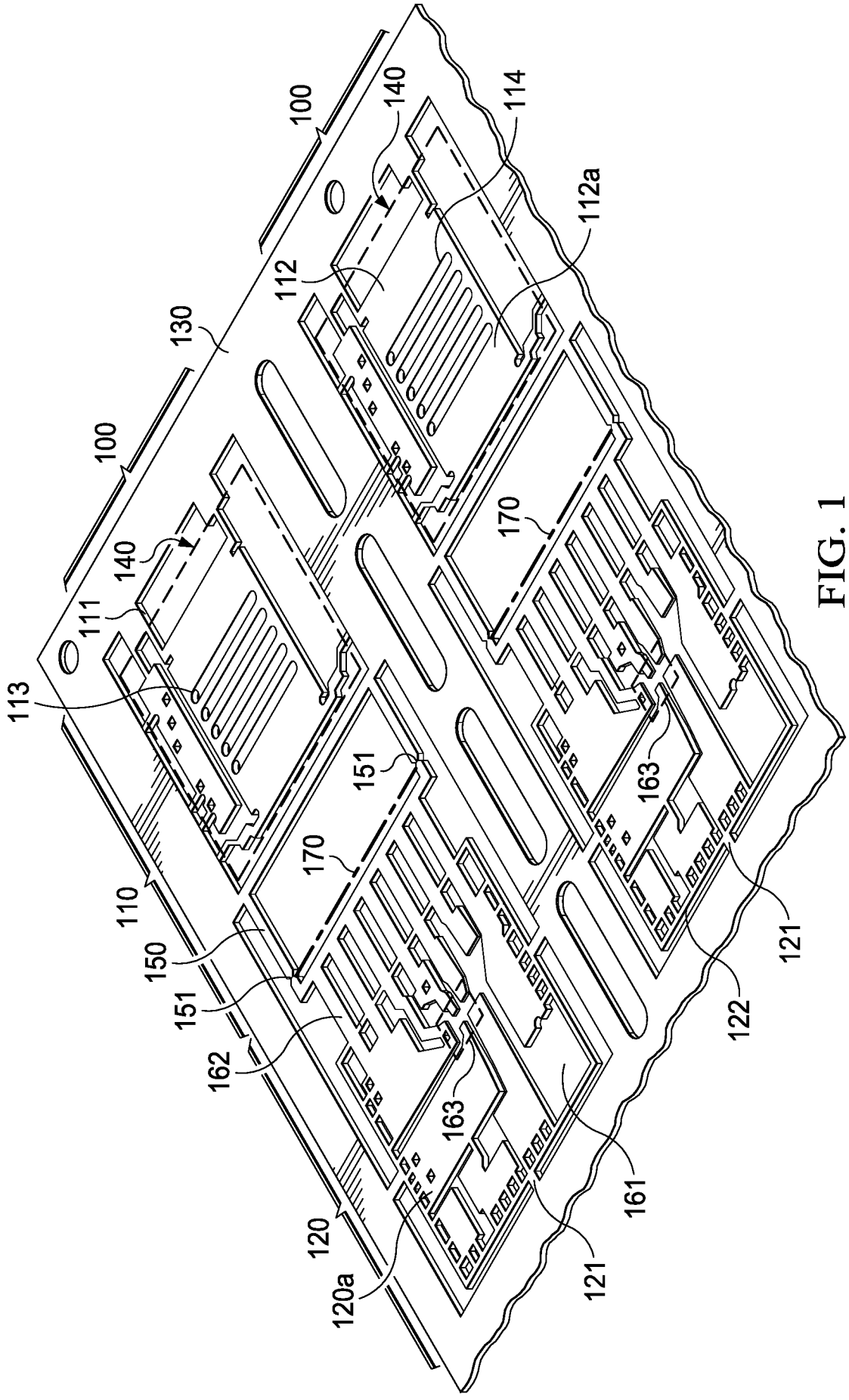
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FIG. 1

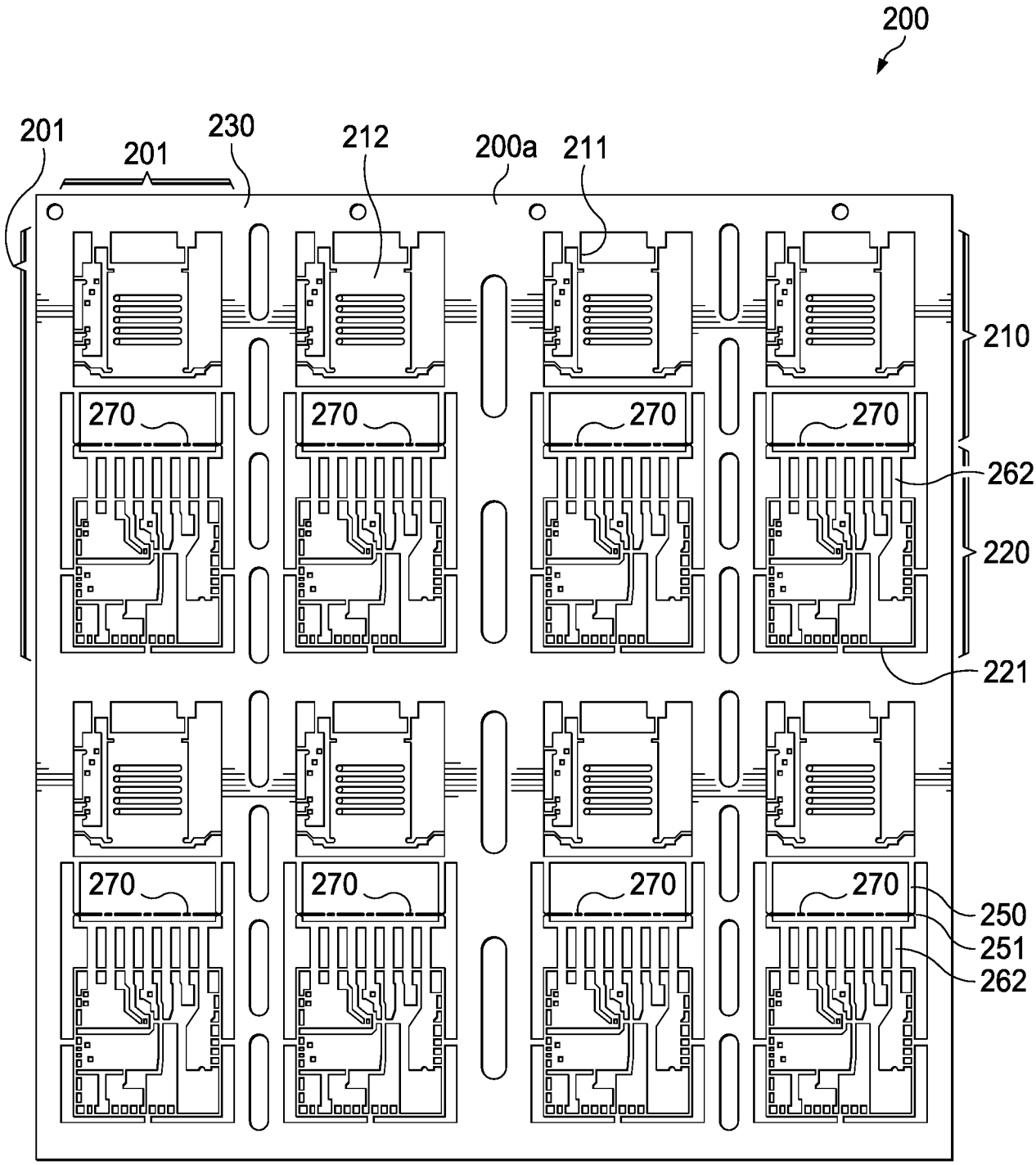
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FIG. 2

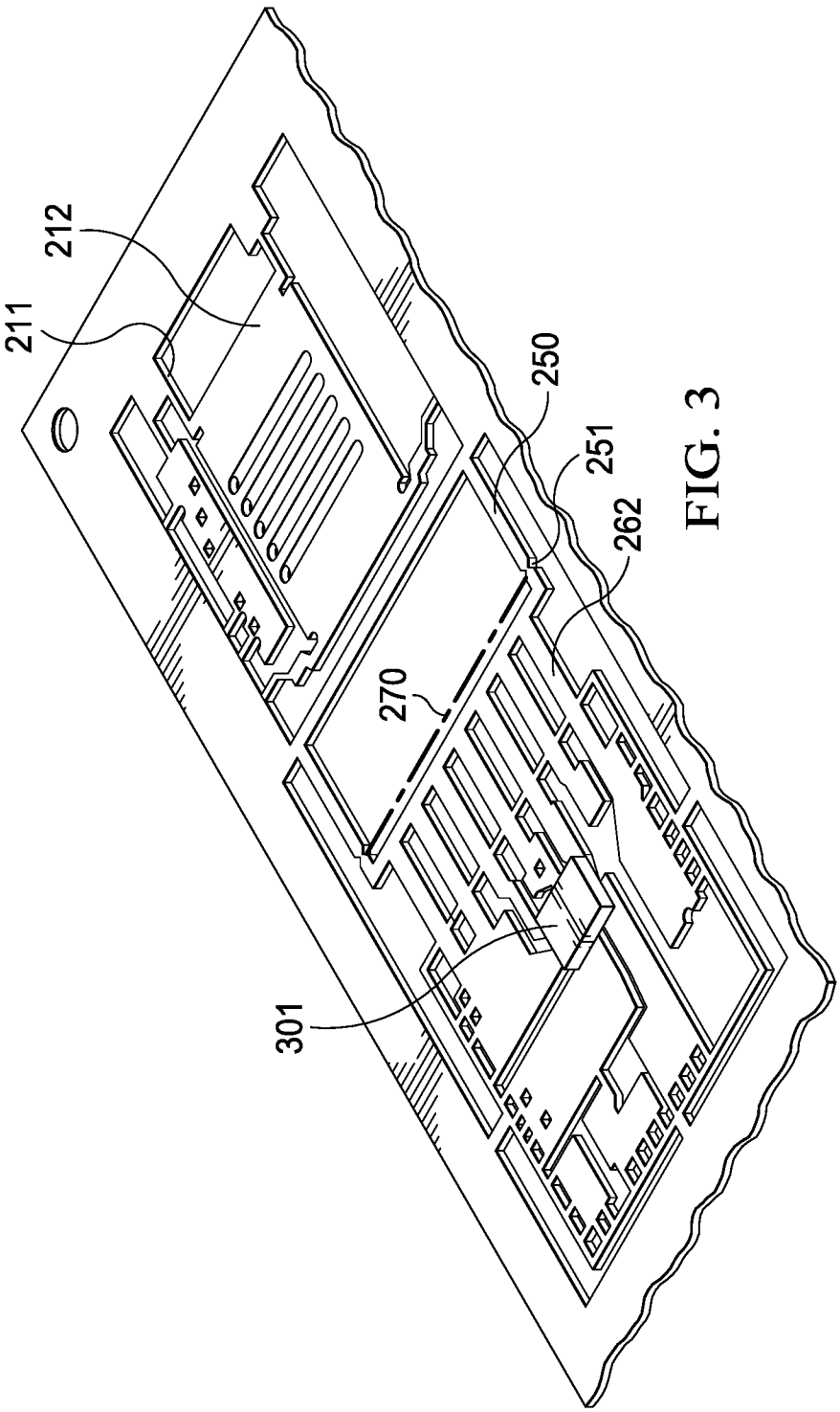

FIG. 3

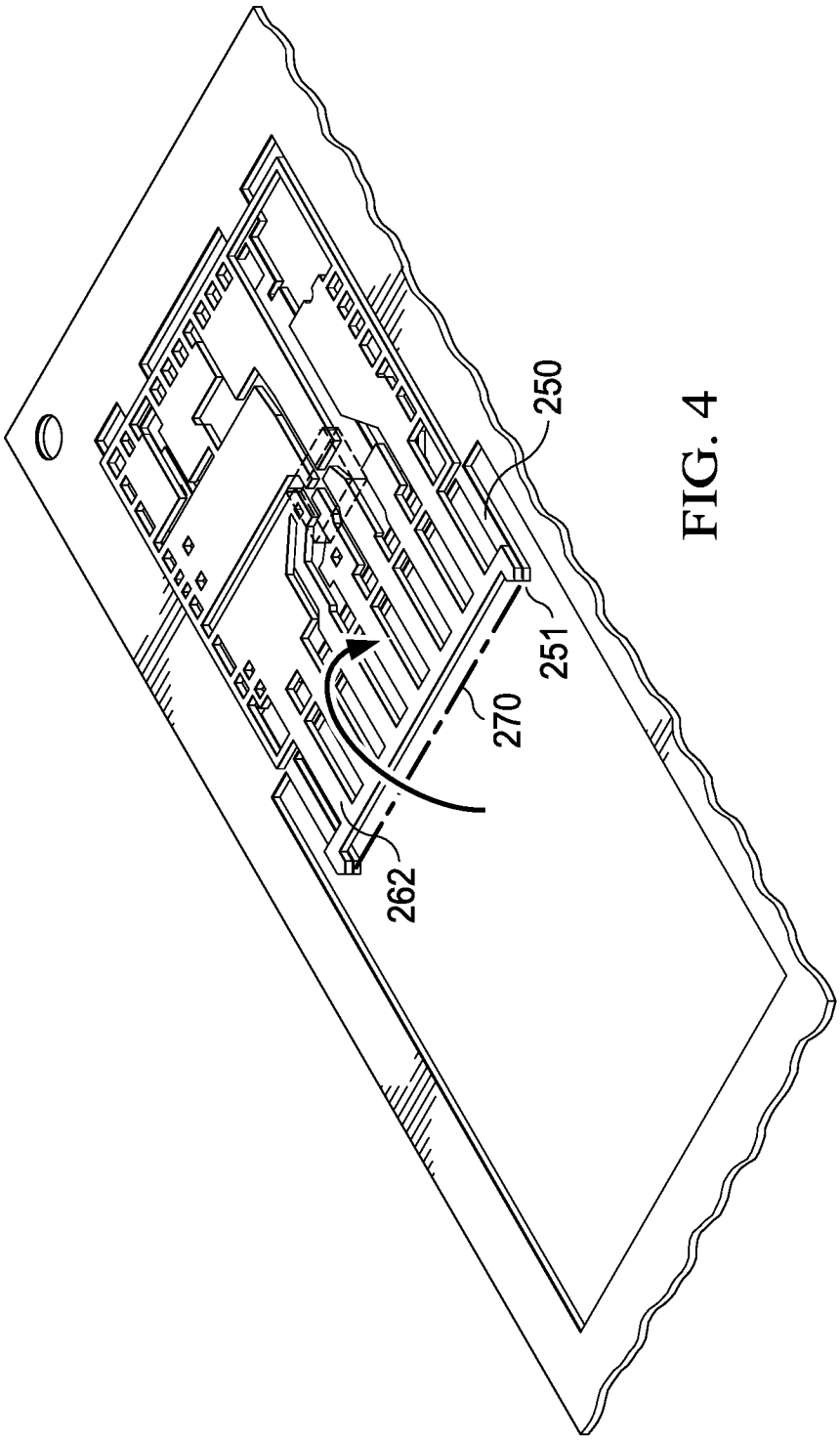

FIG. 4

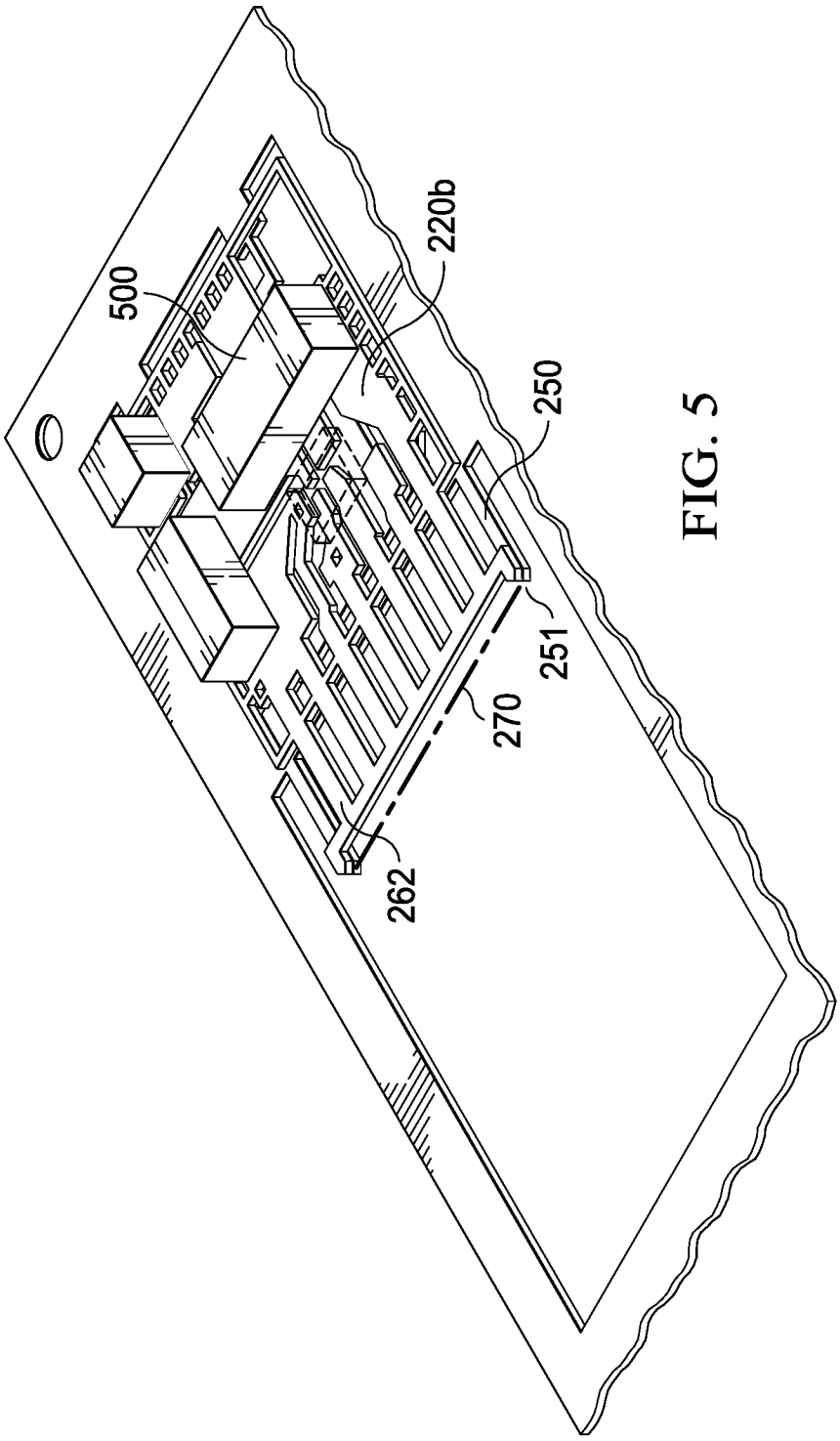

FIG. 5

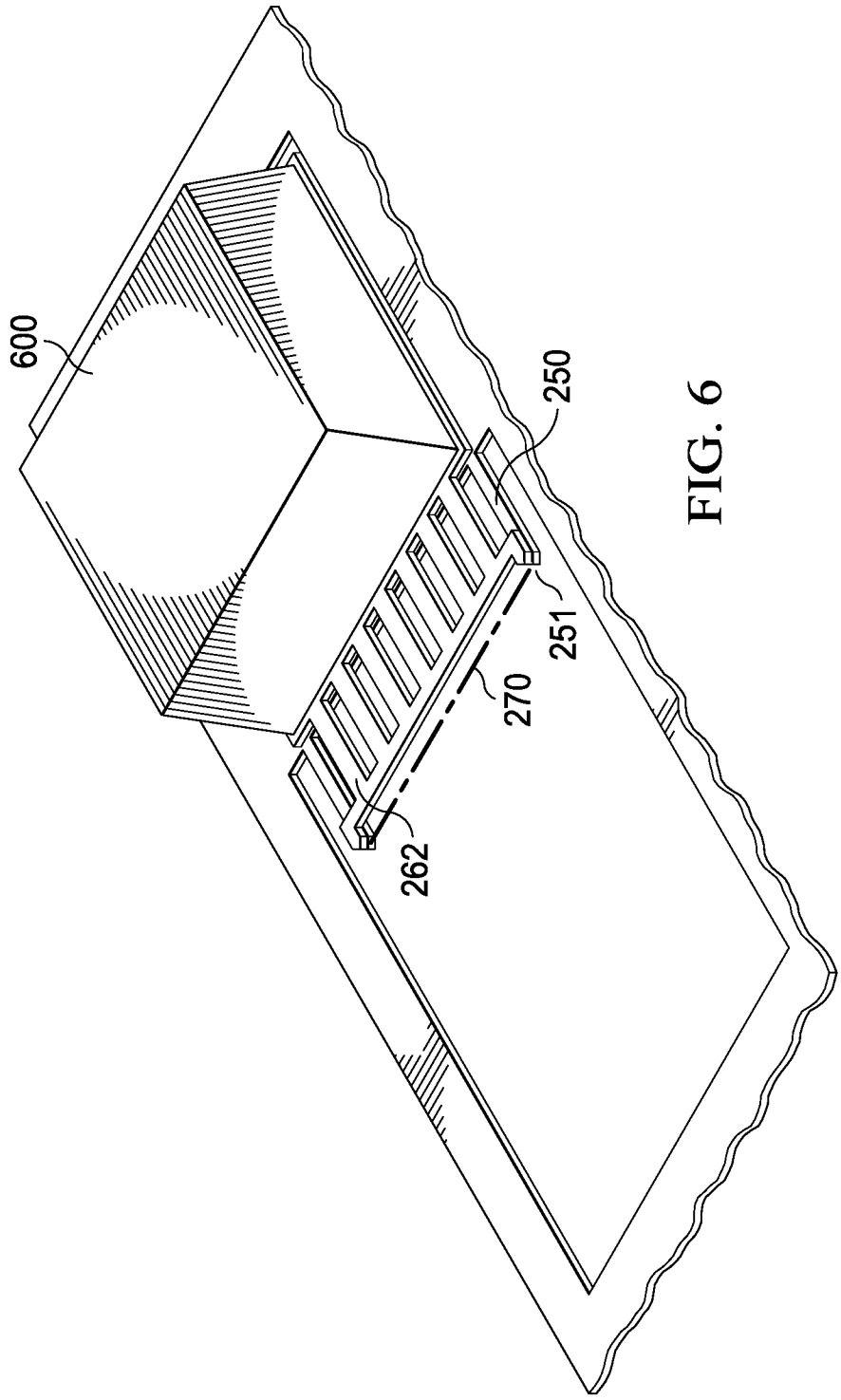

FIG. 6

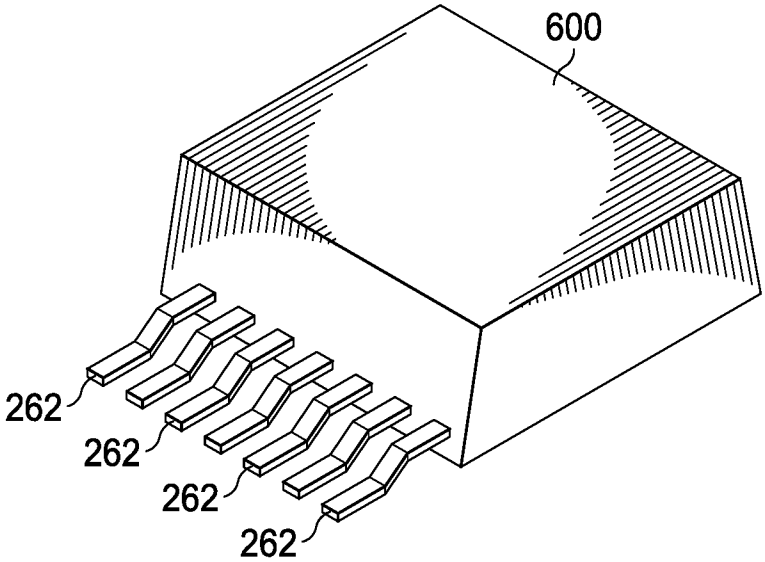

FIG. 7A

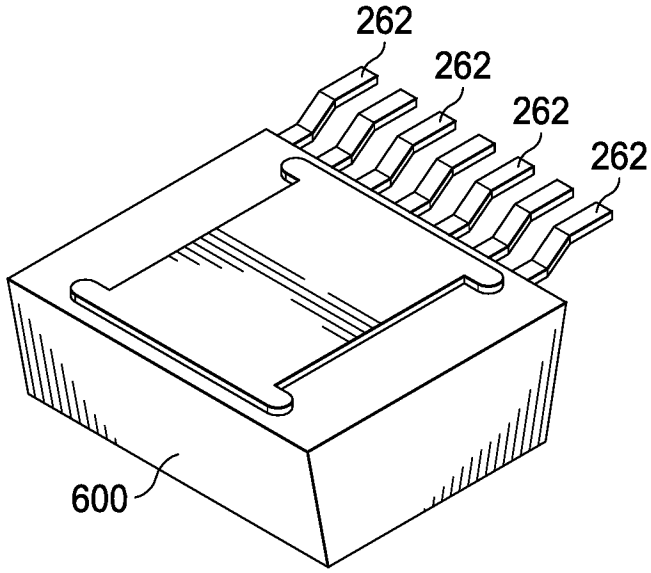

FIG. 7B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 2016/026881

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/495 *(2006.01)*
H01L 25/00 (2006.01)
H01L 21/00 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 23/00, 23/495, 23/48, 25/00, 21/00, 21/60, 21/66, H05K 1/00, 1/18

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2006/0049493 A1 (SAMSUNG TECHWIN CO., LTD.) 09.03.2006, fig. 3-8, paragraphs [0029], [0030], [0043]-[0049]	1-16
A	US 5223738 A (MITSUBISHI DENKI KABUSHIKI KAISHA) 29.06.1993, fig. 1, 2, columns 3, 4	1-16
A	US 6307755 B1 (RICHARD K. WILLIAMS et al) 23.10.2001, fig. 20 a-e, 26 a-c, column 19, lines 63-67, column 20, lines 1-40, column 21, lines 44-51	1-16
A	US 2002/0004251 A1 (JOHN K.ROBERTS et al) 10.01.2002, abstract	1-16

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

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Date of the actual completion of the international search	Date of mailing of the international search report
15 July 2016 (15.07.2016)	11 August 2016 (11.08.2016)

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