

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
30 August 2007 (30.08.2007)

PCT

(10) International Publication Number
WO 2007/098445 A1

(51) International Patent Classification:
G11C 8/04 (2006.01) *G11C 7/10* (2006.01)

(21) International Application Number:
PCT/US2007/062433

(22) International Filing Date:
20 February 2007 (20.02.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/359,205 21 February 2006 (21.02.2006) US

(71) Applicant (for all designated States except US): **CY-
PRESS SEMICONDUCTOR CORP.** [US/US]; 198
Champion Court, San Jose, CA 95134 (US).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **REZEANU, Stefan-
Cristian** [US/US]; 2460 Kittridge Ave., Colorado Springs,
CO 80919 (US).

(74) Agent: **DAFFER, Kevin, L.**; Daffer McDaniel, LLP, P.O.
Box 684908, Austin, TX 78768-4908 (US).

(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN,
CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI,
GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS,
JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS,
LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MY,
MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS,
RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN,
TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

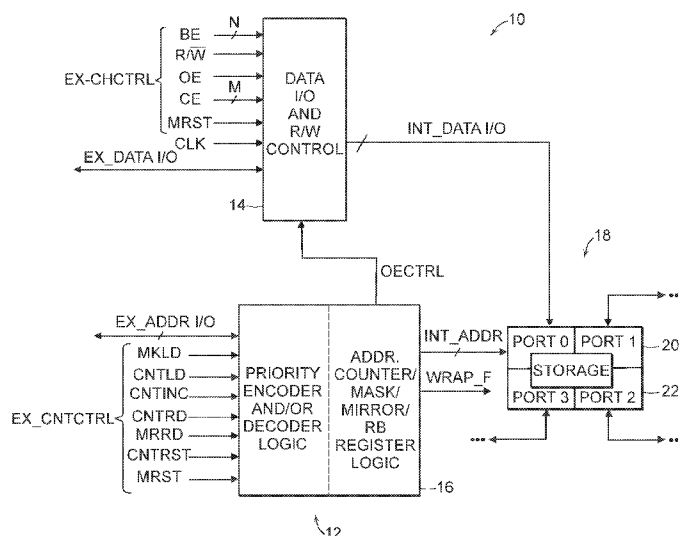
(84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, GH,
GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM,
ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),
European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI,
FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT,
RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA,
GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

- with international search report
- before the expiration of the time limit for amending the
claims and to be republished in the event of receipt of
amendments

For two-letter codes and other abbreviations, refer to the "Guid-
ance Notes on Codes and Abbreviations" appearing at the begin-
ning of each regular issue of the PCT Gazette.

(54) Title: INTERNALLY DERIVED ADDRESS GENERATION SYSTEM AND METHOD FOR BURST LOADING OF A SYNCHRONOUS MEMORY



(57) Abstract: An address generation system and method is provided for internally storing and thereafter producing an address to be sent to a memory device. The address that is stored need not be sent from an external address bus at each clock cycle, but the processing can remain internal to the memory device. The burst-block starting address can be stored in the mirror register (52) and output from a selector circuit, such as a multiplexer (54) when that address is chosen. Otherwise, the multiplexer can simply perform its normal operation of selecting between an address pointed to by a counter (60), the external address (ADDR, IN), or the incremented counter output, based on the state of the external counter control signals. The system includes a mirror register, a counter, and a multiplexer that selects either the mirror register stored address or the internally processed address.

WO 2007/098445 A1

**TITLE: INTERNALLY DERIVED ADDRESS GENERATION SYSTEM AND METHOD
FOR BURST LOADING OF A SYNCHRONOUS MEMORY****BACKGROUND OF THE INVENTION**

5

1. Field of the Invention

The present invention relates to a memory circuit and, more particularly, to a memory that can have a block of address locations synchronously written to or read from in a burst fashion, with the address block bottom address stored in a mirror register, and a counter for
10 incrementally writing to or reading from the memory block at an internally-derived address stored in a counter register and selected using a counter control signal.

2. Description of the Related Art

The following descriptions and examples are given as background only.

15 A typical mechanism in which to store data involves sending an address to that storage location in order to access that location, and reading from that addressable location, or writing to that addressable location. Accordingly, memory generally includes an address bus and a data bus, as well as control signals which control access thereof.

There are numerous forms of memory, such as mass storage devices or hard drives.
20 Alternatively, memory can be embodied upon silicon or a single monolithic substrate, and such forms are known as semiconductor memory. Popular semiconductor memory includes random access memory (RAM), read only memory (ROM), and programmable read only memory (PROM), etc. Because each form of semiconductor memory operates differently from one another, the addressing of the memory locations and the data bus applicable to those locations, as
25 well as the control signals, remain somewhat unique to one another.

As an example, RAM can be accessed in different ways. In many applications, related data are placed in contiguous locations within the RAM. In order to quickly access that data, a RAM can implement synchronous accessing whereby contiguous address spaces (or possibly non-contiguous spaces) can be accessed at sequential transitions of a clocking signal, rather than
30 having to resort to independent accesses that require taking control of the external address bus. Such forms of memory are often referred to as synchronous memory, and a popular such memory is often labeled synchronous RAM.

If accesses can occur synchronously and if the target data is placed in a relatively contiguous space, then a natural benefit of synchronous memories is to perform a burst read or
35 write operation. Essentially, a burst read or write (burst access) involves performing a load

operation of a particular address, and then subsequently incrementing or decrementing a counter to point to the next addressable location until an entire block of addressable locations are accessed. Thus, a burst access involves externally reading a load address upon the external address bus, and then incrementing a counter placed internal to the memory, generally labeled
5 "burst counter". The only access on the external address bus is the initial load operation for the first memory location within the block being read. Thereafter, the counter simply increments or decrements to the next address space. Thus, the data from all address spaces within the block can be accessed by asserting the read/write operation and holding the particular (read or write) chip control signal active for as long as necessary to complete the burst access.

10 The term external address is generally recognized as the address bus that is external to the memory device or, more specifically, is the address bus coming from an execution unit (i.e., microprocessor) that, in response to an instruction, loads a particular address onto the external address bus that is then sent to the memory or the memory controller. Once the externally-loaded address is placed upon the external address bus and subsequently loaded unto the internal
15 address bus, the memory or memory controller then performs the counter increment or decrement internal to the memory or memory controller. A benefit in performing a burst or block access is that the external address bus is only occupied for the first address. The counter, which might transition much faster than the external address, then takes care of the remaining addressable locations without having to thereafter involve the external address bus.

20 It may be desirable for the user to know the current memory address location at which the internal counter is pointing at a particular time, as well as the associated data at that address. Therefore, the concept of a read-back occurs whenever the user might implement an instruction through a control signal external to the memory controller or memory device. That instruction can be fed from an external pin or decoded from multiple pins into the memory device, which
25 then instructs the counter to send back the particular address to which it is pointed and/or the data so that the user can then read that correspondence. Examples of an external-derived read-back mechanism in which the counter pointed-to address and data is read back is set forth in, for example, U.S. Patent Nos. 6,789,180 and 6,782,467.

30 While there is benefit in knowing where the counter is within the block of data, and reading back the address and corresponding data values, there is even more value in being able to control the counter and the address and/or corresponding data values pointed to by that counter. Therefore, it would be desirable to implement a system which can not only read back the internally-derived (counter value) address and corresponding data, but also generate an address via the count value entirely internal to the memory controller or memory device. By

beneficially controlling the count value and, thus, the corresponding address and data values to which that pointer is directed, it would be of even further value to do so without involving or occupying the external address bus.

Therefore, the desired system achieves the stated benefit of being able to derive an address location from among any memory addressable location solely internal to the memory controller or semiconductor memory device without having to take control of, manipulate, or in any way access or place an address upon an external address bus coupled between an execution unit and the memory controller or memory device. This frees up bandwidth on the external address bus and also allows for quicker memory address generation since such generation occurs solely internal to the controller or device without having to contend with or keep track of the pipelined addressing mechanisms normally associated with conventional memories that have priority control signals and coding on the external control signal bus.

SUMMARY OF THE INVENTION

The following description of various embodiments of circuits and methods is not to be construed in any way as limiting the subject matter of the appended claims.

The problems outlined above are in large part solved by a system that can internally load an external address via the external address bus, and thereafter maintain specific addresses that are internally-derived to that system. The system can be at least a part of a memory controller/device, and is maintained internal to the controller/device. The system thereby stores the initially-loaded address coming from the external address bus, and can store those other externally-sent addresses. In addition, the system can store any address pointed to by the internal counter. By storing such addresses, quick recall or retransmit of that address can occur. Thus, if the last externally-sent address is to be retransmitted back to the storage array or address decoder of the memory device, the system simply keeps track of (i.e., stores) the last externally-loaded address within a mirror register internal to the memory controller/device. The last loaded address can then be reloaded solely within or internal to the controller/device without having to seek any information outside of the memory controller/device (i.e., the present system), or involving the external address bus.

Generally, flexibility in selecting particular memory blocks is achieved by giving the internal burst counter the ability to mask certain addresses. This may be achieved by including a mask register that stores the user defined mask configuration (i.e., which counter bits are inactive labeled as “masked,” and which are active labeled as “unmasked”). The mask configuration is loaded via the external address bus, by activating an external mask load instruction, which

requires the external mask load counter control signal activation in a clock cycle when no other higher precedence counter control signal is active.

In addition to being able to quickly jump to the last loaded address, the system can also quickly transition to a zero address within the unmasked memory addressable space. Therefore, the mirror registers can store not only the last loaded address, but also the zero addressable location internal to the controller/device, for quick reloading back onto the address decoder of the memory device without consuming any bandwidth, or accessing or taking control of in any way the external address bus coming from the execution device.

According to one embodiment, the system comprises a maskable counter register for storing an address processed internal to the system as the next address, as well as a mirror register configured to store an address upon receiving a command signal and produce the stored address upon receiving an active clock transition. The command signal can be either sent on the one line within the external command signal for the memory controller/device, or, alternatively, the command signal can be internally-derived by decoding one or more command signals sent externally to the memory controller/device. A generic multiplexer -- having the function of a next state address generator -- is preferably coupled to receive output from the mirror register and the counter for producing the internally processed address upon receiving a command signal and for sending either the mirror register stored address or the internally processed address to become the next address and be stored in the counter register, from which the next address is configured to be sent to a memory address decoder.

According to another embodiment, the stored address can be the last loaded address sent from the external address bus to the controller/device or an address derived by a mirror address generator coupled to receive the external address and a subset of the internal counter control signals and generate a next mirror address forwarded for storing purposes to the mirror register. The last loaded address might be the first address within a block of addresses that are addressable using a count value that increments upward or downward from that externally-loaded address. Alternatively, the mirror-stored address might simply be an address containing all logic 0 voltage values at least in its unmasked portion, typically associated with the first address within the addressable memory space. By having the mirror register present the last loaded address or the all 0's addressable (unmasked) space -- the latter typically expected when the user activates a counter reset instruction, upon receiving either a retransmit (RTX) or a wrap to retransmit-address (WRP0 inactive) command signal in combination with an increment/decrement command when the counter stores its maximum (unmasked) state, the generic multiplexer can selectively send to the counter register the mirror-stored address.

According to yet another embodiment, the memory associated with the memory address decoder can be a single port or multi-port memory. Preferably, the memory is a synchronous memory which performs accesses upon transitions of a clock signal and, therefore, is synchronous to that clock signal. Also, preferably, the memory performs burst accesses (i.e., burst reads or writes) by externally loading an address, and simply counting to the next unmasked address using an internal counter to access all storage locations within the burst block.

The mirror register and the mask register have the same (bit) dimension with the counter register, all of them being components of the internal burst counter. The mirror register would generally store the last loaded address (via the external address bus) when a first (generally a counter load) command signal is activated, or the all logic 0 voltage values in its unmasked bits when a second (counter reset) command signal is activated. The mirror-stored address can be retrieved and sent for storage to the counter register whenever a third command signal is sent to the generic multiplexer. Otherwise, the next address within the count is an internally processed address. The third command signal can either be a retransmit (RTX) or an increment/decrement combined with a counter wrap control (WRP0). The internally processed address is sent to the counter register upon receiving the first or second command signals, but also upon activating an alternate counter control signal (e.g., counter increment).

According to yet another embodiment, a method is provided for addressing memory locations. The method includes storing an address, followed by sequentially incrementing that address. The stored address might be the last loaded address, the unmasked-counter reset address, or might simply be the incremented address of the next counted-to counter value, depending on a logic state of at least one command signal.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in which:

Fig. 1 is a block diagram of a multi-port memory device whose outputs are controlled by byte, read/write, chip enable, and output enable signals, wherein the internal addressing and the address I/O tri-state as well as part of the I/O tri-state data are controlled by a burst counter which can have certain addresses masked and can be loaded with a particular address or incremented to the next unmasked address;

Fig. 2 is a memory address space having a user-loaded address from which a counter can increment synchronous to subsequent unmasked addresses upon sequential clock edges within a block of the address space whose limits are user-defined through masking;

Fig. 3 is a more detailed block diagram of the priority encoder and/or decoder logic and address counter/ mask / mirror / read-back register blocks of Fig. 1;

Fig. 4 is a memory address space being incrementally written to or read from, whereupon the counter receives a retransmit (RTX) command signal or is configured to wrap to 0 or the last loaded address (via the state of the external WRP0 counter control signal) that will cause the mirror register to output the last loaded address or zero address, respectively, to be output from the counter to the memory decoder;

Fig. 5 is only a portion of what is shown in Fig. 3, including more details of the internal structure of block 44 absent the read back and wrap around flag logic shown in Fig. 3, including for example, the mirror address generator and mirror register that typically respond to the CNTLD and CNTRST counter control command signals by storing and producing the last loaded address or zero address (shown in Fig. 4) onto the counter register, via selection in the next state address generator, and eventually to the memory decoder according to a preferred embodiment of the present invention.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the appended claims.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Turning now to the drawings, Fig. 1 illustrates at least a portion of a memory controller/device 10. Controller portion 12 includes a data input/output (I/O) and read-write control block 14, as well as an address control and a priority encoder and/or decoder logic for the counter control signals block 16. The memory devices portion 18 can include a single port or a multi-port memory 20. Contained within the ported memory 20 is an array of storage cells 22. Storage cells 22 comprise semiconductor memory storage elements that can be accessed through an internal address bus INT_ADDR. The data, depending on whether a read or write operation occurs, can be written to or read from the memory device 18 via INT_DATA I/O bus.

For sake of brevity in the drawings, the memory controller 12 is shown applicable to port 0 of memory 18. However, it is recognized that the memory controller 12 is replicated for all of the ports depending on how many ports might be used. Moreover, it is understood that the controller portion 12 and the memory portion 18 can be embodied either on the same monolithic

substrate or across multiple monolithic substrates. In addition, the communication between controller 12 and device 18 is internal to the controller/device. However, communication from an execution unit to system 10 occurs externally via EX_ADDR I/O, EX_DATA I/O, and the external counter control EX_CNTCTRL and chip control EX_CHCTRL signals.

5 System 10 can be configured to externally read on the external address bus (in other words, the EX_ADDR I/O bus can be bidirectional) and to read data in or read data out via the external data bus (EX_DATA I/O). Reading and writing operations or accesses generally occur through control logic 14 via byte manipulation (BE bus), read/write control ($R/\overline{W}$), output enable (OE), chip enable (CE bus), and master reset (MRST) signals. Such signals can be
10 synchronized to an external clocking signal (CLK) to manipulate the data into or data out of memory device portion 18. For exemplification purposes, the size of the BE bus is limited to 2 bits only. If so limited, then UB may be the upper byte, LB may be the lower byte, and depending on which control signal is asserted (note that the Endian signals are not illustrated in Fig. 1), the upper or lower byte might be manipulated first depending on the Endian format
15 chosen. Signals such as read/write ($R/\overline{W}$), output enable (OE), and chip enable (CE) are well-known to enable the data output or the particular chip at which the memory device is embodied.

Memory device 18 and, specifically, storage cells 22 can be implemented as a RAM. Shown are four ports which form a quad-port RAM and, more preferably, a quad-port SRAM (static RAM) device. Ports 0-3 may permit independent, simultaneous access for read/write
20 from/to any location within storage array 22. For example, one of the ports may write to a particular location of memory storage array 22, while another port may read from other locations or the same location simultaneously, the latter of which may have certain timing constraints. An arbitration block might decide which block gets access in case of a potential contention, i.e., conflicting operations coming from different ports (e.g., when 2 or more ports attempt to
25 simultaneously write to the same memory location).

Data I/O control circuit 14 may typically internally generate, for example, upper byte read, upper byte write, lower byte write, and lower byte read signals depending on which format is chosen to output or input the data. Such signals may control the data flow on the internal data I/O bus shown in Fig. 1 (although the system 10 may have separate data read and data write
30 internal busses). Control block 16 performs various functions for addressing memory device 18, and bridges the external address bus (EX_ADDR I/O) and the internal address bus (INT_ADDR). Various control signals grouped as an external counter control bus (EX_CNTCTRL) are labeled as MKLD, CNTLD, CNTINC, CNTRD, MKRD, CNTRST, and MRST (this Master Reset is generally not specific to block 16; note that it was as well included

as an input to the control block 14). MKLD represents a mask register load signal. CNTLD and CNTINC represent counter register load and increment command signals. Both MLKD and CNTLD use the EX_ADDR I/O bus as an input bus to present the address that is to be stored internally. Their “counterparts”, mask read (MKRD) and counter read (CNTRD) command
5 signals, use the EX_ADDR I/O bus as an output bus that presents the internal mask or counter register content to be read out by the external system (external to system 10). The counter and/or mask registers can be reset via CNTRST and/or MRST.. The details of the counter, mask, and read-back registers, as well as the logic used to control such registers are contained within the control circuit 16. These details are further explained in reference to Fig. 3.

As shown in Figs. 1 and 3, block 16 may be implemented as a single-port counter 44 in Fig. 3 (identically - or slightly modified - multiplied by the number of ports in case of a multi-port), with mask, mirror, and read-back capability and/or a synchronous address counter with reset (synchronous and/or asynchronous), parallel load, variable width incrementation, and/or wrap around flagging capability. In a particular example, the counter will be considered to be a
15 16-bit wide counter. Control circuit 16 may also include a 16-bit mask, mirror, and counter register with parallel load and asynchronous/synchronous initialization capability as well as wrap around address control for the 16-bit synchronous counter. A wrap around flag (WRAP_F) may be activated for one or more clock cycles slightly before or after the unmasked portion of the counter is reset – or brought to the retransmit address - through an incrementation operation. In
20 the case when each counter control signal has a dedicated external pin, the user could simultaneously activate several of the control signals. Conflicting external simultaneous active control pin states may be eliminated internally using a priority encoder and decision logic portion 48 of block 16. The decision logic can determine which of the active control pins takes precedence if, for example, multiple control pins are activated simultaneously by the user,
25 externally. Whenever the counter control scheme presupposes the simultaneous external activation of several bits – part of the external counter control bus, in order to activate a certain counter control mode, a decoder would be used inside block 48. The former control scheme is generally used with quad ports, while the latter generally with dual ports.

Referring to Fig. 2, a typical burst operation for performing a block read or write is
30 shown. Specifically, a user might load a certain address by, for example, asserting a counter load (CNTLD) signal on the external counter control bus (EX_CNTCTRL) and loading a particular address via EX_ADDR I/O into control block 16. Control block 16, which contains a burst counter, will then begin the count operation at, for example, a count of CNT0 value (CNT0 could be address 0, in particular, but in general it is a different address, the base address for the

burst block of interest). Thereafter, the counter increments to the next unmasked count value, determined with the aid of a mask register that may be contained within block 16. The mask register stores the mask configuration, i.e., the information about which bits are skipped by an incrementation operation. As illustrated in Fig. 2, masked address 30 is skipped when the counter increments or decrements, so that the counter will then point to the next unmasked address 32. The counter continues its count operation until preferably the entire block is read/written. An important benefit is the fact that the external address needs to only be asserted and loaded internally during the first address access within the block; thereafter is not tied up, accessed, or used. The internal counter will thereafter generate the subsequent addresses (through incrementation or decrementation) to access the storage array which will subsequently produce the data from the contiguous, unmasked addresses. Also, even though the addressable storage region 34 - beginning with the all 0's (000 . . . 000) to the last addressable storage region (111 . . . 111) - can be quite large, it may be only necessary to repeatedly burst read/write the region shown as BURST R/W BLOCK (MASK DEFINED) in Fig. 2. A user can go directly to the first address by simply asserting an external address (EX_ADDR INPUT) and then burst read/write that block on synchronous, subsequent clock cycles and, if necessary, repeatedly doing so without involving other regions of the memory address space 34.

Turning now again to Fig. 3, a more detailed block diagram of control block 16 is shown along with data I/O and R/W control block 14 and the address decoder 40 associated with memory portion 18 (Fig. 1). In particular, in Fig. 3 block 16 also illustrates a read-back operation in which either the address stored in the counter register or the mask configuration stored in the mask register (illustrated as a combined bus CNT_OUT & MK_OUT) can be read back as selected through a MUX_CTRL (selection control) signal to a read-back multiplexer 42. The internal address, stored in the counter register, is simply the next state of a state machine whose output is being masked using the mask configuration stored in the mask register. The address state machine, registers, and register logic is shown generically as reference numeral 44. The logic also produces the output enable control (OCTRL) signal which controls the high impedance state of both the data I/O bus (EX_DATA I/O, off of block 14) and address I/O bus (EX_ADDR I/O, off of block 46).

Once multiplexer 42 selects between its CNT_OUT and MK_OUT input buses using its MUX_CTRL selection control input, the result (counter or mask register content) is then read back via the read-back bus RB_ADD_OUT to the address input/output buffers 46. Buffers 46 are bidirectional, being able to not only buffer an incoming address from EX_ADDR I/O into block 44 via ADDR_IN, but also buffer an output address via the read-back operation. Thus, the

EX_ADDR I/O bus is also bidirectional. The user can thus read on the external address bus EX_ADDR I/O the current internal address that is pointed to by the counter and/or the mask configuration. Generally, through the OCTRL signal, only one of the mentioned bidirectional buses (EX_DATA I/O and EX_ADDR I/O) are in output mode at any given time, but this might not necessarily be so (i.e., they might both put out information at the same time, although because of the typical latency in such memory devices, the information might pertain to different clock cycles). The address and data are sent on the external address and data buses back to, for example, an execution unit which might manipulate that address and data or simply present that data and address to an input/output device. A third output device might be simply an electronic display where the user can then visually examine the current state of the counter and, more specifically, the address and data to which the counter points.

Of significance is a priority decision (encoder) block and/or decoder logic 48. Block 48 receives the external counter control signals, generically referred to as any control signal for controlling an address value. The external control bus (EX_CNTCTRL) can have one or more component signals active. As shown in Fig. 1, for example, if only the MKLD signal of the external counter control bus is active, then the mask register will be loaded with the information presented externally on the EX_ADDR I/O bus. The same would apply (for the counter register, rather than the mask register) if only the CNTLD signal is active. A read-back of the mask register would occur if the MKRD signal was active, and a read-back of the counter would occur if the CNTRD was active. If the CNTINC is active, then the counter will be incremented. Likewise, if the CNTRST or the MRST is active (the latter can be, generally, asynchronous in nature), then the counter and/or mask and/or mirror registers will be reset, respectively, to a 0 logic value at least in their unmasked portions (generally the mask register is set – all bits at 1 – during its reset, although an implementation with all its bits at 0 is not excluded). It may be that more than one signal line of the bus EX_CNTCTRL may be active in order to perform a specific mode of operation. For example, block 48 may assign a priority to one of the signals if multiple signals are active. The priority encoder and/or decoder logic block 48 may, therefore, assign precedence to a reset rather than a load signal. Also, block 48 may contain decoder logic which may assign an altogether different control by decoding all of the incoming signals and assigning an altogether new control if two or more signals are active (generally, but not necessarily, the dual port counter control scheme). The following Table 1 indicates what would occur in the priority decision logic if only one signal were active (generally, but not necessarily, the quad port counter control scheme), showing an active low (L) state:

TABLE 1

CLK	MRST	CNTRST	MKLD	CNTLD	INCDEC	Operation
X	L	X	X	X	X	CNT reset and MK set
L-H	H	L	X	X	X	CNT reset
L-H	H	H	L	X	X	Load ADDR into MK
L-H	H	H	H	L	X	Load ADDR into CNT
L-H	H	H	H	H	L	CNT increment/decrement
L-H	H	H	H	H	H	CNT hold

5 A particular example is outlined in Table 1: if more than two of the signals are active (low), then the priority encoder logic 48 may assign internally the control mode that has the highest precedence. Additional modes will be introduced in the following, such as a retransmit (RTX) operation that can be output from block 48, as will be described in more detail in reference to Figs. 4-5 (note that the RTX counter control input signal was not included in the illustration of Fig. 1, but it has to be part of a EX_CNTCTRL – quad port scheme - bus if the operation is to be made available to the internal burst counter).

Turning now to Fig. 4, an addressable space 50 is shown whereby a user-loaded address can be accessed via EX_ADDR I/O bus. Thereafter, the counter will increment the address forwarding the counter register to the next address value that is unmasked. The masked address 15 52 is shown in cross-hatch. For example, the counter will skip the first masked address 52, and address the second unmasked address 54 at the first count value CNT1. Thereafter, the counter will naturally progress until the last count value is read at CNTN and, in the interim, skipping any masked addresses. It would be desirable to store certain addresses. Those addresses can be stored in a mirror register to be described below. For example, the stored address might be the 20 last address loaded into the counter register via the external address bus (EX_ADDR I/O). That address is shown in this example as a user-loaded address (through a CNTLD operation). It may also be desirable to quickly go (i.e., jump) to the first unmasked address within the user addressable space 50. That address might be at the (000 . . . 000) address, or at least might have all its unmasked bits at logic 0. A control signal can be either externally sent or internally 25 derived to allow the counter to reinitialize back to the last-loaded address (retransmit) or to the address containing all logic 0 voltage values at least in its unmasked portion. Those control signals are represented generically as RTX (retransmit) and WRP0 (wrap to address 0 – generally post masking).

Shown in the blow-up of Fig. 4, generally a RTX command sends the counter back to the 30 last-loaded address (assumed CNT0), and so does a counter wrap around when the WRP0 control signal is inactive (which would designate a “wrap around to retransmit” rather than a

“wrap around to unmasked-address 0”). It may be that in the interim, the last-loaded address is masked. If so, then the counter will be automatically incremented 56 to the first, subsequent address that is not masked. Thus, a jump to CNT0 (or the first unmasked address in the burst block of interest) can occur under a normal counter load (CNTLD), or a counter retransmit (RTX), or a “wrap around to retransmit” (WRP0 inactive) as shown on the upper portion of the blow-up of Fig. 4. Illustrated in the bottom portion of the blow-up of Fig. 4 is the jump to “unmasked address 0,” which can occur under a normal counter load (CNTLD), or a counter reset (CNTRST), or a “wrap around to unmasked-address 0” (WRP0 active).

Referring to Fig. 5, reference numeral 16a describes only a portion of that which is shown in Fig. 3. For example, item 16a illustrates a logic block 48 receiving the external counter control bus (EX_CNTCTRL) implemented as a multi-bit counter control bus which must necessarily include a retransmit control. Another signal ADDR_IN can be implemented also as a multi-bit address bus. The address input bus ADDR_IN as well as the mask register output (MK) is sent to a mirror address generator block 50 along with certain internal counter control signals associated with the counter. In a particular case, those control signals can be a counter load (CNTLD) and/or a counter reset (CNTRST). The counter load and counter reset control signals can be internally or externally derived. For example, the counter load can be derived by decoding two or more control signals (for the most general dual port counter control scheme) upon the external control bus via decoder logic 48. The counter reset may be sent externally via one of the external counter control signals or can be, also, derived internally via decoder logic 48. The same applies to the wrap to 0 control signal (WRP0), shown in dashed line to illustrate the above. Whether produced externally or internally, the control signals will indicate a retransmit (RTX) or a “wrap to the last-loaded address,” or a “wrap to 0” (to the address containing all logic 0 voltage values at least in the unmasked bits), both of which might cause the next state address generator 54 to route the mirror address (MR_ADDR) – stored in the mirror register 52 – to the counter register 60 as the NXT_STATE internal signal. The mirror address generator 50 is the one that produces a particular signal NXT_MR_ADDR that gets stored into the mirror register 52 at the next active clock (CLK) transition. Besides the mirror address MR_ADDR (stored in the mirror register 52), the multiplexer 54 can also select another of its inputs (e.g., ADDR_IN, ADDR_OUT, or INCR_STATE) to become the NXT_STATE signal at its output in response to a select signal that might contain as a subset internal counter control signals like RTX, CNTINC, WRP0, or CNTLD, and to the MK signal. The INCR_STATE signal is generally the output from a partially maskable incrementer 56 controlled by the ADDR_OUT and a subset (MK_LSB) of the mask register internal bus signals (MK) stored and

produced by the mask register 58 at each active clock transition in response to the ADDR_IN and a mask load MKLD signal. The incrementer is controlled by a subset of the mask register internal bus signals (generally not more than a few LSBs are masked in the incrementer) - thus being partially maskable, because of the requirement for a 3-contiguous-region mask needed for cross-port word size multiplication as described, e.g., in U.S. Patent No 6,782,467. As the internal address – stored in the counter register as ADDR_OUT - is incremented via the partially maskable incrementer 56 (INCR_STATE), the address out of the multiplexer (in the case of an incrementation operation) becomes NXT_STATE and is also subsequently masked (using the MK signal that is input of the multiplexer 54) so that the incremented address stored in the counter register 60 at the next active clock transition is only incremented in its unmasked bits.

Therefore, the entire feedback loop shown for the counter register 60, through the multiplexer 54, is a state machine that can either continue the incrementing function of INCR_STATE to NXT_STATE, or can take the mirrored address value on the MR_ADDR bus and apply that to the output NXT_STATE, or can hold the same internal address by “recycling” ADDR_OUT, or can apply ADDR_IN to become NXT_STATE, depending on the status of the multi-bit select signal shown on the S pin of multiplexer 54. Thus, multiplexer 54 receives the MK, ADDR_IN, ADDR_OUT, INCR_STATE, MR_ADDR, and a set of uniquely decoded counter control signals (e.g., CNTINC if the counter is simply to be incremented/decremented – decrementation taking place in response to an additional UP/down control signal, not shown - to the next unmasked address, CNTLD if the external address is to be loaded, or RTX and/or WRP0 control signals if the counter is to execute a retransmitted or be wrapped to retransmit or unmasked-address 0 based on the mirror address). Thus, multiplexer 54 also receives the mirrored address of, for example, the last user-loaded address or the address containing all logic 0 voltage values in its unmasked portion. The signal NXT_STATE may be implemented as a multi-bit bus, and whatever the address output from multiplexer 54 via NXT_STATE is then stored in counter register 60 to be placed into the address decoder of the memory device via the internal address out bus (ADDR_OUT).

The partially maskable incrementer 56 may shift down the bits of the present state via the address out (ADDR_OUT) signal with the number of masked LSBs in the input stage of incrementer block such that the first unmasked bit in the bits ADDR_OUT of the counter register 60 starting from the LSB is routed to the LSB of the binary incrementer block. The increment signal INCR_STATE may correspond to a shift up operation complementary to the shift down operation. Thus, the incremented (unmasked) bits may be routed back to their proper rank.

The NXT_STATE value can be represented as an up count value or a down count value placed into the counter register to produce the appropriate address output to the memory device. No matter what signal is routed by the multiplexer 54 to become NXT_STATE, the NXT_STATE is internally derived and does not involve taking control of and/or otherwise
5 placing an address upon the external address bus. Once the NXT_STATE is derived and the output address is produced, the subsequent count value that are unmasked generate, e.g., a new INCR_STATE and the NXT_STATE is automatically updated, also without taking control of the external address bus.

Burst counter 46 can perform a jump to the last-loaded address without taking control of
10 the external address bus, or without externally loading that address to the counter through a regular counter load operation. Moreover, the burst counter 46 can perform a rollover to the retransmit (mirror) address or the unmasked-address 0, also without taking control of the external address bus. Regardless of any counter load precedence, whereby a counter hold may have lower precedence and be “disregarded” during a counter reset, the internally mirror-stored
15 and/or derived unmasked-address 0 can be placed on the internal address output bus (ADDR_OUT) subsequent to a counter wrap around without performing an external reset and/or setting a counter interrupt to effect the reset through an external (to the memory device) feedback loop.

Mirror register 52 preferably has the same bit size and clocked synchronously with the
20 counter register 60 and mask register 58. Mirror register 52 stores the last-loaded address or the all 0’s (at least in its unmasked bits) address ready to be thereafter parallel-loaded into the counter register 60 whenever an RTX and/or wrap around (controlled by WRP0) operation is initiated for that counter. Block 48 can decode the RTX signal and, through a delay block, a WRP0 signal can be sent externally so that the RTX and WRP0 can arrive to the select control
25 pin of the multiplexer 54 at the same time. The RTX and WRP0 can, therefore, be part of the counter control signal generically sent over an internal or external counter control bus. The mirror register output is preferably parallel-loaded, via multiplexer 54, into the counter register 60.

Beneficially, the last-loaded address and the unmasked-address 0 are internally stored,
30 eliminating the need for any external system to have the last-loaded address or the unmasked-address 0 information. There is also no need for an external feedback connection or for a complex interaction between the maximum count state flag (WRAP_F) and the rollover through a counter reset, which is difficult to handle in a multiple-cycle latency (pipelined) memory. The counter register 60 can be incremented or be simply held in the max count state because the

interaction with rollover to unmasked-address 0 through the counter reset is eliminated. Counter register 60 can simply jump to the last loaded address without impacting system resources. There is no need for the memory to take control of the external address bus for a retransmit operation, because the operation is now controlled entirely internal to the memory controller/device.

The decoder logic can be used to reduce the number of external counter control pins (generally used in the dual port counter control schemes) by decoding two or more counter control signals – part of an encoded external counter control bus - to produce the particular control mode desired (i.e., RTX). Generally, however, a separate WRP0 pin would be used in order to specify the user-controlled rollover, although this signal could be incorporated in the counter control set of signals to be decoded.

It will be appreciated to those skilled in the art having the benefit of this disclosure that this invention is believed to provide an improved reloading of a last loaded address or zero unmasked-address without involving the external address bits sent to the memory device.

Instead, only the control signal states, or a new control signal, are changed to implement the improved reloading method, without needing to access or take control of the external address bus. Further modifications and alternative embodiments of various aspects of the invention will be apparent to those skilled in the art in view of this description. It is intended that the following claims be interpreted to embrace all such modifications and changes and, accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

WHAT IS CLAIMED IS:

1. A system, comprising:
a mirror register configured to store an address and produce the stored address upon
5 receiving a command signal;
a counter for incrementing the stored address to the next address; and
a multiplexer coupled to an output of the mirror register and the counter for sending
either the stored address or the next address to be sent to a memory address
decoder.
10
2. The system as recited in claim 1, further comprising a mirror address generator coupled
to receive the command signal and generate an encoded address forwarded to the mirror register
for retrieving the stored address.
- 15 3. The system as recited in claim 1, wherein the stored address contains all logic 0 voltage
values.
4. The system as recited in claim 1, wherein the stored address is loaded by a user prior to
the counter incrementing the stored address to the next address.
20
5. The system as recited in claim 1, wherein the next address is coupled to the counter for
incrementing the next address to sequential, subsequent addresses, which are then forwarded to
the multiplexer.
- 25 6. The system as recited in claim 5, further comprising a synchronous memory that is
adapted to write to or read from non-masked addresses upon sequential transitions of a clocking
signal and for receiving the sequential, subsequent addresses or the stored address from the
multiplexer.
- 30 7. The system as recited in claim 1, further comprising a multi-port memory, wherein one
port of the multi-port memory is adapted to receive output from the memory address decoder.

8. A system, comprising:
a mirror register configured to store an address and produce the stored address upon receiving a first command signal;
a counter for incrementing the stored address as the next address upon receiving a second
5 command signal;
a multiplexer coupled between an address decoder and output of the mirror register and the counter, wherein the multiplexer is adapted for sending the stored address to the address decoder if the multiplexer receives the first command signal, or the multiplexer is adapted for sending the next address to the address decoder if the
10 multiplexer receives the second command signal; and
an array of storage cells that sequentially receives addresses from the address decoder upon consecutive transitions of a clocking signal.
9. The system as recited in claim 8, wherein the first command signal is a signal instructing
15 the multiplexer to retransmit the last address loaded by an instruction.
10. The system as recited in claim 9, wherein the instruction is a counter load instruction.
11. The system as recited in claim 8, wherein the first command signal is a signal instructing
20 the multiplexer to retransmit an address containing all logic 0 voltage values.
12. The system as recited in claim 8, wherein the second command signal is a signal instructing the counter to increment its count value.
- 25 13. The system as recited in claim 8, further comprising:
a mask register configured to store masked addresses; and
wherein the counter is coupled to receive the masked addresses and to increment the stored addresses to the next non-masked address.
- 30 14. A method for addressing memory, comprising:
storing an address;
incrementing the address;
sending either the stored address or the incremented address to the memory depending on a logic state of at least one command signal.

15. The method as recited in claim 14, wherein said storing comprises loading the address by executing an instruction and placing the address upon an address bus.

16. The method as recited in claim 14, wherein said storing comprises loading the address
5 containing all logic 0 voltage values.

17. The method as recited in claim 14, wherein said incrementing comprises:
masking select addresses among a sequence of addresses; and
incrementing a counter to point to the next address among the sequence of addresses that
10 is not masked.

18. The method as recited in claim 14, wherein said incrementing comprises selecting the next address within a sequence of non-masked addresses.

15 19. The method as recited in claim 14, wherein said sending comprises:
applying the stored address and the incremented address to the input of a multiplexer; and
sending a first command or a second command to a select pin of the multiplexer for
sending the stored address if the first command is active, or sending the
incremented address if the second command is active.

20 20. The method as recited in claim 19, wherein said activating the first command comprises asserting either a retransmit signal or a wrap to zero signal onto an input pin.

21. The method as recited in claim 19, wherein said activating the first command comprises
25 decoding either a retransmit signal or a wrap to zero signal from among a set of counter control commands sent to a counter and/or register.

1/5

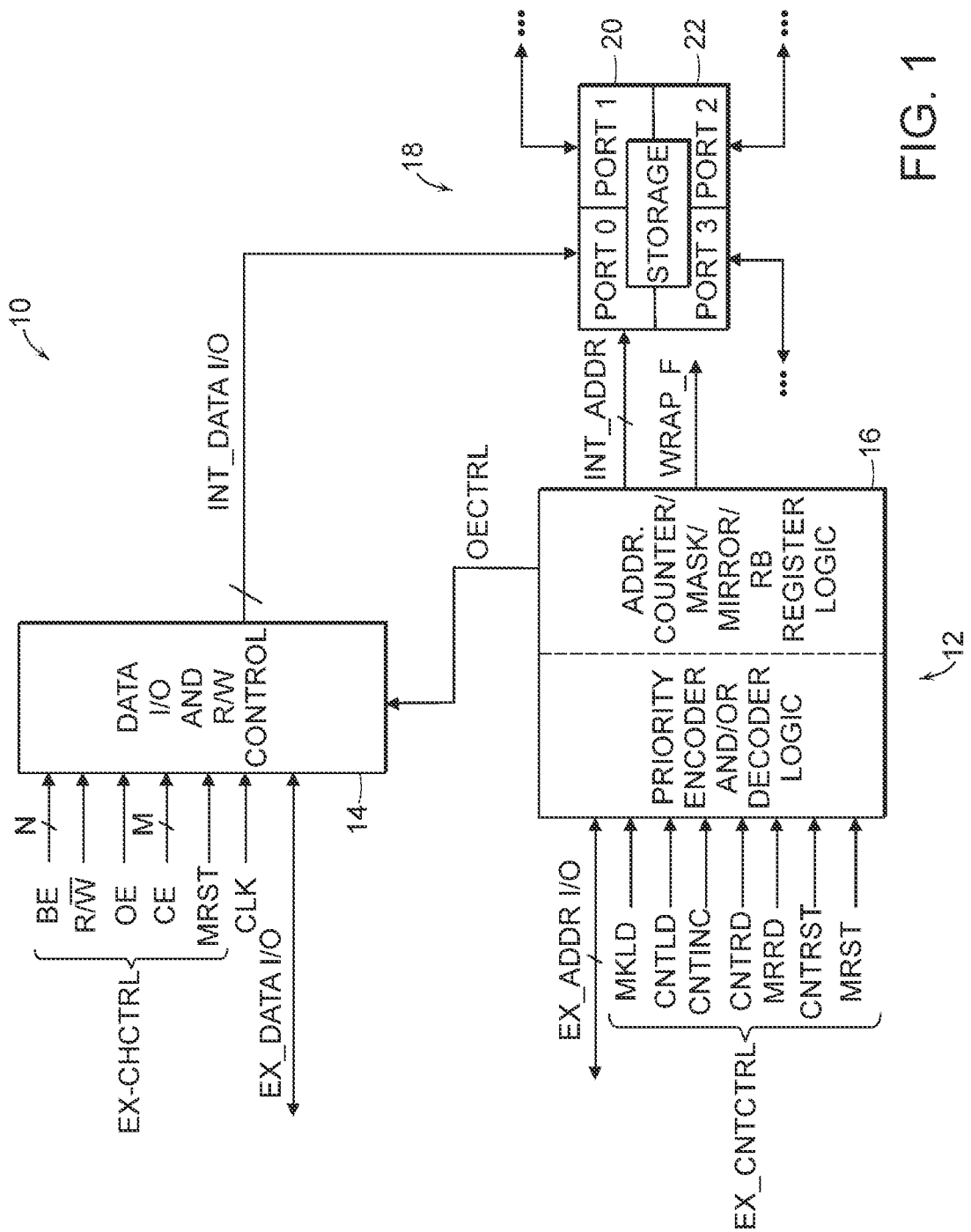


FIG. 1

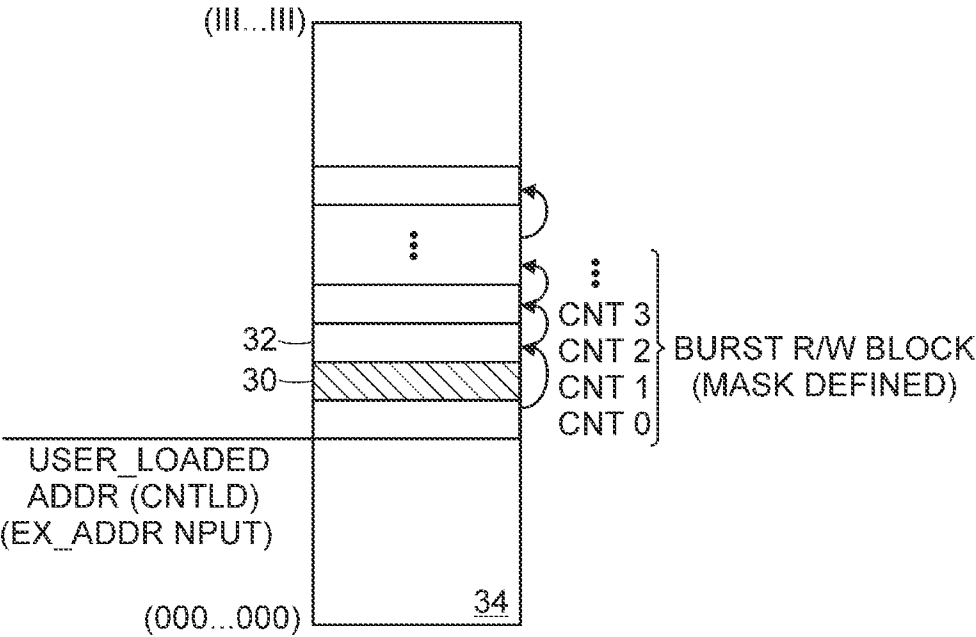


FIG. 2

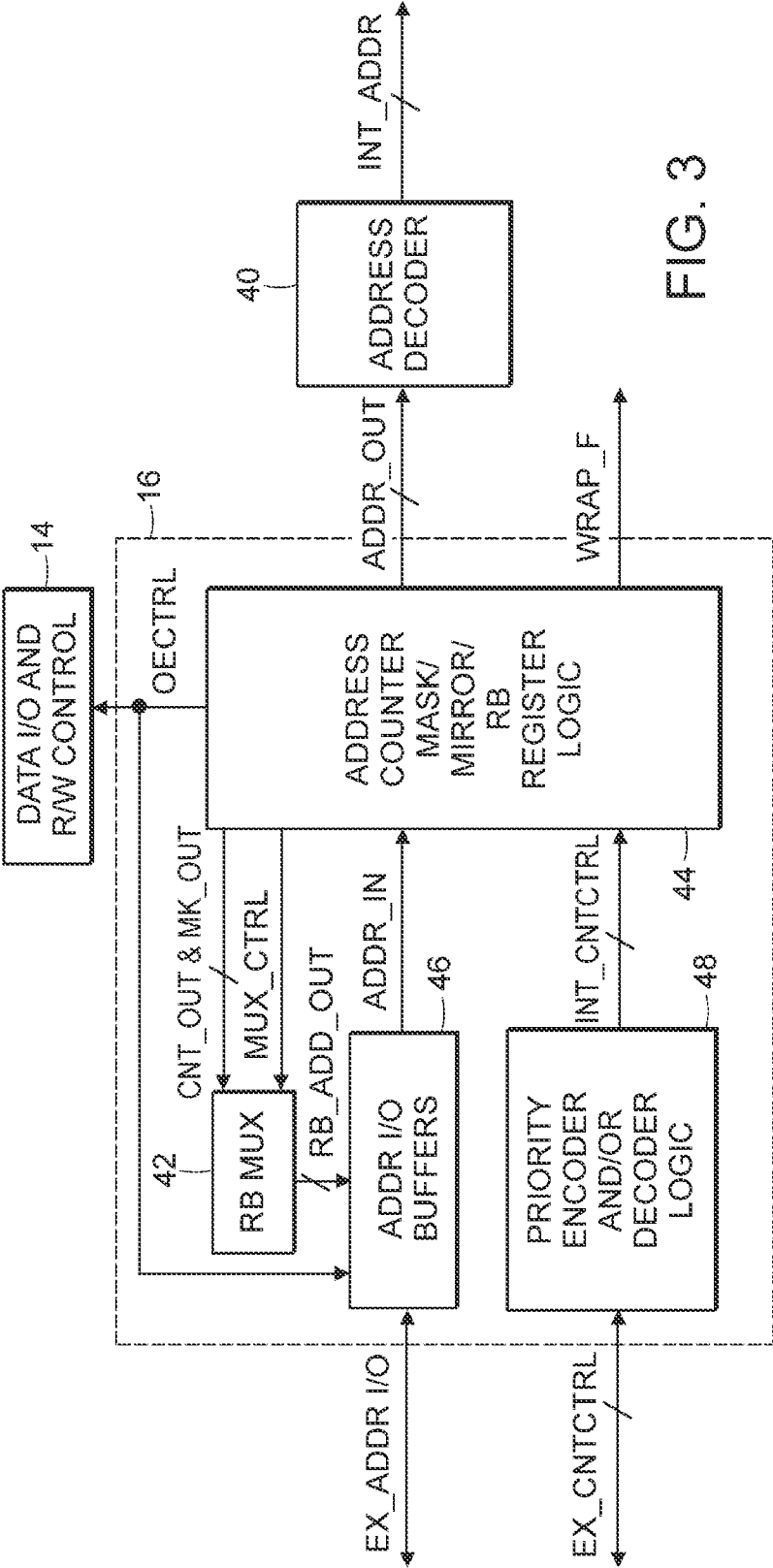
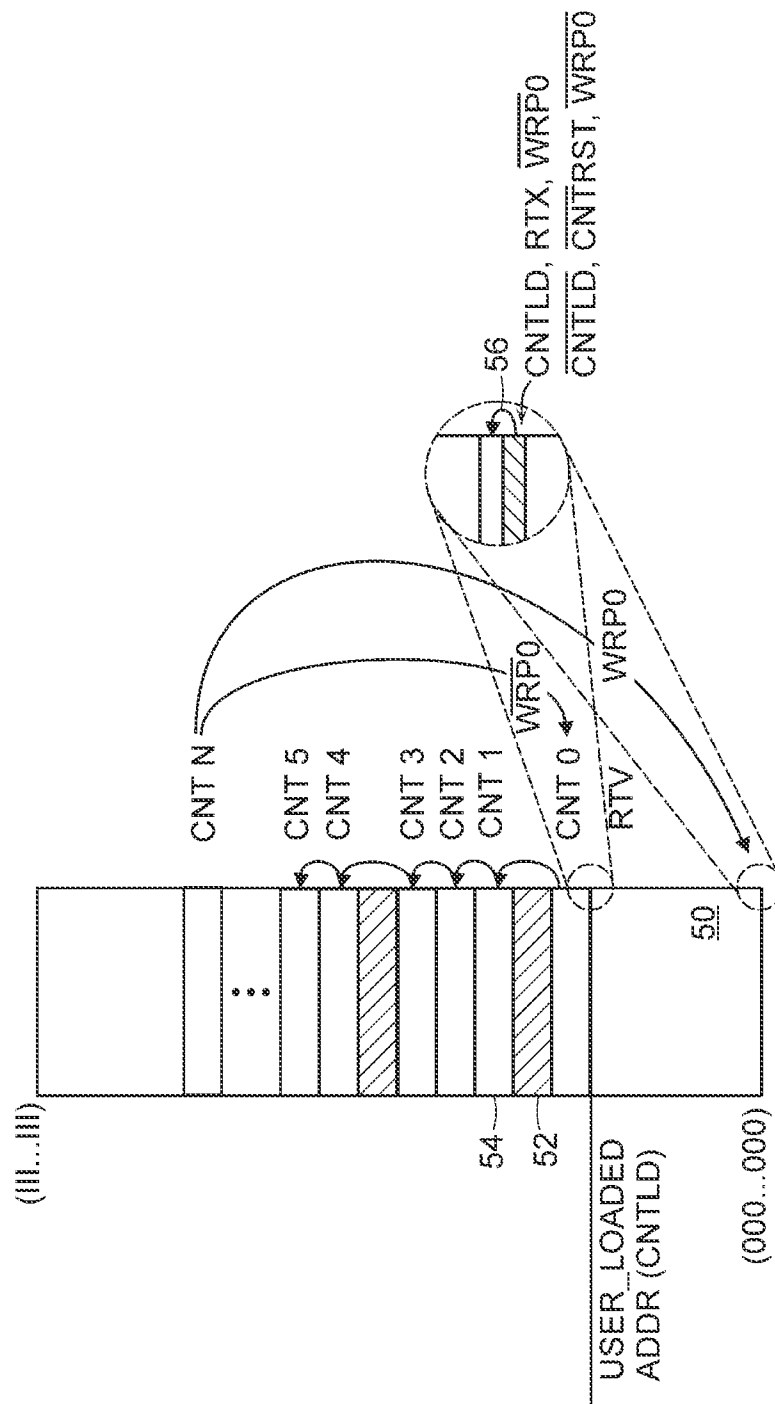


FIG. 3



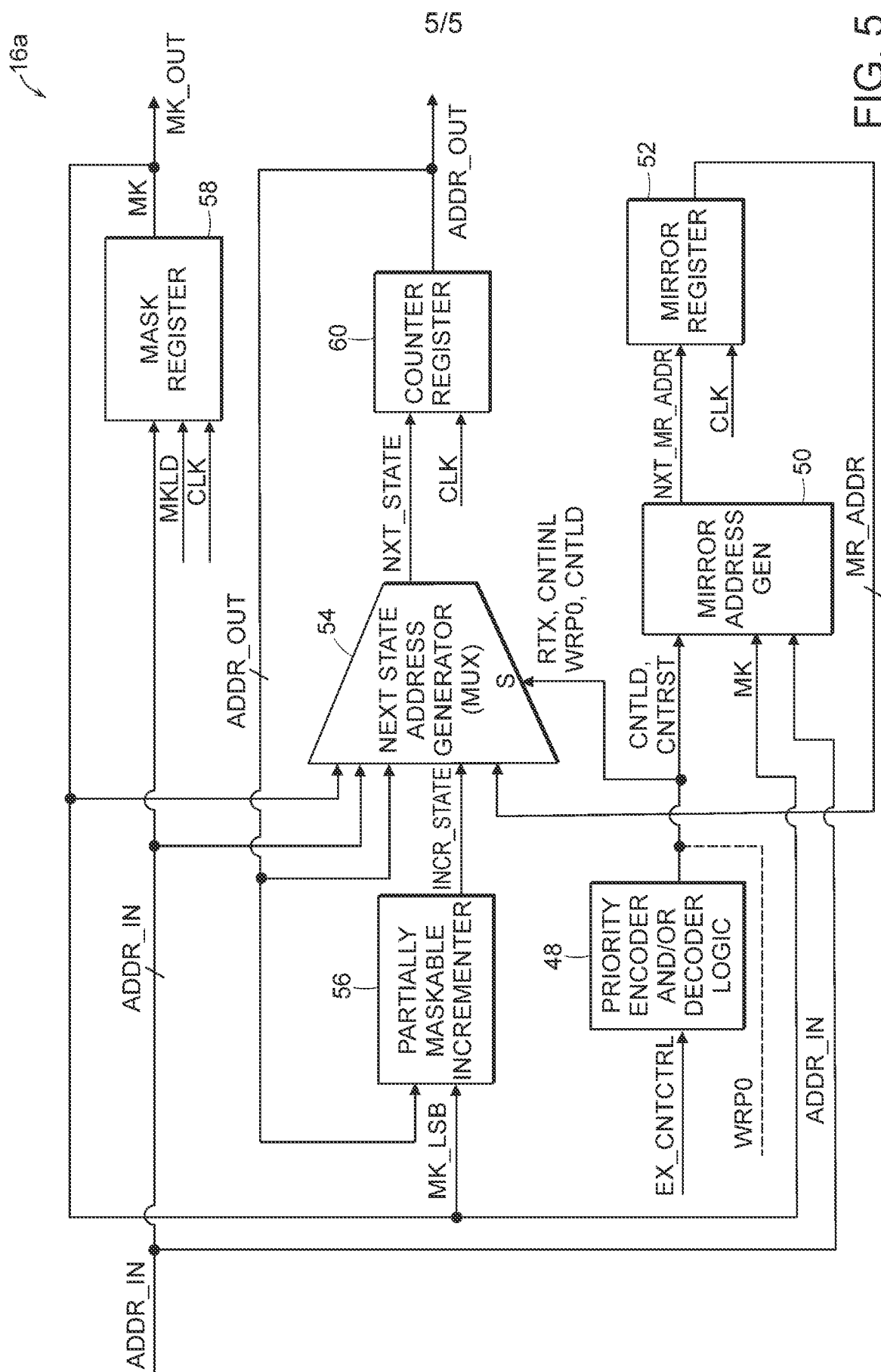


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2007/062433

A. CLASSIFICATION OF SUBJECT MATTER
INV. G11C8/04 G11C7/10

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 304 510 B1 (NOBUNAGA DEAN [US] ET AL) 16 October 2001 (2001-10-16)	1-5, 8-12, 14-16, 19
Y	column 2, line 63 - column 5, line 54; figures 1,2; tables 1,2 column 5, line 66 - column 7, line 57; figures 5-7	6,7,13, 17,18, 20,21
X	US 6 212 615 B1 (TAKAHASHI HIROYUKI [JP]) 3 April 2001 (2001-04-03) column 1, line 19 - column 2, line 37; figure 1; tables 1,2 ----- -/--	1-4, 8-12, 14-16, 19

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

- *A* document defining the general state of the art which is not considered to be of particular relevance
- *E* earlier document but published on or after the international filing date
- *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- *O* document referring to an oral disclosure, use, exhibition or other means
- *P* document published prior to the international filing date but later than the priority date claimed

- *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- *&* document member of the same patent family

Date of the actual completion of the international search

13 July 2007

Date of mailing of the international search report

23/07/2007

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

BALAGUER LOPEZ, J

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2007/062433

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 782 467 B1 (REZEANU STEFAN-CRISTIAN [US]) 24 August 2004 (2004-08-24) cited in the application column 2, line 52 - column 3, line 30; figure 1	1-21
Y	column 3, line 31 - column 7, line 54; figures 2,3; table 1	20,21
A	US 6 789 180 B1 (REZEANU STEFAN-CRISTIAN [US]) 7 September 2004 (2004-09-07) cited in the application column 3, line 44 - column 4, line 49; figure 2	1-21
Y	column 4, line 50 - column 9, line 32; figures 3-5; tables 1,2	6,7,13, 17,18
A	US 6 011 751 A (HIRABAYASHI OSAMU [JP]) 4 January 2000 (2000-01-04) column 2, line 16 - column 3, line 39; figures 1-4 column 2, line 16 - column 3, line 39; figures 1-4 column 7, line 10 - column 8, line 2; figure 7 column 21, line 58 - column 23, line 39; figure 22	1-21
A	US 5 311 468 A (ANDERSON DANIEL F [US]) 10 May 1994 (1994-05-10) column 8, line 1 - column 9, line 26; figure 4	1-21
A	US 6 031 785 A (PARK HEE-CHOUL [KR] ET AL) 29 February 2000 (2000-02-29) column 1, line 14 - column 2, line 54; figure 1	1-21
A	US 6 075 748 A (BHULLAR GURPREET [CA]) 13 June 2000 (2000-06-13) column 2, line 27 - column 4, line 67; figure 1	1-21

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2007/062433

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6304510	B1	16-10-2001	NONE
US 6212615	B1	03-04-2001	CN 1188934 A 29-07-1998 JP 3748648 B2 22-02-2006 JP 10188566 A 21-07-1998 TW 385391 B 21-03-2000
US 6782467	B1	24-08-2004	NONE
US 6789180	B1	07-09-2004	NONE
US 6011751	A	04-01-2000	JP 3386705 B2 17-03-2003 JP 11191292 A 13-07-1999
US 5311468	A	10-05-1994	JP 6208787 A 26-07-1994
US 6031785	A	29-02-2000	JP 10289588 A 27-10-1998
US 6075748	A	13-06-2000	NONE