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Hatano et al.

[11] **3,761,766**

[45] **Sept. 25, 1973**

[54] **ELECTRONIC INDICIA DISPLAY SYSTEM**

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[22] Filed: **Nov. 26, 1971**

[21] Appl. No.: **202,474**

[30] **Foreign Application Priority Data**

Nov. 25, 1970 Japan 45/104275

[52] **U.S. Cl.** ..... **315/84.6,** 315/84.5, 315/169 R, 315/169 TV, 340/336

[51] **Int. Cl.** **H01j 17/36,** G09b 13/00

[58] **Field of Search** ..... 315/84.5, 169 R, 315/169 TV, 84.6; 340/336

[56] **References Cited**

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Primary Examiner—Roy Lake
Assistant Examiner—Lawrence J. Dahl
Attorney—Craig, Antonelli & Hill

[57] **ABSTRACT**

An electronic indicia display system having a plurality of figure indicating discharge tubes wherein an improvement is made to eliminate unnecessary luminance of one or more anode segments which results from the pulse deformation. To this end, the generation and termination of either the input signal to the anodes or the input signal to the grid of the tube is delayed and accelerated, respectively, with respect to the other input signal.

13 Claims, 8 Drawing Figures

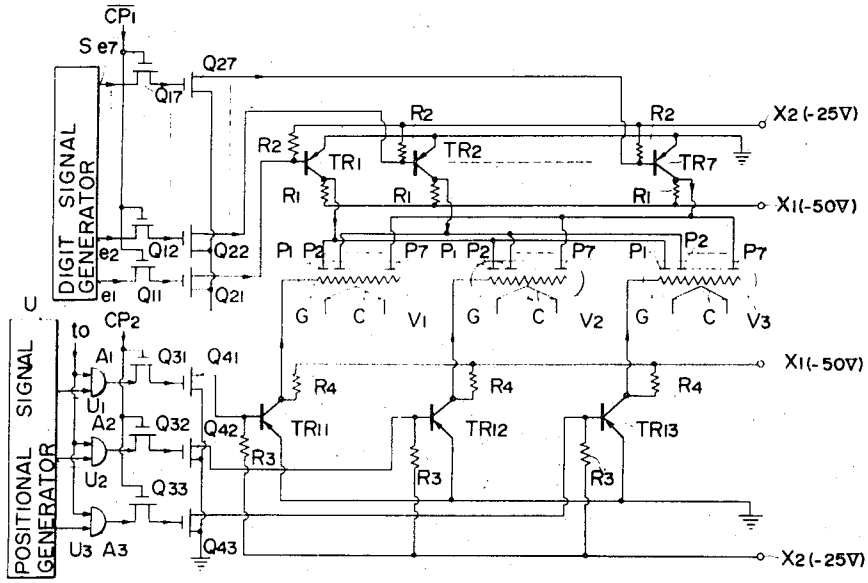


FIG. 1 Prior Art

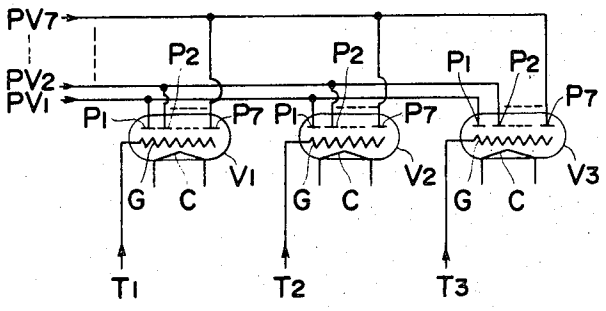


FIG. 2 Prior Art

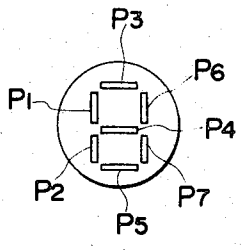


FIG. 3 Prior Art

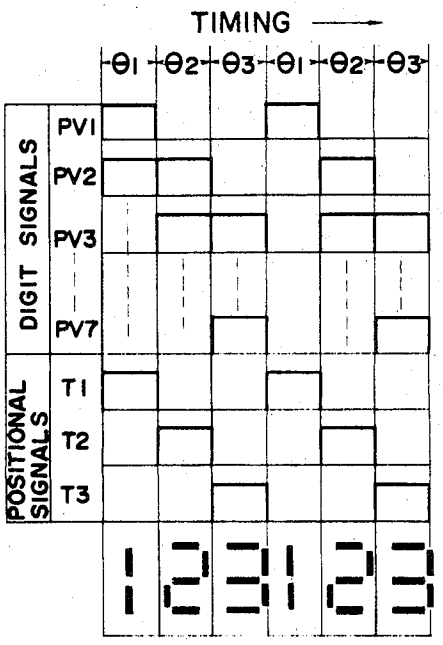


FIG. 4 Prior Art

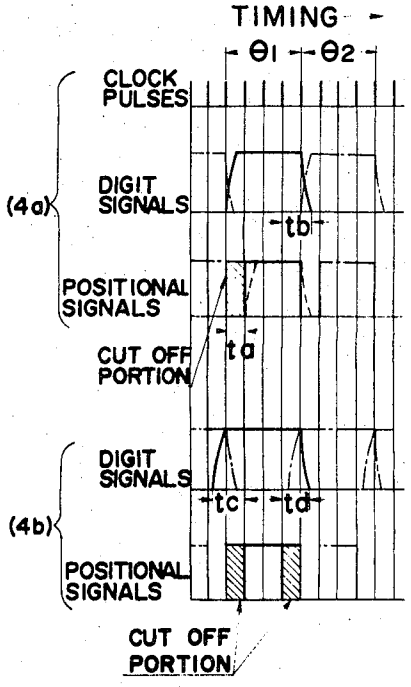
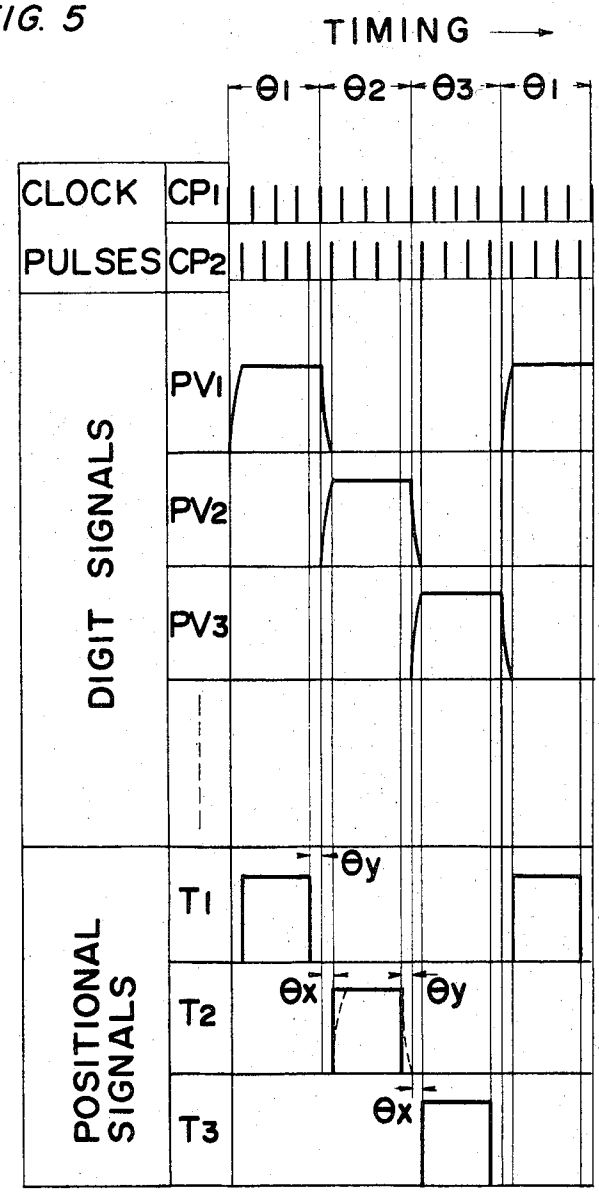


FIG. 5


TIMING
θ1
θ2
θ3
θ1
CLOCK PULSES
CP1
CP2
DIGIT SIGNALS
PV1
PV2
PV3
POSITIONAL SIGNALS
T1
T2
T3
θy
θx
θy
θx

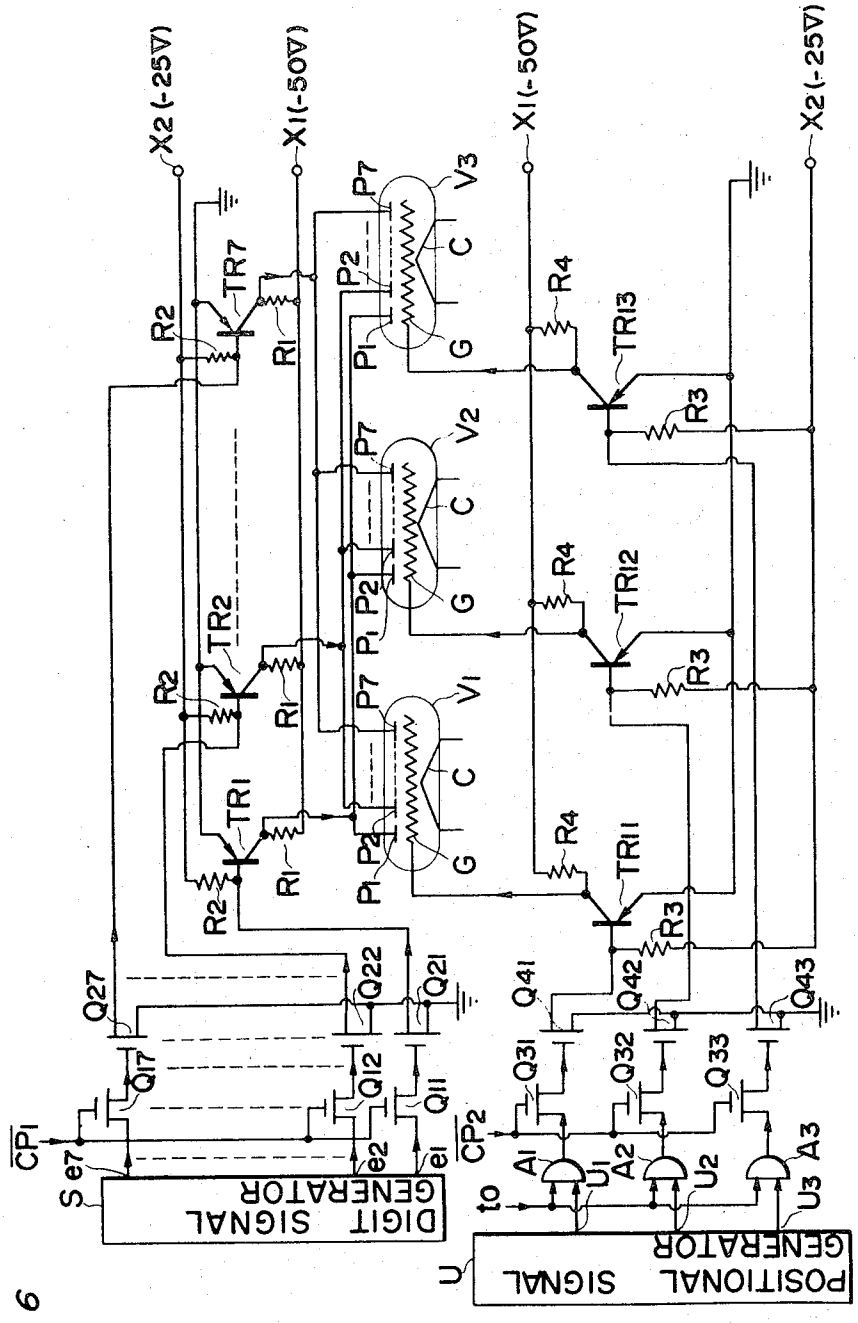

X2 (-25V)
X1 (-50V)
X1 (-50V)
X2 (-25V)
TR7
TR2
TR1
TR13
TR12
TR11
R1
R2
R3
R4
P1
P2
P7
V1
V2
V3
C
G
Q27
Q22
Q21
Q17
Q12
Q11
Q41
Q42
Q43
Q31
Q32
Q33
CP1
CP2
S e7
e2
e1
A1
A2
A3
U1
U2
U3
to U
DIGIT SIGNAL GENERATOR
POSITIONAL SIGNAL GENERATOR

FIG. 6

FIG. 8

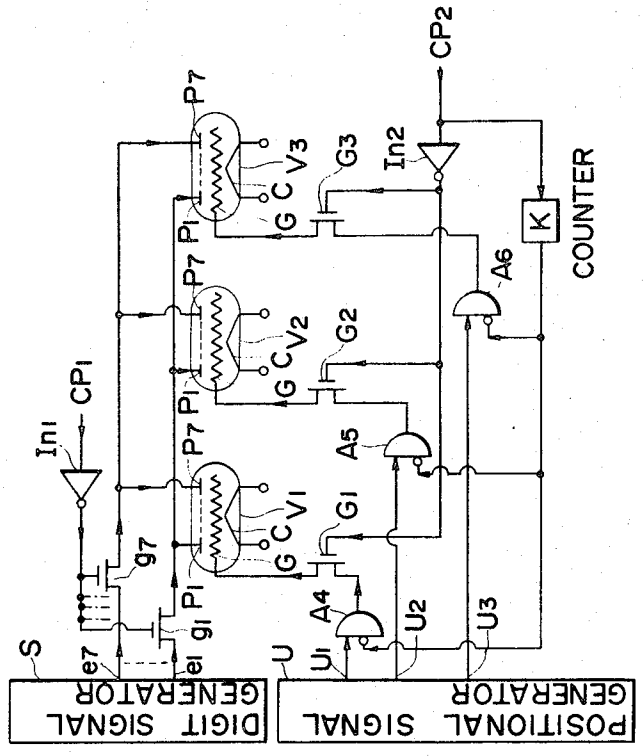
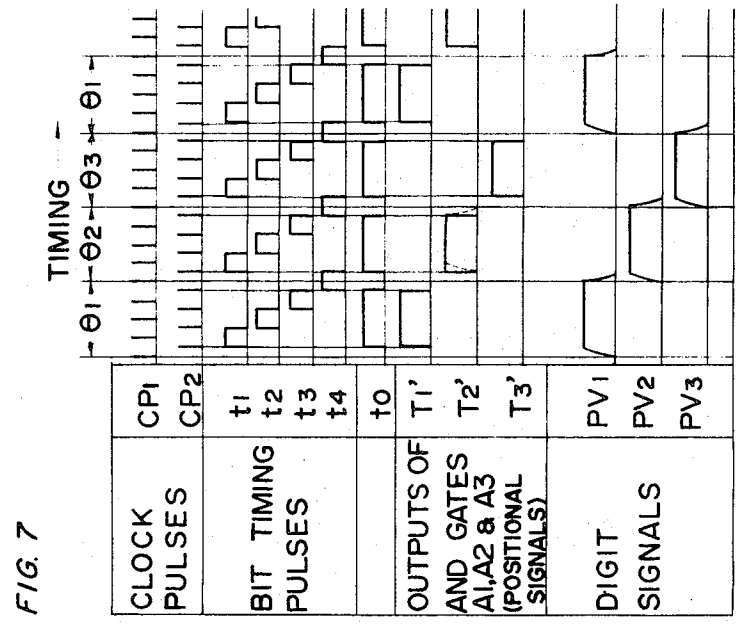

DIGIT SIGNAL GENERATOR
POSITIONAL SIGNAL GENERATOR
COUNTER
CP1
CP2
In1
In2
P7
P1
V1
V2
V3
G1
G2
G3
A4
A5
A6
K
S
U
e7
e1
g7
g1
U1
U2
U3

FIG. 7


TIMING
θ1 θ2 θ3 θ1
CLOCK PULSES
CP1
CP2
BIT TIMING PULSES
t1
t2
t3
t4
t0
OUTPUTS OF AND GATES A1,A2 & A3 (POSITIONAL SIGNALS)
T1'
T2'
T3'
DIGIT SIGNALS
PV1
PV2
PV3

ELECTRONIC INDICIA DISPLAY SYSTEM

The present invention relates to an improved indicating system and, more particularly, to an improved indicia display device having a plurality of figure indicating discharge tubes wherein the provision has been made for eliminating the luminance interference in which condition two figures to be successively illuminated by means of adjacently located different discharge tubes are illuminated in a superimposed manner.

Before the description proceeds, the term "luminance interference" as hereinabove and hereinafter employed will be defined.

As is well known to those skilled in the art, a figure indicating discharge tube largely employed in an indicia display device of, for example, an electronic desk-top calculator or the like is generally in the form of a triode having a filament or cathode C, a plurality of anode segments P_1, P_2, . . . and P_7 arranged to display predetermined indicia and a grid G for controlling the flow of electrons from the cathode C to the anode segments P_1, P_2, . . . P_7, such as shown in FIGS. **1** and **2**. All of these elements of the discharge tube are enclosed within an inert gas filled envelope (not shown) with a necessary number of lead wires (not shown) extending from these elements to the outside of the envelope. In operation, a suitable voltage is applied to the cathode C to cause it to emit electrons toward the anode segments. The electrons thus emitted are accelerated and caused to diverge by the grid G and upon energizing one or more of the anode segments the electrons uniformly bombard the energized anode segments and cause them to luminesce. This operation of a figure indicating discharge tube is well known in the art and, therefore, the details thereof are herein omitted for the sake of brevity. However, it is to be noted that a potential used to energize one or more of the anode segments and a high potential applied to the grid G relative to the cathode potential are hereinafter referred to as "digit signal" and "positional signal," respectively.

In practice, the indicia display device, for example, in an electronic desk-top calculator, is generally provided with a plurality of figure indicating discharge tubes of the above construction, each of these discharge tubes having its own position with respect to a number of digits constituting a decimal number. For example, if a decimal number having up to three digits is to be represented through the indicia display device, a corresponding number of figure indicating discharge tubes is sufficient, as indicated by V_1, V_2 and V_3 in FIG. **1**.

In the display device of 3-digit display capacity above referred to, when a decimal number "**123**" is to be displayed, a digit signal corresponding to any one of the digits of the decimal number, for example, a digit signal corresponding to the most significant digit "**1**" is first applied to each of the discharge tubes V_1, V_2 and V_3 to energize the anode segments P_1 and P_2 shaped to represent the digit "**1**" as shown in FIG. **2**, during a time period θ_1 as shown in FIG. **3**, while a positional signal T1 is applied only to the grid G of one of the tubes which is located so as to display the most significant digit. In this condition, even though the digit signal is applied in common to the discharge tubes V_1, V_2 and V_3, only one of the tubes can be illuminated to represent the digit "**1**" upon application of the positional signal T1 to the grid G thereof.

Subsequently, during a time period θ_2, a digit signal corresponding to the next most significant digit "**2**" is applied to each of the discharge tubes V_1, V_2 and V_3 to energize the anode segments P_3, P_6, P_4, P_2 and P_5 while a positional signal T2 is applied only to the grid G of the tube V_2 located so as to display the next most significant digit. Similarly, during a time period θ_3 and upon application of a positional signal T3 to the grid G of the tube V_3, the least significant digit "**3**" can be displayed through the tube V_3.

As long as the operation of each of the discharge tubes V_1, V_2 and V_3 as hereinbefore described is repeated many times per second in different time periods and in a rapid sequence, the human eyes have a tendency to perceive the decimal number "**123**" displayed by the indicia display device.

FIG. **3** shows ideal waveforms of the digit signals and positional signals with respect to various periods of time, wherein none of these waveforms is deformed. However, according to the prior art, it has been, in fact, found that the digit signal generated during the time period θ_1 or θ_2 exists in the region of the time period θ_2 or θ_1, respectively, such as shown in FIG. **4**. In such a case, in view of the fact that the digit signal corresponding to the digit "**2**" is applied to the tubes during the time period θ_2, while the digit signal corresponding to the digit "**1**" has been applied thereto, the tube V_2 by which the decimal digit "**2**" is to be displayed through the anode segments P_3, P_6, P_4, P_2 and P_5 displays the digit "**2**" superimposed with the digit "**1**" in which condition the anode segment P_1 is unnecessarily caused to luminisce. As long as the operation of the tube V_2 is repeated in such a way as hereinbefore described, although the intensity of light transmitted by the anode segment P_1 of the tube V_2 is somewhat lower than that of each of the anode segments representing the digit "**2,**" the superimposed figures of the digits "**2**" and "**1**" can be perceived by the human eyes. Such occurrence is herein defined as "luminance interference." In other words, the term" luminance interference " stands for the occurrence in which a certain figure indicating discharge tube displays a digit superimposed with a different digit which is to be displayed through another figure indicating discharge tube located right or left to the discharge tube which has displayed the superimposed digits.

Once the luminance interference occurs between two adjacently located figure indicating discharge tubes in a manner as hereinbefore described, an exact individual number displayed by the display device cannot be read off by the operator.

One reason for deformation in the waveform of either the digit signal or the positional signal with respect to the other is because of the rise and fall of the pulses are respectively delayed. Once the waveform of the positional signal is deformed, an inclined trailing edge of the waveform is placed in a superimposed relation to an inclined leading edge of the waveform of the subsequently applied digit signal, resulting in the occurrence of the luminance interference. Whether the digit signal or the positional signal is delayed in phase depends upon time constants or other factors of circuit elements employed in circuits for generating the digit and positional signals and circuits to be driven by these signals.

However, in the event that the problem is the phase deformation such as shown in FIG. **4** (a), elimination the luminance interference can be accomplished by

cutting off one-fourth of a cycle, as indicated by portion ta, of the positional signal in each time period at the beginning of the duration of the positional signal or cutting one-fourth of a cycle, as indicated by portion tb, of the digit signal in each time period at the termination of the duration of the digit signal.

On the other hand, in the event that the problem is such as shown in FIG. 4 (b), wherein the leading and trailing edges of the waveform of either the digit signal (as shown in FIG. 4 (b)) or the positional signal in one time period exist in the regions of the previous and following time periods, respectively, cutting off of either of the leading and trailing edges tc or td cannot eliminate the luminance interference. This is, because in this condition, the luminance interference occurs among three figure indicating discharge tubes, two of which are positioned on the both sides of the remaining one. The only method to eliminate the luminance interference in this case is to cut off each tube one-fourth of a cycle of the digit signal or the positional signal at the beginning and termination of the duration of said signal.

However, if the both ends of the duration of the digit or positional signal is cut off as hereinbefore described, a period of time in which the figure indicating discharge tube is illuminated will be reduced and, as a result thereof, the operator of the display device will find it difficult to identify the number displayed.

Although in FIG. 4(a) the positional signal has been shown in the form of an ideal waveform, the luminance interference will be brought about substantially in the same way as brought about by the deformed digit signal at the end of the duration of said digit signal, if the waveform of the positional signal is deformed as indicated by the dotted lines in FIG. 4(a). Even in this case, portions of the waveform of the deformed positional signal should be preferably cut off in a similar manner as hereinbefore described and such as shown in FIG. 4(b).

Attention is now directed to the reason that one-fourth of the duration of a pulse is cut off as hereinbefore described. As is well known by those skilled in the art, the operation of various components of an electronic calculator are synchronized by a clock pulse. In addition, each bit within a 4-binary coded digit framework is represented by the bit timing pulses t_1, t_2, t_3 and t_4 each having a pulse width substantially equal to one cycle of a clock pulse. In an electronic calculator of this character, the digit signal and the positional signal, as hereinabove referred to corresponding to each decimal digit, are produced in response to each four cycles of the clock pulses. In this arrangement, in order to eliminate the luminance interference, it has been considered to be desirable to utilize the clock pulse in cutting off a portion of the waveform of the digit or positional signal, this portion corresponding to one cycle of the clock pulse or substantially equal to the duration of one bit timing pulse, rather than cutting off that portion of the waveform over an arbitrary duration. Although it seems that cutting off the waveform in a portion crresponding to one cycle of the clock pulse is excessive, there has been found an advantage in that the calculator can be simplified in structure without any accompanying reduction in the performance thereof.

As hereinbefore described, according to the conventional method of eliminating luminance interference, the digit signal or the positional signal has been cut off at the leading or trailing edge thereof in such a way that the cut-off portion of the signal corresponds with one cycle of the clock pulse. However, the extent of displacement between the digit signal and the positional signal and the direction of such displacement vary depending upon the time constants or other factors of the circuit elements, which cannot be easily predicted at the time of design. Furthermore, in view of the fact that even the time constants of each circuit element varies depending upon the design of the circuit element, the manner in which the both signals are displaced with respect to each other varies even though two circuit components are manufactured according to the same design.

In view of the foregoing, according to the prior art display device, the luminance interference cannot be eliminated unless the manner of displacement is otherwise predicted.

Accordingly, one essential object of the present invention is to provide an improved indicia display system including a plurality of figure indiciating discharge tubes wherein means for eliminating the luminance interference is provided.

Another object of the present invention is to provide an improved indicia display system of the type above referred to wherein the clock pulse employed in synchronizing the operations of circuit components of an electronic calculator is utilized to cut off each portion of the waveform of the digit or positional signal at the beginning and termination of the duration of the signal, each cut-off portion corresponding with a half cycle of the clock pulse.

These and other objects and features of the present invention will become apparent from the following description made in conjunction with preferred embodiments thereof with reference to the accompanying drawings, in which;

FIG. 1 is a schematic circuit diagram showing the prior art arrangement of an indicia display device of similar character;

FIG. 2 is a schematic diagram showing an arrangement of anode segments used in a figure indicating tube shaped to represent any one of decimal digits zero through nine;

FIG. 3 is a schematic diagram showing various waveforms of the digit signal and the positional signal;

FIG. 4 is a schematic diagram showing the deformed waveforms of the digit signal and the positional signal;

FIG. 5 is a schematic diagram showing waveforms of the digit signal and the positional signal achieved by the present invention;

FIG. 6 is a circuit diagram of one preferred embodiment of the present invention;

FIG. 7 is a schematic diagram showing waveforms of various signals employed in an essential portion of FIG. 6, and

FIG. 8 is a circuit diagram of another preferred embodiment of the present invention.

Referring first to FIG. 5, digit signals PV_1, PV_2, PV_3 and so on are each controlled by a first clock pulse CP1 so that the duration of each of said digit signals is rendered to be substantially equal to four cycles of said first clock pulse CP1. In other words, each of the digit signals is generated at an interval of four cycles of the first clock pulse CP1.

Similarly, each of the positional signals T1, T2, T3 and so on is generated at an interval of three cycles of

a second clock pulse CP2 of which the duration is substantially equal to that of said first clock pulse CP1, but displaced in phase a half cycle with respect to the latter.

Accordingly, it is clear that the positional signals T1, T2, T3 and so on are generated a half cycle of the first clock pulse CP1 after the digit signals have been generated. Namely, during a certain time period, the positional signal is generated in response to a first cycle of the clock pulse CP2 and ceases in response to the end of the third cycle of the clock pulse CP2. In this case, the waveform of the positional signal represents each portion of the waveform thereof corresponding with a half cycle of the clock pulse CP1 substantially cut off, as indicated by θ_x and θ_y, at the beginning and termination of the duration of said positional signal, respectively. Therefore, even though the leading and trailing edges of the waveform of the digit signal in one time period exist in the regions of different time periods due to the pulse deformation of said signal substantially as shown in FIG. 5, no positional signal is applied to the grid of the figure indicating discharge tube at the beginning and termination of the relevant time period, the period of which is substantially equal to half cycle θ_x or θ_y of the clock pulse. Accordingly, during this half cycle, no discharge tube can be illuminated even though the voltage has been applied to the anode segment without accompanying the luminance interference.

In such a case, the period in which the figure indicating discharge tube is prevented from being illuminated is substantially equal to the duration of the bit timing pulse and no reduction in the intensity of light transmitted from the discharge takes place as compared with the conventional tube. In addition, since each portion of the positional signal is cut off at the leading and trailing edges of the waveform thereof, elimination of the luminance interference can be ensured regardless of the direction of displacement of the waveform of the positional signal with respect to the digit signal, vice versa. It is to be noted that, instead of the positional signal, each portion of the digit signal may be cut off at the leading and trailing edges of the waveform thereof.

FIG. 6 shows a circuit diagram in which the signal thus processed as hereinbefore described are utilized. However, it is to be noted that, for the sake of brevity, description will be made in connection with the display device having three figure indicating discharge tubes V_1, V_2 and V_3 the cathode potential of each of which is maintained at −50 volt.

Referring now to FIG. 6, reference character S indicates a digit signal generator capable of generating a digit signal having a square waveform during each time period in synchronism with the clock pulse CP1 upon receipt of an output signal from a decoder (not shown) of an electronic calculator, said output signal being indicative of a converted decimal number. This digit signal generator S is provided with a plurality of output terminals e_1, e_2, . . . and e_7 individually connected with the gates of MOS transistors Q_{21}, Q_{22}, . . . and Q_{27}, each serving as an inverter, through different MOS transistor Q_{11}, Q_{12}, . . . and Q_{17}, respectively, the gate of each of said transistors Q_{11}, Q_{12}, . . . and Q_{17} being adapted to receive the clock pulse CP1.

The source of each of the transistors Q_{21}, Q_{22}, . . . and Q_{27} is grounded while the drain thereof is connected with the base of each of tube driving transistors TR1, TR2, . . . and TR3 of PNP type, each of said driving transistors being adapted to control the voltage to be supplied to the anode segments P_1, P_2, . . and P_7 of the discharge tubes V_1, V_2 or V_3. The collector of each of said tube driving transistors TR1, TR2, . . . and TR7 is connected with the anode sigments of each discharge tube and on the other hand with, for example, a −50 volt power source X1 through resistor R_1. The emitter of each transistor TR1, TR2, . . . and TR7 is grounded while the base thereof is connected with, for example, a −25 volt power source X2 through resistor R_2.

Reference character U indicates a positional signal generator capable of generating in succession positional signals T1, T2 and T3 during respective time periods θ_1, θ_2 and θ_3 in synchronism with the clock pulse CP1. This positional signal generator is provided with a plurality of output terminals U_1, U_2 and U_3 connected with first input terminals of AND gates A_1, A_2 and A_3, respectively. These AND gates A_1, A_2 and A_3 have other second input terminals, respectively, to which a timing pulse t_0 can be commonly applied from a suitable source of the timing pulse, output terminals of which are respectively connected with the gates of MOS transistors Q_{41}, Q_{42} and Q_{43} through MOS transistors Q_{31}, Q_{32} and Q_{33}. The gate of each transistor Q_{31}, Q_{32} and Q_{33} is adapted to receive the clock pulse CP2 from a suitable source.

The timing pulse t_0 has a duration substantially equal to the sum of the durations of bit timing pulses t_1, t_2 and t_3 as shown in FIG. 7, the bit timing pulses t_1, t_2, t_3 and t_4 being generated in synchronism with the clock pulses CP2.

The source of each of the MOS transistors Q_{41}, Q_{42} and Q_{43} is grounded while the drain thereof is connected with the base of each PNP transistor TR11, TR12 and TR13 having respective emitters connected with the ground. The base of each transistor Q_{41}, Q_{42} and Q_{43} is connected with the power source X2 through resistors R_3.

The collectors of the transistors TR11, TR12 and TR13 are connected with respective grids of the discharge tubes V_1, V_2 and V_3 and, on the other hand, with the power source X1 through the resistors R_4, respectively.

While in the arrangement as hereinbefore described, unless no output signal is otherwise generated from the digit signal generator S, namely, as long as the voltages at the output terminals e_1, e_2, . . . and e_7 of the generator S are negative, the transistors Q_{11}, Q_{12}, . . . and Q_{17} can be switched on by the clock pulse CP1. On the other hand, the negative voltages at the terminals e_1, e_2, . . . and e_7 of the generator S can be supplied to the gates of the transistors Q_{21}, Q_{22}, . . . and Q_{27} to thereby switch on these transistors. Accordingly, the voltage at the base of each of the tube driving transistors TR1, TR2, . . . and TR7 becomes zero so that the driving transistors can be maintained in the non-conductive state. Therefore, the anode segments P1, P2, . . . and P7 of each of the figure indicating discharge tubes V_1, V_2 and V_3 are applied with a potential of −50 volts and no luminance thereof take place.

However, in the event that a digit signal is generated through one, for example, e_1, of the output terminals of the generator S during the time period θ_1, namely, when the voltage at the output terminal e_1 is zero volts, the transistor Q_{11} can be switched on, upon receipt of the clock pulse CP1 and, as a result thereof, the voltage at the gate of the transistor Q_{21} becomes zero. Accord-

ingly, the transistor Q_{21} can be switched off by the output of the transistor Q_{11} applied to the gate of said transistor Q_{21} and the transistor TR1 can be brought into the conductive state. Therefore, the anode segment P_1 of each discharge tube receives zero volts.

It is to be noted that, even if output signals are generated from the other output terminals of the digit signal generator S, the above-mentioned similar process takes place to thereby apply zero volts to one or more of the anode segments. In addition, the same may apply during any one of the other time periods θ_2 and θ_3.

On the other hand, during the time periods θ_1 and θ_2 and θ_3, the positional signals T1, T2 and T3 can be successively generated from the output terminals U_1, U_2 and U_3 of the positional signal generator U, respectively, which are, in turn, applied to the first input terminals of the AND gates A1, A2 and A3. Since these AND gates are adapted to receive the timing pulse t_0 through their second input terminals, they can be triggered "on" during different time periods θ_1, θ_2 and θ_3, to thereby generate an output signal. The output signal from each AND gate, as indicated by T1', T2' and T3' in FIG. 7, is in the form of pulse synchronized with the clock pulse Cp2, but delayed half a cycle of the clock pulse after the potential at the anode segment P1 has become zero. However, this pulse T1', T2' or T3' has a duration substantially equal to the sum of the durations of three bit timing pulses, such as shown in FIG. 7. From FIG. 7, it is also clear that, as compared with the digit signal corresponding to one decimal digit, the duration of each of the output pulses T1', T2' and T3' or the positional signals that have passed through the respective AND gates A1, A2 and A3 begins at a time delayed ½ cycle of the clock pulse and ends at the time one-half cycle earlier than the clock pulse diminishes.

When the output T1' has been generated from the corresponding AND gate A1, this can be, in turn, applied to the gate of the MOS transistor Q_{41} through the MOS transistor Q_{31} that has been brought into the conductive state by the clock pulse CP2. The transistor Q_{41} is then brought into the non-conductive state as long as the signal T1' is applied thereto, to thereby cause the transistor TR_{11} to conduct and, accordingly, the potential at the grid of the tube V_1 becomes zero volts. At this time, as long as the condition above mentioned is established, the figure indicating discharge tube V_1 can be illuminated.

Similarly, upon conduction of the transistors TR_{12} and TR_{13} during different time periods θ_2 and θ_3, the discharge tubes V_2 and V_3 can be respectively illuminated without accompanying the luminance interference.

From the foregoing description, it is clear that, since portions of the waveform of each positional signal has been cut off at the beginning and termination of the corresponding timing, each of said portions being substantially equal to ½ cycle of the clock pulse, elimination of the luminance interference can be advantageously ensured.

Referring now to FIG. 8, another embodiment of the present invention is shown as having three figure indicating discharge tubes V_1, V_2 and V_3 in an arrangement similar to FIG. 6. Reference character S indicates a digit signal generator capable of generating a digit signal having a square waveform during each time period in synchronism with the clock pulse CP1 upon receipt of an output signal from a decoder (not shown) of an electronic calculator, said output signal being indicative of a converted decimal number. Reference characters g_1 through g_7 indicate MOS transistors inserted between the output terminals of the generator S and the anode segments of each of the discharge tubes V_1, V_2 and V_3. The first clock pulse CP1 is adapted to be impressed through an inverter In_1 upon each MOS transistor g_1 through g_7. Each transistor g_1 through g_7 is to conduct during each pulse interval of the clock pulse CP1. At this time, one or more outputs of the generator S are applied to the corresponding anode segments of each tube.

Reference character U indicates a positional signal generator, the operation of which is synchronized with the second clock pulse CP2 and outputs therefrom are generated every four pulses of the clock pulses CP2 through respective terminals U_1, U_2 and U_3 to thereby impress a positive voltage, at different time periods, upon the grids of the tubes V_1, V_2 and V_3. Inhibit gates A_4, A_5 and A_6 are disposed between the positional signal generator U and the grid of each of the discharge tubes. The output of a four-scale counter K, in which the clock pulses CP2 are counted and the output is produced every four pulses, is connected with the input terminals of each inhibit gate A_4, A_5 and A_6, so that these gates can generate respective outputs, unless the counter K otherwise completes its counting operation up to the number four. MOS transistors G1, G2 and G3, each serving as a gating element, are inserted between the output of each inhibit gate A_4, A_5 and A_6 and each grid of the discharge tubes V_1, V_2 and V_3. The gate of each of the MOS transistor G1, G2 and G3 is connected with another inverter In_2 capable of inverting the clock pulse CP2 so that, as long as the clock pulse CP2 is not applied to the inverter In_2, the output of said inverter will be [1] thereby to trigger the transistors G1, G2 and G3 on during different time periods.

Hereinafter, the operation of the arrangement shown in FIG. 8 will be described on the assumption that the decimal number "123" is to be displayed through the figure indicating discharge tubes V_1, V_2 and V_3, where the tube V_3 is in the least significant position.

During the time period θ_1, digit signals can be generated from the generator S through its output terminals e_1 and e_2 which are, in turn, applied to the anode segments P_1 and P_2 of each of the figure indicating discharge tubes V_1, V_2 and V_3. On the other hand, during the same time period, a positional signal T1 can be generated from the output terminal U_1 of the positional signal generator U, which is, in turn, applied to the inhibit gate A_4. However, this signal from the generator U is delayed ½ cycle of the clock pulse CP1 with respect to the digit signal, as mentioned above.

The counter K upon receipt of the clock pulse CP2 commences to count the number of pulses. However, no output signal is generated from the counter K unless the number of pulses counted thereby exceeds three during the time period θ_1 and, accordingly, no signal is applied to the inhibit gate A_4. Under this condition, the gate A_4 is in the conductive state so that the positional signal T1 from the output terminal U_1 of the positional signal generator U can be applied to the source of the MOS transistor G1. This transistor G1 can be brought into conductive state by the signal from the inverter In_2 which is generated during a period in which no clock pulse CP2 is applied to the inverter In_2. Therefore, as long as the gate A_4 and the MOS transistor G1 are re-

spectively in the conductive state, the positional signal can be applied to the grid G of the discharge tube V_1. Thus, upon receipt of this positional signal, the tube V_1 can be illuminated to display a number "1."

Subsequently, upon computation up to four pulses during the same time period θ_1, the counter K generates an output signal to the input terminal of the gate A_4. Upon receipt of the output signal from the counter K, the gate A_4 can be brought into the conductive state which can be maintained until the counter K is reset. During this period, application of the positional signal T1 to the grid G of the discharge tube V_1 can be prohibited and, therefore, this discharge tube V_1 can be brought into an inoperative condition.

In brief, the discharge tube V_1 can be brought into the operative condition ½ cycle of the clock pulse delayed at the beginning of the time period θ_1, can be maintained in the operative condition during three cycles of the clock pulse and finally, can be brought into the inoperative condition ½ cycle earlier than the end of the time period θ_1.

During the subsequent time period θ_2, the generator S generates digit signals indicative of a decimal number "2" through its output terminals e_2, e_3, e_4, e_5 and e_6, which are, in turn, applied to the anode segments P_3, P_6, P_4, P_2 and P_5 of each of the figure indicating discharge tubes V_1, V_2 and V_3.

At this time, it is assumed that the anode segment P_1 is applied with the digit signal from the generator S since each digit signal that have been generated during the previous time period θ_1 exists in the region of the time period θ_2 for a certain period of time, that is, ½ cycle of the clock pulse, due to the pulse deformation as hereinbefore discussed.

On the other hand, the positional signal generator U generates the positional signal T2 in response to the clock pulse CP2 during time period θ_2, which is, in turn, applied to the grid G of the discharge tube V_2 in a similar manner as afforded during the time period θ_1. Of course, even during the time period θ_2, the figure indicating discharge tube V_2 can be operated substantially in the same way as the tube V_1 during the time period θ_2.

In view of the foregoing, since the positional signal generated ½ cycle later than the clock pulse from the beginning of the duration thereof during the time period θ_2 is adapted to be applied to the grid of the discharge tube V_2, no anode segments of any one of the discharge tubes V_1, V_2 and V_3 is illuminated during this ½ cycle of the clock pulse, even though the digit signals have been applied thereto. Accordingly, it is clear that prevention of the anode segment P_1 of the tube V_2 from being illuminated during the time period θ_2 can be advantageously ensured. In addition, even in the case where the digit signal to be generated during the time period θ_2 exists during the previous time period θ_1, due to pulse deformation, no luminance takes place at the anode segments P_3, P_6, P_4, and P_5 of the tube V_1 during the time period θ_1, since the positional signal in time period θ_1 disappears ½ cycle earlier than the clock pulse disappears.

As for the discharge tube V_3, a similar process takes place during the time period θ_3 and substantially the same result as hereinbefore described can be appreciated.

Thus, from the foregoing description, it is apparent that, as long as the above-mentioned operation is repeated in rapid sequence, the number "123" can be displayed and perceived by the human eyes without any difficulty in identifying the number "123."

Although the present invention has been fully disclosed by way of example in conjunction with the preferred embodiment thereof with reference to the accompanying drawings, it is to be noted that various changes and modifications are apparent to those skilled in the art without departing from the scope of the present invention. Therefore, unless otherwise departing from the scope of the present invention, such changes and modifications should be construed as included therein. It is also apparent that, even in the case where the positional signal is deformed as indicated by the dotted lines in FIGS. 5 and 7, the present invention ensures the elimination of the interference.

What we claim is:

1. An indicating system for displaying indicia comprising:
- a plurality of indicating tubes each having a filament, a plurality of anode segments shaped to display predetermined indicia and a grid for controlling the flow of electrons from the filament to the anodes;
- means applying a low potential to said filaments;
- circuit means, interconnected with the anode segments of each indicating tube, for applying a high potential to select anode segments of said tubes in response to a first input signal fed to said circuit means; and
- means, connected with the grids of said indicating tubes, for operating selected tubes, by applying a high potential to the grids of the selected tubes and a low potential to the grids of the other tubes in response to a second input signal fed to said last-mentioned means,
- whereby portions of the waveforms of either one of said first and second input signals respectively applied to said circuit means and said last -mentioned means are cut off at the beginning and termination of time periods allocated to said indicating tubes for a predetermined period of time substantially equal to one-half cycle of a clock pulse used to determine said time periods ; to thereby reduce the pulse width of said cut-off input signals.

2. An indicating system for displaying indicia comprising:
- a plurality of indicating tubes each having a filament, a plurality of anode segments shaped to dsplay predetermined indicia and a grid for controlling the flow of electrons from the filament to the anodes;
- means applying a low potential to said filaments;
- circuit means interconnected with the anode segments for each indicating tube for applying a high potential to selected anode segments of said indicating tubes in response to a first input signal fed to said circuit means;
- means for generating a series of clock pulses;
- first generator means for supplying a digit signal in the form of pules to be coupled to said anode segments of the indicating tubes, each of said pulses being generated therefrom in synchronism with a clock pulse used to determine the duration of time periods allocated to said indicating tubes and having a duration substantially equal to the sum of a number of said clock pulses ;
- first gating means for transmitting said digit signal to said circuit means;

means connected with the grids of said indicating tubes for operating selected tubes by applying a high potential to the grids of the selected tubes and a low potential to the other tubes; second generator means for supplying a positional signal to the grids of the indicating tubes during different time intervals; and

second gating means for transmitting a signal to said second generator means, said last-mentioned signal being generated upon receipt of said positional signal during each time interval from said second generator means one-half cycle of said clock pulse delayed from the beginning of one time interval and capable of terminating one-half cycle of a clock pulse earlier than the end of said time interval.

3. An indicating system as claimed in claim **2**, wherein each of said first gating means comprises a first gating element capable of being triggered on by said clock pulse, to thereby pass therethrough said digit signal and a second gating element capable of applying the output of said first gating element to said circuit means.

4. An indicating system as claimed in claim **2**, wherein each of said second gating means comprises an AND gate having one input terminal adapted to receive the positional signal from the positional signal generator means and another input terminal adapted to receive a signal generated during three cycles of the clock pulse in one time period and another AND gating element adapted to be triggered on by another clock pulse displaced half a cycle relative to the first-mentioned clock pulse for applying the positional signal to the grid of a tube.

5. An indicating system for displaying indicia comprising:

a plurality of indicating tubes each having a filament, a plurality of anode segments shaped to display predetermined indicia and a grid for controlling the flow of electrons from the filament to the anodes;

means for generating a series of clock pulses;

means for applying a low potential to said filament;

first generator means for generating a digit signal in the form of pulses to said anode segments of said indicating tubes, each of said pulses being generated therefrom in synchronism with a clock pulse used to determine the duration of time intervals allocated to said indicating tubes and having a duration substantially equal to the sum of a number of said clock pulses;

a plurality of gating elements each capable of being triggered by a signal in the form of an inverted clock pulse to thereby apply said digit signal to the anode segments of each of the indicating tubes;

a second generator means for supplying a positional signal to the grids of the indicating tubes during different time intervals in response to a second clock pulse which is ½ cycle displaced relative to said first-mentioned clock pulse, said positional signal having a duration substantially equal to that of each time interval;

a counter capable of generating an output signal for every four of said second clock pulses;

a plurality of inhibit gating elements each having one input terminal adapted to receive the positional signal from said second generator means and another input terminal adapted to receive the output signal from said counter; and

a plurality of gating devices each capable of being triggered on by signal corresponding to an inverted second clock pulse to thereby apply an output of said inhibit gating element to each grid of said indicating tubes.

6. An indicating system for displaying indicia comprising:

a plurality of indicating tubes each having a filament, a plurality of anode segments shaped to display predetermined indicia, and a grid for controllint the flow of electrons from the filament to the anodes;

first means for applying a low potential to said filaments;

second means, responsive to a first indicia signal having a prescribed duration, for supplying a high potential to selected anode segments of said tubes; and

third means, coupled to the grids of said tubes, for supplying a control potential to the grids of selected tubes and a low potential to the grids of the other tubes, said third means including control means, responsive to successive indicia signals, for supplying successive energizing signals to the control grids of said plurality of tubes, said energizing signals being supplied to said grids a predetermined period of time delayed by a delay circuit after the initiation of the duration of the signal to be applied to the anode segments, and terminating a second predetermined period of time corresponding to one bit timing earlier than the termination of the duration of said signal to be applied to the anode segments , the length of time between said start and termination of the supply of an energizing signal being sufficient to be integrated by the human eye.

7. An indicating system according to claim **6**, wherein said third means further includes first gate means, responsive to a first series of clock pulses and said first indicia signal, for gating said indicia signal to the grids of said tubes during the receipt of a predetermined number of clock pulses.

8. A system according to claim **7**, wherein said prescribed duration of said first indicia signal corresponds to an integral number of said clock pulses and said predetermined number of clock pulses is less than said integral number of clock pulses.

9. An indicating system according to claim **8**, wherein said first and second predetermined periods of time correspond to a fraction of the period of time of a clock pulse.

10. An indicating system according to claim **7**, wherein said first gating means comprises a plurality of field effect transistors coupled between the grids of said tubes and a set of terminals receiving said clock pulses.

11. An indicating system according to claim **6**, wherein said second means comprises second gate means, responsive to a second series of clock pulses and a series of digital signals for gating said digital signals to said selective anodes.

12. A system according to claim **11**, wherein said first and second series of clock pulses has the same frequency and are delayed with respect to each other by one-half the period of the clock pulse.

13. An indicating system according to claim **12**, wherein each of said first and second gate means comprises a plurality of field effect transistors coupled between terminals receiving said first and second respective series of clock pulses and the grids and anodes of said tubes.

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