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(71) Applicant: **MOTOROLA, INC.** [US/US]; 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

(72) Inventors: **PASSLACK, Matthias**; 5382 West Linda Lane, Chandler, AZ 85226 (US). **HARTIN, Olin, L.**; 4030 East White Aster Street, Phoenix, AZ 85044 (US). **RAY, Marcus**; 8062 South Dateland Drive, Tempe, AZ 85284 (US). **MEDENDORP, Nicholas**; 6898 Meadowlace Court, Santa Barbara, CA 93117 (US).

(74) Agents: **PICKENS, S., Kevin** et al.; MOTOROLA, INC., Intellectual Property Section, 7700 West Parmer Lane, MD: PL02/TX32, Austin, TX 78729 (US).

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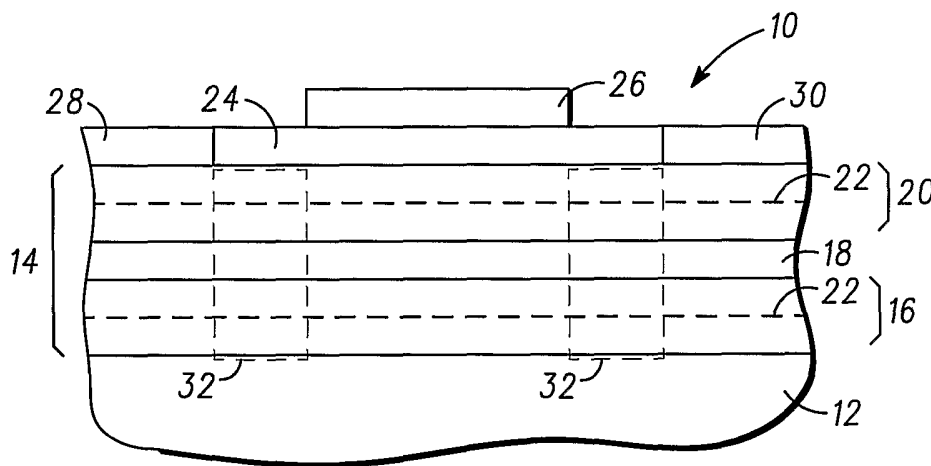
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(54) Title: AN ENHANCEMENT MODE METAL-OXIDE-SEMICONDUCTOR FIELD EFFECT TRANSISTOR AND METHOD FOR FORMING THE SAME



(57) Abstract: An implant-free enhancement mode metal-oxide semiconductor field effect transistor (EMOSFET) is provided. The EMOSFET has a III-V compound semiconductor substrate and an epitaxial layer structure overlying the III-V compound semiconductor substrate. The epitaxial material layer has a channel layer and at least one doped layer. A gate oxide layer overlies the epitaxial layer structure. The EMOSFET further includes a metal gate electrode overlying the gate oxide layer and source and drain ohmic contacts overlying the epitaxial layer structure.

AN ENHANCEMENT MODE METAL-OXIDE-SEMICONDUCTOR FIELD
EFFECT TRANSISTOR AND METHOD FOR FORMING THE SAME

Field of the Invention

5 The present invention relates generally to compound semiconductor field effect devices and more specifically to enhancement mode metal-oxide-compound semiconductor field effect transistors and methods for fabricating the same.

Background of the Invention

10 The enhancement-mode metal-oxide-semiconductor field effect transistor (EMOSFET) is one of the most widely used devices in the design of metal-oxide semiconductor (MOS) integrated circuits. Silicon complementary MOS (CMOS) technology is a mature technology for EMOSFET design, offering simplicity in design and low power consumption. However, Group III-V compound semiconductor
15 technology continues to serve as an attractive technology for EMOSFET design due to its superior speed/power performance and efficiency.

 One class of EMOSFETs is designed with self-aligned ion implants to form low resistivity source and drain extensions. However, manufacturing III-V compound semiconductor EMOSFETs with ion implanted source and drain extensions is
20 difficult. The implant material can act as both a donor or an acceptor depending on its association with either the Group III or the Group V site in the lattice, respectively. Further, annealing temperatures used to form the source and drain extensions, typically higher than 700°C in n-channel devices, may be incompatible with the semiconductor/gate oxide interface stability. The ion implantation process used to

form the source and drain extension also may result in an undesirably high trap density at the semiconductor/gate oxide interface. Moreover, formation of the source and drain extensions requires in most technologies that the gate electrode be used as a mask and thus be formed before ion implantation, therefore limiting manufacturing flexibility. Further, the source and drain extensions of such devices typically have sheet resistances of greater than 300 to 400 ohms/square when annealed at temperatures of about 800°C and above, and of greater than about 500 ohms/square when annealed at temperatures of about 700°C.

Accordingly, a need exists for an “implant-free” III-V compound semiconductor EMOSFET. As used herein, the term “implant-free” shall mean free from source and drain extensions formed by ion implantation. A need also exists for a method for fabricating an implant-free enhancement mode metal-oxide-semiconductor field effect transistor. Other desirable features and characteristics of the present invention will become apparent from the subsequent description and the appended claims, taken in conjunction with the accompanying drawings.

Brief Description of the Drawings

The present invention is illustrated by way of example and not limitation in the accompanying figures, in which like references indicate similar elements, and in which:

FIG. 1 illustrates schematically, in cross section, an enhancement mode metal-oxide-semiconductor field effect transistor in accordance with an exemplary embodiment of the present invention;

FIG. 2 is a graphical representation of the relationship between the work function of a metal gate electrode and the sheet resistance of an enhancement mode metal-oxide-semiconductor field effect transistor in accordance with an exemplary embodiment of the present invention;

5 FIG. 3 is a flowchart of a method for forming an enhancement mode metal-oxide-semiconductor field effect transistor in accordance with an exemplary embodiment of the present invention;

FIG. 4 illustrates an energy band diagram for an enhancement mode metal-oxide semiconductor field effect transistor of the prior art;

10 FIG. 5 illustrates an energy band diagram for an enhancement mode metal-oxide-semiconductor field effect transistor in accordance with an exemplary embodiment of the present invention;

FIG. 6 is a graphical representation of a measured relationship between the trap energy and total trap density at a gallium oxide/gallium arsenide interface of a
15 metal-oxide-semiconductor capacitor in accordance with an exemplary embodiment of the present invention;

FIG. 7 illustrates schematically, in cross section, an enhancement mode metal-oxide-semiconductor field effect transistor in accordance with another exemplary embodiment of the present invention;

20 FIG. 8 illustrates schematically, in cross section, an enhancement mode metal-oxide-semiconductor field effect transistor in accordance with a further exemplary embodiment of the present invention; and

FIG. 9 illustrates schematically, in cross section, an enhancement mode metal-oxide-semiconductor field effect transistor in accordance with yet another exemplary embodiment of the present invention.

5 Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help to improve understanding of embodiments of the present invention.

Detailed Description of the Drawings

10 The following detailed description is of exemplary embodiments only and is not intended to limit the invention or the application and uses of the invention. Rather, the following description provides a convenient illustration for implementing exemplary embodiments of the invention. Various changes to the described embodiments may be made in the function and arrangement of the elements described without departing from the scope of the invention as set forth in the appended claims.

FIG. 1 illustrates schematically, in cross section, an enhancement mode compound semiconductor MOSFET device 10 in accordance with one exemplary embodiment of the present invention. Device 10 has a substrate 12 formed of any suitable monocrystalline III-V compound semiconductor material. Preferably, 20 substrate 12 is a high quality monocrystalline gallium arsenide (GaAs) substrate as used in the semiconductor industry.

An epitaxial layer structure 14 overlies substrate 12. Epitaxial layer structure 14 comprises a buffer layer 16, a channel layer 18 and a spacer layer 20. Buffer layer 16, channel layer 18 and spacer layer 20 each may be formed of any suitable III-V

material, although preferably buffer layer 16, channel layer 18 and spacer layer 20 are each formed of a different III-V material. In a preferred embodiment of the present invention, buffer layer 16 is formed of gallium arsenide (GaAs), channel layer 18 comprises indium gallium arsenide (InGaAs) and spacer layer 20 comprises aluminum gallium arsenide (AlGaAs). It will be appreciated that, while buffer layer 16 is illustrated in FIG. 1 as a layer separate from substrate 12, buffer layer 16 and substrate 12 may form one continuous layer depending on the materials from which these layers are formed.

Epitaxial layer structure 14 also comprises at least one doped layer, such as doped layer 22 illustrated in FIG. 1. While epitaxial layer structure 14 is illustrated in FIG. 1 as having two doped layers, it will be appreciated that epitaxial layer structure 14 may have one, two or more doped layers. Doped layers 22 may be positioned above, below and/or within channel layer 18. Doped layers 22, and any additional doped layers, may comprise any suitable doping component known in the semiconductor industry, such as, for example, silicon (Si) (n-channel devices) and beryllium (Be) (p-channel devices). As described in more detail below, the doped layers of epitaxial layer structure 14 may be selected, that is, the doping levels of doped layers 22 may be selected, such that, for a particular MOSFET configuration, enhancement mode operation is achieved.

A gate oxide layer 24 overlies epitaxial layer structure 14. Preferably, gate oxide layer 24 comprises gallium oxide (Ga_2O_3), although gate oxide layer 24 may comprise any other suitable oxide material.

A metal gate electrode 26 that is stable in the presence of the gate oxide material overlies gate oxide layer 24. As described in more detail below, the material

for metal gate electrode 24 may be selected to have a work function such that for a particular MOSFET configuration enhancement mode operation is achieved.

Source and drain ohmic contacts 28, 30 are formed overlying epitaxial layer structure 14 and are separated from metal gate electrode 26 by source and drain access regions 32. Source and drain access regions 32 comprise those areas of epitaxial layer structure 14 between the source ohmic contact 28 and metal gate electrode 26 and between drain ohmic contact 30 and metal gate electrode 26, respectively. Source and drain ohmic contacts 28, 30 may be formed of any suitable electrically conductive material as is known in the semiconductor industry.

Enhancement mode operation of device 10 may be realized based on a relationship between the work function of metal gate electrode 26 and the dopant level of doped layers 22. While the doped layers 22 of epitaxial layer structure 14 serve as a source for free carriers, thus eliminating the need for ion-implanted source and drain extensions within epitaxial layer structure 14, without a suitable metal gate electrode, doped layers 22 may adversely shift the threshold voltage of device 10 preventing enhancement mode operation. For example, doped layers 22 may cause the threshold voltage of an n-channel MOSFET to have a negative value, thus preventing enhancement mode operation. Use of a metal gate electrode 26 having a suitably high work function may compensate for this shift and may result in a threshold voltage greater than zero, thus enabling enhancement mode operation. Similarly, doped layers 22 may cause the threshold voltage of a p-channel MOSFET to have a positive value, thus preventing enhancement mode operation. Use of a metal gate electrode 26 having a suitably low work function may compensate for this

shift and may result in a threshold voltage less than zero, thus enabling enhancement mode operation.

Without intending to be limited to any particular theory, in one exemplary embodiment of the invention, the relationship between the work function of metal gate electrode 26 and the doping level of doped layers 22 may be obtained from the following first order equations:

$$\rho_s = 1 / (Q_s \times \mu \times q), \quad (1)$$

where ρ_s is the sheet resistivity (ohms/square) of the source and drain access regions 32, μ is the channel mobility and q is the electronic charge (1.6×10^{-19} As) and

$$Q_s = (\epsilon_{ox} \times (\Phi_m - \Phi(0))) / (t_{ox} \times q), \quad (2)$$

where Q_s is the sheet charge (cm^{-2}) of doped layers 22 measured at source and drain access regions 32, ϵ_{ox} is the dielectric constant of gate oxide layer 24, t_{ox} is the thickness of gate oxide layer 24, Φ_m is the work function of metal gate electrode 26, and $\Phi(0)$ is the reference work function of metal gate electrode 26 for a specific threshold voltage and no doping layers ($\Phi(0)$ may be obtained by two-dimensional device simulation). It will be appreciated that while a relationship between the work function of metal gate electrode 26 and the doping level of doped layers 22 may be obtained from the above-described first order equations, such a relationship may be obtained from other higher order equations.

Tables 1 and 2 illustrate one exemplary relationship between the work function of metal gate electrode 26 and the doping levels of doped layers 22 for an n-channel MOSFET. In this example, the sheet resistance ρ_s and sheet charge Q_s are calculated for a threshold voltage V_T of 0.3V using a dielectric constant ϵ_{ox} of 20, a channel mobility μ of $5900 \text{ cm}^2/\text{Vs}$, a $\Phi(0)$ of 4.6 eV and a charge centroid located at

the oxide-epitaxial layer structure interface. The actual position of the charge centroid may vary with operating conditions and epitaxial layer structure configuration and may deviate to some extent from the position assumed in this example.

$Q_s(\text{cm}^{-2}), V_T = 0.3\text{V}$						
$\Phi_m(\text{eV})$	$t_{\text{ox}}(\text{nm})$	50	40	30	20	10
4.7		2.2×10^{11}	2.8×10^{11}	3.7×10^{11}	5.5×10^{11}	1.1×10^{12}
4.8		4.4×10^{11}	5.5×10^{11}	7.4×10^{11}	1.1×10^{12}	2.2×10^{12}
4.9		6.6×10^{11}	8.3×10^{11}	1.1×10^{12}	1.7×10^{12}	3.3×10^{12}
5.0		8.8×10^{11}	1.1×10^{12}	1.5×10^{12}	2.2×10^{12}	4.4×10^{12}
5.1		1.1×10^{12}	1.4×10^{12}	1.8×10^{12}	2.8×10^{12}	5.5×10^{12}
5.2		1.3×10^{12}	1.7×10^{12}	2.2×10^{12}	3.3×10^{12}	6.6×10^{12}
5.3		1.5×10^{12}	1.9×10^{12}	2.6×10^{12}	3.9×10^{12}	7.7×10^{12}
5.4		1.8×10^{12}	2.2×10^{12}	2.9×10^{12}	4.4×10^{12}	8.8×10^{12}
5.5		2.0×10^{12}	2.5×10^{12}	3.3×10^{12}	5.0×10^{12}	9.9×10^{12}
5.6		2.2×10^{12}	2.8×10^{12}	3.7×10^{12}	5.5×10^{12}	1.1×10^{13}
5.7		2.4×10^{12}	3.0×10^{12}	4.1×10^{12}	6.1×10^{12}	1.2×10^{13}

Table 1

$\rho_s(\text{Ohm/Square}), V_T = 0.3\text{V}$						
$\Phi_m(\text{eV})$	$t_{\text{ox}}(\text{nm})$	50	40	30	20	10
4.7		4786	3829	2871	1914	957
4.8		2393	1914	1436	957	479
4.9		1595	1276	957	638	319
5.0		1196	957	718	479	239
5.1		957	766	574	383	191
5.2		798	638	479	319	160
5.3		684	547	410	273	137
5.4		598	479	359	239	120
5.5		532	425	319	213	106
5.6		479	383	287	191	96
5.7		435	348	261	174	87

Table 2

5 FIG. 2 illustrates graphically the relationship between the work function of metal gate electrode 26 and the sheet resistance ρ_s of source and drain access regions

32 for five different gate oxide thicknesses where $V_T = 0.3V$. Curve 40 represents the sheet resistance for a gate oxide 24 having a thickness of 50 nm, curve 42 represents the sheet resistance for a gate oxide 24 having a thickness of 40 nm, curve 44 represents the sheet resistance for a gate oxide 24 having a thickness of 30 nm, curve 5 46 represents the sheet resistance for a gate oxide 24 having a thickness of 20 nm, and curve 48 represents the sheet resistance for a gate oxide 24 having a thickness of 10 nm. As is evident from the curve, the higher the work function of metal gate electrode 26 of device 10, the lower the sheet resistance. Similarly, the thinner the gate oxide 24 of device 10, the lower the sheet resistance.

10 Tables 3 and 4 illustrate the sheet resistance ρ_s and sheet charge Q_s as calculated for a threshold voltage V_T of 0.5V using a dielectric constant ϵ_{ox} of 20, a channel mobility μ of 5900 cm²/Vs, a reference work function $\Phi(0)$ of 4.8 eV and a charge centroid located at the oxide-epitaxial layer structure interface. Again, the actual position of the charge centroid may vary with operating conditions and 15 epitaxial layer structure configuration and may deviate to some extent from the position assumed in this example.

$Q_s(\text{cm}^{-2}), V_T = 0.5\text{V}$						
$\Phi_m(\text{eV})$	$t_{\text{ox}}(\text{nm})$	50	40	30	20	10
4.9		2.2×10^{11}	2.8×10^{11}	3.7×10^{11}	5.5×10^{11}	1.1×10^{12}
5.0		4.4×10^{11}	5.5×10^{11}	7.4×10^{11}	1.1×10^{12}	2.2×10^{12}
5.1		6.6×10^{11}	8.3×10^{11}	1.1×10^{12}	1.7×10^{12}	3.3×10^{12}
5.2		8.8×10^{11}	1.1×10^{12}	1.5×10^{12}	2.2×10^{12}	4.4×10^{12}
5.3		1.1×10^{12}	1.4×10^{12}	1.8×10^{12}	2.8×10^{12}	5.5×10^{12}
5.4		1.3×10^{12}	1.7×10^{12}	2.2×10^{12}	3.3×10^{12}	6.6×10^{12}
5.5		1.5×10^{12}	1.9×10^{12}	2.6×10^{12}	3.9×10^{12}	7.7×10^{12}
5.6		1.8×10^{12}	2.2×10^{12}	2.9×10^{12}	4.4×10^{12}	8.8×10^{12}
5.7		2.0×10^{12}	2.5×10^{12}	3.3×10^{12}	5.0×10^{12}	9.9×10^{12}

Table 3

$\rho_s(\text{Ohm/Square}), V_T = 0.5\text{V}$						
$\Phi_m(\text{eV})$	$t_{\text{ox}}(\text{nm})$	50	40	30	20	10
4.9		4786	3829	2871	1914	957
5.0		2393	1914	1436	957	479
5.1		1595	1276	957	638	319
5.2		1196	957	718	479	239
5.3		957	766	574	383	191
5.4		798	638	479	319	160
5.5		684	547	410	273	137
5.6		598	479	359	239	120
5.7		532	425	319	213	106

Table 4

The following example illustrates a method, in accordance with one embodiment of the invention, for fabricating an EMOSFET semiconductor structure

such as structure 10 depicted in FIG. 1. Referring to FIG. 3, the method begins at step 50 by providing a monocrystalline III-V semiconductor substrate. In accordance with a preferred embodiment of the invention, the semiconductor substrate is a monocrystalline gallium arsenide (GaAs) substrate.

5 Next, doped epitaxial layer structure 14 is grown overlying gallium arsenide substrate 12. Epitaxial layer structure 14 is formed by growing buffer layer 16, preferably of GaAs, then growing channel layer 18, preferably of InGaAs, and then growing spacer layer 20, preferably of AlGaAs. Methods of fabricating epitaxial layer structure 14 include, but are not limited to, molecular beam epitaxy (MBE) and
10 metal organic chemical vapor deposition (MOCVD). Preferably, epitaxial layer structure 14 is formed in an ultra high vacuum (UHV) MBE system so that it is formed with an atomically ordered and chemically clean semiconductor surface.

During growth of epitaxial layer structure 14, one or more doped layers 22 are formed above, below or within channel layer 18 using any standard doping technique.
15 In a preferred embodiment of the invention, doped layers 22 are formed using delta doping, as is well known and practiced in the semiconductor industry. Thus, as illustrated in step 52, a thickness of epitaxial layer structure 14 is grown and, as illustrated in step 54, delta doping is then performed to form a first delta-doped layer 22. Epitaxial layer structure growth then may continue to another desired thickness
20 and, in another embodiment of the invention, another delta doping procedure may be performed to form a second delta-doped layer. The process may continue until the desired number of delta-doped layers 22 has been formed. Epitaxial layer structure 14 then may be grown to its final thickness, as illustrated in step 56.

The level of dopant used for forming delta-doped layers 22 may be determined using models developed from the equations set forth above. For example, for an n-channel EMOSFET for which a threshold voltage of 0.3 V is desired, Tables 1 and 2 may be used. Referring to Tables 1 and 2, by way of example, if design constraints for the n-channel MOSFET require a gate oxide 26 thickness of 30 nm, and a sheet resistance below 500 ohms/square is desired, Table 2 indicates that a metal gate electrode 26 having a work function of 5.2 to 5.7 eV can be used. If iridium ($\Phi_m = 5.3$ eV) is available for metal gate electrode 26, an acceptable sheet resistance of 410 ohms/square would result. Thus, Table 1 indicates that for a gate oxide thickness of 30 nm and a work function Φ_m of 5.3 eV, the delta-doping level could be about $2.6 \times 10^{12} \text{ cm}^{-2}$ or less. Accordingly, doped layers 22 could be doped to about $2.6 \times 10^{12} \text{ cm}^{-2}$ or less to achieve $V_T \geq 0.3\text{V}$, that is, to achieve an operable n-channel enhancement-mode MOSFET with a gate oxide 24 thickness of 30 nm and an iridium metal gate electrode 26. If platinum ($\Phi_m = 5.7$) is available for metal gate electrode 26, Table 2 indicates that a very low sheet resistance of 261 ohms/square would result. Table 1 indicates that for a gate oxide thickness of 30 nm and a work function Φ_m of 5.7 eV, the delta-doping level could be about $4.1 \times 10^{12} \text{ cm}^{-2}$ or less. Accordingly, doped layers 22 could be doped to about $4.1 \times 10^{12} \text{ cm}^{-2}$ or less to achieve $V_T \geq 0.3\text{V}$, that is, to achieve an operable n-channel enhancement-mode MOSFET with a gate oxide 24 thickness of 30 nm and a platinum metal gate electrode 26.

Referring again to FIG. 3, as illustrated in step 58, a gate oxide layer 24 is formed overlying epitaxial layer structure 14. Methods of forming gate-quality oxides overlying III-V compound semiconductor substrates are known. One method for

forming a gate-quality oxide overlying a III-V compound semiconductor substrate is disclosed in U.S. Patent No. 6,159,834, issued to Yu et al, on December 12, 2000, which patent in its entirety is herein incorporated by reference.

As illustrated in step 60, source and drain ohmic contacts 28, 30 are deposited
5 overlying epitaxial layer structure 14 using standard processes well known in the semiconductor industry.

Next, as illustrated in step 62, metal gate electrode 26 is formed overlying gate oxide layer 24. Metal gate electrode 26 is formed by depositing a metal layer overlying gate oxide layer 24 and subsequently patterning the metal layer using
10 standard lithography and lift-off or etching techniques, as is well known in the semiconductor industry. As described above, the material for metal gate electrode 26 may be selected based on a relationship with the dopant level of doped layers 22.

One embodiment of the present invention can be explained using simplified energy band diagrams. FIG. 4 illustrates a simplified energy band diagram 70 for an
15 EMOSFET of the prior art, that is, an EMOSFET having ion-implanted source and drain extensions. Represented on the energy band diagram 70 is a III-V compound semiconductor substrate 72, a undoped channel layer 74, a spacer layer 76, a gate oxide layer 78, a metal gate electrode 80, a Fermi level 84, a conduction band edge in off state 82, and a conduction band edge in on-state 86. As illustrated in FIG. 4, the
20 Fermi level at the interface between gate oxide layer 78 and the spacer layer 76 moves from about midgap in the off state into the vicinity of the spacer layer conduction band edge when the EMOSFET is switched from off-state into on-state. In the specific embodiment shown in FIG. 4, the conduction band edge (E_c) is only about 0.2eV above the Fermi level in on-state, as indicated by reference number 88.

FIG. 5 illustrates a simplified energy band diagram 90 for an EMOSFET in accordance with an exemplary embodiment of the present invention. Represented on the energy band diagram 90 is a III-V compound semiconductor substrate 92, a channel layer 94, a spacer layer 96, a gate oxide layer 98, a metal gate electrode 100, a Fermi level 104, a conduction band edge in off state 106, and a conduction band edge in on-state 108. Also shown is a doped layer 102. As illustrated in FIG. 5, the Fermi level 104 at the interface between the gate oxide 98 and the spacer layer 96 does not move into the vicinity of the spacer layer conduction band edge when the device is switched from the off-state into the on-state. In the specific embodiment shown in FIG. 5, the conduction band edge (E_c) is about 0.5 eV above the Fermi level in on-state, as indicated by reference number 110.

FIG. 6 illustrates graphically the measured relationship between the trap energy E_T and the total trap density with reference to the conduction band edge E_c for an Ga_2O_3 -GaAs interface. As the Fermi level moves toward E_c , traps of energy E_T below the Fermi level are occupied (charged) and traps of energy E_T above the Fermi level remain empty (neutral). As illustrated by curve 120, the total density of charged traps for the Fermi level being 0.2eV below E_c (approximately $4 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$), such as that illustrated in FIG. 4 for the prior art, is significantly higher than the total density of charged traps for the Fermi level being 0.5eV below E_c (approximately $4 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$), such as that illustrated in FIG. 5.

FIG. 7 illustrates schematically, in cross section, an enhancement mode compound semiconductor MOSFET device 130 in accordance with another exemplary embodiment of the present invention. Elements of FIG. 7 that have the same reference numbers as FIG. 1 are the same as the corresponding FIG. 1 elements.

Device 130 comprises III-V compound semiconductor substrate 12 and epitaxial layer structure 14 that overlies substrate 12. Epitaxial layer structure 14 comprises buffer layer 16, channel layer 18, a spacer layer 20, and one or more doped layers 22. Device 130 further comprises gate oxide layer 24, metal gate electrode 26 and source and drain ohmic contacts 28 and 30.

Device 130 further comprises a field plate 132. Field plate 132 may be used in a variety of devices, including, but not limited to, power devices that require high breakdown voltage. Field plate 132 may be formed overlying gate oxide layer 24 or, as illustrated in FIG. 7, may be formed at least partially recessed within gate oxide layer 24. Field plate 132 may create an equivalent to a lightly doped drain (LDD) region. The partial depletion of free carriers in the area under the field plate may be controlled by at least partially recessing field plate 132 within gate oxide layer 24 and/or fabricating field plate 132 from a metal with a suitable work function.

Referring to FIG. 8, in another exemplary embodiment of the invention, a device 140 may utilize a low dose implantation of a conductivity type opposite to that of doped layers 22 to reduce free carrier concentration in an LDD region 142 in epitaxial layer structure 14. LDD regions are well known and widely used in semiconductor devices such as MOSFETs. In the case of n-channel devices, low dose acceptor implantation may require a thermal annealing step at temperatures of about 600°C, which is compatible with the thermal budget of the gate oxide-epitaxial layer structure interface.

It will be appreciated that any number of other modifications can be made to the EMOSFET of the present invention to arrive at various configurations suitable for desired applications. For example, FIG. 9 illustrates, schematically, in cross section,

an enhancement mode compound semiconductor MOSFET device 150 in accordance with yet a further exemplary embodiment of the present invention. Elements of FIG. 9 that have the same reference numbers as FIG. 1 are the same as the corresponding FIG. 1 elements. Device 150 comprises III-V compound semiconductor substrate 12 and epitaxial layer structure 14 that overlies substrate 12. Epitaxial layer structure 14 comprises buffer layer 16, channel layer 18, a spacer layer 20, and one or more doped layers 22. Device 150 further comprises gate oxide layer 24, and source and drain ohmic contacts 28 and 30. In this exemplary embodiment, device 150 further comprises a metal step gate electrode 152. As described above with reference to metal gate electrode 26, metal step gate electrode 152 may be selected to have a work function such that, for a particular MOSFET configuration, enhancement mode operation is achieved. Metal step gate electrode 152 is isolated from drain access region 32 by a dielectric layer 154. Dielectric layer 154 may comprise silicon nitride, silicon oxide or any other suitable insulating material.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of the present invention.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or

solution to occur or become more pronounced are not to be construed as a critical, required, or essential features or elements of any or all the claims. As used herein, the terms “comprises,” “comprising,” or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that
5 comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.

CLAIMS

1. An implant-free enhancement mode metal-oxide semiconductor field effect transistor (EMOSFET) comprising:
- 5 a III-V compound semiconductor substrate;
- an epitaxial layer structure overlying said III-V compound semiconductor substrate, said epitaxial material layer comprising a channel layer and at least one doped layer;
- a gate oxide layer overlying said epitaxial layer structure;
- 10 a metal gate electrode overlying said gate oxide layer; and
- source and drain ohmic contacts overlying said epitaxial layer structure.
2. The implant-free EMOSFET of claim 1, said at least one doped layer comprising a delta-doped layer.
- 15
3. The implant-free EMOSFET of claim 1, said epitaxial layer structure comprising a spacer layer overlying said channel layer and underlying said gate oxide layer.
4. The implant-free EMOSFET of claim 1, said channel layer comprising indium gallium arsenide (InGaAs).
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5. The implant-free EMOSFET of claim 3, said spacer layer comprising aluminum gallium arsenide (AlGaAs).
6. The implant-free EMOSFET of claim 1, said III-V compound semiconductor substrate comprising gallium arsenide (GaAs).

7. The implant-free EMOSFET of claim 1, said gate oxide comprising Ga_2O_3 .
8. The implant-free EMOSFET of claim 1, further comprising a field plate
5 positioned at least partially within said gate oxide.
9. The implant-free EMOSFET of claim 1, further comprising a field plate positioned overlying said gate oxide.
- 10 10. The implant-free EMOSFET of claim 1, further comprising a low dose implantation region positioned within said epitaxial layer structure, said low dose implantation region of a conductivity type opposite to said at least one doped layer.
11. The implant-free EMOSFET of claim 1, wherein said metal gate electrode is a
15 metal step gate electrode.

12. A method for fabricating an implant-free enhancement mode metal-oxide-semiconductor field effect transistor, the method comprising the steps of:

providing a III-V compound semiconductor substrate;

growing a first thickness of an epitaxial layer structure overlying said III-V

5 compound substrate;

doping said first thickness of said epitaxial layer structure to form a doped layer within said first thickness of said epitaxial layer structure;

growing said epitaxial layer structure to a second thickness;

forming a gate oxide layer overlying said epitaxial layer structure;

10 forming source and drain ohmic contacts overlying said epitaxial layer structure; and

forming a metal gate electrode overlying said gate oxide layer.

13. The method of claim 12, said step of doping comprising delta doping.

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14. The method of claim 12, wherein said step of forming a metal gate electrode comprises selecting a metal gate electrode having a work function and said step of doping comprises doping at a dopant level so that enhancement mode operation is achieved.

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15. The method of claim 12, wherein said steps of growing are performed in an ultra high vacuum molecular beam epitaxy system.

16. The method of claim 12, wherein said step of growing a first thickness of said epitaxial layer structure and said step of doping said first thickness are repeated until a desired number of doped layers within said epitaxial layer structure are fabricated.
- 5 17. The method of claim 12, further comprising the step of forming a field plate overlying said gate oxide layer.
18. The method of claim 12, further comprising the step of forming a field plate at least partially recessed within said gate oxide layer.
- 10 19. The method of claim 12, further comprising the step of forming a low dose implantation region within said epitaxial layer structure, said low dose implantation region of a conductivity type opposite to said doped layer.
- 15 20. The method of claim 12, wherein said step of forming a metal gate electrode comprises forming a metal step gate electrode.

21. An enhancement mode metal-oxide semiconductor field effect transistor (EMOSFET) comprising:

a III-V compound semiconductor substrate;

an epitaxial layer structure overlying said III-V compound semiconductor substrate, said epitaxial layer structure comprising a channel layer and at least one
5 delta-doped layer;

a gate oxide layer overlying said epitaxial layer structure;

a metal gate electrode overlying said gate oxide layer, said metal gate electrode having a work function; and

10 source and drain ohmic contacts overlying said epitaxial layer structure;

wherein said metal gate electrode is selected to have a work function and said delta-doped layer is selected so that enhancement mode operation is achieved.

22. The EMOSFET of claim 21, said III-V compound semiconductor substrate
15 comprising gallium arsenide (GaAs).

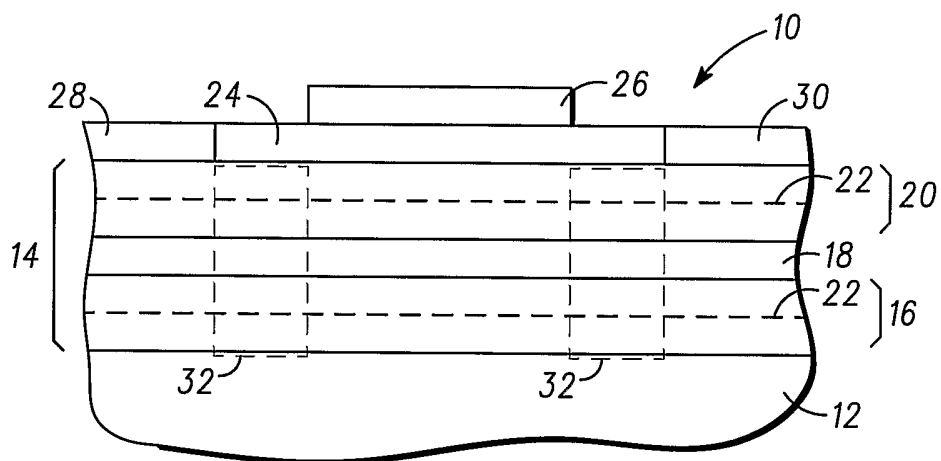


FIG. 1

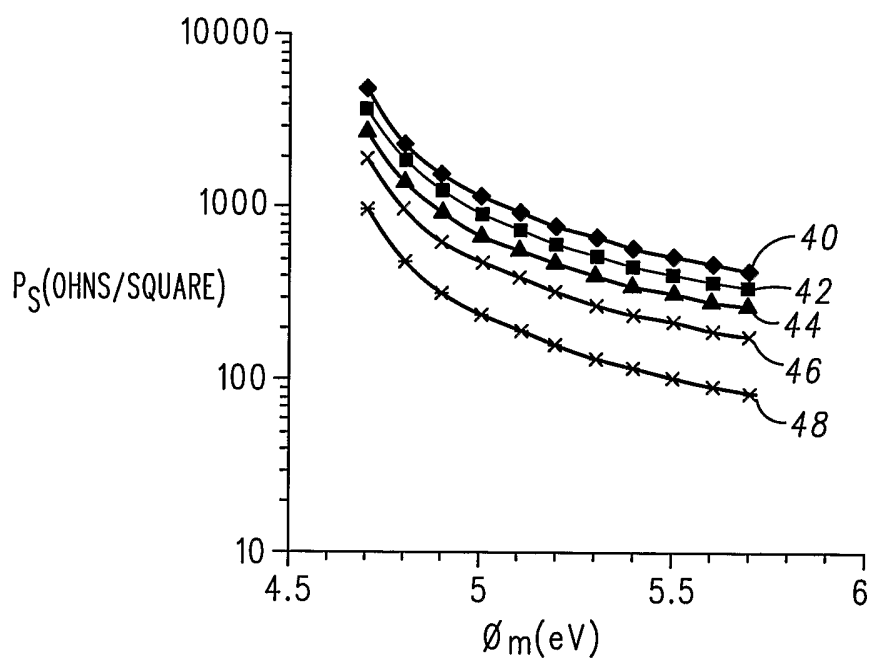
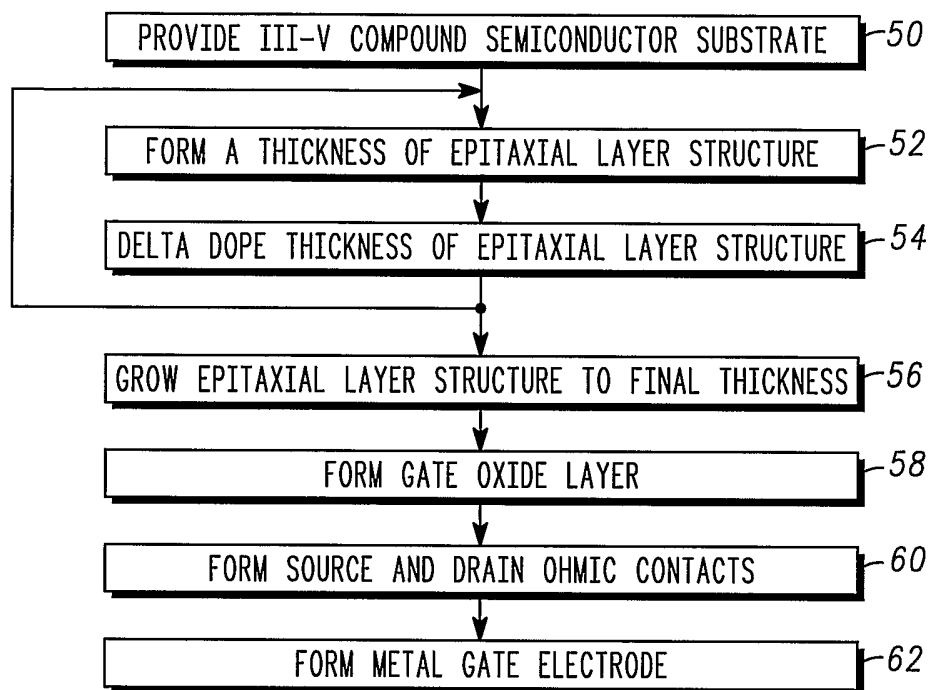
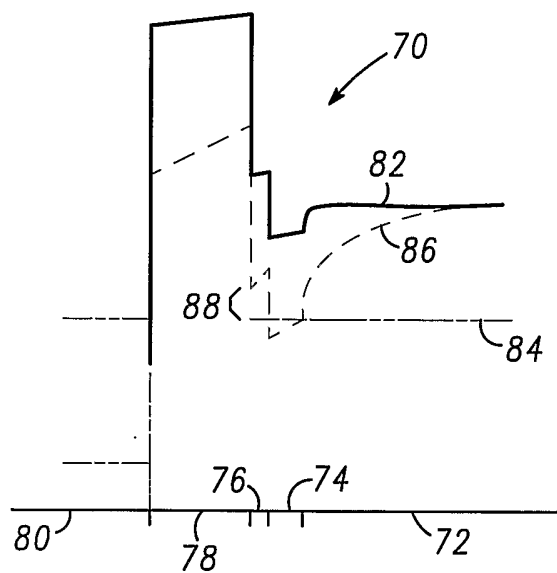
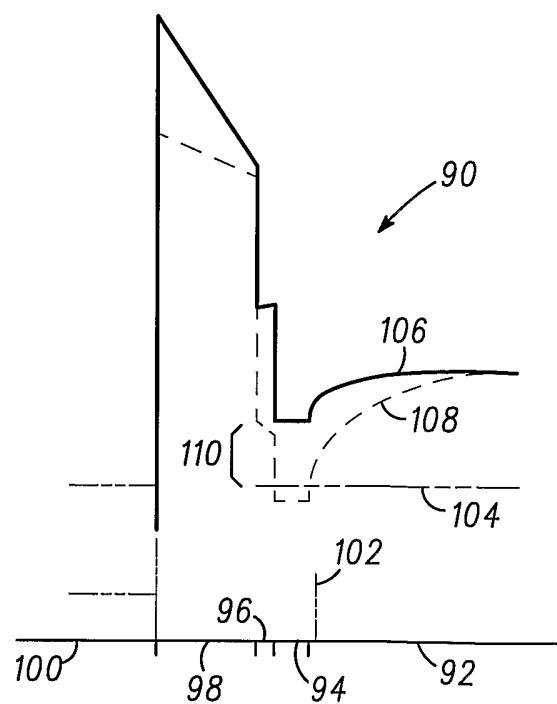


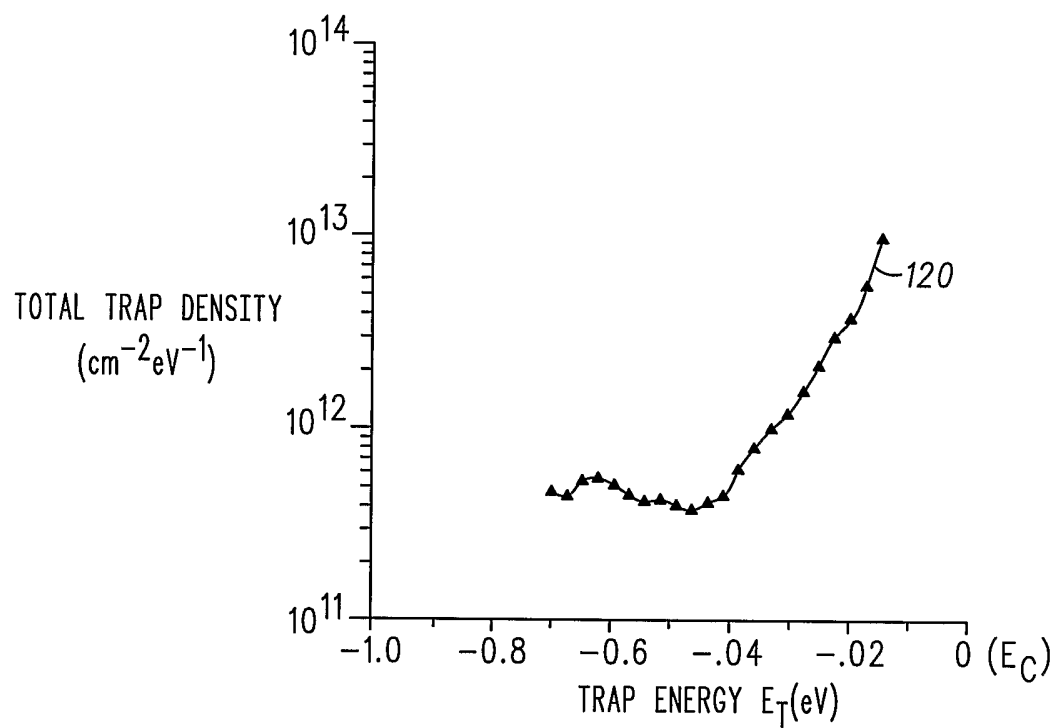
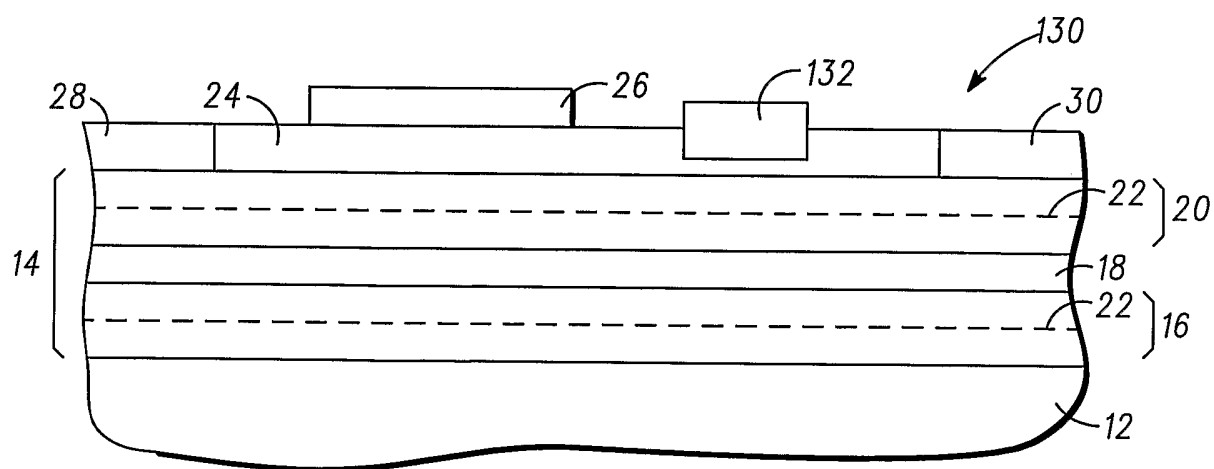
FIG. 2

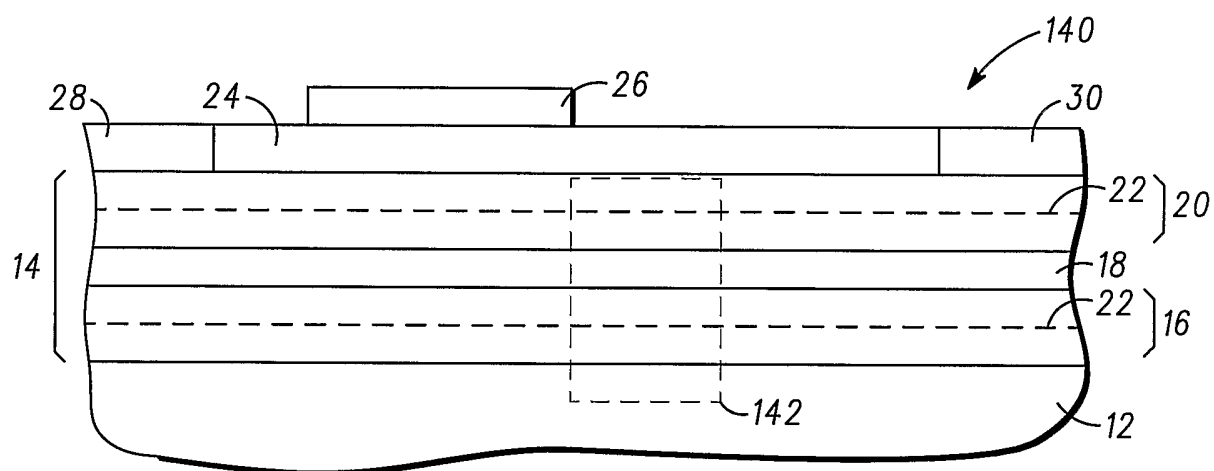
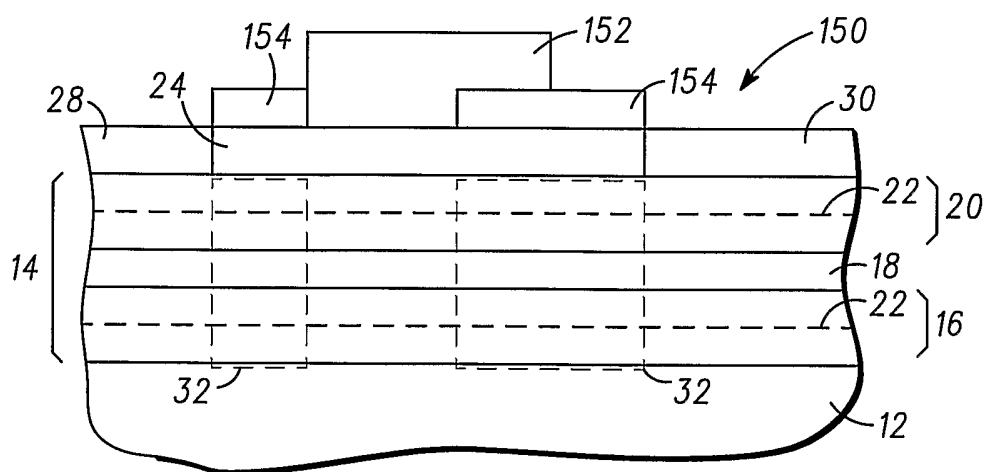
*FIG. 3*

-PRIOR ART-

FIG. 4*FIG. 5*

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*FIG. 6**FIG. 7*

**FIG. 8****FIG. 9**