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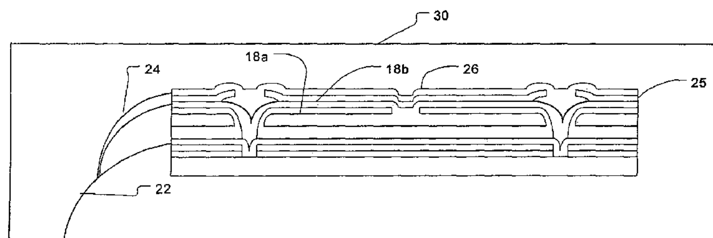
(54) **Title:** REDUCTION OF ETCHING CHARGE DAMAGE IN MANUFACTURE OF MICROELECTROMECHANICAL DEVICES



(57) **Abstract:** A method of manufacturing a microelectromechanical device includes forming at least two conductive layers on a substrate. An isolation layer is formed between the two conductive layers. The conductive layers are electrically coupled together and then the isolation layer is removed to form a gap between the conductive layers. The electrical coupling of the layers mitigates or eliminates the effects of electrostatic charge build up on the device during the removal process.

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REDUCTION OF ETCHING CHARGE DAMAGE IN MANUFACTURE OF MICROELECTROMECHANICAL DEVICE

Background

5 Microelectromechanical system devices (MEMS) may be manufactured from thin film processes. These processes may involve a series of thin films deposited in layers, the layers being patterned and etched to form the devices. In order to allow the devices to move, one layer may be an isolation layer. An isolation layer is one that is used in forming the layers of the device acting as a structural member, but that may be removed when the device is complete.

10 Removal of the isolation layers may involve an etching process, using a material as the etchant that only acts on the sacrificial layer material. In some cases, the isolation layer may be an oxide that may be removed with a dry gas etch. Other forms of isolation layers are also possible, as are other methods of removal. The removal of the isolation layer typically results in a gap, through which a member of the device will move upon actuation.

15 MEMS devices often actuate through the use of electrical signals that cause a voltage differential between a first conductive layer and a second conductive layer separated by the gap. During dry, gas etching of the isolation layer, an electrostatic charge may build up on the layers, causing the movable member to become attracted to the other conductive layer. In extreme cases, the two layers may become stuck together and the device becomes inoperative. In less extreme 20 cases, the movable element may become damaged or deformed and subsequently not operate correctly.

Brief Description of the Drawings

The invention may be best understood by reading the disclosure with reference to the drawings, wherein:

25 Figure 1 shows an embodiment of a microelectromechanical device formed using an isolation layer.

Figure 2 shows an embodiment of a microelectromechanical device rendered inoperable by a static charge buildup during an etch process.

Figure 3 shows an embodiment of an apparatus to mitigate the effects of static charge 30 buildup during an etch process.

Figure 4 shows an alternative embodiment of an apparatus to mitigate the effects of static charge during an etch process.

Figure 5 shows a flowchart of an embodiment of a method to manufacture a microelectromechanical device.

35 Figures 6a and 6b show embodiments of an alternative apparatus to mitigate the effects of static charge during an etch process.

Detailed Description of the Embodiments

Figure 1 shows an example of a microelectromechanical device that is formed from thin film processes including an isolation layer. This particular example is of an interferometric modulator, but embodiments of the invention may be applicable to all kinds of MEMS devices that are formed from thin film processes with an isolation layer. The modulator is formed on a transparent substrate 10. An optical stack typically comprising layers of metal and oxides such as 12 and 14 is formed upon the substrate 10. A metal membrane 18 is formed upon a sacrificial layer, not shown. The sacrificial layer may also be referred to as an isolation layer, as it acts to electrically isolate conductive layers from each other during processing. Prior to the formation of the membrane, vias are patterned into the isolation layer to allow metal from the membrane to fill in the vias and form posts, such as 16.

Upon completion of the modulator structures, such as the metal membrane 18, the isolation layer is removed. This allows portions of the membrane 18 to deflect towards the electrode layer 12 of the optical stack. In the case of interferometric modulators, the membrane 18 is attracted to the metal layer 12 by manipulation of the voltage differential between the membrane 18 and the electrode layer 12. The layer 12 and the membrane 18 may be metal, as discussed here, or any conductive material. The cell formed by the portion of the membrane shown in Figure 1 is activated by applying a voltage to the conductive layer 14, which differs from the voltage of the membrane at 18. This causes the membrane to become electrostatically attracted to the electrode, or first conductive, layer 12. The conductive layers may be metal or any other conductive material.

During removal of the isolation layer, enough electrostatic charge can build up on the surfaces of the two conductive layers to cause the membrane to attract towards the conductive layer 14 without being activated. This condition is shown in Figure 2. This is normally the activated state of the interferometric modulator, but the difference is that the membrane does not release from the oxide layer 12 upon changing of the voltage potential. The membrane has assumed the activated state permanently. This may be caused by a combination sticking and friction, often referred to as stiction, aggravated by the electrostatic forces between the conductive layer 12 and the conductive membrane 18.

Removal of the isolation layer may be achieved in many different ways. Typically, it is removed with the use of a dry, gas etch, such as a xenon-difluorine (XeF_2) etch. While these are examples of etching processes, any etch process may be used. It may be the dry environment that contributes to the build up of the electrostatic charge. However, it would be better to not have to change the materials or basis of the processes used to manufacture the MEMS devices, but instead to adapt the process to eliminate the electrostatic charge build up.

There are some benefits to be obtained by grounding the conductive layers during wet etch processes as well. There may be effects on the device electrochemistry that are either

enabled, if desirable, or mitigated, if undesirable, by grounding. In one embodiment, the layers are grounded together, the isolation layers are removed and the grounding left in place so the devices can be safely transported without fear of electrostatic discharge. This would be helpful if the etch were a wet etch or a dry etch.

5 The grounding process may be an external grounding, by an apparatus or mechanism external to the structure of the device. Alternatively, the grounding may be as part of the internal structure of the device enabled during manufacture. Initially, external grounding will be discussed.

An apparatus for mitigating the build up of electrostatic charge during etching processes
10 is shown in Figure 3. An alternative embodiment is shown in Figure 4. In Figure 3, a conductive wire 22 has been attached to the first and second conductive layers 14 and 18 to hold them at the same potential. The same potential could involve attaching them to a ground plane, or just attaching them together. By holding them at the same potential, the electrostatic charge build up will not cause a differential between the two layers, and will therefore avoid the problem of
15 having the membrane actuate during the etch process. As will be discussed in more detail further, this will typically be done just prior to the etch process, although the two layers could be electrically coupled together at any point prior to the etch process. It may be desirable to restrict the electrical coupling to the inactive area of the substrates upon which the devices are manufactured.

20 The alternative embodiment of Figure 4 shows a device being manufactured out of three conductive layers and two isolation layers. In this embodiment of an interferometric modulator, the equivalent to the second conductive layer 18 in Figures 1 and 3 is actually two conductive layers 18a and 18b. They are generally deposited as two separate layers but are in physical or electrical connection with each other. This will typically result in the combination of the flex
25 layer and the mirror layer only requiring one connection to be connecting with the other conductive layers. This particular formation may require two isolation layers as the equivalent of the first isolation layer, because an isolation layer may be formed between the layers 18a and 18b in addition to the one formed between layer 18a and the electrode layer 12. The connection between layers 18a and 18b may be formed by a via in the second portion of the first isolation
30 layer. For purposes of discussion here, this isolation layer is not of interest in that the conductive layer deposited upon does not generally need a conductive wire to connect it to the other conductive layers.

A second isolation layer 25 may be formed on the flex layer 18b, to provide a separation between the conductive layer 18b and a third conductive layer 26. The third conductive layer in
35 this example is the bus layer, used to form a signaling bus above the flex and mirror layers to aid in addressing of the cells of the modulator. Regardless of the application or the MEMS device in which embodiments of the invention may be employed, this is just intended as an example of

multiple conductive layers being electrically coupled to mitigate or eliminate the electrostatic charge build up during the etch process.

Also shown in Figure 4 is an alternative to a connection between the two layers alone. In Figure 24, the conductive wire 22 is attached to a ground plane, in this example the frame of the etch chamber 30. This may be more desirable than having the two or more layers electrically connected together, as they will be to a 'known' potential, that is ground. Alternatively, the conductive wires 22 and 24 could be attached to other structures. As long as the two or more layers are held at the same potential, the build up of electrostatic charge should not cause the membrane to be attracted to the conductive layer on the substrate.

As mentioned previously, it is probably more desirable to use a means of avoiding or mitigating electrostatic charge build up that does not interfere with current process flows for manufacturing of MEMS devices. An example of a method of manufacturing a MEMS device, in this case the interferometric modulator mentioned previously, is shown in flowchart form in Figure 5.

It must be noted that the process flow given as a particular example in this discussion is for an interferometric modulator. However, embodiments of this invention may be applied to any MEMS device manufacturing flow having isolation layers removed by dry, gas etching. As discussed previously, the interferometric modulator is built upon a transparent substrate such as glass. An electrode layer is deposited, patterned and etched at 32 to form electrodes for addressing the cells of the modulator. The optical layer is then deposited and etched at 34. The first isolation layer is deposited at 36, then the mirror layer at 38. In this example, the first conductive layer will be the mirror layer.

The first conductive layer is then patterned and etched at 40. A second isolation layer is deposited at 42. Again, this is specific to the example of Figure 4, in which the second conductive layer is actually formed from two conductive layers, the flex layer and the mirror layer. The first and second isolation layers may be treated as one isolation layer, as the electrostatic charge buildup between the conductive layers on either side of the second isolation layer is not a concern. The flex layer is then deposited at 44, and patterned and etched at 46.

At 48, the typical process flow is altered to include the grounding of the first and second conductive layers, in this case the electrode layer and the mirror/flex layer. For a device having two conductive layers and one effective isolation layer, the process may end at 50, with the isolation layer being removed with an etch. This is only one embodiment, and the ending of the process is therefore shown in a dashed box. For a device having more than two conductive layers, the process may instead continue at 52.

At 52, a third isolation layer is deposited at 52 in this particular example. As discussed above, this may actually be only a second, effective isolation layer. The bus layer, or third conductive layer, is deposited at 54, patterned and etched at 56. At 58, the conductive layers, in

this example there are three, are grounded or electrically coupled together at 58, and the isolation layers are removed at 60. Depending upon the functionality of the device and the electrical drive scheme, the conductive layers may be decoupled at 62. For the example of the interferometric modulator, where the operation of the device relies upon the electrostatic attraction arising between conductive layers being held at different voltage potentials, the coupling would have to be removed.

The wire coupling is an example of an external process of coupling the conductive layers. Other external examples include using test probe structures to provide coupling between the layers, and the use of an ionized gas, where the molecules of the gas itself provides coupling between the layers.

It must be noted that the process of connecting the layers together, or connecting them all to the same potential is referred to as coupling the layers. This is intended to cover the situations in which the layers are just connected together, connected together to a common potential where that potential includes ground, or connected individually to a common or same potential. No restriction on how the layers are electrically coupled together is in intended.

An example of an internal grounding apparatus is shown in Figures 6a and 6b. As part of the manufacture of the MEMS devices, typically many devices are manufactured on one substrate, a portion of which is shown at 70 in Figure 6a. During manufacture of the device, leads may be provided from the various layers, such as the electrode layer 12, the mechanical or mirror layer 18, and the bussing layer 26, of the device to test pads or tabs such as 76. It is possible to couple these pads together, such as by connection 74 that ties all of the pads together, as part of the conductive layer patterning and etching processes of manufacturing the devices. This would couple the conductive layers together for further processing.

As mentioned above, for devices that cannot operate with the layers coupled together, this internal coupling would have to be removed. As shown in Figure 6b, the connections between the pads 76 and the coupling connection 74 could be broken. When the substrate is divided up into its individual devices, it may be sawn, scribed, or otherwise broken. The lines used to form the breaks, such as the scribe line 78, would sever the coupling between the pads 76 and the coupling connection 74. This is an example of internal coupling.

In this manner, MEMS devices having conductive layers and at least one isolation layer can be etched using current processes while avoiding electrostatic charge build up that may render the devices inoperable. Prior to packaging, and typically upon removal of the device from the etch chamber, the connections are removed or otherwise eliminated from the devices.

Thus, although there has been described to this point a particular embodiment for a method and apparatus for mitigating or eliminating the effects of electrostatic charge during etch processes, it is not intended that such specific references be considered as limitations upon the scope of this invention except in-so-far as set forth in the following claims.

WHAT IS CLAIMED IS:

1. A method of manufacturing a microelectromechanical device, comprising:

forming at least first and second conductive layers on a substrate;

forming an isolation layer between the first and second conductive layers;

electrically coupling the first and second conductive layers together; and

removing the isolation layer to form a gap between the first conductive layer and the second conductive layer.

2. The method of claim 1, further comprising forming a third conductive layer.

3. The method of claim 2, wherein forming an isolation layer further comprises forming two isolation layers.

4. The method of claim 1, wherein removing the isolation layer comprises performing an etch of the isolation layer.

5. The method of claim 4, wherein performing an etch comprises performing a dry gas etch.

6. The method of claim 5, wherein performing a dry gas etch comprises performing a xenon-difluorine etch.

7. The method of claim 1, wherein electrically coupling the conductive layers together comprises coupling the conductive layers together externally.

8. The method of claim 7, wherein coupling the conductive layers together externally comprises using a conductive wire, applying a probe structure, or using an ionized gas to remove the isolation layers.

9. The method of claim 1, wherein electrically coupling the conductive layers together comprises coupling the conductive layers together internally.

10. The method of claim 1, wherein electrically coupling the conductive layers together comprises using a conductive wire to provide electrical connection to the conductive layers.

11. The method of claim 1, wherein electrically coupling the conductive layers together comprises using a conductive wire to provide electrical connection to the conductive layers and then connecting the wire to a common voltage potential.

12. The method of claim 1, wherein electrically coupling the conductive layers together comprises using conductive wires for each conductive layer and electrically connecting all of the wires to the same potential.

13. The method of claim 1, wherein electrically coupling the conductive layers together comprises electrically coupling the conductive layers together in an inactive area of the substrate.

14. An apparatus for manufacturing a microelectromechanical device, comprising:

a conductive wire configured to electrically connect at least two conductive layers together prior to an etch process wherein the at least two conductive layers form at least a portion of the micromechanical device.

15. The apparatus of claim 14, wherein the conductive wire comprises an external conductive wire configured to connect the conductive layers together.

16. The method of claim 14, wherein the conductive wire comprises an internal conductive connection configured to connect the conductive layers together.

17. The apparatus of claim 14, wherein the conductive wire comprises a conductive wire configured to connect the conductive layers together and to a common potential.

18. The apparatus of claim 14, wherein the conductive wire comprises a conductive wire configured to connect the conductive layers individually to a common potential.

19. The apparatus of claim 14, wherein the conductive wire is provided in a gas etch chamber.

20. The apparatus of claim 14, wherein one of the at least two conductive layers comprises metal layer.

21. The apparatus of claim 14, wherein one of the at least two conductive layers comprises an electrode.

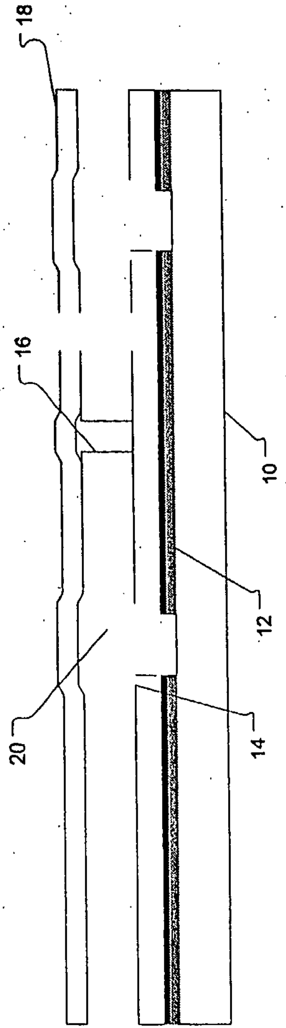

Figure 1

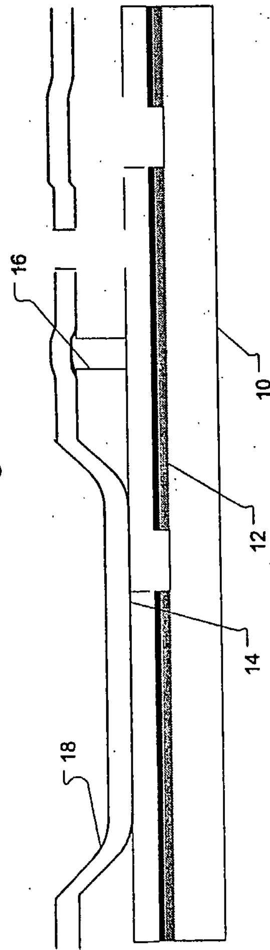

Figure 2

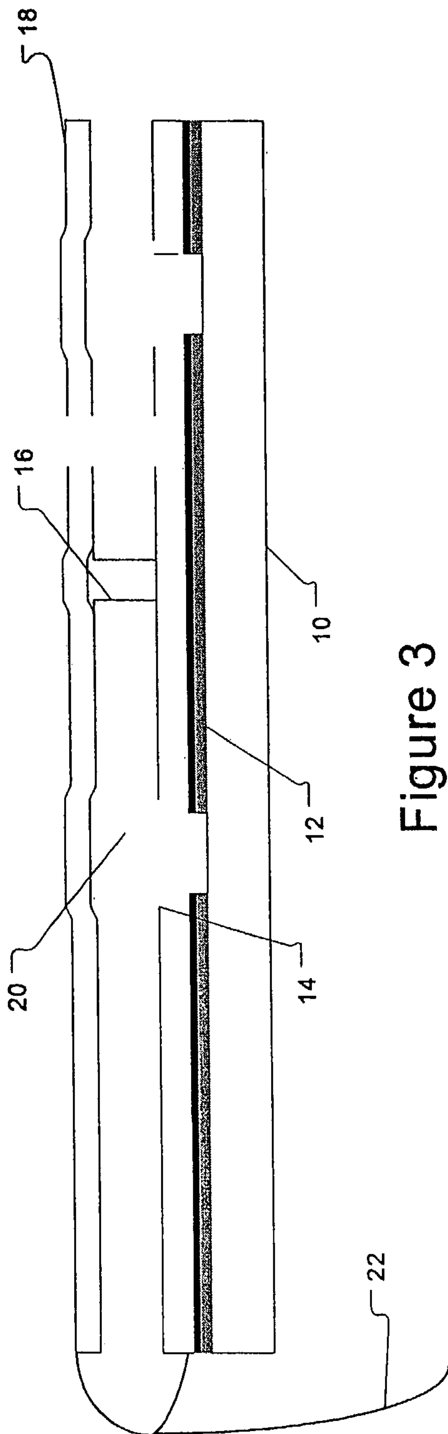

Figure 3

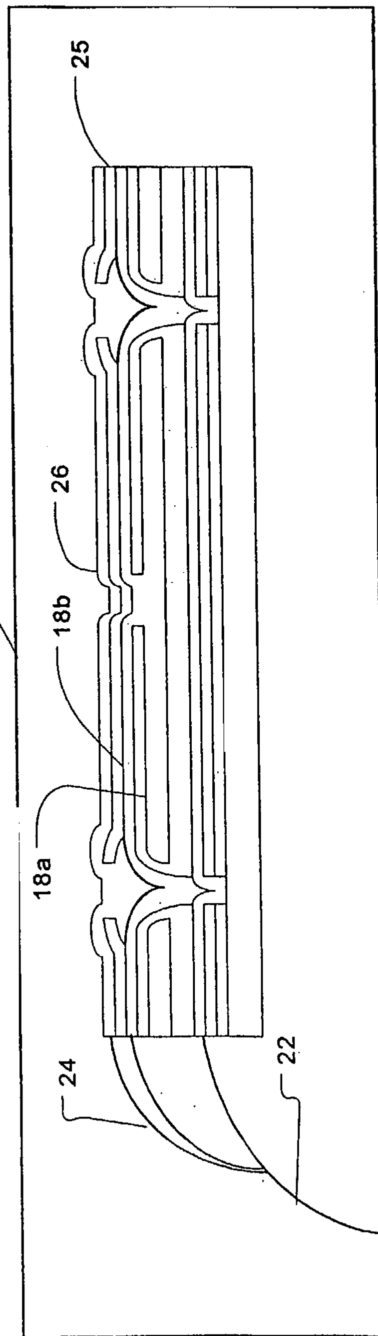

Figure 4

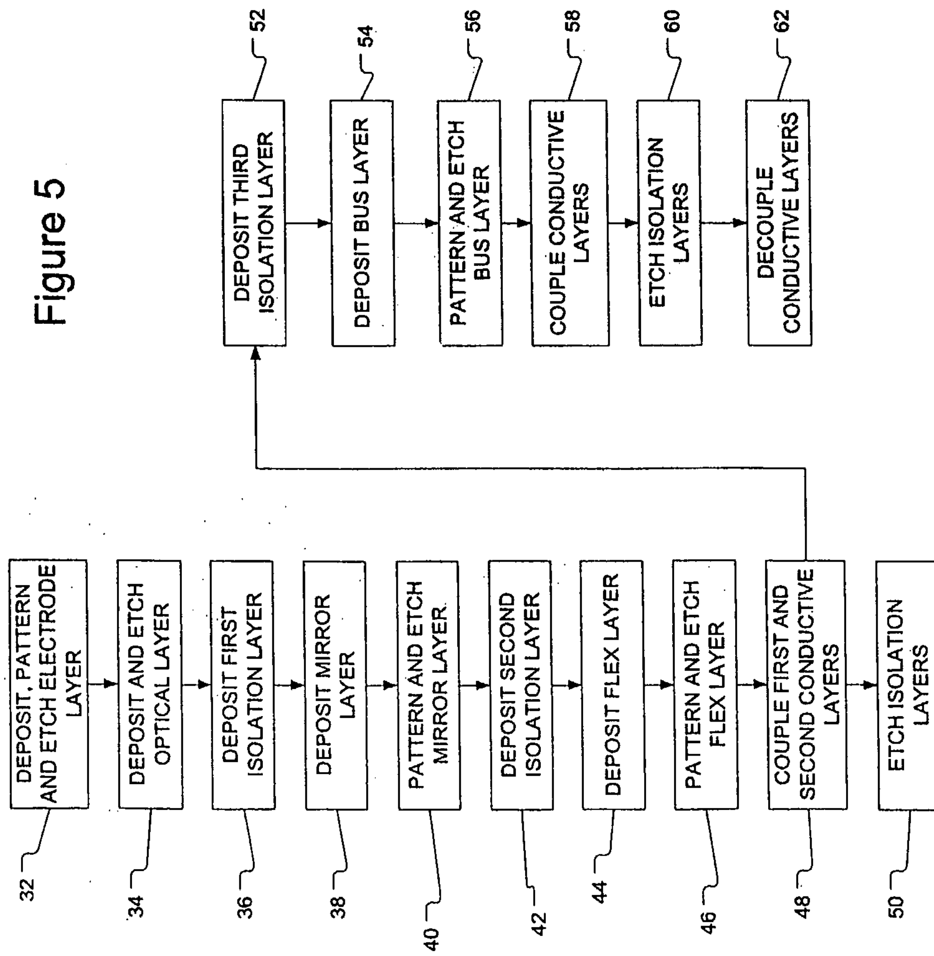

Figure 5

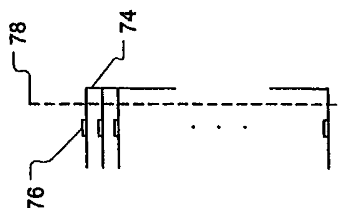

Figure 6b

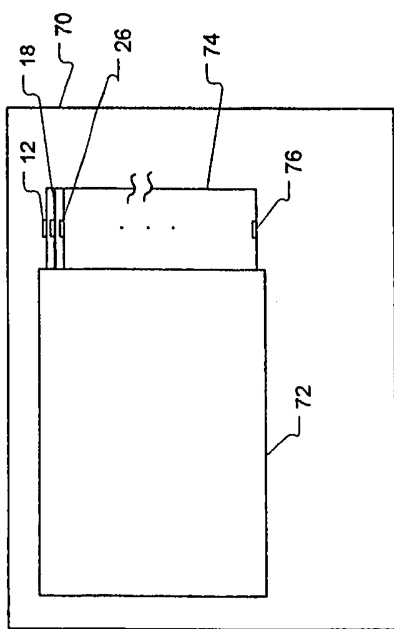

Figure 6a

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2005/013462

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 B81C1/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 B81C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 096 279 A (HORNBECK ET AL) 17 March 1992 (1992-03-17) figures 6-8,10 paragraph '0052! - paragraph '0065! -----	1-6,9, 10,14, 16,19-21
X	US 2004/008402 A1 (PATEL SATYADEV R ET AL) 15 January 2004 (2004-01-15) figures 1a,1b,4,7,15,35a-35e,37a-37c column 9, lines 28-44 column 13, lines 14-36 column 24, line 39 - column 25, line 63 -----	1,4,5,7, 8,11-15, 17-21

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
15 September 2005	04/10/2005

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2002/158348 A1 (PETRUCCI JOSEPH ET AL) 31 October 2002 (2002-10-31) figure 3 paragraphs ‘0012! - ‘0020! paragraph ‘0025!	1-21
A	US 2002/111031 A1 (CHASE TROY A ET AL) 15 August 2002 (2002-08-15) paragraph ‘0027!; figures 1-3	1,14

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2005/013462

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
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US 2004008402	A1	15-01-2004	NONE	
US 2002158348	A1	31-10-2002	NONE	
US 2002111031	A1	15-08-2002	NONE	