METHOD FOR LOW-COST REDISTRIBUTION AND UNDER-BUMP METALLIZATION FOR FLIP-CHIP AND WAFER-LEVEL BGA SILICON DEVICE PACKAGES

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ABSTRACT

A method for redistributing bond pad locations on an IC die incorporates steps of (a) depositing a dielectric layer over the IC die and opening vias through the dielectric layer to the bond pads; (b) depositing a thin seed layer of electrically conductive material over the dielectric layer and exposed bond pads, and patterning the seed layer to provide redistribution lines from individual ones of the bond pads to new locations for the bond pads; and (c) increasing the thickness of the redistribution lines by electroplating a conductive material onto the seed layer material. In some cases multiple relocations are made in the distribution.

1. Apply Dielectric Material and Develop to Open vias to Bond Pads
2. Sputter Seed Layer of Copper or Copper Alloy, Pattern and etch
3. Plate up RDL by electroplating
4. Optionally electroplate UBM and Solder Bumps

Low-Cost Redistribution
Apply Dielectric Material and Develop to Open vias to Bond Pads

Sputter Seed Layer of Copper or Copper Alloy, Pattern and etch

Plate up RDL by electroplating

Optionally electroplate UBM and Solder Bumps

Low-Cost Redistribution

Fig. 3
501

Apply First Dielectric Material and Develop to Open vias to Original Bond Pads

502

Deposit and Pattern First RDL to Intermediate Locations

504

Apply Second Dielectric Material and Develop to Open vias to Intermediate Locations

505

Deposit and Pattern Second RDL to Final Locations

506

Provide UBM as Needed

507

Solder-Bumping

Multiple-Level Redistribution

Fig. 5
METHOD FOR LOW-COST REDISTRIBUTION AND UNDER-BUMP METALLIZATION FOR FLIP-CHIP AND WAFER-LEVEL BGA SILICON DEVICE PACKAGES

FIELD OF THE INVENTION

[0001] The present invention is in the field of low-profile electronic circuit devices, and pertains more particularly to methods for wafer-level bond pad redistribution, solder bumping and under bump metallization in a wafer-level or flip-chip package.

BACKGROUND OF THE INVENTION

[0002] The field of integrated circuit interconnection and packaging is a rapidly-evolving technology associated with semiconductor manufacturing, and modern microelectronic products require integrated electronic packages that address the driving forces of reduced size and weight, as well as increased performance and reliability. Wafer-level manufacturing and flip-chip packaging technologies for Ball Grid Array (BGA) silicon devices are at the forefront of preferred miniaturization solutions, and the need for smaller size, increased I/O and finer pitch in a BGA device has driven much work related to methods for chip stacking and interconnection.

[0003] Most silicon wafers for use in current flip-chip packaging schemes are designed for wire bonding with peripheral pad configurations in ultra fine pitch, allowing many flip-chip package to reduce production costs by preparing the inexpensive and widely available wafer level chips for a flip-chip package by redistributing the peripheral bond pads to area-array pads on a substrate with larger pad sizes and a relaxed pitch.

[0004] In semiconductor manufacturing technology, chip design typically has contact pads around the peripheral edges of a finished chip. This is because the conventional connection technology is for bonding wires to these pads to lead away from the chip, to connect the circuitry on the chip to other circuits, such as printed circuit boards. In the development of such methods in the art, more recent technologies make connection from the chip by other means than wire bonding, such as solder bumping. In the use of these technologies it is often desirable to have the bond pads in a different pattern at a different place on the chips. This requirement has led to what is known in the art as redistribution, wherein connection points on a chip, originally at the edges of the chip, are redistributed to other places. Redistribution is a well-known concept to the skilled in the art.

[0005] In a flip-chip packaging scheme where redistribution methods are utilized, several deposition methods are well known in the art for forming redistribution lines (RDL) and under-bump metallization (UBM), and for solder bumping of the redistributed contact pads. At the time of the present application a standard technology for a wafer RDL process is based on sputtering and the use of high-end dielectrics such as benzo-cyclo buthen (BCB) or polyimide. These dielectrics, however, are invariably associated with high cost. RDL in a typical application of current art usually comprise multi-metal layers for adhesion and diffusion, having an aluminum (Al) outer coating that provides a conductive layer to the bond pads of die on the wafer, also typically aluminum, and the new solder bump location.

[0006] In conventional techniques an additional passivation layer is required to protect the aluminum lines of the RDL. Also in current art the standard technology for UBM is based on the well-known sputtering processes, which requires several layering process steps similar to those required for RDL, and also involves the use of costly dielectric materials.

[0007] Conventional deposition techniques are often prohibitively expensive because each require a multitude of complex process steps, often involving excessive material, time and resource waste. Many successive layers also add significantly to the profile of the finished structure. In current solder printing methods closeness of the pitch of printed solder bumps is somewhat limited, and costly equipment is often required to handle larger wafers using such conventional deposition methods, further limiting scalability and economy of the operation.

[0008] What is clearly needed is an improved RDL and UBM method for flip-chip and wafer level packages that avoids conventional sputtering and evaporation processes, and involves fewer process steps in the deposition of layers, masking and photo imaging, and other related processes. In the present invention such an improved redistribution method incorporates electroplating technology, using, in a preferred embodiment, improved copper materials in the formation of RDL and UBM layers, and resulting in a very low-profile silicon structure with RDL and UBM formed with fewer layers and having increased reliability, conductivity and economy, and providing lower capital cost and improved productivity when compared to conventional methods and materials. The equipment utilized in the improved process in preferred embodiments is capable of high-volume production and is able to handle a variety of wafer sizes, pitches and area array configurations. Such an improved redistribution method for wafer level and flip-chip packages is described below in enabling detail.

SUMMARY OF THE INVENTION

[0009] In a preferred embodiment of the present invention a method for redistributing bond pad locations on an IC die is provided, comprising the steps of (a) depositing a dielectric layer over the IC die and opening vias through the dielectric layer to the bond pads; (b) depositing a thin seed layer of electrically conductive material over the dielectric layer and exposed bond pads, and patterning the seed layer to provide redistribution lines from individual ones of the bond pads to new locations for the bond pads; and (c) increasing the thickness of the redistribution layers by electroplating a conductive material onto the seed layer material.

[0010] In preferred cases the seed layer is no more than 2000 Angstrom units in thickness. There may also be a step for providing solder bumps at the new bond pad locations. Also in preferred embodiments the seed layer conductive material is copper or a copper alloy, and the electroplating step plates copper or a copper alloy onto the seed layer.

[0011] In some cases there is a further step in the method for applying an under-bump metallization by plating technique before the step for solder bumping.

[0012] In preferred embodiments, in step (a), the dielectric layer is one of silicon oxide or polyamide material. Also in preferred embodiments, in step (b), the seed layer is deposi-
ated by sputtering technique, but the seed layer may also be deposited by an electropolishing plating technique.

[0013] In another aspect of the invention a method for redistributing bond pad locations on an IC die is provided, comprising the steps of (a) depositing a first dielectric layer over the IC die and opening vias through the first dielectric layer to the bond pads; (b) depositing a first layer of electrically conductive material over the dielectric layer and exposed bond pads, and patterning the first layer to provide redistribution lines from individual ones of the bond pads to first redistributed locations for the bond pads; (c) depositing a second dielectric layer over the first redistribution lines and opening vias through the second dielectric layer to the intermediate locations; and (d) depositing a second layer of electrically-conductive material over the second dielectric layer and exposed intermediate locations, and patterning the second layer to provide redistribution lines from individual ones of the intermediate locations to second redistributed locations.

[0014] There may be, in some embodiments, more than two intermediate locations of the bond pads. Also in some embodiments one or both of the first and second electrically-conductive layers is provided by applying a thin seed layer and then increasing the thickness of the electrically-conductive layer by plating technique. The seed layer in preferred embodiments is no more than 2000 Angstrom units in thickness. Also, there may be a step for providing solder bumps at the second redistributed locations.

[0015] In preferred embodiments the seed layer conductive material is copper or a copper alloy, and the electroplating step plates copper or a copper alloy onto the seed layer. There may also be a step for applying an under-bump metallization by plating technique before the step for solder bumping.

[0016] In preferred embodiments of the invention, in step (a), the dielectric layer is one of silicon oxide or polyamide material, and the seed layer is deposited by sputtering technique or an electropolishing plating technique.

[0017] In embodiments of the invention taught in enabling detail herein, for the first time a redistribution technique using plating is provided, and a technique for relocating bond pads in a multiple of steps.

BRIEF DESCRIPTIONS OF THE DRAWING FIGURES

[0018] FIG. 1a is a cross-sectional view of a conventional semiconductor substrate showing a bond pad and a primary passivation layer in a redistribution method according to prior art.

[0019] FIG. 1b is a cross-sectional view of the semiconductor structure of FIG. 1a showing a redistribution line.

[0020] FIG. 1c is a cross-sectional view of the semiconductor structure of FIG. 1b showing a secondary passivation layer.

[0021] FIG. 1d is a cross-sectional view of the semiconductor structure of FIG. 1c showing UBM and solder bump.

[0022] FIG. 2a is a cross-sectional view of a conventional semiconductor substrate with a bond pad and a primary passivation layer in an improved redistribution method according to an embodiment of the present invention.

[0023] FIG. 2b is a cross-sectional view of the semiconductor structure of FIG. 2a showing a redistribution line layer.

[0024] FIG. 2c is a cross-sectional view of the semiconductor structure of FIG. 2b showing UBM and solder bump.

[0025] FIG. 3 is a process flow chart for a low-cost redistribution method according to a preferred embodiment of the present invention.

[0026] FIG. 4 is a cross-section view of a semiconductor structure showing redistribution in multiple steps to a series of locations.

[0027] FIG. 5 is a flow diagram for steps in producing the structure shown in FIG. 4.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0028] FIG. 1a is a cross-sectional view of a conventional semiconductor substrate with a bond pad and a primary passivation layer in a redistribution method according to prior art. In FIG. 1a a conventional semiconductor structure 101 is shown that is built upon a silicon substrate 103 having active circuitry (not shown). Substrate 103 has a pad 113 formed on the top surface 105 of substrate 103 for the purpose of making electrical connections to outside circuitry. Bond pad 113 is electrically connected to active circuits (not shown) within substrate 103. Bond pad 113 in this example may be formed of any one of a variety of metals for different purposes, and may have overlayers to prevent diffusion of metal atoms in subsequent steps, as is known in the art.

[0029] In this prior art example a passivation layer 109 is applied to the upper surface 115 of bond pad 113 and to upper surface 105 of substrate 103 using one of a variety of well-known application methods. Passivation layer 109 is typically a dielectric material using any one of the various insulating materials used in current art such as silicon oxide, polyamide or benzocyclobutene (BCB), or other commercially used material, and has the purposes of planarization and physical protection of circuits formed on structure 101. Passivation layer 109 is then developed and etched using a known photolithography process to pattern an opening 117 above the existing bond pad 113 to expose at least a portion of bond pad 113 for the purpose of allowing an electrical connection to bond pad 113. In subsequent layering, RDL and UBM layers are deposited onto upper surface 111 of passivation layer 109.

[0030] FIG. 1b is a cross-sectional view of semiconductor structure 101 of FIG. 1a showing further development. In this view a multi-layer RDL is formed, using conventional sputtering technology, onto the upper surface 111 of passivation layer 109, completely covering passivation layer 109 and the exposed upper surface 115 of pad 113. As is true for conventionally formed redistribution lines, RDL layer 119 is formed of multiple layers (121, 123) of metals such as titanium alloys and sometimes chrome or copper, with a final coating of aluminum. In the next step a photoresist layer is applied, by various means known in the art, to the top surface of RDL layer 119, and the photoresist layer is then
developed to pattern the desired RDL placement, and the excess RDL metal is then etched away using known processes to form the final RDL traces. An additional passivation layer is then typically required for structure 101 in order to protect the aluminum sputtered redistribution lines of RDL layer 119.

[0031] FIG. 1c is a cross-sectional view of a semiconductor structure 101 of FIG. 1b showing in addition a secondary passivation layer 125. Layer 125 is applied to the top surface of RDL layer 119 using methods known in the art, and is then developed to form an opening 127 that is strategically located to expose a portion of the upper surface of RDL layer 119, onto which solder bumping of the new redistributed bond pad will take place. The next step in the conventional redistribution method of FIGS. 1a through 1d is the formation of the under-bump metallurgy for improving electrical contact between the redistribution lines and the solder bumps.

[0032] FIG. 1d is a cross-sectional view of a semiconductor structure 101 of FIG. 1c with UBM and solder bump. UBM 131, as is typical in a conventional application as shown, is multilayered with different metals, typically beginning with an adhesion/diffusion layer of titanium/tungsten alloy or possibly chrome or some other metal, and a final solder-wettable layer typically formed of copper or nickel or suitable alloys. The primary UBM layer is deposited, by sputtering, in this example, to the upper surface 126 of passivation layer 125. Additional sputtered layers may be used in UBM 131 in this conventional example, such as a thin phase layer, or seed layer, between the adhesion/diffusion layer and the wettable layer, or possibly a gold layer formed over the copper or nickel layer in order to prevent oxidation of the copper prior to subsequent processing.

[0033] Once all of the various layers have been deposited for UBM 131, a known photolithography process is used to define the area onto which solder bumping will take place at the newly redistributed contact location, and the excess UBM metal is then etched away leaving UBM metal only at the desired locations. Solder bumping is then performed using solder print technology in this example, to form a solder bump or ball 133 directly above and in electrical contact with UBM 131, which now makes electrical contact with RDL 119. The resulting bridge circuitry electrically connects bond pad 113 of substrate 103 to solder ball 133, therefore redistributing peripheral bond pad 113 to the area-array location of solder ball 133. The skilled artisan will easily recognize that the cross sections shown above and described are for relocation of one contact pad, and that typically an entire array of pads are relocated.

[0034] Utilizing the above conventional methods for deposition of RDL and UBM, and for formation of solder bumps, involves a relatively large number of steps and processes, each involving significant time, materials and expense, and considerable capital cost. Further, vacuum deposition is a technique that requires high vacuum equipment, and imposes a production limitation. The many successive layers also add significantly to the thickness of the finished structure. In a typical application where a sputtering/evaporation process is used for deposition of RDL, each resulting layer deposited may have a thickness of from 5 to 10 microns, with the final aluminum layer adding an additional thickness to the structure. Subsequent sputtered UBM adds again to the overall height of the finished structure.

[0035] An improved method for UBM, RDL and solder bumping for low-cost redistribution is an important object of the present invention. The method of the invention in a preferred embodiment uses some of the known steps outlined above, but avoids the technology of sputtering/evaporation for UBM and, instead, uses advanced electroplating techniques for at least part of the metal deposition process. The methods of the present invention are enhanced by many known benefits of electroplating, such as lower process costs and the ability to achieve desired contact reliability for very high I/O and tight pitch; and the invention in various embodiments involves a smaller number of process steps, such as for masking and photo imaging, when compared to conventional deposition methods as described above with reference to FIGS. 1a through 1d. The result is a method for redistribution that produces a reliable, high-performance silicon structure that has a desired low profile and can be quickly and economically manufactured.

[0036] Such an improved method for low-cost redistribution is illustrated and described in the following examples. FIG. 2a is a cross-sectional view of a conventional semiconductor substrate with a bond pad and a primary passivation layer in a low-cost redistribution method according to an embodiment of the present invention. It is emphasized that the processes of the invention are preferably applied at wafer-level, before die are separated.

[0037] FIG. 2a shows a silicon substrate 203 that can be considered to be equivalent to the conventional silicon substrate 103 of FIG. 1. However, in this example an improved process comprising electroplating is utilized for forming one, several, or all of the RDL, UBM, and solder bumping, described below in further detail. Referring again to FIG. 2a, a semiconductor structure 201 is provided to illustrate the process steps in the method of the invention. Structure 201 has a substrate 203 similar to that of structure 101 of FIG. 1a, having at least one bond pad 213 formed on top surface 205 of substrate 203. Bond pad 213 is electrically connected to active circuitry (not shown) within substrate 203. Bond pad 213 is formed typically of a metal or alloy as previously described. A passivation layer 209 consisting of dielectric material or some other known passivation compound is applied to the upper surface 215 of bond pad 213 and to upper surface 205 of substrate 203, using a known application method. Passivation layer 209 is then developed by conventional lithographic technique, and etched to pattern an opening 217 above bond pad 213, exposing the upper surface 215 of bond pad 213 for the purpose of allowing an electrical connection from bond pad 213 to outside circuitry. Passivation layer 209 has an upper surface 211 onto which the layers of RDL and UBM metals are to be deposited.

[0038] FIG. 2b is a cross-sectional view of a semiconductor structure 201 of FIG. 2a with a RDL layer in a low-cost redistribution method according to an embodiment of the present invention. In a preferred embodiment a seed layer of titanium/copper alloy is applied by sputtering onto the upper surface 211 of passivation layer 209, to a thickness of about 1000 to 2000 Angstrom units. In the prior art vacuum deposition is required to deposit layers of from 5000 to 30,000 Angstroms in thickness. Further, an additional adhe-
A key difference between the invention in a preferred embodiment and the prior art is that, after plate up in the present process, no UBM steps may be needed. The copper or copper alloy pads resulting from plating are inherently solder-wettable, as opposed to the aluminum or aluminum alloy pads that result from conventional processing. Further, in the prior art, a copper layer is sometimes sputtered on the aluminum or aluminum alloy pads to provide wettability, but solder, when applied, can absorb the copper from the thin sputtered coating, and destroy the adhesion. In the case of the present invention the pads are all copper or copper alloy, and the absorption of copper by the solder is not a problem. The resulting bonds are much more robust than in the prior art.

FIG. 2c is a cross-sectional view of semiconductor structure 201 of FIG. 2b. The improved redistribution method of the invention utilizes advanced electroplating deposition techniques forming an UBM layer as well as for solder bump deposition at the new contact location. An advantage is gained over conventional redistribution methods based on sputtering, for example, for RDL and UBM formation because several process steps required for such conventional methods for are not required in the improved method of the present invention. Patterning and location of solder bumps in an electroplating deposition process such as it is used in the method of the current invention is accomplished through photolithography techniques, allowing for a broad range of solder bump sizes, patterns and pitch.

Referring now to FIG. 2c, an UBM layer is deposited in this example utilizing electroplating techniques, comprising, in a preferred embodiment a layer of nickel and a wettable copper outer layer. Other similar metals may be used, however, in alternative methods of the present invention. The UBM layer is then patterned using known photolithography techniques to leave a deposition of UBM metals shown in this view as UBM 231, covering opening 222 and metallurgically attached to the exposed surface of RDL 219, thereby forming a new redistributed bond pad for solder bumping.

A preferred embodiment of the method of the present invention utilizes known electroplating techniques for solder bumping over the UBM. Solder bump 233 is formed directly over and completely covering UBM 231, metallurgically attaching to UBM 231. In an alternative method of the present invention solder bumping may be accomplished through known screen print soldering techniques, by some other known method. The excess metal of RDL 219 is then etched away using known methods.
pads, an RDL conductive layer is formed, then patterned and etched, to provide conductive lines to new locations to relocate the bond pads, then under-bump metallization is accomplished, if needed, and solder bumps are added to provide for such as flip-chip and other processes.

[0050] In conventional processes, and even in the new processes described above for embodiments of the present invention, there is still some room for improvement in the area of strength and shock absorbancy. Because of these relative shortcomings, extra procedures in assembly are often used, such as underfill, wherein a filler material is added between solder-bumped devices and other devices or boards to which they are assembled.

[0051] In a preferred embodiment of the present invention redistribution is done in at least two steps, using at least two dielectric layers, to provide additional shock resistance, fatigue resistance, and compressive, torsional, and tensile strength.

[0052] FIG. 4a is a cross-sectional view of a structure wherein redistribution has been accomplished in two steps according to an embodiment of the present invention. A portion 401 of a wafer is illustrated in cross-section having one original bond pad 402. In preferred embodiments the processes of the invention are accomplished at wafer-level over many IC die, and each die has, of course, many bond pads. One original bond pad, however, for a single die, is sufficient to illustrate the features of the present invention, and will avoid confusion.

[0053] In FIG. 4a a first dielectric layer 403 has been added to the front surface of the wafer over bond pad 402, and a via opened in layer 403 to expose the bond pad. Then a first RDL layer has been deposited and patterned and etched to leave a redistribution line 404 in contact with pad 402, but separated from the wafer by dielectric layer 403. This RDL redistributes bond pad 402 to a new and intermediate location 406. In various embodiments of the invention the RDL may be made by conventional methods or by any of the unique processes described above as embodiments of the present invention.

[0054] Following the first redistribution a second dielectric layer 405 is deposited over the first RDL 404, and a via is opened to expose the intermediate location at 406. A second RDL layer is now deposited and patterned to provide a second redistribution line 407 in contact with RDL 404 at position 406. RDL 407 leads to a new location where an under-bump metallization 408 may be added (if needed), and a solder bump 409 provided. Solder bump 409 is now relocated (redistributed from original pad 402) location, and has been redistributed through an intermediate location (406) in two geographic steps.

[0055] The cross-section of FIG. 4a suggests that the redistribution in the second step is directly back toward the original bond pad location, but this is exemplary only. After the redistribution to the intermediate location, second and subsequent redistributions can be in any direction substantially parallel to the surface of the wafer or die, and the two-step shown may be a three-step or more distribution. It should be noted that each redistribution involves a new dielectric layer, and the end result has as many new layers as RDL steps made.

[0056] This unique multiple-step redistribution may be accomplished with conventional processing techniques, as described above for the prior art, using sputtering or vapor deposition for the RDL, or may be accomplished using the plate-up techniques described above as embodiments of the present invention, in which case UBM may not be necessary. Solder bumping, as previously described, may be by screening, plating, or by other technique. Further, the second and subsequent RDL steps may be accomplished upon a wafer or die upon which a first redistribution has already been done.

[0057] The multiple-layer redistribution described with reference to FIG. 4a has been found by the inventor to significantly enhance strength and durability for the structures created, compared to the single-level RDL as practiced in the current art, providing improved shock resistance, fatigue resistance, and compressive, torsional, and tensile strength.

[0058] To further illustrate the range of applications and situations, at least in part, that may be accomplished, FIGS. 4b, 4c and 4d, 4e and 4f are provided. FIG. 4b illustrates a situation wherein an original location associated with pad 410 has been moved in a first jump to position 411, and in a second jump to position 412 where a solder ball 413 has been added.

[0059] FIG. 4c illustrates a situation wherein a pad 414 has been moved to an intermediate location 415 in a first step, and then to a final location in a second step, just as in the case according to FIG. 4b, and a wire has been bonded at the final location.

[0060] FIG. 4d illustrates a situation wherein a pad at a first location 418 has been moved to an intermediate location 419, and then back to a third location 420, which is substantially over the original location 418, so redistribution has not been accomplished in the sense of having a new matrix of connection locations for the device, but which does accomplish the strengthening and durability enhancement that is at the heart of the present invention.

[0061] FIG. 4e is a cross-section very much like that of FIG. 4d, wherein the final location 422 is over the original location 423, after relocation to intermediate location 424, except that a wire bond 425 is done at the final location instead of a solder bump.

[0062] FIG. 4f is a cross section to illustrate yet another geography in an embodiment of the invention. In this case a first location 426 is moved to two intermediate locations 427 and 428, and then to a final location 429, where a solder bump 430 is implemented. Clearly, the same geography might be used with a wire bond instead.

[0063] All of the illustrations provided are two layer processes, but it will be clear to the skilled artisan that more layers and relocations may be done as well.

[0064] FIG. 5 is a flow chart 501 illustrating steps in practice of the multiple-layer redistribution described above in an embodiment of the invention. At step 502 a first dielectric layer is formed and developed to open vias to original bond pad locations on a wafer or die. At step 503 a first RDL is done to redistribute the original locations to intermediate locations. At step 504 a second dielectric material is deposited and patterned to open vias to the intermediate locations. At step 505 a second RDL is accomplished to redistribute the intermediate locations to final locations. At step 506 UBM is provided, if needed, and at step 507 solder-bumping is done.
[0065] Again, the two step process can be three or more steps in alternative embodiments of the invention, and the processing can follow any mixture of conventional techniques or the unique techniques taught herein in embodiments of the present invention.

[0066] It will be apparent to one with skill in the art that the methods of the present invention may be practiced in variations of presented configurations without departing from the spirit and scope of the invention. The inventor has provided exemplary illustrations and flow charts for describing at least one embodiment of the present invention, therefore, the inclusion of illustrated or described well-known devices, processes, and materials in the embodiments presented should not be construed as a limitation in any way to the practice of the invention. Furthermore, the methods of the present invention for low-cost redistribution described herein, although illustrated primarily with reference to certain deposition methods such as sputtering and electroplating, should be recognized as applicable also to various types of silicon wafers with bond pads comprising various metals, and to a wide variety of peripheral to area array redistribution configurations and wafer level or flip-chip operations. Therefore the method of the present invention should be afforded the broadest possible scope under examination. This spirit and scope of the present invention is limited only by the claims that follow.

What is claimed is:

1. A method for redistributing bond pad locations on an IC die, comprising the steps of:
   (a) depositing a dielectric layer over the IC die and opening vias through the dielectric layer to the bond pads;
   (b) depositing a thin seed layer of electrically conductive material over the dielectric layer and exposed bond pads, and patterning the seed layer to provide redistribution lines from individual ones of the bond pads to new locations for the bond pads; and
   (c) increasing the thickness of the redistribution lines by electroplating a conductive material onto the seed layer material.

2. The method of claim 1 wherein the seed layer is no more than 2000 Angstrom units in thickness.

3. The method of claim 1 further comprising a step for providing solder bumps at the new bond pad locations.

4. The method of claim 1 wherein the seed layer conductive material is copper or a copper alloy.

5. The method of claim 1 wherein the electroplating step plates copper or a copper alloy onto the seed layer.

6. The method of claim 3 further comprising a step for applying an under-bump metallization by plating technique before the step for solder bumping.

7. The method of claim 1 wherein, in step (a), the dielectric layer is one of silicon oxide or polyamide material.

8. The method of claim 1 wherein, in step (b), the seed layer is deposited by sputtering technique.

9. The method of claim 3 wherein, in step (b), the seed layer is deposited by an electroless plating technique.

10. A method for redistributing bond pad locations on an IC die, comprising the steps of:
   (a) depositing a first dielectric layer over the IC die and opening vias through the first dielectric layer to the bond pads;
   (b) depositing a first layer of electrically conductive material over the dielectric layer and exposed bond pads, and patterning the first layer to provide redistribution lines from individual ones of the bond pads to first redistributed locations for the bond pads;
   (c) depositing a second dielectric layer over the first redistribution lines and opening vias through the second dielectric layer to the intermediate locations; and
   (d) depositing a second layer of electrically-conductive material over the second dielectric layer and exposed intermediate locations, and patterning the second layer to provide redistribution lines from individual ones of the intermediate locations to second redistributed locations.

11. The method of claim 10 comprising steps for more than two intermediate locations of the bond pads.

12. The method of claim 10 wherein one or both of the first and second electrically-conductive layers is provided by applying a thin seed layer and then increasing the thickness of the electrically-conductive layer by plating technique.

13. The method of claim 12 wherein the seed layer is no more than 2000 Angstrom units in thickness.

14. The method of claim 10 further comprising a step for providing solder bumps at the second redistributed locations.

15. The method of claim 10 wherein the seed layer conductive material is copper or a copper alloy.

16. The method of claim 12 wherein the electroplating step plates copper or a copper alloy onto the seed layer.

17. The method of claim 14 further comprising a step for applying an under-bump metallization by plating technique before the step for solder bumping.

18. The method of claim 10 wherein, in step (a), the dielectric layer is one of silicon oxide or polyamide material.

19. The method of claim 12 wherein the seed layer is deposited by sputtering technique.

20. The method of claim 12 wherein the seed layer is deposited by an electroless plating technique.

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