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(54) SEMICONDUCTOR DEVICES AND METHODS OF MANUFACTURING
 THE SAME

(71) We, NIPPON TELEGRAPH AND TELEPHONE PUBLIC CORPORATION, a corporation organised and existing under the laws of Japan, of 6, 1, Uchisaiwai-cho 1-chome, Chiyoda-ku, Tokyo, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor devices in which an electrode is formed on a polycrystalline silicon body extending upwardly from a semiconductor substrate, and to methods of manufacturing the same.

In the manufacture of various semiconductor devices, such as transistors and integrated circuits, improvements in the accuracy of the manufacturing techniques are desirable for the purpose of improving the characteristics of the devices. In particular, for improving the high frequency characteristics of bipolar silicon transistors for use at ultra high frequencies it is necessary to provide close tolerance working techniques for increasing the cutoff frequency and decreasing the base resistance and the collector-base junction capacitance.

However, in prior art transistors of this type the emitter, base and collector electrodes are formed in the same plane. It is therefore usual to instal these electrodes at a spacing of about one micron for the purpose of electrically insulating them from each other. It has been recognized that when the spacing is made smaller, the transistor can be operated at higher frequencies. However, such spacing is limited by the accuracy of a photomask.

More particularly, among the problems regarding the photomasks are included (a) the dimensional accuracy of a device pattern formed on a photomask, (b) the pitch accuracy of the device pattern formed on the photomask, and (c) the accuracy of alignment between the device pattern already formed on a semiconductor wafer

and the device pattern of the photomask to be subsequently used. For this reason, when designing a photomask it is necessary to prepare the photomask having sufficient dimensions of the device pattern which permit respective errors in the accuracies described above. Where a device pattern having a small allowance for the alignment of the semiconductor wafer and the photomask is used with sacrifice of the yield, and the alignment is made carefully with a sufficient time, the chance of contaminating and damaging the semiconductor wafer increases and the characteristics of the resulting semiconductor device are degraded.

Furthermore, the working of metal films which are used to form electrodes also requires highly accurate working. More particularly, in order to obtain an electrode having a large current capacity the electrode should have a correspondingly larger cross-sectional area so that where the pattern width is limited due to design considerations, the thickness of the metal film to be worked becomes thick. When a thick metal film is etched a substantial undercut appears thus making it difficult to attain the desired high accuracy of working.

Even when a skilled engineer carefully works there are errors of about ± 0.2 micron in a dimension of the device pattern on the photomask, about ± 0.3 micron in the device pattern pitch, and about ± 0.3 micron in the alignment, namely a cumulative error of about ± 0.8 micron. In addition, it is necessary to take into consideration errors in the dimensions of the device pattern on the photomask, a photoresist pattern which is formed by baking the device pattern on the photoresist film and then developing, and a pattern formed by etching the substrate of the mask by using the photoresist pattern. In this manner, when photoetching techniques are used to obtain products having dimensions of the order of microns it is inevitable that dimensional errors occur in the products.

In the case of an integrated circuit, lead wires for interconnecting various electrodes should be arranged in a plane with insulating spacings therebetween or in multilayers 5 with insulator layers interposed therebetween.

According to the present invention, there is provided a semiconductor device comprising a semiconductor substrate, a polycrystalline silicon semiconductor body containing an impurity at a substantially uniform concentration and extending upwardly from a portion of the surface of the semiconductor substrate, and a metal electrode formed on the top surface of the polycrystalline silicon semiconductor body by a plating technique and extending in the lateral direction beyond the periphery of 10 the top surface of said polycrystalline silicon semiconductor body.

In another aspect the invention provides a method of manufacturing a semiconductor device comprising forming a polycrystalline silicon semiconductor body on a portion of 15 a surface of a semiconductor substrate, and then forming a metal electrode by a plating technique on the top surface of said polycrystalline silicon body to extend in the lateral direction beyond the periphery of 20 the top surface of said polycrystalline silicon semiconductor body.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in 25 which:

Figs. 1A and 1B are sectional views showing portions of previously proposed semiconductor devices of the type wherein one of the electrodes is formed on a polycrystalline silicon body extending upwardly 30 from the semiconductor substrate;

Fig. 2 is a sectional view showing one embodiment of a semiconductor device embodying the invention;

Figs. 3A to 3N are sectional views showing successive manufacturing steps of the semiconductor device shown in Fig. 2;

Figs. 4A to 4D are sectional views corresponding to Figs. 3A to 3N and showing successive steps of manufacturing a modified semiconductor device of this invention;

Figs. 5A and 5B are sectional views showing various steps of manufacturing another modification of the semiconductor device 55 of this invention;

Figs. 6A to 6D are sectional views, partly in perspective, showing successive steps of manufacturing resistors and inside wirings of an integrated circuit embodying the 60 invention;

Fig. 7 shows a sectional view of a portion of a MOS transistor embodying the invention; and

Figs. 8A to 8C are sectional views showing 65 the relationship between a polycrystal-

line silicon body and a metal mask useful to explain the invention.

For the purpose of improving the characteristics of certain integrated circuits it has been proposed to dispose one of the coplanar electrodes in the longitudinal direction with respect to other electrodes, thereby eliminating the spacing between electrodes. This is disclosed in copending Japanese patent publication No. 16312, 70 1976, and will be described hereunder with reference to Figs. 1A and 1B.

Fig. 1A shows the electrode construction of a transistor of the Japanese patent publication wherein an emitter electrode 12a is formed on a saucer shaped polycrystalline silicon body 11a, and Fig. 1B shows a similar electrode construction of a transistor wherein an emitter electrode 12b is formed on a polycrystalline silicon body of an inverted frustum shape. These transistors having polycrystalline silicon bodies of the saucer or inverted frustum shape are characterised in that the polycrystalline silicon bodies are used to form diffused emitter layers 13a and 13b; that the width W_1 of the upper surface is made larger than the width W_2 at the lower end of the body where it contacts the silicon substrate; and that base electrodes 14a and 14b are formed by utilizing the difference in the widths ($W_1 - W_2$). If desired, base contact diffusion can also be made. In Figs. 1A and 1B, 15a and 15b show diffused base regions and 16a and 16b diffused collector 80 regions.

With the constructions shown in Figs. 1A and 1B, the positional relationship between the emitter electrodes 12a and 12b and the base electrodes 14a and 14b of the 105 transistors is determined by the shape (saucer and inverted frustum) of the polycrystalline silicon bodies so that the high frequency characteristic of the transistor can be improved.

Where such electrode construction is applied to the gate electrode of a MOS transistor it is possible to assure self-alignment of the source and drain electrodes. Also in an integrated circuit it becomes 115 possible to form, at a high density, internal wirings and resistor elements without using interlead insulating layers.

However, such advantages can be realized in the transistors of the type described 120 above only by shaping the sectional configuration of the polycrystalline silicon body to have accurate saucer or inverted frustum shape. Accordingly, it is necessary to etch the polycrystalline silicon bodies to have accurate sectional configuration. In the construction shown in Fig. 1A, when the position of the photoresist pattern, not shown, that determines the position of the polycrystalline silicon body 11a, differs 125 130

slightly from the position of the diffused emitter layer 13a, a non-uniform current distribution or a short circuit between the emitter and base electrodes results thus degrading the characteristics of the transistor. In the construction shown in Fig. 1B, unless the difference between W_1 and W_2 is made substantial the isolation between the emitter electrode 12b and the base electrode 14b becomes difficult to achieve thus causing short circuiting or current leakage.

Considering these problems in more detail, the inverted frustum is formed by utilizing the variation in the etching speed which is different depending upon the concentration of the impurities contained in the polycrystalline silicon body. With a chemical etching method it is difficult to independently control the amount of etching in the horizontal and vertical direction. Consequently, if the amount of etching is not sufficient at the inclined side surface of the inverted frustum short circuiting between the emitter and base electrodes would be resulted. On the other hand, if the amount of etching of these portions were too large the area of the emitter electrode would become too small, thus limiting the current capacity. Furthermore, in the constructions shown in Figs. 1A and 1B it is impossible to make sufficiently large the thickness of the emitter electrode, since if the thickness of the emitter electrode were too large, for example 0.3 micron or more, the spacing between the base and emitter electrodes would become too small thus causing short circuiting. For this reason, with this construction it is impossible to obtain transistors having a large current capacity (that is emitter electrode having a large sectional area).

Fig. 2 shows one embodiment of semiconductor device according to this invention, more particularly a NPN type bi-polar transistor comprising a P type silicon semiconductor substrate 21 and an N type silicon epitaxial layer 21a formed on one surface of the substrate 21. An isolating layer 21b is formed at a suitable region of the epitaxial layer by diffusing a P type impurity to reach the P type silicon substrate 21 so that a collector region 23 is formed by the portion of the N type silicon epitaxial layer isolated by the isolating layer 21b. A base region 24 is formed by diffusing a P type impurity into a portion of the collector region 23. Furthermore, an N^+ emitter region 25 is formed by diffusing an N type impurity into a portion of the base region 24. There are provided an N^+ type buried layer 27 and N^+ diffused contact region formed in the collector region 23 and electrically connected with the buried layer 27. Reference characters 30 and 31 show P^+ contact regions formed in the base region

24. A polycrystalline semiconductor body 33 (for example polycrystalline silicon body) is disposed on the emitter region 25 to extend upwardly. The polycrystalline silicon body 33e has substantially uniform impurity concentration and its sectional configuration at the base in contact with the emitter region 25 and that at the top are substantially the same, that is the vertical section of the polycrystalline silicon body is rectangular. Insulating films, for example SiO_2 films 34, are provided to cover the side surfaces of the polycrystalline silicon body 33, and portions of the emitter region 25 and the base region 24. A prime metal layer 35 is provided on the top surface of the polycrystalline silicon body 33 and an electro plated metal layer 36 is provided to cover the prime metal layer 35. A metal layer 37 is vapor deposited on the plated metal layer 36.

A polycrystalline semiconductor body 40, for example a polycrystalline silicon body, is mounted on the diffused contact region 28 is the collector region 23 to extend upwardly. In the same manner as in the polycrystalline silicon body 33, the periphery of this polycrystalline silicon body 40 is also covered by an insulating film 41 and a prime metal layer 42, a plated metal layer 43 and a vapor deposited metal layer 44 are formed to cover the top surface of the polycrystalline silicon body 40. Prime metal layers 46 and 46a are formed on the base region 30 and the contact region 31 respectively and covered by vapor deposited metal layers 47 and 47a, respectively. Reference characters 46b and 46c represent prime metal layers, 47b and 47c vapor deposited metal layers and 48 an insulating film.

The semiconductor device constructed as above described has the following advantages.

1. Since one of the electrodes of the semiconductor device is formed on a cubic polycrystalline silicon body having a uniform impurity concentration, and since the metal electrode is mounted on the polycrystalline silicon body to laterally extend beyond the periphery thereof it is possible to miniaturize the semiconductor device and to improve the high frequency characteristics thereof just in the same manner as in the semiconductor device provided with peak or inverted frustum shaped electrode. For this reason, the semiconductor device of the invention is suitable to fabricate an integrated circuit.

2. Since the electrode having the construction described above is used as a mask, there is no fear of degrading the characteristics of the transistor due to the misalignment of the photoresist pattern as in the semiconductor device utilizing a peak shaped electrode. Furthermore, with this

construction respective electrodes are positively isolated so that such problems as short circuiting of electrodes and leakage of current do not occur as in the prior art 5 semiconductor device utilizing an inverted frustum shaped electrode.

3. With the electrode constructed as above described, there is no factor that limits the thickness of the electrode as in 10 the prior art construction. Accordingly, it is possible to form an electrode having any desired current capacity.

Sequential steps of manufacturing the 15 semi-conductor device described above will now be described with reference to Figs. 3A through 3N.

At first a semiconductor substrate 50 comprising a P type silicon having thickness of about 200 microns and a specific 20 resistance of 5 to 50 ohms is prepared and then arsenic is diffused into one surface of the semiconductor substrate to form a buried layer 51 having a depth of about 25 two microns and a specific resistance of about 5 to 15 ohms. Then, a N type silicon layer having a specific resistance of from 0.2 and 1 ohm is epitaxially grown on the semiconductor substrate 50 to a thickness of 2 to 3 microns. Thereafter, 30 an oxide film (SiO_2) having a thickness of 0.4 to 0.6 micron is formed. After forming perforations of a predetermined pattern through the oxide film, a P type impurity, for example, is diffused through the 35 perforations to depth of about 3.5 microns and at a concentration of $1 \times 10^{20}/\text{cm}^3$ to form isolating regions 52 and 53. Thereafter, an oxide film is formed over the entire area of the N type silicon epitaxially grown layer 40 and the oxide layer is removed according to a predetermined pattern on a portion of the collector region 54 formed by the isolating region 53. Then a N type impurity, arsenic or phosphorus, is diffused into the 45 exposed portion to the depth of from 2 to 2.5 microns at a concentration of about $1 \times 10^{20}/\text{cm}^3$ to form diffused collector region 55. The oxide film on the other portion of the collector region is removed 50 according to a predetermined pattern and the boron is diffused into the exposed portion of the collector region at a concentration of 5×10^{18} to $1 \times 10^{19}/\text{cm}^3$ to form a base region 56. Then the oxide film on 55 the diffused contact region 55 in the collector region 54 is removed. Reference characters 57a, 57b and 57c show remaining portions of the oxide film. Then, a 60 polycrystalline silicon layer 60 having an impurity concentration of about $1 \times 10^{21}/\text{cm}^3$ and a thickness of 0.35 micron or more is formed on the oxide layer. Thereafter etchant resistant patterns 61a and 61b are formed at suitable positions on the polycrystalline silicon layer 60. These patterns

are not required to have extremely accurate 70 positions as in the prior art semiconductor device. The etchant resistant patterns 61a and 61b can be formed by a photoresist pattern prepared by conventional photoetching technique, or by photoetching a silicon oxide film or a silicon nitride film formed on the polycrystalline film 60 by chemical vapor deposited method.

Then the polycrystalline silicon layer 60 75 on the silicon substrate shown in Fig. 3A is etched by utilizing the etchant resistant patterns 61a and 61b to form a polycrystalline silicon portion 60a for forming an emitter electrode and a polycrystalline silicon portion 60b for forming a collector terminal. One example of the method of forming the polycrystalline silicon portions 60a and 60b for forming the emitter electrode and the collector terminal respectively comprises the steps of masking the etchant resistant patterns 61a and 61b and then etching the silicon wafer in an etching solution of the composition $\text{HF} : \text{HNO}_3 : \text{H}_2\text{O} = 1 : 60 : 60$. Alternatively, the portions 60a and 60b can be formed by plasma etching technique utilizing freon 80 gases.

Then, the etchant resistant patterns 61a 85 and 61b are removed and the surface of the silicon wafer is covered by an insulating silicon oxide film 63 as shown in Fig. 3B. Although this silicon oxide film 63 can be formed by heating the silicon wafer in an oxygen atmosphere at a high temperature 100 (1050°C), it can also be formed by chemical deposition method or by exposing the silicon wafer to a gaseous mixture of hydrofluoric acid and nitrous acid. An oxide film which is formed at the time of forming 105 the emitter layer and the collector contact layer to be described hereunder can be used as the insulating oxide film 63. In this case, the thickness of the oxide film may 110 be of the order of 0.2 to 0.3 micron.

Then, the arsenic doped in the polycrystalline silicon electrode and the collector terminal respectively is caused to diffuse 115 into the base layer 56 and the diffused collector contact region 55 to form an emitter layer 64 and a contact layer 65 by heat treating the silicon wafer at a temperature of 1000°C for 7 minutes. When the depth of the emitter junction X_1 is selected to be 120 0.1 micron, the diffusion occurs uniformly also in the lateral direction so that the width of the emitter layer 64 becomes wider by 0.2 micron than the width of the portion 60a of the polycrystalline silicon body which is used to form the emitter and is in contact with the base layer 56. At the same time, the collector contact layer 65 which is wider than the portion 60b of the polycrystalline silicon for forming the collector 125 terminal by 0.2 micron is formed in the 130

diffused collector contact region 55. Fig. 3B shows this condition, in which only portions relating to subsequent steps are shown.

5 Then a metal film 67 acting as a prime film for plating is applied to cover the entire surface of the insulating silicon oxide film 63 of the silicon wafer in the condition shown in Fig. 3B. This prime metal film 67 can be formed by vapor depositing such metals as nickel, molybdenum, platinum and gold and has a thickness of about 0.1 micron. Fig. 3C shows this condition.

10 Then, a relatively thick photoresist film 68 (positive type) having a thickness of about 1.5 micron is applied on the portions 60a and 60b to cover the insulating silicon oxide film 63 and the prime metal film 67 on surface P of the portion 60a of the polycrystalline silicon for forming the emitter electrode, and the upper surface P' of the portion 60b of the polycrystalline silicon for forming the collector terminal as shown in Fig. 3D. This photoresist film 68 can be formed by applying AZ-1350H sold by Shipley Co. with a conventional film forming device (usually called "spinner") in the following manner. More particularly after mounting the silicon wafer on the spinner, liquid photoresist is dropped in a quantity sufficient to wet the surface of the silicon wafer. Then, the silicon wafer is rotated to remove excess liquid photoresist except a definite quantity remaining on the silicon wafer. The rotation of the silicon wafer is stopped before the photoresist dries, that is while it is still flowable, and the liquid photoresist is dried while the silicon wafer is maintained at the horizontal position.

15 The relationship between the spinning speed and the thickness is disclosed in "Proceedings of the 1970 Kodak Seminar on micro-miniaturization" page 68, Fig. 25, published by Eastman Kodak Co.

20 Then, ultraviolet rays having a uniform intensity is irradiated from above over the entire surface of the silicon wafer in a state shown in Fig. 3D, without using a photomask, as shown in Fig. 3E. Then, the irradiated silicon wafer is developed to remove a portion 68a of the photoresist film 68 to expose a portion R_o of the prime metal film 67 overlying the top surface P of the polycrystalline silicon for forming the emitter electrode. Thus, the portion R_o of the prime metal film protrudes through the remaining portion 68b of the photoresist film. At the same time, a portion R_o' of the prime metal film on the top P' of the portion 60b of the polycrystalline silicon for forming the collector terminal is also exposed. To remove the portion of the photoresist film up to the top surfaces P and P' of the portions 60a and 60b of the polycrystalline silicon by exposing

to light the relatively thick photoresist film 68 it is necessary to control the amount of exposure and the condition of development. Where the thickness of the photoresist is equal to 1.5 microns, the amount of exposure is limited to about 80% of the standard exposure and a development temperature lower than room temperature is used to obtain better results. Where a 200W mercury lamp is used, the lamp is spaced about 40 cm from the silicon wafer and a developing liquid suitable for AZ-1350H photoresist is diluted for a concentration of $\frac{1}{3}$ of the normal and the development is performed for 15 to 30 seconds at a temperature of 10°C. Under these circumstances, it is possible to reduce the thickness of the photoresist film to a thickness of about 1.5 microns while watching the etching operation.

Then under the condition shown in Fig. 3E, the prime metal film exposed through the remaining photoresist film 68b is plated with a metal film by applying a plating potential to the prime metal film 67. By this electroplating mask patterns 70 and 71 are formed having widths R₁ and R₁' respectively which are wider than the bottom surfaces of the polycrystalline silicon semiconductor bodies 60a and 60b as shown in Fig. 3F. A case wherein the mask patterns 70 and 71 are made of gold will be described in the following.

Electrolyte: Temperex 401 (a trade name of Kabushiki Kaisha Nippon Electroplating Engineers)

Plating conditions: current 8mA/cm², 150 sec.

When plating is performed under the conditions described above, the thickness of the plated gold film increases while at the same time as the gold ions uniformly deposit in the lateral direction, the widths R₁ and R₁' of the plating films increase with the increase in the thickness. When a gold film having a thickness of one micron is plated the width thereof becomes 2 microns with the result that the sectional configuration of a combination of the mask pattern 70 and the underlying portion 60a of the polycrystalline silicon for forming the emitter electrode will have a shape of the head of a nail. In the same manner, the combination of the mask pattern 71 and the underlying portion 60b of the polycrystalline silicon for forming the collector terminal also takes the form of the head of a nail. Such phenomena of lateral extension of the mask patterns are described in an article "Metal Does not Deposit Uniformly with Respect to Thickness on All Surfaces" on pages 69-63, of Electroplating Engineering Handbook published in the year of 1955 by Book division Reinhold Publishing Corporation.

Then the photoresist film 68b remaining on the silicon wafer as shown in Fig. 3F is irradiated from above with uniform ultra-violet rays. After development the portions 5 of the photoresist film other than the portions 68c-68f thereof underlying the mask patterns and not exposed to the ultra-violet rays, and the prime metal film are removed by etching, thus preserving metal 10 films 67a and 67b. Such etching can also be performed by plasma etching technique. Then, boron is implanted at a high concentration into the base layer 56 to form base 15 contacts 73 and 74. The implanted boron readily transmits through the insulating silicon oxide film 63 but not through silicon oxide films 57a through 57c which are formed by a thermal treatment. This condition 20 is shown in Fig. 3G.

This process step is characterized in that the base contact, an important element of 25 transistor, is easily and accurately positioned by utilizing the nail head shaped portions underlying the mask patterns 70 and 71. Thus, for example, at the time of forming the emitter layer 64 and the base 30 contacts 73 and 74, the amount of the impurity that moves in the lateral direction through the base layer does not exceed the amount of the impurity (X_1) that moves in the thickness direction. Consequently, when $X_1 = 0.1$ micron, the sum of the 35 thicknesses of the silicon oxide film and the prime metal film is equal to 0.3 micron and the width W of the portion underlying the mask pattern is equal to 0.4 micron, whereby a small spacing W' of 0.6 micron can be assured between the emitter layer 64 and the base contacts 73 and 74 by self-alignment 40 without using any photomask.

This means that the spacing W' between the emitter layer and the base contacts is constant regardless of the fact that the 45 dimensions of the etchant resistant patterns 61a and 61b formed by transfer printing of a conventional photomask differ in a wafer or among different wafers.

After forming the base contacts 73 and 74 as shown in Fig. 3G, the overlying insulating silicon oxide film 63 is removed by 50 etching which is performed by dipping the silicon wafer in a hydrofluoric acid buffer solution. Thus, the portions of the insulating silicon oxide film 63 adjacent the base layer 56 and protected by the overlying photoresist films 68c through 68f and mask patterns 70 and 71 are not etched off. However, other portions of the oxide film 55 63 are etched off. Accordingly, when the silicon wafer is taken out of the hydrofluoric acid buffer solution after completion of the etching step, the surfaces of the base contacts 73 and 74 are exposed.

Then the remaining photoresist films 68c 60 to 68f, the mask patterns 70 and 71 and

underlying prime metal films 67a and 67b are removed by a chemical technique. Thereafter, the wafer is heat-treated to form stable base contacts 73 and 74.

When the base contacts are formed by a vapor phase diffusion process utilizing a BN (boron nitride) plate instead of the ion implantation process, the portion of the insulating silicon oxide film 63 not covered by the remaining photoresist films 68c through 68f and by mask patterns 70 and 71 is removed by such suitable method as chemical etching or sputtering etching to expose a portion of the base layer 56, and an impurity is diffused into the exposed portion by vapor phase diffusion. For example, treatment at 900°C for 10 minutes gives a P^{++} base contact having a thickness of 0.1 micron and having a width in the lateral direction. Of course, the vapor phase diffusion treatment should be made after removing the remaining photoresist films 68c to 68f, mask patterns 70 and 71 and the prime metal film 67.

Fig. 3H shows the silicon wafer under these conditions. As shown, the portions of the silicon wafer other than the base contacts 73 and 74 are covered by silicon oxide films 57a-57c and insulating silicon oxide films 63a and 63b.

Then, the silicon oxide films 63a and 63b overlying the portions 60a of the polycrystalline silicone for forming the emitter electrode and the portion 60b of the polycrystalline silicon for forming the collector terminal are removed by for example exposing a portion to be etched off later through a photoresist film 76 formed by forming a relatively thick photoresist film and then exposing the entire area thereof to light and then removing the exposed portion by a suitable method. This condition is shown in Fig. 3I.

Then, the photoresist film 76 shown in Fig. 3I is removed by etching. After washing the surface with a dilute hydrofluoric acid solution, a wiring metal film 77 is applied over the entire surface of the silicon wafer. The metal film 77 is formed directly on the base contacts 73 and 74 and the 110 upper and side surfaces of the polycrystalline silicon bodies 60a and 60b. In other portion, the metal film 77 is formed on the oxide films 57a to 57c, 63a and 63b.

There is no limit on the type of the 115 wiring metal film 77. A single metal film or a composite metal film may be used so long as it can be plated electrically. In the illustrated example, nickel was deposited to a thickness of 0.1 micron by vapor deposition technique.

Then, the silicon wafer is heat-treated for the purpose of providing ohmic connections to the upper surface P and P' of the portions 60a and 60b of the polycrystalline sili-

con bodies. Then, a relatively thick photoresist film is formed on the surface of the silicon wafer by the same process steps described in connection with Fig. 3D. Then, 5 by the total exposure and the development treatments, the portions of the wiring metal film 77 overlying the polycrystalline silicon bodies 60a and 60b are exposed through the photoresist film 78 thereby forming an 10 emitter electrode 80 and a collector electrode 81 by the plating step similar to that used for preparing the mask patterns 70 and 70' shown in Fig. 3F. This condition is shown in Fig. 3J. As shown, the electrodes 80 and 81 form nail head shape when combined with the polycrystalline silicon bodies 60a and 60b in the same manner as the mask patterns 70 and 71 shown in Fig. 15 3F.

20 Then, the surface of the silicon wafer in the condition shown in Fig. 3J is subjected to uniform exposure and development to preserve remaining photoresist films 78a through 78d beneath the emitter electrode 25 80 and the collector electrode 81. Then, a plating potential is applied to the wiring metal film 77 to plate metal on the wiring metal film 77 and the electrodes 80 and 81 except the portions protected by the remaining 30 photoresist films 78a to 78d, thus forming an emitter conductor metal film 83, a collector conductor metal film 84 base conductor metal films 85, 86 and inner wiring conductor metal film 87 respectively on the emitter electrode 80, collector electrode 81 and wiring metal film 77 under the same conditions described with reference to Fig. 3F and used for preparing the mask patterns. The thickness of the photoresist 35 40 films 78a and 78b underlying the nail head shaped emitter electrode 80 is immaterial to the determination of the relative position between the emitter layer 64 and base contacts 73 and 74 which has been described 45 in connection with Fig. 3G. In other words, the purpose of the remaining photoresist films 78a and 78b is to prevent electrical contact between the emitter conductor metal film 83 on the emitter electrode 50 55 60 65 80, the collector conductor metal film 84 and the base conductor metal films 85 and 86 and to prevent the collector conductor metal film 84 from contacting the base conductor metal films 85 and 86 and the inner wiring conductor metal film 87. As a consequence, the electrodes formed on the polycrystalline silicon bodies 60a and 60b are made of metal so that they have a large current capacity, thus improving the characteristics of the transistor. If desired, these metal films may be formed by vapor deposition technique instead of electroplating.

65 Then, the remaining photoresist films 78a to 78d on the silicon wafer are re-

moved in the condition shown in Fig. 3K, and then the exposed wiring metal film 77 is removed by using Resist Strip J-100 sold by Indust Richen Laboratory Corporation, or hydrochloric acid for dividing the film 77 into sections 77a to 77c. As a consequence, the collector conductor metal film 84, the base conductor metal film 86 and inner wiring conductor metal film 87 which have been interconnected through the metal film 77 will be isolated from each other. This condition is shown in Fig. 3L. Then, a photoresist film 89 made of AZ-1350H and having a thickness sufficient to cover the emitter conductor metal film 83 and the collector conductor metal film 84 is formed and separating photomasks designated by 90a and 90b are superposed on the photoresist mask 89 and the assembly is exposed to light as shown by arrows in Fig. 3M and the portions Sa and Sb of the photoresist film are removed by development. Then, the exposed base conductor metal films 85 and 86 and underlying wiring metal films 77a and 77c are removed with the result that the base conductor metal film 86 is divided into two sections 86a and 86b, the latter serving as the collector conductor metal film. If necessary, the wiring metal film about the collector conductor metal film and two layers of the inner wiring conductor metal film which are not necessary to constitute a transistor are also removed. Fig. 3M shows this condition. The application of the relatively thick photoresist film, exposure and development thereof can be made by the same method as above described. The accuracy of aligning the positions of the silicon wafer and the photomask for exposing unnecessary areas of the conductor metal is not necessary to be accurate. The two layers of the metal at unnecessary area can be removed by aqua regia at a temperature of 40°C.

Then, under the condition shown in Fig. 3M, the thick photoresist films 89a and 89b on the surface of the silicon wafer are removed to complete the transistor of this invention. Fig. 3N is a perspective view, partly in section, of the completed transistor. As shown, since the emitter electrode 80 is covered by the emitter conductor metal film 83, the overall thickness is larger than that of the prior art construction. In the same manner, since the collector electrode 81 is covered by the collector conductor metal film 84, its thickness is larger than that of the prior art. Element 86a is used as the base electrode whereas element 91 as the inner wiring conductor.

Figs. 4A to 4D show successive steps of a modified method of this invention. In this modification, up to Fig. 3B the same process steps are used. After completing the step shown in Fig. 3B, the surface of

the silicon wafer is covered by a thick photoresist film 100 comprising AZ-1350H by using the spinner described above. Then, in the same manner as above described with reference to Fig. 3D, the surface of the silicon wafer is uniformly irradiated with ultraviolet rays and then the photoresist film 100 is developed to remove a portion thereof. Then, the upper surfaces of the polycrystalline silicon bodies 60a and 60b for forming the emitter electrode and the collector terminal respectively will expose through the remaining portion 100a of the photoresist film 100. Then, the portions of the insulating silicon oxide film overlying the polycrystalline silicon bodies 60a and 60b are removed by etching. Fig. 4A shows this condition.

After removing the photoresist film 100a, a prime metal film 101 for plating and comprising nickel or molybdenum is formed on the entire surface of the silicon wafer by vacuum vapor deposition for example to a thickness of about 0.1 micron. Fig. 4B shows this condition.

Then, mask patterns 105 and 106 are formed on the polycrystalline silicon bodies 60a and 60b by the same process steps as shown in Figs. 3F and 3G. More particularly, the entire surface of the silicon wafer is again covered by a photoresist film, and the top surfaces of the polycrystalline silicon bodies 60a and 60b are exposed. Then, mask patterns 105 and 106 are formed on the exposed top surfaces by electroplating. Then, the entire surface of the silicon wafer is irradiated with ultraviolet rays by using the mask patterns 105 and 106 as masks. Then, development and etching are made to remove the plated metal film 101 except the portions 101a and 101b thereof underlying the portions 107a through 107d of the photoresist film and the mask patterns 105 and 106. Fig. 4C shows this condition.

Then, base contacts 108 and 109 are formed by the same process steps as shown in Fig. 3G. More particularly, boron is implanted into the silicon wafer shown in Fig. 4C by using an energy that causes boron to transmit through the insulating silicon oxide film 63 but not through the silicon oxide film 57a which is formed by heat treatment thus forming base contacts 108 and 109. Then, the portions 107a to 107d and the portions 101a and 101b of the prime metal films underlying the mask patterns 105 and 106 are removed and the unnecessary portion of the insulating silicon oxide film 63 is removed. Then, wiring metal films 110a through 110e are formed by vapor deposition, for example. Fig. 4D shows this condition showing that the same construction as that shown in Fig. 3L can be obtained. Although diffusion of the base contact is optional, ion implantation

requires high temperature treatment so that it is advantageous to use such metal as molybdenum which does not diffuse deeply into the polycrystalline silicon bodies 60a and 60b when subjected to high temperature treatment as to form the plating prime metal films 101a and 101b and the mask pattern metal films 105 and 106. Where base contact diffusion is not necessary, any metal can be used for the metal films 101a, 101b, 105 and 106. Subsequent process step is the same as the step shown in Fig. 3M, and finally a transistor shown in Fig. 3N can be obtained.

Comparing with each other the embodiments shown in Fig. 3 and Fig. 6 it will be clear that the latter embodiment requires a smaller number of steps. This is true especially when the base contact diffusion is not necessary.

In the embodiment shown in Fig. 3, since the purpose of the process step shown in Fig. 3M is to remove metals at unnecessary portions, this step may be performed in other step by a well known method. For example, when removing the photoresist in the step shown in Fig. 3I, it is possible to vapour deposit the prime metal film 26 while preserving a thin photoresist layer at a portion where the metal film is to be removed in a later step, then proceed to the step shown in Fig. 3K through the step shown in Fig. 3J and finally remove unnecessary metal film 86 and the wiring prime metal film 77c together with the photoresist film by dipping the silicon wafer in a photoresist removing liquid.

Figs. 5A and 5B show still another embodiment of this invention in which the mask patterns are formed by electrodeless plating.

When the process steps up to Fig. 4A have been performed, metal films are applied onto the polycrystalline silicon bodies 60a and 60b to form mask pattern metal films 120a and 120b on the polycrystalline silicon bodies as shown in Fig. 5A. Thereafter, the entire surface of the silicon wafer is irradiated with ultraviolet rays by using these mask pattern metal films as a mask and the wafer is then developed. Then, the wafer is subjected to a chemical etching to remove the insulating silicon oxide film except the portion thereof covered by the portions 100b to 100e of the photoresist film 63 underlying the mask pattern metal films 120a and 120b. Fig. 5B shows the state at this time.

Subsequent step is the same as that shown in Fig. 4B.

Where a base contact containing an impurity at a high concentration is to be formed by an boron ion implantation process, the implantation energy is adjusted to a low level not to cause the boron ions

to transmit through the oxide film so that the ions are implantation directly into a predetermined depth (for example, 0.05 micron) in the base region. Where, it is desired to efficiently perform the electrodeless plating on the top surface of the polycrystalline silicon bodies 60a and 60b, the etchant resistant patterns 61a and 61b are formed after growing the polycrystalline silicon bodies shown in Fig. 3A and then vapor depositing thin metal films thereon. With these treatments, the electrodeless plating film is applied on to the thin metal film so that the efficiency of the plating can be improved. When the mask pattern metal films are formed by the electrodeless plating described above, it is possible to greatly reduce the number of steps than the steps shown in Figs. 3A through 3M, as well as the steps shown in Figs. 4A through 4D. As the solutoin for the electrodeless plating may be used ATOMEX (trade name) sold by Engechard Co.

Although in the foregoing description, the insulating film was a silicon oxide film, it may be replaced by any insulating film, for example a silicon nitride film.

Furthermore, the mask pattern metal films 70, 81, 105, 106, 120a and 120b were formed in the presence of a photoresist layer (for example 68b shown in Fig. 3F) the presence of the photoresist layer is not essential to form the mask pattern metal films. However when the mask pattern metal films are formed in the absence of the photoresist layer the portions of the metal films projecting beyond the polycrystalline silicon body will not be horizontal but directed slightly toward lower. However, since it is only necessary that the mask pattern metal film should project laterally from the lower end of the polycrystalline silicon body and that the metal film should not contact the base electrode formed on the semiconductor substrate, the photoresist layer may be provided if desired when forming the mask pattern metal film.

In this manner, it is possible to manufacture a transistor similar to that prepared by the process steps shown in Figs. 3A to 3N without using a photoresist layer such as 68b shown in Fig. 3F. More particularly a polycrystalline silicon semiconductor layer 60 as shown in Fig. 3A is prepared, a metal layer is formed on the polycrystalline silicon bodies 60a and 60b are formed by using etchant resistant patterns 61a and 61b as shown in Fig. 3A. At this time, since the top surfaces of the polycrystalline silicon bodies are covered by the metal films, no oxide film is formed but the surface of the metal films on the polycrystalline silicon bodies are etched to remove the oxidized portion. At this time, since

the other portions are covered by the oxide film formed by heat treatment, they will not be eroded by the etchant for the metal films. Then a mask pattern metal film is formed on said metal film by electrodeless plating and an impurity is diffused into the base contact by the ion implantation process. When the thickness of silicon oxide film 57 is made larger than that of the silicon oxide film 63, it is possible to control the implantation energy such that, at the portion where the oxide film 57 presents, impurity ions will not implant into the semiconductor substrate but reach only to the surface of the oxide film 57. With this method of ion implantation, it is possible to diffuse the impurity ions into the portion of the semiconductor substrate which underlies the mask pattern metal film and where the silicon oxide film 57 formed by heat treatment does not present. When an ion implanted oxide film is compared with an oxide film not implanted with impurity ions the etching speed of the former is several times larger. By using this characteristic, it becomes possible to selectively etch off the insulating silicon oxide film 63 except its portion underlying the mask pattern metal film. Accordingly, it is possible to obtain a transistor having a construction as shown in Fig. 3N by vapor depositing the base electrode and by using the process step shown in Fig. 3M.

A method of forming resistors and inner wirings when the invention is applied to the manufacture of a high density LSI will now be described. Fig. 6A shows the first step of the method of manufacturing the resistors and the inner wirings, in which reference numeral 200 shows a silicon wafer, 201 a silicon oxide film formed by heat treatment and overlying the wafer 200, 202 a polycrystalline silicon layer formed on the silicon oxide film 201 and 203 an etchant resistant pattern. The material and construction of these elements are the same as those of the transistor described above.

The silicon wafer shown in Fig. 6A is subjected to the steps shown in Figs. 3B to 3G to obtain a construction shown in Fig. 6B. For the purpose of forming a resistor with the polycrystalline silicon layer 202 in contact with the silicon oxide film 201 on the silicon wafer 200, a polycrystalline silicon body 202a is shaped as a frustum and on the surface of the polycrystalline silicon body 202a are formed an insulating silicon oxide film 205, a plating prime metal film 206 and a mask pattern metal film 207, and portions 208a and 208b of the metal film 206 underlying the mask pattern metal film 206 and not protected by a photoresist are removed by etching.

The construction shown in Fig. 6C is obtained by subjecting the wafer shown in

Fig. 6B to the steps shown in Figs. 3H to 3L. Briefly stated, the portions of the silicon oxide film 205 underlying the mask pattern metal film 207 and not protected by the photoresist film are removed by etching. Thereafter, the mask pattern metal film 207, the photoresist film and the plating prime metal film 206 underlying the mask pattern metal film 207 are removed and the silicon oxide film on the top Q of the polycrystalline silicon body 202a in the form of frustum is also removed thus preserving the portions 205a and 205b of the silicon oxide film on the side surfaces of the frustum. Then, a wiring metal film 210 (not shown) is formed on the wall surface of the silicon wafer and a relatively thick photoresist film 211 is coated such that the top Q of the polycrystalline silicon body 202a is exposed. Then, a resistor electrode 212 is electroplated on the exposed top Q by using the wiring film and inner wiring metal films 213a and 213b are vapor deposited by using the electrode 212 as a mask. At the same time, a resistor metal film 213c is also formed on the electrode 212.

Then the inner wiring metal films 213a and 213b, and the inner wiring metal films 210a and 210b not covered by the resistor metal film 213c are removed and these portions are covered by a thick photoresist film. An area of the photoresist film having a width L_1 and a length L_2 on the resistor metal is exposed to light and then developed, this exposing the resistor metal film 213c in that area. Then the resistor metal film 213c in this area, the resistor electrode 212 and the wiring metal film 210 are etched off to expose the top Q' of the frustum shaped polycrystalline silicon body 202a as shown in Fig. 6D (remaining portion of the photoresist film is not shown). The frustum shaped polycrystalline silicon body 202a is used as a resistor and the resistor metal films 213c constitute the terminals of this resistor.

Further, portions 213a and 213b are used as the inner wiring conductors when the wafer is used as an integrated circuit.

In the foregoing description, the steps of manufacturing a transistor and inner wirings were described with reference to Figs. 3A to 3N, Figs. 4A to 4D and Figs. 5A and 5B while the steps of manufacturing a resistor and inner wirings were described with reference to Figs. 6A to 6D. To form an integrated circuit including a resistor and inner wirings on the same wafer, the resistor and the inner wirings are formed by the steps shown in Fig. 6c, and the transistor by the steps shown in Figs. 3M and 3N. Accordingly, an integrated circuit will be completed by forming an insulating film having a thickness of about one micron

on the silicon wafer, forming perforations through the insulating film which are necessary to make connections necessary to form a desired circuit and by forming wirings with a metal film.

Although not described, it will be clear that a transistor, a resistor and inner wirings can also be formed by the methods shown in Figs. 4A to 4D and Figs. 5A and 5B.

Fig. 7 is a sectional view showing the invention as applied to n channel type MOS transistor. The MOS transistor comprises a P type silicon wafer 250 having a resistivity of 0.5 to 1 ohm-cm a silicon oxide film 251 prepared by heating, a gate polycrystalline silicon body 252, a gate electrode 254, a source electrode 255, a drain electrode 256, a P type impurity diffused layer 258 containing a P type impurity, for example boron at a low density ($1 \times 10^{17}/\text{cm}^3$), a gate silicon oxide film 259 having a thickness of about 0.1 micron and formed on the diffused layer 258, and source and drain electrodes 260 and 261 formed by heat-diffusing or implanting into the P type silicon wafer 250, such n type impurity as arsenic or phosphor. Such MOS transistor can readily be formed by the steps shown in Figs. 3A to 3M and respective electrodes can be insulated from each other by micro-gaps formed by self-aligning.

The embodiment described above relates to an integrated circuit including a n-p-n type transistor, a MOS transistor and their method of manufacturing. It will be clear that the invention is also applicable to p-n-p type transistor as well as various diodes and that the semiconductor material is not limited to silicon, and germanium and intermetallic compounds, for example antimony-arsenide, and gallium-arsenide, can also be used.

The method of this invention for manufacturing a semiconductor device having a step shaped (nail head shaped) electrode is characterized by an improved yield. More particularly, in the prior art semiconductor device, the sectional configuration of the polycrystalline silicon body is limited to inverted frustum whereas the sectional configuration of the polycrystalline silicon body of this invention is irregular as shown in Figs. 8A, 8B and 8C. Even with these irregular configurations, it is sufficient that the base of the polycrystalline silicon body be included in the vertical projection S_0 of the mask pattern A on a substrate (that is silicon wafer) with a margin S_1 . This feature is more advantageous than the prior art stepped electrode construction wherein the polycrystalline silicon body is worked to have an inverted frustum shape by varying the etching speed by adjusting the amount of impurity contained in the polycrystalline

silicon body and the diffusion of the impurity by heat treatment.

By the process steps described above a n-p-n type transistor for use in ultra high frequencies and an integrated circuit utilizing the same can be manufactured. When the pattern of a ultra high frequency transistor of this invention is designed, by setting the minimum dimension at 2 microns, the external base resistance was decreased to $\frac{1}{2}$ of that of a transistor of a conventional planar construction and the capacitance of the collector-base junction immediately beneath the external base was reduced to $\frac{1}{2}$ of that of the prior art construction showing great improvement of the high frequency characteristics. Although the maximum oscillation frequency of the prior art construction is 7.3GH_z, that of the novel transistor having the same emitter area increases to 13.3 GH_z.

As above described, according to this invention it is possible to eliminate regions not necessary to the operation of a prior art transistor and to improve the high frequency characteristics.

Furthermore, according to the method of this invention, it is possible to simplify the photomask pattern utilized to form electrodes and to eliminate the photomask pattern for forming the base contact window. Consequently, these steps which require extremely accurate positioning in the prior art construction are simplified, thus rendering easy manufacture.

Further, according to the method of this invention it is possible to readily form electrodes having a large current capacity and arranged at a high density. The thickness of the metal films utilized for forming emitter and collector electrodes, resistors and electrode wirings can be made to be twice or more of the prior art construction.

The invention is further characterized in that the deviation in the characteristics of the semiconductor devices manufactured by the method of this invention is small. Even when there are some pitch or dimensional errors in the device pattern which is formed on the photomask at the first step, the relative spacing between the emitter and base contacts which has an influence upon the characteristics of the resulting semiconductor device is definite and would not vary depending upon the sectional configuration of the polycrystalline silicon body as in the prior art construction so that it is possible to obtain semiconductor devices having identical characteristics at high yields.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising a semiconductor substrate, a polycrystalline silicon semiconductor body containing an impurity at a substantially uniform con-

centration and extending upwardly from a portion of the surface of the semiconductor substrate, and a metal electrode formed on the top surface of the polycrystalline silicon semiconductor body by a plating technique and extending in the lateral direction beyond the periphery of the top surface of said polycrystalline silicon semiconductor body. 70

2. A semiconductor device according to claim 1, including an electrically insulating film which covers the side surfaces of said polycrystalline silicon body and extends from the base thereof in the lateral direction. 75

3. A semiconductor device according to claim 2, including a plurality of diffused regions which, together with said metal electrode, constitute a transistor. 80

4. A semiconductor device according to claim 2, including an additional metal electrode spaced from said first mentioned metal electrode, and the portion of said polycrystalline silicon body between said two metal electrodes serves as a resistor. 85

5. A semiconductor device according to claim 3, wherein said transistor comprises a MOS transistor. 90

6. A method of manufacturing a semiconductor device comprising forming a polycrystalline silicon semiconductor body on a portion of a surface of a semiconductor substrate, and then forming a metal electrode by a plating technique on the top surface of said polycrystalline silicon body to extend in the lateral direction beyond the periphery of the top surface of said polycrystalline silicon body. 95

7. A method according to claim 6, including the steps of forming a plurality of diffused regions in said semiconductor substrate by using a first electrically insulating film on said substrate as a mask, forming a polycrystalline silicon semiconductor layer having a substantially uniform impurity concentration on said diffused regions and on said first insulating film, and forming said polycrystalline silicon semiconductor body by preserving a portion of said layer on a said diffused region, and said metal electrode is formed by the steps of forming a second electrically insulating film on the entire upper surface of said substrate, applying a first photoresist film upon said second insulating film, exposing the top surface of said body, forming a first prime metal film over the entire surface of said substrate, forming a second photoresist film on said first prime metal film, exposing the top surface of said body, forming a metal mask pattern on the top surface of said body by applying a voltage to said first prime metal film such that said metal mask pattern extends in the lateral direction beyond the periphery of said top surface, removing said second photoresist film and said 130

first prime metal film by using said metal mask pattern as a mask, forming a contact region in the other diffused region adjacent said one diffused region by using said 5 metal mask pattern as a mask, removing said metal mask pattern, said photoresist film and said first prime metal film, applying a third photoresist film over the entire surface of said substrate, exposing the top 10 surface of said body, removing said third photoresist film, forming a second prime metal film over the entire surface of said substrate, forming a fourth photoresist film on said second prime metal film, exposing the second prime metal film on the top 15 surface of said body, and forming said metal electrode on the exposed second prime metal film by applying a voltage thereto such that the metal electrode extends in the lateral direction from the periphery of the top 20 surface of said body, and said method further comprising the steps of removing said third photoresist film by utilizing said metal electrode as a mask, applying a conductor metal film on said metal electrode and said second prime metal film by applying a voltage on said second prime metal film, and removing remaining third photoresist film, unwanted conductor metal film 25 and said second prime metal film.

8. A method according to claim 7, wherein the last mentioned step comprises the steps of removing the remaining third photoresist film and the second prime metal film underlying the same, forming a fourth photoresist film on the entire surface of said substrate, removing the portion of the photoresist film corresponding to unwanted conductor metal and the second prime metal film, then removing said unwanted conductor metal film and said second prime metal film and finally completely removing said 30 fourth photoresist film.

9. A method according to claim 6 or 45 claim 7, wherein said metal electrode is formed by the steps of forming a second insulating film on the entire upper surface of said semiconductor substrate, forming a first photoresist film on said second insulating film, exposing the top surface of said body, removing said first photoresist film, forming a first prime metal film over the entire surface of said substrate, exposing the top surface of said first prime metal film, forming a second prime metal film over the entire surface of said substrate, forming a second photoresist film on said second prime metal film, and forming said metal electrode on the top surface of said body by applying a voltage to said second prime metal film such that said metal electrode extends in the lateral direction beyond the periphery of said top surface, and said method further comprising the steps of removing said second photoresist film by 50 using said metal electrode as a mask, forming a conductor metal film on said metal electrode and said second prime metal film by applying a voltage thereto, and removing second photoresist film, unwanted conductor metal film, and the second prime metal film.

10. A method according to claim 6 or 55 claim 7, wherein said metal electrode is formed by the steps of forming a second insulating film on the entire upper surface of said substrate, forming a first photoresist film on said second insulating film, exposing the top surface of said body, forming by electrodeless plating said metal electrode on the exposed top surface of said body such that said metal electrode extends in the lateral direction beyond the periphery of said top surface, and said method further comprising the steps of removing said first photoresist film by using said metal electrode as a mask, forming a contact region in the other diffused region adjacent said one diffused region by using said metal electrode as a mask, forming a second photoresist film on the entire surface of said substrate, and removing a predetermined portion of said second photoresist film to form wiring conductors.

11. A method according to claim 6 or 60 claim 7, wherein said metal electrode is formed by the steps of forming a second insulating film on the entire upper surface of said substrate, forming a first photoresist film on said second insulating film, exposing the top surface of said body, forming a metal film over the entire surface of said substrate, forming a mask on a predetermined portion of said metal film, and forming said metal electrode by electrodeless plating on the top surface of said body such that said metal electrode extends in the lateral direction beyond the periphery of the top surface of said body, and said method further comprising the steps of removing said first photoresist film, forming a contact region in the other diffused region adjacent said one diffused region by using said metal electrode as a mask, forming a second photoresist film over the entire surface of said substrate, and removing a predetermined portion of said photoresist film for forming wiring conductors.

12. A method as claimed in claim 6 or 65 claim 7, wherein said metal electrode is formed by the steps of forming a second insulating film on the entire upper surface of said substrate, forming a first photoresist film on said second insulating film, exposing the upper surface of said body, forming a first prime metal film over the entire surface of said substrate, forming a second photoresist film on said first prime metal film, exposing the top surface of said body, and forming said metal electrode on the top

surface of said body by applying a voltage to said first prime metal film such that said metal electrode extends in the lateral direction beyond the periphery of said top surface, and said method further comprising the steps of removing said second photoresist film, applying a conductor metal on said metal electrode and on a predetermined portion of said substrate and removing an intermediate portion of said metal electrode, and said conductor metal for exposing said body.

13. A method as claimed in claim 6 wherein a polycrystalline silicon semiconductor layer is formed on a semiconductor substrate, a metal layer is formed on a predetermined portion of the polycrystalline layer, a polycrystalline silicon semiconductor body is formed by selectively etching the polycrystalline layer, an insulating layer is formed over the entire surface of the substrate, an oxide on the surface of the metal layer on the body is removed, a metal mask pattern is formed by electrodeless plating on the top surface of the body such that the metal mask pattern extends in the lateral direction beyond the periphery of the top surface, an impurity is diffused into the body by using the metal mask pattern as a mask, and an unwanted portion of the insulating film is selectively removed.

14. A method of manufacturing a MOS transistor wherein diffused source and collector regions are formed on a semiconductor substrate, a gate oxide film is formed on the portion of the substrate between the diffused regions, a polycrystalline silicon semiconductor layer is formed on the entire surface of the substrate, the polycrystalline layer is selectively removed to form a polycrystalline silicon semiconductor body on the gate oxide film, an insulating film is formed over the entire surface of the substrate, a first photoresist film is formed on the insulating film, the top surface of said body is exposed, a first prime metal film is formed over the entire surface of the substrate, said first photoresist film is again formed on the first prime metal film, the top surface of said body is exposed, a metal mask pattern is formed on the top surface of said body by applying a voltage to the first prime metal film such that the metal mask pattern extends in the lateral direction beyond the periphery of said top surface, the first photoresist film and the first prime metal film are removed by using the metal mask pattern as a mask, a contact region is formed in the diffused source and drain regions by using the metal mask pattern as a mask, the metal mask pattern is removed, the first photoresist film and the first prime metal film are removed by using the metal mask pattern as a mask, a second photoresist film is formed over the entire surface of the substrate, the top surface of said body is exposed, the second photoresist film is removed, a second prime metal film is formed over the entire surface of the substrate, a third photoresist film is formed on the third photoresist film, the second prime metal film overlying the top surface of said body is exposed, a metal electrode is formed on the exposed second prime metal film by applying a voltage thereto such that the metal electrode extends in the lateral direction beyond the periphery of the top surface of said body, the second photoresist film is removed by using the metal electrode as a mask, a conductor metal film is applied on the metal electrode and the second prime metal film by applying a voltage to the second prime metal film, and the remaining portion of the second photoresist film, unwanted portions of the conductor metal film and the second prime metal film are removed.

15. A method of manufacturing a semiconductor device substantially as described herein with reference to Figs. 3A to 3N, or Figs. 4A to 4D, or Figs. 5A and 5B, or Figs. 6A to 6D, of the accompanying drawings.

16. A semiconductor device when manufactured by a method as claimed in any one of claims 6 to 15.

17. A semiconductor device substantially as described herein with reference to Fig. 2, or Fig. 3N, or Fig. 4D, or Fig. 5B, or Fig. 6D, or Fig. 7, of the accompanying drawings.

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FIG. 1A PRIOR ART

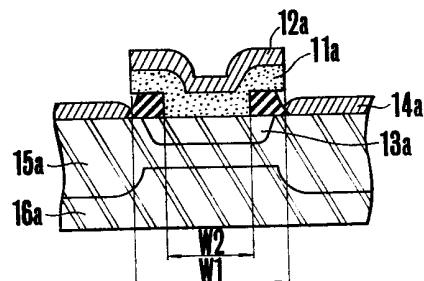


FIG. 1B PRIOR ART

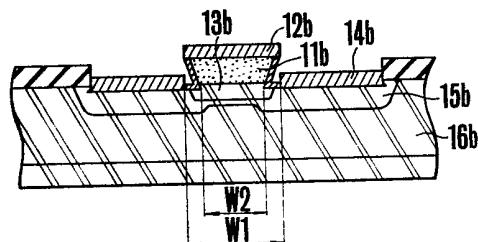


FIG. 2

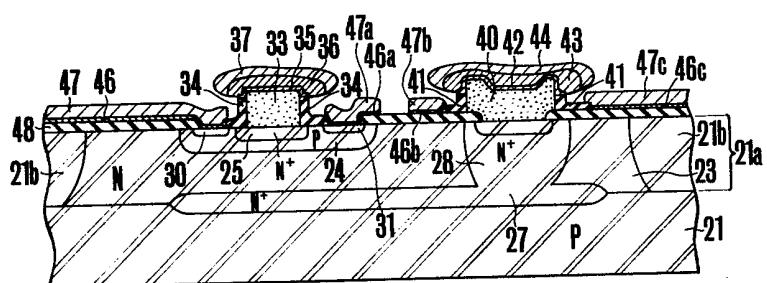


FIG.3A

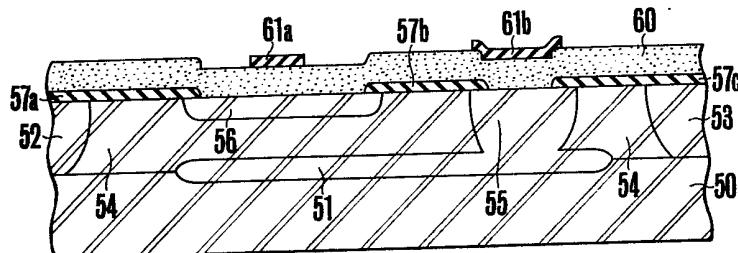


FIG.3B

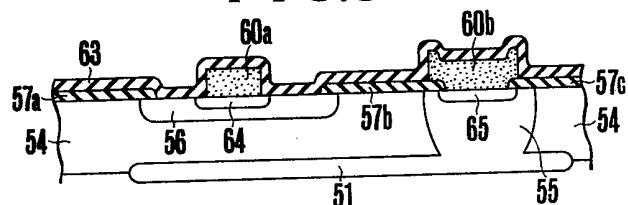


FIG.3C

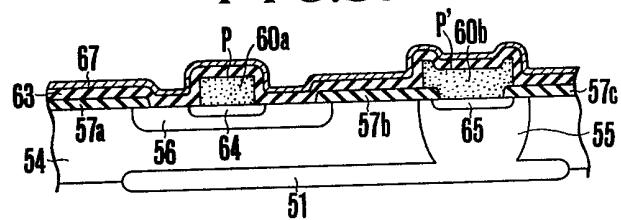


FIG.3D

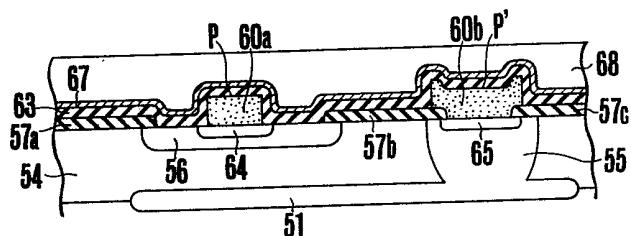


FIG.3E

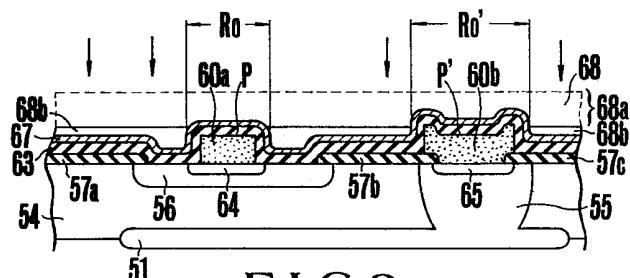


FIG.3F

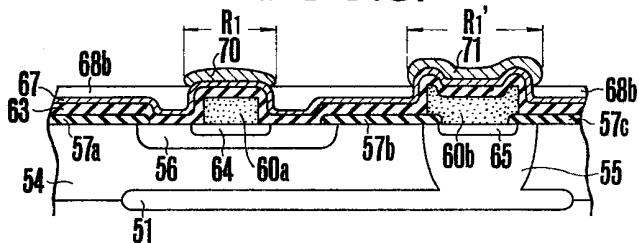


FIG.3G

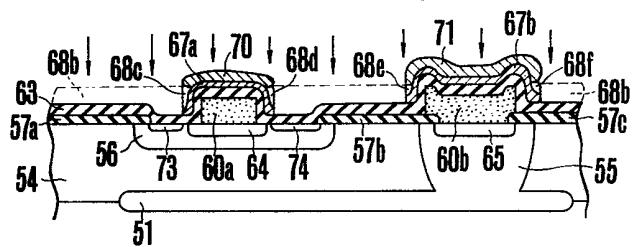


FIG.3H

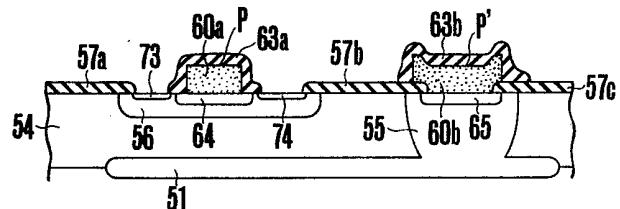


FIG.3I

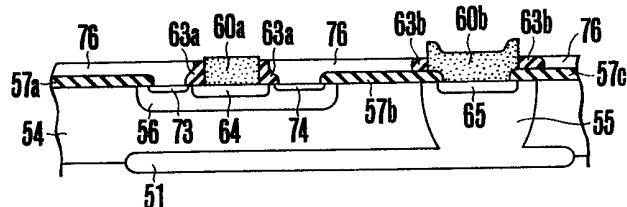


FIG.3J

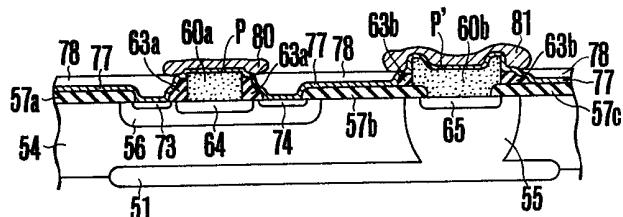


FIG.3K

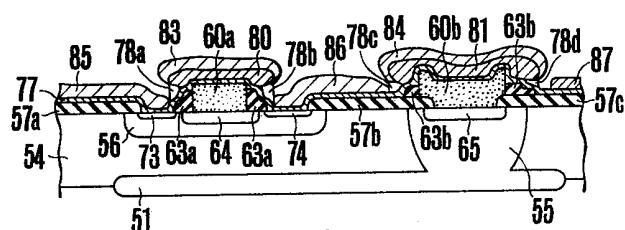


FIG.3L

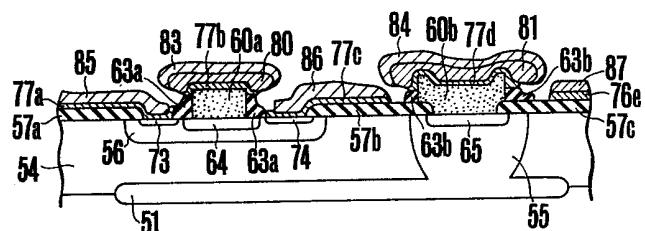


FIG. 3M

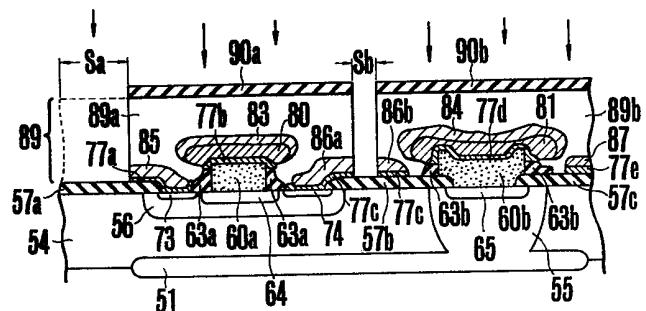
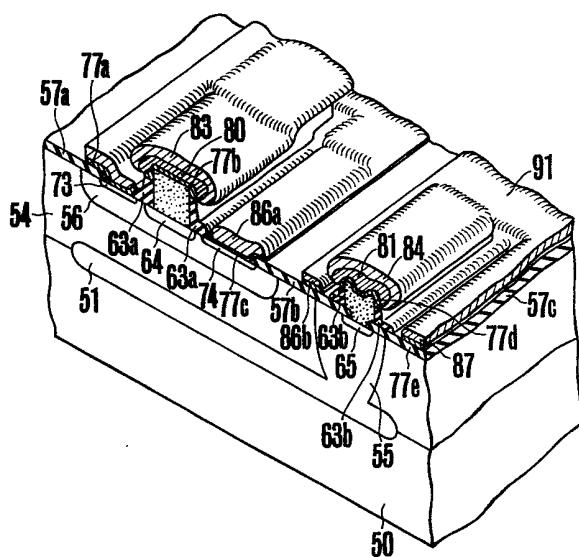
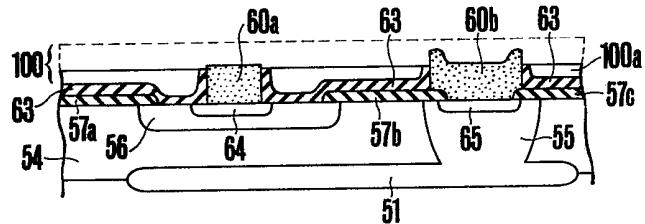


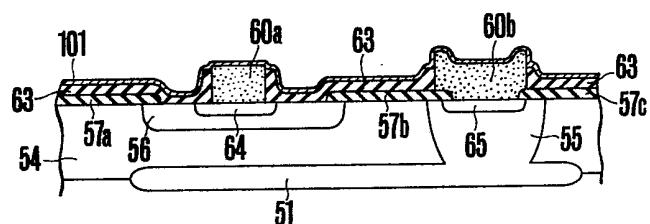
FIG. 3N



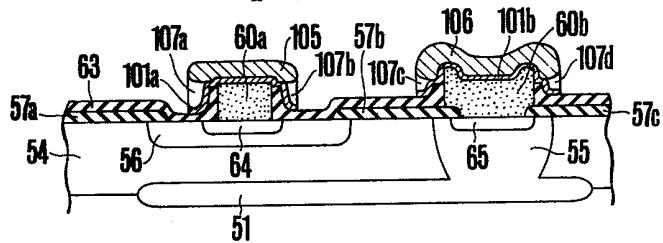
F I G.4 A



F I G.4 B



F I G.4 C



F I G.4 D

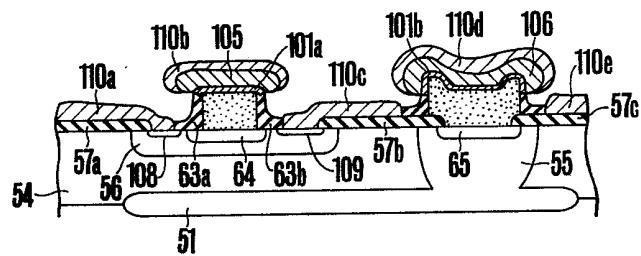


FIG.5A

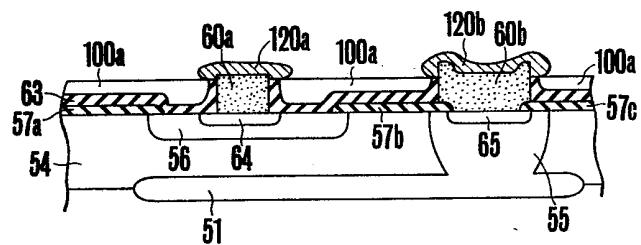


FIG.5B

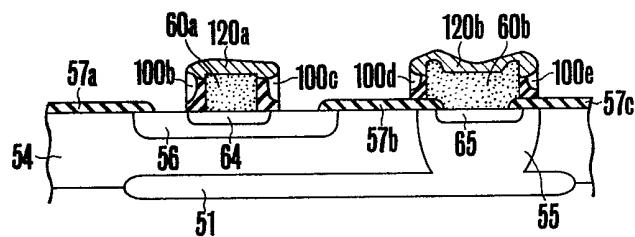


FIG.6A

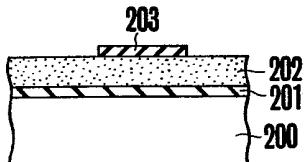


FIG.6B

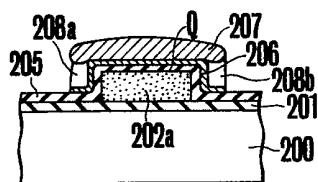


FIG.6C

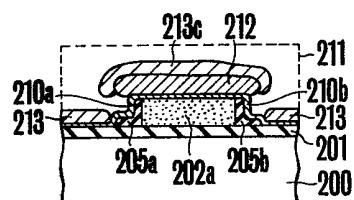


FIG.6D

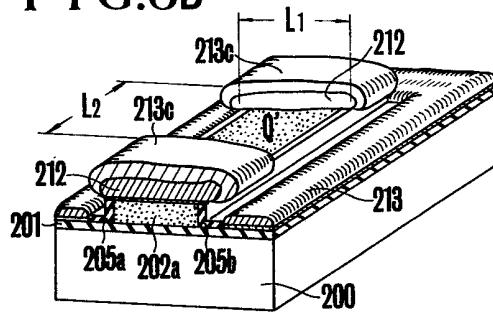


FIG.7

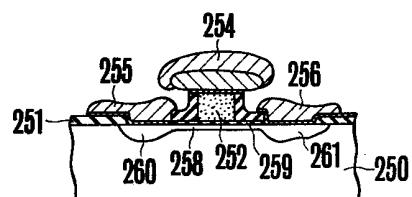


FIG.8A

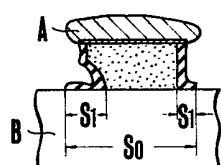


FIG.8B

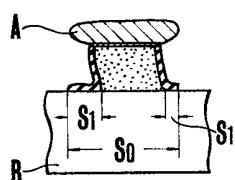


FIG.8C

