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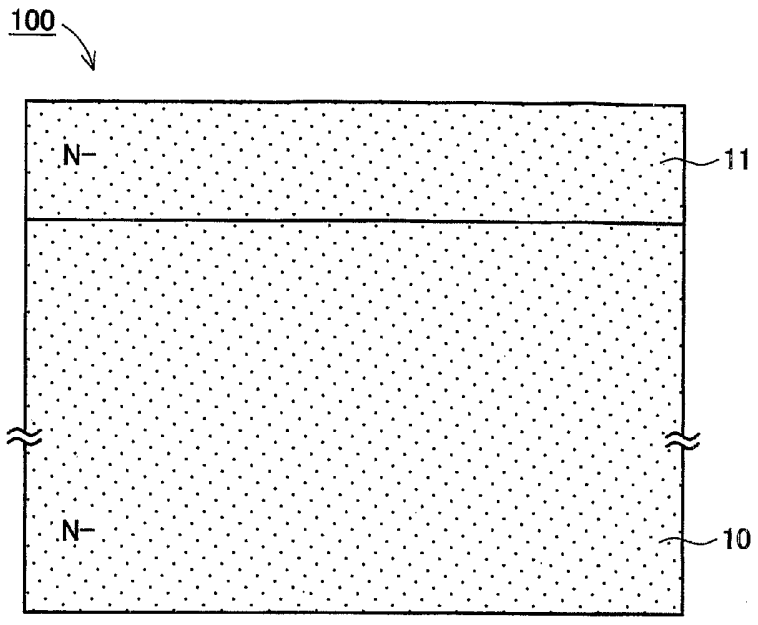
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[Continued on next page]

(54) Title: SEMICONDUCTOR SUBSTRATE AND SEMICONDUCTOR DEVICE, AND MANUFACTURING METHODS THEREOF



(57) Abstract: An object is to provide a semiconductor substrate having a large diameter, high mechanical strength and less crystal defects; and a semiconductor device making use of the semiconductor substrate; and manufacturing methods of them. The semiconductor substrate 100 has an N^- type silicon substrate 10 formed by the MCZ method and an N^- type epitaxial layer 11 formed over the silicon substrate 10 by the epitaxial growth. The silicon substrate 10 has a dopant concentration within a range of from 1.0×10^{13} atoms/cm^3 to 1.0×10^{15} atoms/cm^3. The oxygen concentration in the silicon substrate 10 is 8.0×10^{17} atoms/cm^3 or less.

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DESCRIPTION

SEMICONDUCTOR SUBSTRATE AND SEMICONDUCTOR DEVICE, AND MANUFACTURING METHODS THEREOF

TECHNICAL FIELD

The present invention relates to a semiconductor substrate to be used mainly as a high breakdown voltage semiconductor element and a semiconductor device making use of the semiconductor substrate, and manufacturing methods of them. More specifically, the present invention pertains to a semiconductor substrate having a large diameter but less crystal defects and a semiconductor device making use of the semiconductor substrate, and manufacturing methods of them.

BACKGROUND ART

Wafers manufactured by the MCZ method (magnetic field applied Czochralski method) or the FZ method (floating zone method) have conventionally been employed as wafers for high voltage semiconductor elements such as NPT (non punch-through) type or FS (field stop) type IGBT (insulated gate bipolar transistor). Hereinafter, a wafer manufactured by the MCZ method will be called "MCZ wafer", while that manufactured by the FZ method will be called "FZ wafer".

It is usually necessary to take the following problems into consideration upon use of MCZ wafers. MCZ wafers contain therein interstitial oxygen as an impurity. This interstitial oxygen sometimes becomes an oxygen donor by the thermal process of from 300 to 600°C during the manufacturing process of a high breakdown voltage semiconductor element. To obtain wafers having high resistance, the oxygen concentration in the wafers is preferably low. It is, on the other

hand, known that the lower the concentration of interstitial oxygen, the lower the mechanical strength of the wafers. In short, there exists a trade-off relationship in the wafers between increase of resistance and improvement in mechanical strength.

On the contrary, FZ wafers have an oxygen concentration as low as 1.0×10^{16} atoms/cm^3 or less. Their resistance can therefore be heightened readily, which enables the wide use of them for power devices. They however involve the drawback that cracks or slips tend to occur because of low mechanical strength.

There has been a demand for wafers having a larger diameter upon manufacture of semiconductor elements. In recent years, MCZ wafers usually have a diameter of 12 inches, while FZ wafers have a diameter less than 8 inches. This diameter difference results from their manufacturing methods. Described specifically, in the case of FZ wafers, single crystal silicon is supported at the neck portion thereof so that a drastic increase in its weight easily breaks the neck portion. Another cause is difficulty in the conversion of polycrystalline silicon into uniform single crystal one. Accordingly, it is difficult to increase the diameter of FZ wafers.

As a measure for satisfying the above-described demand, improvement of mechanical strength and increase in the wafer diameter using MCZ wafers are considered. MCZ wafers however contain crystal defects such as oxygen precipitation owing to high oxygen concentration. In addition, the resistivity of the wafers themselves varies because the interstitial oxygen becomes a donor and contributes as a dopant. Variations in resistivity, lowering in the breakdown voltage of an oxide film and deterioration in life time may presumably occur when a semiconductor element is formed on an MCZ wafer. According to the manufacturing method of a semiconductor silicon substrate as disclosed in Patent

Document 1, a low-defect layer is formed by epitaxial growth on an MCZ wafer having a high oxygen concentration. This document says that a wafer with less crystal defects in an element region can be manufactured by this method.

[Patent Document 1] Japanese unexamined patent application publication No. 2003-286094

When an epitaxial layer is formed on an MCZ wafer having a high oxygen concentration, as the semiconductor substrate disclosed in Patent Document 1, problems as described below may occur. FIG. 14 illustrates the concentration distribution of oxygen before and after thermal process. In FIG. 14, the oxygen concentration (unit: atoms/cm^3) in an MCZ wafer is plotted on the ordinate, while the depth (unit: μm) from the surface of a semiconductor substrate is plotted on the abscissa. The thickness of the epitaxial layer formed over the MCZ wafer is 10 μm. As illustrated in FIG. 14, almost no oxygen exists in the epitaxial layer before thermal process. In the MCZ wafer, however, a region of a high oxygen concentration spreads uniformly. After thermal process, however, oxygen in the MCZ wafer diffuses in the epitaxial layer. This means the diffusion of interstitial oxygen in the element region by the thermal process. Even when defects contained in the epitaxial layer just after formation are not so much, crystal defects appear by the thermal process. Specific problems which may presumably occur include variations in the resistivity due to incorporation of oxygen as a donor, deterioration in life time due to oxygen precipitation and lowering in the breakdown voltage of an oxide film.

Even when the epitaxial layer stays as a low-defect region after thermal process, when a semiconductor element formed on this semiconductor substrate is a vertical type one, that is, a semiconductor element (for example, a trench-gate IBGT as illustrated in FIG. 9) having a

current path disposed also in the MCZ wafer, variations in resistivity due to oxygen donor or oxygen precipitation occur. There is therefore a fear of electrical properties becoming unstable owing to a high oxygen concentration of the MCZ wafer.

The present invention has been made in order to overcome the problems that the conventional wafer involves. An object of the present invention is therefore to provide a semiconductor substrate having a large diameter, high mechanical strength and less crystal defects and a semiconductor device utilizing the semiconductor substrate, and manufacturing methods of them.

DISCLOSURE OF THE INVENTION

The semiconductor substrate developed for attaining the above-described object comprises a semiconductor wafer substrate manufactured by the MCZ method and having an oxygen concentration of 8.0×10^{17} atoms/cm^3 or less and an epitaxial layer existing on the semiconductor wafer substrate and formed by the epitaxial growth.

Since the semiconductor substrate in the present invention is a semiconductor wafer substrate made by the MCZ method, the diameter of the wafer can be easily enlarged compared with that of an FZ wafer. In addition, the semiconductor wafer substrate has an oxygen concentration as low as 8.0×10^{17} atoms/cm^3 or less. Thus the oxygen amount diffused in the epitaxial layer formed over the semiconductor substrate is remarkably small. The epitaxial layer therefore maintains its low-defect condition, making it possible to stabilize the electrical properties. There is a fear of a wafer having a lowered mechanical strength when it has a low oxygen concentration. It has however been found by the test that lowering in the mechanical strength of a wafer does not occur at an oxygen

concentration exceeding 2.0×10^{17} atoms/cm^3. The details of the test on the mechanical strength will be described later. In addition, the MCZ wafer has higher mechanical strength than an FZ wafer because its oxygen concentration is higher than that of the FZ wafer (usually, 1.0×10^{16} atoms/cm^3 or less).

The present invention also embraces a semiconductor device which has a current flow controlled by the application of voltage to a gate electrode; and comprises a semiconductor wafer substrate manufactured by the MCZ method and having an oxygen concentration of 8.0×10^{17} atoms/cm^3 or less and an epitaxial layer existing on the semiconductor wafer substrate and formed by the epitaxial growth, the epitaxial layer having a channel region formed therein. By using a semiconductor wafer having a low oxygen concentration, the epitaxial layer does not lose its low defect state even by the thermal process during the manufacturing process. The semiconductor device of the present invention therefore has good electrical properties. In particular, the semiconductor wafer having a low oxygen concentration is effective for a semiconductor device whose epitaxial layer has a channel region formed therein.

It is especially effective when a semiconductor wafer substrate of the semiconductor device of the present invention has a current path through which electric current flows by the application of a voltage to a gate electrode. This means that owing to a low oxygen concentration of a semiconductor wafer substrate itself, an oxygen precipitation amount in the semiconductor wafer substrate is small. In addition, an oxygen donor amount can be reduced. Variations in the resistivity are therefore small. It is therefore possible to stabilize the electrical properties of a vertical type semiconductor element having a semiconductor wafer substrate provided with a current path.

The manufacturing method of the semiconductor substrate according to the present invention comprises a semiconductor wafer forming step of growing a silicon single crystal rod by the MCZ method and processing the resulting silicon single crystal rod into a semiconductor wafer, and an epitaxial growth step of forming an epitaxial layer, by the epitaxial growth, on the semiconductor wafer thus formed by the semiconductor wafer forming step. The silicon single crystal rod formed by the semiconductor wafer forming step has an oxygen concentration of 8.0×10^{17} atoms/cm^3 or less.

According to the manufacturing method of the semiconductor substrate of the present invention, an MCZ wafer is formed in the semiconductor wafer forming step. Upon formation, strength of a magnetic field, rotation speed of a crucible shaft, rotation speed or pulling up rate of a silicon single crystal rod are adjusted so that the resulting MCZ wafer has an oxygen concentration of 8.0×10^{17} atoms/cm^3 or less. In the epitaxial growth step, an epitaxial layer is then formed on the semiconductor wafer. By forming the epitaxial layer on the MCZ wafer having a low oxygen concentration, diffusion of oxygen into the epitaxial layer is suppressed. By this, the epitaxial layer is able to maintain a low defect state. Even when a semiconductor having, in the epitaxial layer thereof, a channel region, the element has good electrical properties.

It is recommended to adjust the silicon single crystal rod to have a desired dopant concentration by forming a silicon single crystal rod without adding thereto a dopant impurity and then subjecting the resulting silicon single crystal rod to NTD treatment. In short, an N type semiconductor having reduced variations in phosphor concentration can be manufactured by subjecting the wafer to NTD treatment. The semiconductor substrate subjected to NTD treatment can therefore be

produced in a high yield.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 is a cross-sectional view illustrating a semiconductor substrate according to a first embodiment;

FIG. 2 illustrates one example of a single crystal growing apparatus for manufacturing a silicon single crystal rod;

FIG. 3 is a graph showing the oxygen concentration distribution of the semiconductor substrate of the first embodiment before and after thermal process;

FIG. 4 is a graph showing the relationship between the oxygen donor concentration and wafer oxygen concentration of the MCZ wafer according to the first embodiment;

FIG. 5 illustrates an image of the three-point bending method for evaluating the strength of a wafer;

FIG. 6 is a graph showing a breaking load of the MCZ wafer according to the first embodiment at each oxygen concentration;

FIG. 7 illustrates a simulation model of a sample IGBT;

FIG. 8 is a graph showing the relationship of electrical properties of IGBT in the MCZ wafer as a simulation model;

FIG. 9 is a cross-sectional view of IGBT making use of the semiconductor substrate according to the first embodiment;

FIG. 10 is a cross-sectional view illustrating a semiconductor substrate according to a second embodiment;

FIG. 11 is a cross-sectional view illustrating CMOS making use of the semiconductor substrate according to the second embodiment;

FIG. 12 is a cross-sectional view illustrating a semiconductor substrate according to a third embodiment;

FIG. 13 is a cross-sectional view illustrating IGBT making use of the semiconductor substrate according to the third embodiment; and

FIG. 14 is a graph illustrating an oxygen concentration distribution of the conventional semiconductor substrate before and after thermal process.

BEST MODE FOR CARRYING OUT THE INVENTION

Embodiments of the present invention will next be described in detail referring to accompanying drawings. In these embodiments, the present invention is applied to a wafer utilized for NPT type or FS type IGBT.

[First Embodiment]

A semiconductor substrate 100 according to a first embodiment has, as illustrated in FIG. 1, an N^- type silicon substrate 10 formed by the MCZ method and an N^- type epitaxial layer 11 formed over the silicon substrate 10 by the epitaxial growth. The silicon substrate 10 has a dopant concentration within a range of from 1.0×10^{13} atoms/cm^3 to 1.0×10^{15} atoms/cm^3. This dopant concentration falls within a range of from 5 Ωcm to 500 Ωcm in terms of resistivity. The oxygen concentration in the silicon substrate 10 is 8.0×10^{17} atoms/cm^3 or less. The thickness of the epitaxial layer 11 is about 10 μm.

The manufacturing method of the semiconductor substrate 100 as illustrated in FIG. 1 will next be described. First, a silicon single crystal rod having an oxygen concentration, when formed into a wafer, of 8.0×10^{17} atoms/cm^3 or less, thus having a remarkably low oxygen concentration and not containing a dopant impurity is manufactured by the MCZ method.

For the manufacture of this silicon single crystal rod, an ordinary

single crystal growing apparatus can be used. It is, for example, a single crystal growing apparatus 50 which pulls up a silicon single crystal rod 51 by a wire 52 as illustrated in FIG. 2. This single crystal growing apparatus 50 has a rotary crucible having a quartz crucible 53 disposed in a graphite crucible 54 and a graphite heater 57 disposed at the periphery of the rotary crucible. The quartz crucible 53 contains molten silicon 56 obtained by heating and melting by the graphite heater 57. A horizontal magnetic field is generated in the rotary crucible by a coil 58 disposed at the periphery of the rotary crucible. A tip portion of a seed crystal is dipped in the molten silicon 56 in the quartz crucible 53 and by gradually pulling it up, a single crystal is caused to grow. In this manner, the silicon single crystal rod 51 is manufactured. The silicon single crystal rod 51 having a desired oxygen concentration can be obtained only by adjusting the strength of the magnetic field, rotation speed of the crucible shaft 55, or the rotation speed or pulling-up speed of the silicon single crystal rod 51.

Each end (head and tail portions) is cut from the silicon single crystal rod thus pulled up and the resulting rod is shaped into a single crystal silicon block in the cylindrical form. The single crystal silicon block is subjected to NTD (neutron transmutation doping) while turning it in a heavy water reactor. This NTD treatment converts a portion of silicon (Si) into phosphorus (P). Accordingly, an N^- type single crystal silicon block having a dopant concentration within a range of from 1.0×10^{13} atoms/cm^3 to 1.0×10^{15} atoms/cm^3 is formed. Upon NTD treatment, the single crystal silicon block is exposed uniformly to neutrons so that the single crystal silicon block after treatment has a uniform phosphorus concentration.

Defect recovery annealing at 700°C or greater is then performed after the radioactivity level is reduced by half, whereby the damage by the

NTD treatment is removed. The single crystal silicon block is cut into each wafer, whereby an N^- type MCZ wafer is manufactured. The MCZ wafer thus obtained corresponds to the silicon substrate 10 of the semiconductor substrate 100 as illustrated in FIG. 1.

On the MCZ wafer, an N^- type epitaxial layer having a thickness of about 10 μm and a phosphorus concentration of about 1.0×10^{14} atoms/cm^3 is formed by the epitaxial growth. This means the formation of a low defect region on the surface of the MCZ wafer. For the formation of the epitaxial layer, a conventional epitaxial growth apparatus can be used. For example, a single wafer furnace is used as the epitaxial growth apparatus. As a raw material gas, SiH_4 is employed. Thermal process is given over the MCZ wafer, which has been heated to high temperature (about 1100°C), for a period of time determined depending on the film thickness, forming the epitaxial layer. The epitaxial layer thus formed corresponds to the epitaxial layer 11 of the semiconductor substrate 100 as illustrated in FIG. 1. In the above-described manner, the semiconductor substrate 100 as illustrated in FIG. 1 is manufactured.

In the semiconductor substrate 100 manufactured by the above manufacturing method, the MCZ wafer has an oxygen concentration of 8.0 $\times 10^{17}$ atoms/cm^3 or less so that the amount of oxygen diffused into the epitaxial layer is small. In other words, since interstitial oxygen in the MCZ wafer is, as illustrated in FIG. 3, less than that in the conventional MCZ wafer (refer to FIG. 14), the amount of oxygen diffused into the epitaxial layer is small. This leads to a drastic reduction in the generation of an oxygen donor or oxygen precipitation in the epitaxial layer. As a result, variations in the resistivity can be suppressed and the life time can be stabilized.

The electrical properties of the semiconductor substrate 100

according to the first embodiment were evaluated by three tests. By the first test, dependence of the oxygen donor concentration on the wafer oxygen concentration was evaluated. Described specifically, in the wafer manufactured by the MCZ method, the interstitial oxygen becomes an oxygen donor by the thermal process at from 300 to 600°C. The oxygen donor thus generated becomes a cause of the problems such as variations in the resistivity. When the MCZ wafer is used for a vertical type semiconductor element such as trench gate type IGBT, it is preferred to suppress the oxygen donor concentration to 1.0×10^{13} atoms/cm^3 or less.

FIG. 4 illustrates the results of SR measurement of the MCZ wafer after the formation of the semiconductor element. In other words, the relationship between the oxygen donor concentration (unit: /cm^3) and the oxygen concentration (unit: $\times 10^{17}$ atoms/cm^3) in the wafer is shown in the graph. As illustrated in FIG. 4, it has been found that the oxygen concentration in the wafer must be suppressed below 8.0×10^{17} atoms/cm^3 in order to suppress the oxygen donor concentration to 1.0×10^{13} atoms/cm^3 or less. When the semiconductor substrate 100 of this embodiment is used for a trench gate type IGBT, variations in the resistivity of the wafer can be reduced and resistance of the wafer can be heightened by adjusting the oxygen concentration in the wafer to 8.0×10^{17} atoms/cm^3 or less.

In the second test, dependence of the mechanical strength of the wafer on the wafer oxygen concentration or dependence of the slip length on the wafer oxygen concentration was evaluated. It is known that the lower the oxygen concentration in the wafer, the wafer has decreased mechanical strength. There is therefore a fear of inconveniences such as cracks of wafer occurring by a reduction in the oxygen concentration. The mechanical strength of the wafer was therefore measured by the three-point bending method as illustrated in FIG. 5. In this test, Support A and

Support B are disposed at both ends on the reverse side of a sample wafer and a load is applied to Center C on the surface side of the sample wafer. The load (unit: gf) when a crack appears in the sample wafer is measured as a breaking load.

FIG. 6 illustrates the measurement results of a breaking load of the MCZ wafer of this embodiment after the formation of a semiconductor element. In FIG. 6, a breaking load is plotted on the ordinate. In FIG. 6, the oxygen concentration (unit: atoms/cm^3) in the wafer is plotted along the abscissa. In FIG. 6, the wafers used for the measurement have an oxygen concentration exceeding 5.0×10^{17} atoms/cm^3 but this test or other test results reveal that the wafer can maintain its strength when the oxygen concentration is at least 2.0×10^{17} atoms/cm^3. As a result, it has been found that almost no change occurs in the mechanical strength of the wafer when the oxygen concentration in the wafer falls within a range of 2.0×10^{17} atoms/cm^3 to 11.0×10^{17} atoms/cm^3. In other words, it has been found that when the oxygen concentration is at least 2.0×10^{17} atoms/cm^3, it has no influence on the strength of the wafer.

It is known that upon thermal process at high temperatures, contact of a wafer with a boat causes slip and its growth. The XRT (X-ray topography) observation was made on the MCZ wafer thermally processed for 6 hours at 1150°C in an N^2 atmosphere. As a result, when the wafer had an oxygen concentration of 2.0×10^{17} atoms/cm^3, the maximum slip length was 35 mm. When the wafer had an oxygen concentration of 11.0×10^{17} atoms/cm^3, on the other hand, the maximum slip length was 32 mm. This reveals that there occurs almost no change in the slip length when the wafer has an oxygen concentration within a range of from 2.0×10^{17} atoms/cm^3 to 11.0×10^{17} atoms/cm^3.

By the third test, the dependence of the electrical properties of

IGBT on life time was evaluated. The life time of the wafer lowers greatly owing to oxygen precipitation or metal contamination. In particular, it is known that electrical properties (turnoff time, on voltage) of IGBT depends much on the life time. By using a simulation model as illustrated in FIG. 7, the relationship between the electrical properties of IGBT and life time was analyzed. The electrical properties of IGBT were determined whenever the life time of the x part in FIG. 7 was reduced by one tenth from 1000 μs. FIG. 8 shows the measurement results of the electrical properties of IBGT by using the MCZ wafer as a simulation model. As illustrated in FIG. 8, as the life time decreases, the on voltage rises with a decrease in the turnoff time. The results reveals that the life time is preferably 100 μs or greater.

Over the semiconductor substrate 100 of this Embodiment, a trench gate IGBT was manufactured by way of trial and the electrical properties of the IGBT were evaluated. As a result, the wafer had a life time of from 100 to 500 μs. In the simulation results, the turnoff time and on voltage were values at which the life time fell within a range of from 100 μs to 1000 μs, meaning that the electrical properties of the IGBT were favorable.

It has been found from these test results that by utilizing the MCZ wafer having an oxygen concentration of 8.0×10^{17} atoms/cm^3 or less, a high breakdown voltage semiconductor element with good electrical properties can be manufactured. It has also been found that the mechanical strength of the wafer does not lower when the oxygen concentration in the wafer is at least 2.0×10^{17} atoms/cm^3.

A high breakdown voltage semiconductor element making use of the semiconductor substrate 100 of this embodiment will next be described. FIG. 9 is an application example of the semiconductor substrate 100 of this embodiment to a trench gate type IGBT 110. The IGBT 110 as illustrated

in FIG. 9 is provided with a P well region 12, an N^+ emitter region 13, a P^+ collector region 14, a gate insulating film 15, an interlayer insulating film 16, a gate electrode 17, an emitter electrode 18 and a collector electrode 19. A gate material constituting the gate electrode 17 is, for example, polysilicon. An electrode material constituting the emitter electrode 18 or collector electrode 19 is, for example, aluminum.

In the IGBT 110 having such a structure, a channel effect is caused in the P well region 12 by the application of voltage to the gate electrode 17, whereby electrical conduction between the N^+ emitter region 13 and N^- type epitaxial region 11 is controlled. When the gate is on, transfer of carriers between the N^+ emitter region 13 and P^+ collector region 14 occurs, whereby the IGBT 110 becomes on state.

The IGBT 110 is fabricated in the following manner. First, a P well region 12 is formed over an epitaxial layer 11 of the semiconductor substrate 100 as illustrated in FIG. 1 by making use of ion implantation and thermal diffusion. In the P well region 12, an N^+ emitter region 13 is formed by making use of ion implantation and thermal diffusion. A gate trench is then formed by dry etching downward from the N^+ emitter region 13. A gate insulating film 15 is then formed by thermal oxidation, followed by deposition of a gate material over the gate insulating film 15 by CVD. By this deposition, the gate material is filled in the gate trench, whereby a gate electrode 17 is formed. An interlayer insulating film 16 is then formed by CVD, followed by the formation of an emitter electrode 18 by sputtering.

In the next place, the silicon substrate 10 is polished from its reverse side to adjust its thickness. By using ion implantation and thermal diffusion, a P^+ collector region 14 is formed on the reverse side of the silicon substrate 10, followed by the formation of a collector electrode

19 by sputtering, whereby the IGBT 110 as illustrated in FIG. 9 is fabricated.

The channel region of the IGBT 110 is disposed in the P well region 12 in the epitaxial layer which is a low defect region. The epitaxial layer is therefore thicker than the depth of the gate trench. When the element region is provided with a guard-ring at its periphery, the epitaxial layer is thicker than the depth of the guard-ring. This ensures stabilization of the electrical properties.

As described above, in the semiconductor substrate 100 according to the first embodiment, the oxygen concentration in the silicon substrate 10 is adjusted to 8.0×10^{17} atoms/cm^3 or less. This enables to suppress the oxygen donor concentration to not greater than 1.0×10^{13} atoms/cm^3, whereby variations in the resistivity of the wafer itself can be suppressed and resistance increase of the silicon substrate can be attained. In particular, in a semiconductor device which has, in the silicon substrate 10, a current path as the IGBT 110 illustrated in FIG. 9, the electrical properties can be stabilized by forming the silicon substrate 10 as a low defect region.

In addition, owing to a small oxygen content in the silicon substrate 10, the diffusion amount of oxygen into the epitaxial layer 2 is small. This leads a small oxygen donor amount or oxygen precipitation amount in the epitaxial layer (element region) compared with that in the conventional MCZ wafer. This makes it possible to attain a reduction in the variations in resistivity, improvement in the breakdown voltage of an oxide film and stabilization of the life time of carriers.

Moreover, even when the oxygen concentration of the silicon substrate 10 is adjusted to 8.0×10^{17} atoms/cm^3 or less, it does not influence on the mechanical strength (refer to FIG. 6). More specifically,

at an oxygen concentration in the wafer within a range of from 2.0×10^{17} atoms/cm^3 to 11.0×10^{17} atoms/cm^3, almost no change occurs in the mechanical strength of the wafer. The silicon substrate 10 which is an MCZ wafer has a higher oxygen concentration than an FZ wafer (usually, 1.0×10^{16} atoms/cm^3 or less). It has therefore higher mechanical strength than the FZ wafer.

Since the silicon substrate 10 is an MCZ wafer, an increase in the diameter of the wafer, improvement of its mechanical strength and cost reduction can be attained more readily than the FZ wafer. Accordingly, a semiconductor substrate having a large diameter, high mechanical strength and less crystal defects can be actualized.

In the manufacturing method of the semiconductor substrate 100, an N^- type single crystal silicon block is obtained by converting a portion of silicon into phosphorus by the NTD treatment upon manufacturing of the N^- type silicon substrate 10. The phosphorus concentration in the single crystal silicon block becomes uniform by this NTD treatment so that the resistivity can be controlled very stably. Compared with the manufacturing of an N^- type single crystal silicon block by doping of phosphorus, a production yield is better. This leads to a cost reduction.

[Second embodiment]

A semiconductor substrate 200 according to a second embodiment has, as illustrated in FIG. 10, a P^+ type silicon substrate 20 formed by the MCZ method and an N type epitaxial layer 21 formed over the silicon substrate 20 by the epitaxial growth. The semiconductor substrate 200 of this embodiment has, formed over the silicon substrate 20, the epitaxial layer 21 different in the conductivity type from the silicon substrate 20. In this point, it is different from the semiconductor substrate 100 of the

first embodiment having, formed over the silicon substrate 10, the epitaxial layer 11 having the same conductivity type. The silicon substrate 20 has a dopant concentration within a range of from 1.0×10^{14} atoms/cm^3 to 1.0×10^{19} atoms/cm^3. The oxygen concentration in the silicon substrate 20 is 8.0×10^{17} atoms/cm^3 or less. The epitaxial layer 21 has a thickness of about 25 μm.

The manufacturing method of the semiconductor substrate 200 as illustrated in FIG. 10 will next be described. First, a P^+ type silicon single crystal rod having the oxygen concentration, as a wafer, not greater than 8.0×10^{17} atoms/cm^3, having a concentration of impurities including boron within a range of 1.0×10^{14} atoms/cm^3 to 1.0×10^{19} atoms/cm^3, and having a low oxygen concentration is manufactured by the MCZ method. For the manufacture of the silicon single crystal rod, an ordinary single crystal growth apparatus can be used necessary. The silicon single crystal rod having a desired oxygen concentration can be obtained only by adjusting the strength of the magnetic field, rotation speed of the crucible shaft, or the rotation speed or pulling-up seed of the silicon single crystal rod.

Each end (head and tail portions) is cut from the silicon single crystal rod thus pulled up and the resulting rod is shaped into a single crystal silicon block in the cylindrical form. The single crystal silicon block is then cut into each wafer, whereby a P^+ type MCZ wafer is manufactured. The MCZ wafer thus obtained corresponds to the silicon substrate 20 of the semiconductor substrate 200 as illustrated in FIG. 10.

On the MCZ wafer, an N type epitaxial layer having a thickness of about 25 μm and a phosphorus concentration of from 1.0×10^{14} atoms/cm^3 to 1.0×10^{16} atoms/cm^3 is formed. For the formation of the epitaxial layer, a conventional epitaxial growth apparatus can be used. The epitaxial layer thus formed corresponds to the epitaxial layer 21 of the

semiconductor substrate 200 as illustrated in FIG. 10. In the above-described manner, the semiconductor substrate 200 as illustrated in FIG. 10 is manufactured.

In the semiconductor substrate 200 manufactured in the above manufacturing method, the MCZ wafer has an oxygen concentration of 8.0 $\times$ 10^{17} atoms/cm^3 or less so that the amount of oxygen diffused into the epitaxial layer is small. This makes it possible to reduce the generation of oxygen donor or precipitation of oxygen in the epitaxial layer, suppress the variations in the resistivity and stabilize the life time.

A high-voltage semiconductor element making use of the semiconductor substrate 200 of this embodiment will next be described. FIG. 11 illustrates an application example of the semiconductor substrate 200 of this embodiment to a CMOS 210. The CMOS 210 is provided with an NMOS 211 and a PMOS 212 and these MOSs are isolated from each other by a trench wall 213. The CMOS 210 has a P well region 22, an N body region 23, a P body region 24, a gate insulating film 25, an interlayer insulating film 26, a gate electrode 27, a source electrode 28 and a drain electrode 29.

In the CMOS 210 having such a structure, a channel effect is caused in the P well region 22 in the NMOS 211 or in the epitaxial layer 21 in the PMOS 212, whereby electrical conduction between the adjacent N body regions 23 and 23 or adjacent P body regions 24 and 24 is controlled.

The CMOS 210 is manufactured in the following manner. First, a region in the epitaxial layer 21 as illustrated in FIG. 10 wherein the NMOS 211 is to be formed, a P well region 22 is formed by making use of ion implantation and thermal diffusion. An N body region 23 is formed in the P well region 22 by making use of ion implantation and thermal diffusion. In a region in the epitaxial layer 21 wherein the PMOS 212 is

to be formed, a P body region 24 is formed making use of ion implantation and thermal diffusion. A trench 213 is then formed by dry etching. A gate insulating film 25 is then formed by thermal oxidation, followed by the formation of an oxide film over the side walls of the trench 213. Over the gate insulating film 25, a gate material is deposited by CVD to form a gate electrode 27. An interlayer insulating film 26 is formed by CVD. A source electrode 28 and a drain electrode 29 are then formed by sputtering, whereby the CMOS 210 as illustrated in FIG. 11 is fabricated.

In the semiconductor substrate 200 according to the second embodiment, the oxygen concentration in the P^+ type silicon substrate 20 is adjusted to 8.0×10^{17} atoms/cm^3 or less. As in the first embodiment, this enables to suppress the oxygen donor concentration to 1.0×10^{13} /cm^3 or less, whereby the variations in the resistivity of the P^+ type silicon substrate 20 and epitaxial layer 21 can be suppressed. The semiconductor substrate 200 is made of a P^+ type MCZ wafer. This means that the MCZ wafer is required to have the oxygen concentration of 8.0×10^{17} atoms/cm^3 or less so that even the P type silicon substrate 20 is effective for suppressing an oxygen donor amount. The CMOS 210 is fabricated using the semiconductor substrate 200. Even when the semiconductor device is either a horizontal type or vertical type, the electrical properties can be stabilized by maintaining the low defect state of the epitaxial layer 21.

[Third Embodiment]

The semiconductor substrate 300 according to the third embodiment has, as shown in FIG. 12, a P^+ type silicon substrate 30 formed by the MCZ method, an N^+ type first epitaxial layer 31 formed over the silicon substrate 30 by the epitaxial growth, an N^{--} type second epitaxial layer 32 formed over the first epitaxial layer 31, and an N^- type

third epitaxial layer 33 formed over the second epitaxial layer 32. In short, the semiconductor substrate 300 of this embodiment has multiple epitaxial layers stacked over the silicon substrate 30. In this point, the semiconductor substrate of this embodiment is different from the semiconductor substrate 100 of the first embodiment having, formed thereon, only the epitaxial layer 11 of about 10 μm thick. The dopant concentration of the silicon substrate 30 falls within a range of from 1.0×10^{17} atoms/cm^3 to 1.0×10^{19} atoms/cm^3. The oxygen concentration in the silicon substrate 30 is 8.0×10^{17} atoms/cm^3 or less. With regards to the thickness of each epitaxial layer, the first epitaxial layer 31 is about 5 μm thick, the second epitaxial layer 32 is about 25 μm thick, and the third epitaxial layer 33 is about 90 μm thick.

The manufacturing method of the semiconductor substrate 300 as illustrated in FIG. 12 will next be described. First, a P^+ type silicon single crystal rod having an oxygen concentration, as a wafer, not greater than 8.0×10^{17} atoms/cm^3, having a concentration of impurities including boron within a range of from 1.0×10^{17} atoms/cm^3 to 1.0×10^{19} atoms/cm^3 and having a low oxygen concentration is manufactured by the MCZ method. For the manufacture of this silicon single crystal rod, an ordinary single crystal growing apparatus can be used. The silicon single crystal rod having a desired oxygen concentration can be obtained only by adjusting the strength of the magnetic field, rotation speed of the crucible axis, or the rotation speed or pulling-up speed of the silicon single crystal rod.

Each end (head and tail portions) is cut from the silicon single crystal rod thus pulled up and the resulting rod is shaped into a single crystal silicon block in the cylindrical form. The single crystal silicon block is then cut into each wafer, whereby a P^+ type MCZ wafer is manufactured. The MCZ wafer thus obtained corresponds to the silicon

substrate 30 of the semiconductor substrate 300 as illustrated in FIG. 12.

On the MCZ wafer, an N^+ type first epitaxial layer having a thickness of about 5 μm and a phosphorus concentration within a range of from 1.0×10^{17} atoms/cm^3 to 1.0×10^{19} atoms/cm^3 is formed. Over the first epitaxial layer, an N^{--} type second epitaxial layer having a thickness of about 25 μm and having a phosphorus concentration of about 5.0×10^{13} atoms/cm^3 is formed. Over the second epitaxial layer, an N^- type third epitaxial layer having a thickness of about 90 μm and having a phosphorus concentration of about 1.0×10^{14} atoms/cm^3 is formed. In short, three-layer epitaxial structure of about 120 μm thick is formed on the surface of the MCZ wafer. For the formation of the epitaxial layer, an ordinary epitaxial growth apparatus can be used. These epitaxial layers correspond to the first epitaxial layer 31, the second epitaxial layer 32, and the third epitaxial layer 33 of the semiconductor substrate 300 as illustrated in FIG. 12, respectively. In the above-described manner, the semiconductor substrate 300 as illustrated in FIG. 12 is manufactured.

In the semiconductor substrate 300 manufactured in the above manufacturing method, the MCZ wafer has an oxygen concentration of 8.0×10^{17} atoms/cm^3 or less so that the amount of oxygen diffused into the first epitaxial layer is small. Diffusion of oxygen into the second epitaxial layer and third epitaxial layer is hardly observed. This leads to a reduction in the generation of an oxygen donor or oxygen precipitation in each epitaxial layer. As a result, variations in the resistivity can be suppressed and the life time can be stabilized.

A high voltage semiconductor element making use of the semiconductor substrate 300 of this embodiment will next be described. FIG. 13 is an application example of the semiconductor substrate 300 of this embodiment to a trench gate type IGBT 310. The IGBT 310 as

illustrated in FIG. 13 is provided with a P well region 34, an N^+ emitter region 35, a gate insulating film 36, an interlayer insulating film 37, a gate electrode 38, an emitter electrode 39 and a collector electrode 40. The P^+ type silicon substrate 30 is used as a collector region of the IGBT 310.

In the IGBT 310 having such a structure, a channel effect is caused in the P well region 34 by the application of voltage to the gate electrode 38, whereby electrical conduction between the N^+ emitter region 35 and N^- type third epitaxial region 33 is controlled. When the gate is on, transfer of carriers between the N^+ emitter region 35 and P^+ type silicon substrate 30, that is, the collector region occurs, whereby the IGBT 310 becomes on-state.

The IGBT 310 is fabricated in the following manner. First, a P well region 34 is formed over the third epitaxial layer 33 of the semiconductor substrate 300 as illustrated in FIG. 12 by making use of ion implantation and thermal diffusion. In the P well region 34, an N^+ emitter region 35 is formed by making use of ion implantation and thermal diffusion. A gate trench is then formed by dry etching downward from the N^+ emitter region 35. A gate insulating film 36 is then formed by thermal oxidation, followed by deposition of a gate material over the gate insulating film 36 by CVD. By this deposition, the gate material is filled in the gate trench, whereby a gate electrode 38 is formed. An interlayer insulating film 37 is then formed by CVD, followed by the formation of an emitter electrode 39 by sputtering. In the next place, the silicon substrate 30 is polished from its reverse side to adjust its thickness. By sputtering, a collector region 40 is then formed, whereby the IGBT 310 as illustrated in FIG. 13 is fabricated.

In the semiconductor substrate 300 according to the third embodiment, the oxygen concentration in the P^+ type silicon substrate 30 is

adjusted to 8.0×10^{17} atoms/cm^3 or less. As in the first embodiment, this enables to suppress the oxygen donor concentration to not greater than 1.0×10^{13} atoms/cm^3, whereby variations in the resistivity can be suppressed and resistance increase of the silicon substrate can be attained. In particular, in a semiconductor device which has, in the silicon substrate 30, a current path as IGBT 310 as illustrated in FIG. 13, the electrical properties become stable because the silicon substrate 30 is a low defect region.

The embodiments so far described are offered by way of illustration and not by way of limitation of the present invention. It is therefore possible to improve or modify the present invention within a range not departing from the scope of the invention. With regards to each semiconductor region, the P type and N type may be changed each other. In the first embodiment, a non-doped silicon single crystal rod is formed for the manufacture of the N^- type silicon substrate 10 by the NTD treatment. Alternatively, a phosphorus-containing N^+ type silicon single crystal rod having a low oxygen concentration may be formed without NTD treatment.

INDUSTRIAL APPLICABILITY

The present invention makes it possible to reduce the problems caused by crystal defects such as variations in resistivity, oxygen precipitation and diffusion of oxygen into the epitaxial layer because the semiconductor wafer substrate has an oxygen concentration as low as 8.0×10^{17} atoms/cm^3 or less. The semiconductor wafer substrate has a larger diameter than an FZ wafer, because it is an MCZ wafer. The decrease in mechanical strength does not occur when the wafer has an oxygen concentration of 2.0×10^{17} atoms/cm^3 or greater. Therefore, the present invention has succeeded in the actualization of a semiconductor substrate

having a large diameter, a high mechanical strength and less crystal defects, and a semiconductor device utilizing the semiconductor substrate and manufacturing methods thereof.

CLAIMS

1. A semiconductor substrate comprising:

a semiconductor wafer substrate manufactured by the MCZ method (magnetic field applied Czochralski method) and having an oxygen concentration of 8.0×10^{17} atoms/cm^3 (ASTM F121 1979: which will hereinafter equally apply to the oxygen concentration) or less, and

an epitaxial layer existing on the semiconductor wafer substrate and formed by the epitaxial growth.

2. A semiconductor substrate according to Claim 1, wherein:

the semiconductor wafer substrate having an oxygen concentration within a range of from 2.0×10^{17} atoms/cm^3 to 8.0×10^{17} atoms/cm^3.

3. A semiconductor device controlling an electric current by the application of a voltage to a gate electrode, which comprises:

a semiconductor wafer substrate manufactured by the MCZ method and having an oxygen concentration of 8.0×10^{17} atoms/cm^3 or less, and

an epitaxial layer existing on the semiconductor wafer substrate and formed by the epitaxial growth, wherein:

the epitaxial layer includes a channel region.

4. A semiconductor device according to Claim 3, wherein:

the semiconductor wafer substrate has an oxygen concentration within a range of from 2.0×10^{17} atoms/cm^3 to 8.0×10^{17} atoms/cm^3.

5. A semiconductor device according to Claim 3 or Claim 4, wherein:

the semiconductor wafer substrate is provided with a current path through which an electric current flows when voltage is on a gate electrode.

6. A manufacturing method of a semiconductor substrate, which comprises:

a semiconductor wafer forming step of growing a silicon single

crystal rod by the MCZ method and processing the silicon single crystal rod into a semiconductor wafer, and

an epitaxial growth step of forming an epitaxial layer in the epitaxial growth over the semiconductor wafer formed by the semiconductor wafer forming step, wherein:

the silicon single crystal rod formed in the semiconductor wafer forming step has an oxygen concentration of 8.0×10^{17} atoms/cm^3 or less.

7. A manufacturing method of a semiconductor substrate according to Claim 6, wherein:

the silicon single crystal rod formed in the semiconductor wafer forming step has an oxygen concentration within a range of from 2.0×10^{17} atoms/cm^3 to 8.0×10^{17} atoms/cm^3.

8. A manufacturing method of a semiconductor substrate according to Claim 6 or 7, wherein:

in the semiconductor wafer forming step, after formation of a silicon single crystal rod not containing a dopant impurity, the silicon single crystal rod is subjected to NTD (neutron transmutation doping) treatment to give it a desired dopant concentration.

9. A manufacturing method of a semiconductor device controlling an electric current by the application of a voltage to a gate electrode, which comprises:

a semiconductor wafer forming step of growing a silicon single crystal rod by the MCZ method and processing the silicon single crystal rod into a semiconductor wafer,

an epitaxial growth step of forming an epitaxial layer by the epitaxial growth on the semiconductor wafer formed in the semiconductor wafer forming step, and

a semiconductor element forming step of forming a semiconductor

element on the epitaxial layer formed in the epitaxial growth step, wherein:

the silicon single crystal rod formed in the semiconductor wafer forming step has an oxygen concentration of 8.0×10^{17} atoms/cm^3 or less.

10. A manufacturing method of a semiconductor device according to Claim 9, wherein:

the silicon single crystal rod manufactured in the semiconductor wafer forming step has an oxygen concentration within a range of from 2.0×10^{17} atoms/cm^3 to 8.0×10^{17} atoms/cm^3.

11. A manufacturing method of a semiconductor device according to Claim 9 or 10, wherein:

in the semiconductor wafer forming step, after formation of a silicon single crystal rod not containing a dopant impurity, the silicon single crystal rod is subjected to NTD treatment to give it a desired dopant concentration.

FIG. 1

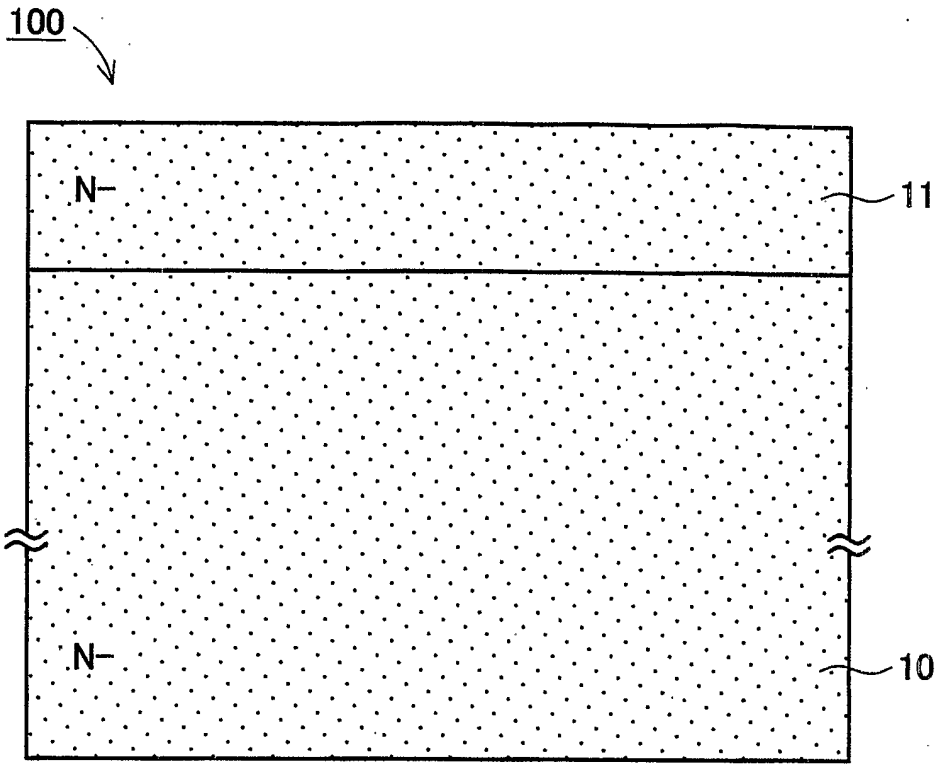


FIG. 2

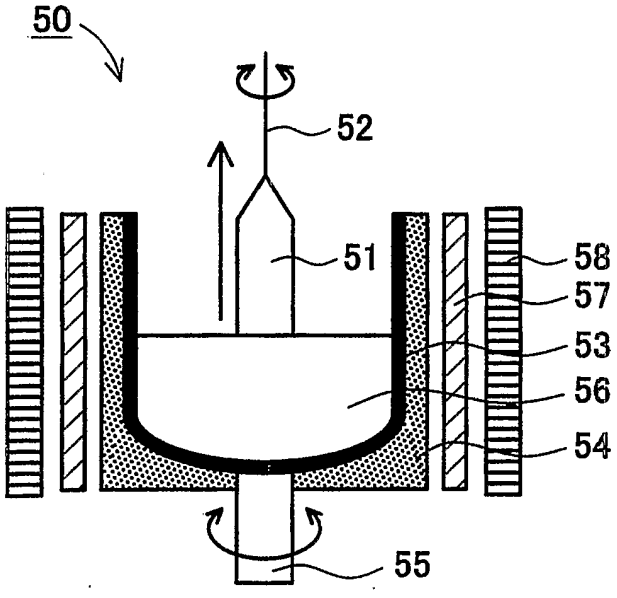


FIG. 3

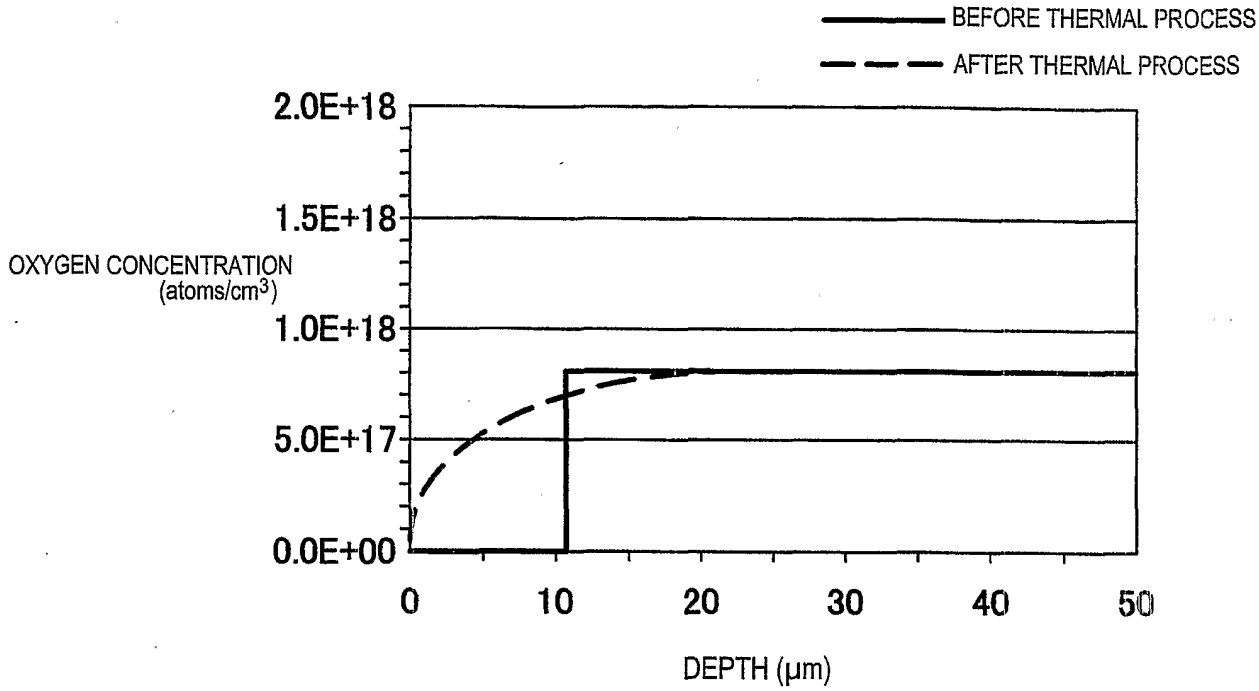

BEFORE THERMAL PROCESS
AFTER THERMAL PROCESS
OXYGEN CONCENTRATION (atoms/cm3)
2.0E+18
1.5E+18
1.0E+18
5.0E+17
0.0E+00
0
10
20
30
40
50
DEPTH (μm)

FIG. 4

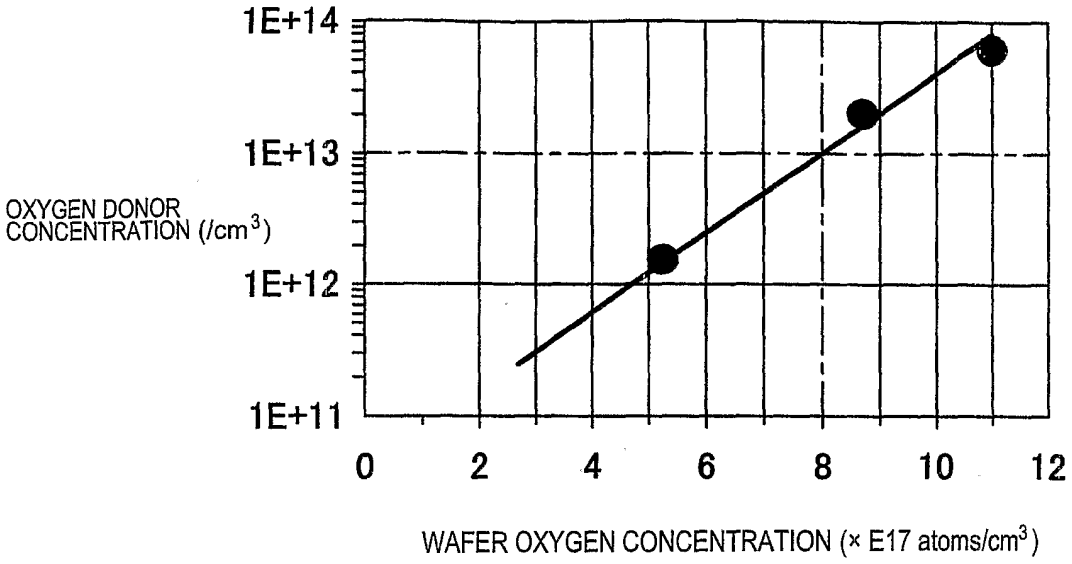

1E+14
1E+13
1E+12
1E+11
OXYGEN DONOR CONCENTRATION (/cm3)
0
2
4
6
8
10
12
WAFER OXYGEN CONCENTRATION (× E17 atoms/cm3)

FIG. 5

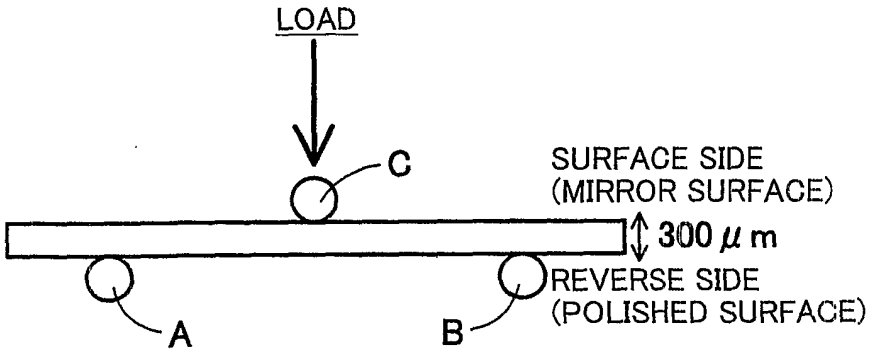

LOAD
C
SURFACE SIDE
(MIRROR SURFACE)
300 μm
REVERSE SIDE
(POLISHED SURFACE)
A
B

FIG. 6

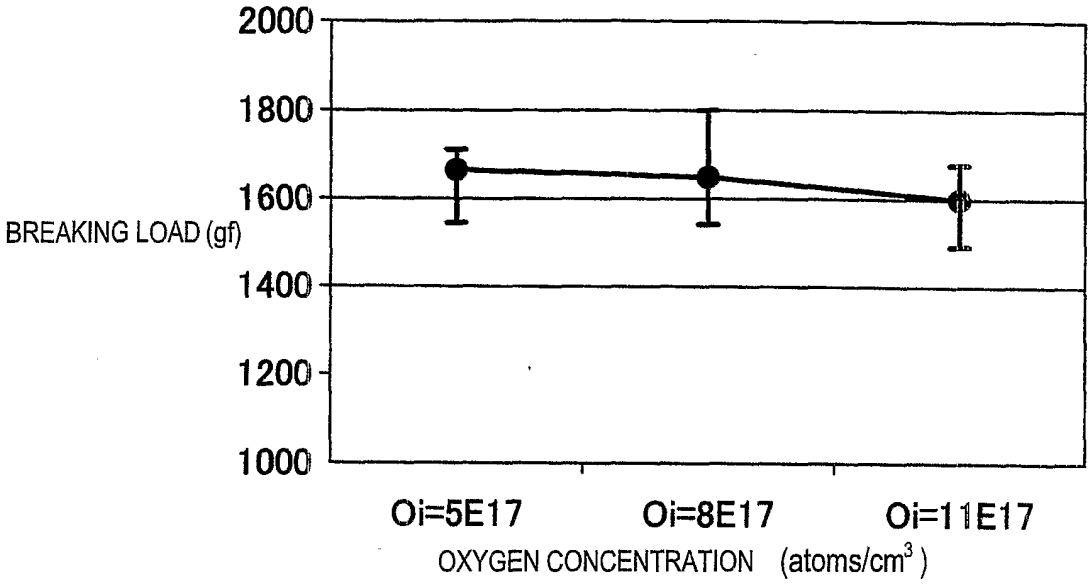

2000
1800
1600
1400
1200
1000
BREAKING LOAD (gf)
Oi=5E17
Oi=8E17
Oi=11E17
OXYGEN CONCENTRATION (atoms/cm3)

FIG. 7

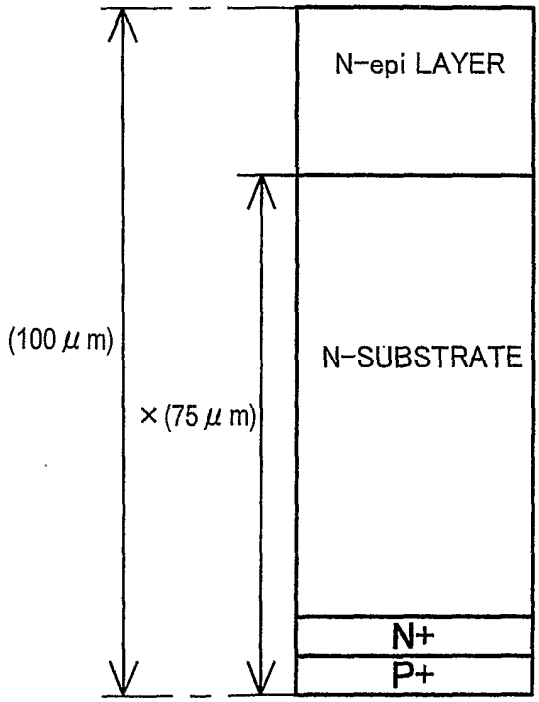

N-epi LAYER
N-SUBSTRATE
N+
P+
(100 μ m)
× (75 μ m)

FIG. 8

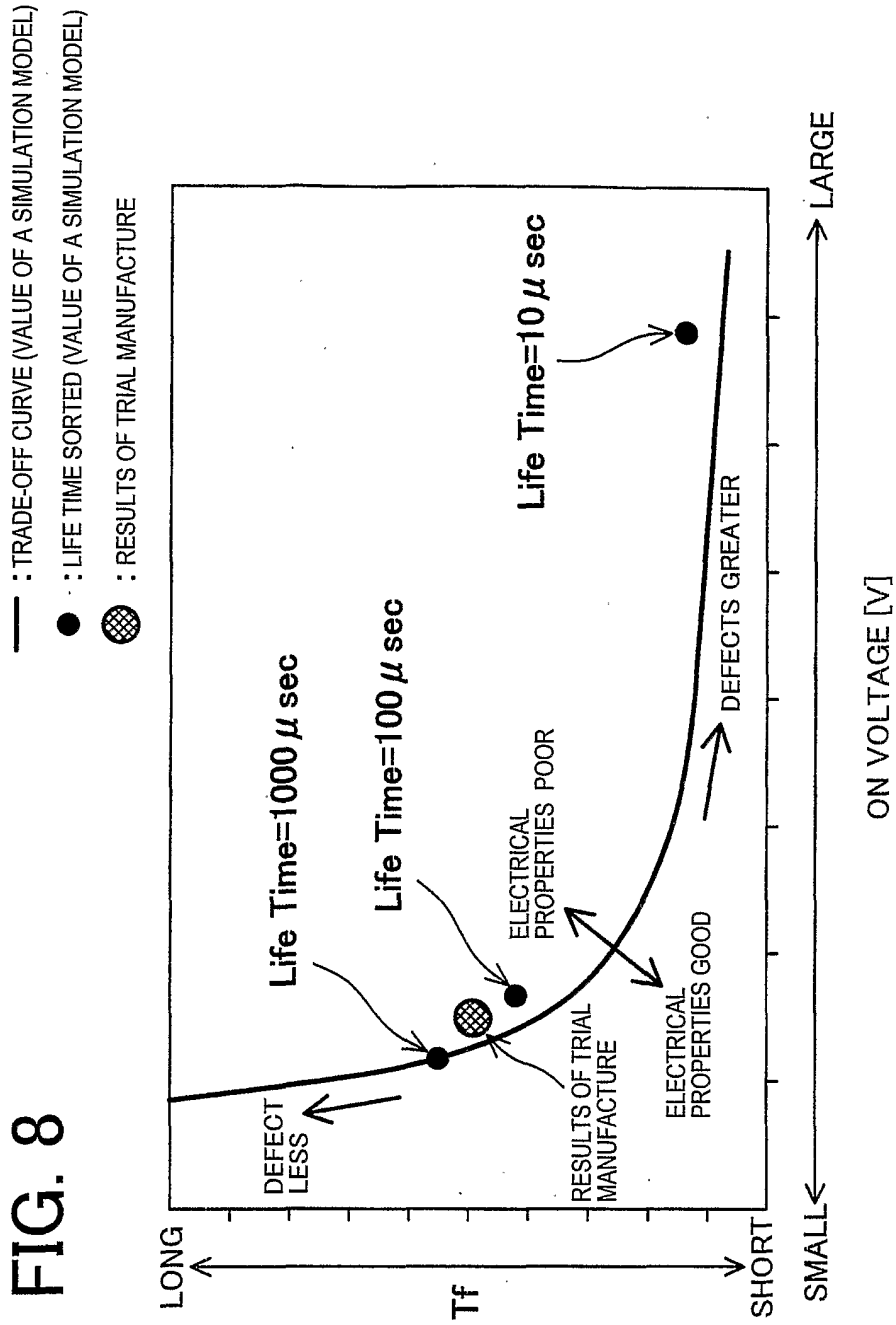

: TRADE-OFF CURVE (VALUE OF A SIMULATION MODEL)
: LIFE TIME SORTED (VALUE OF A SIMULATION MODEL)
: RESULTS OF TRIAL MANUFACTURE
Life Time=1000 μ sec
Life Time=100 μ sec
Life Time=10 μ sec
DEFECT LESS
RESULTS OF TRIAL MANUFACTURE
ELECTRICAL PROPERTIES POOR
ELECTRICAL PROPERTIES GOOD
DEFECTS GREATER
LONG
Tf
SHORT
SMALL
LARGE
ON VOLTAGE [V]

FIG. 9

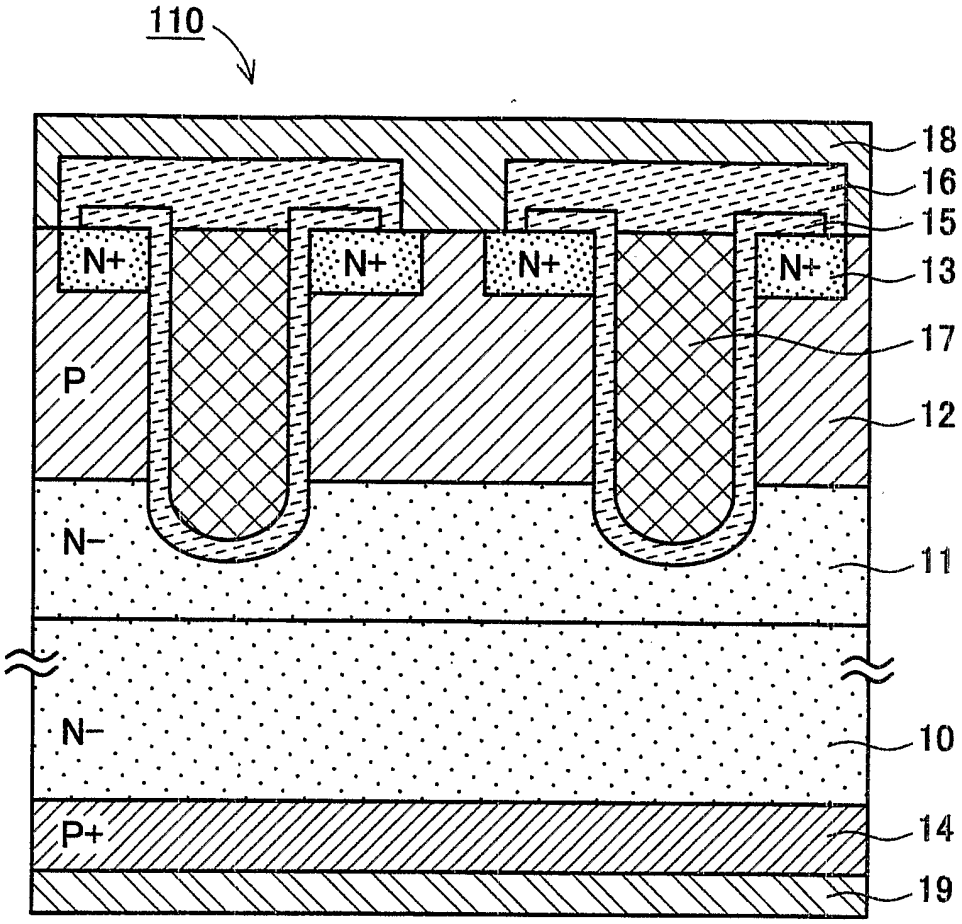


FIG. 10

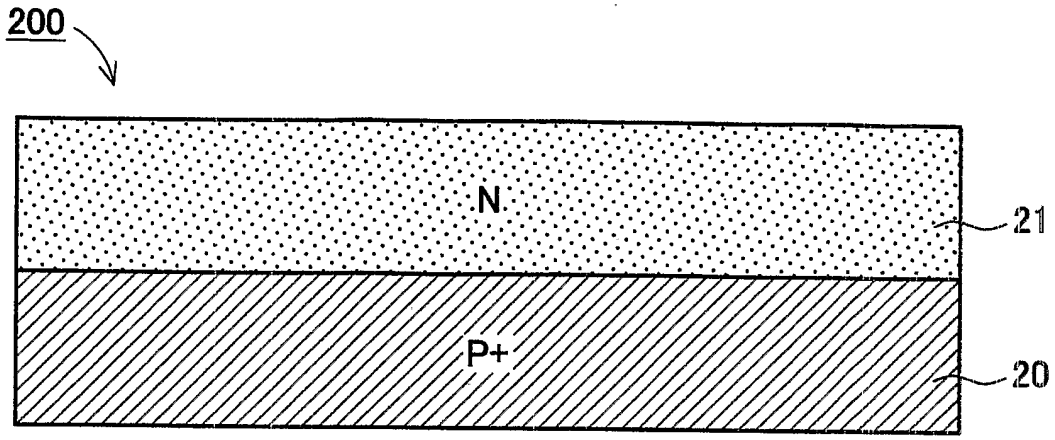

200
N
21
P+
20

FIG. 11

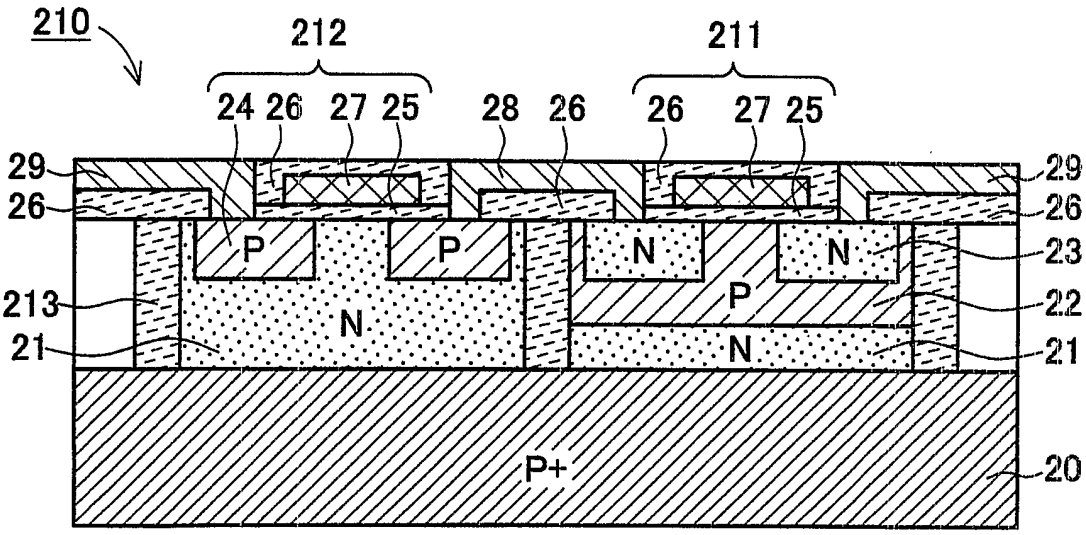

210
212
211
24 26 27 25
28 26
26 27 25
29
26
P
P
N
N
23
213
N
P
22
21
N
21
P+
20

FIG. 12

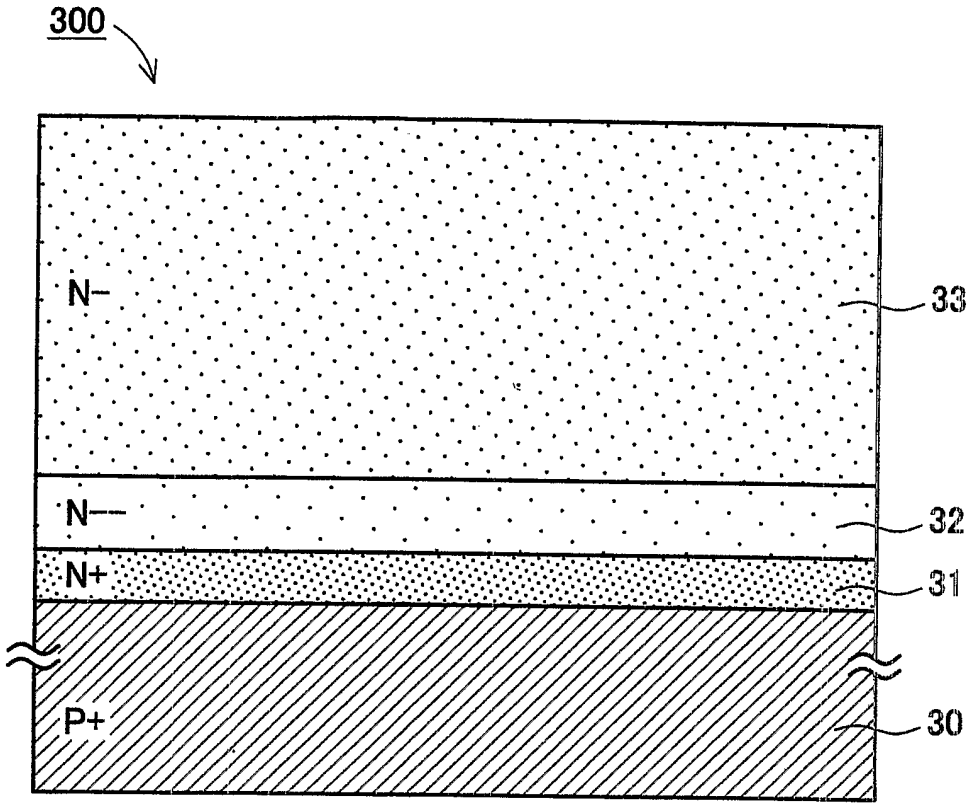


FIG. 13

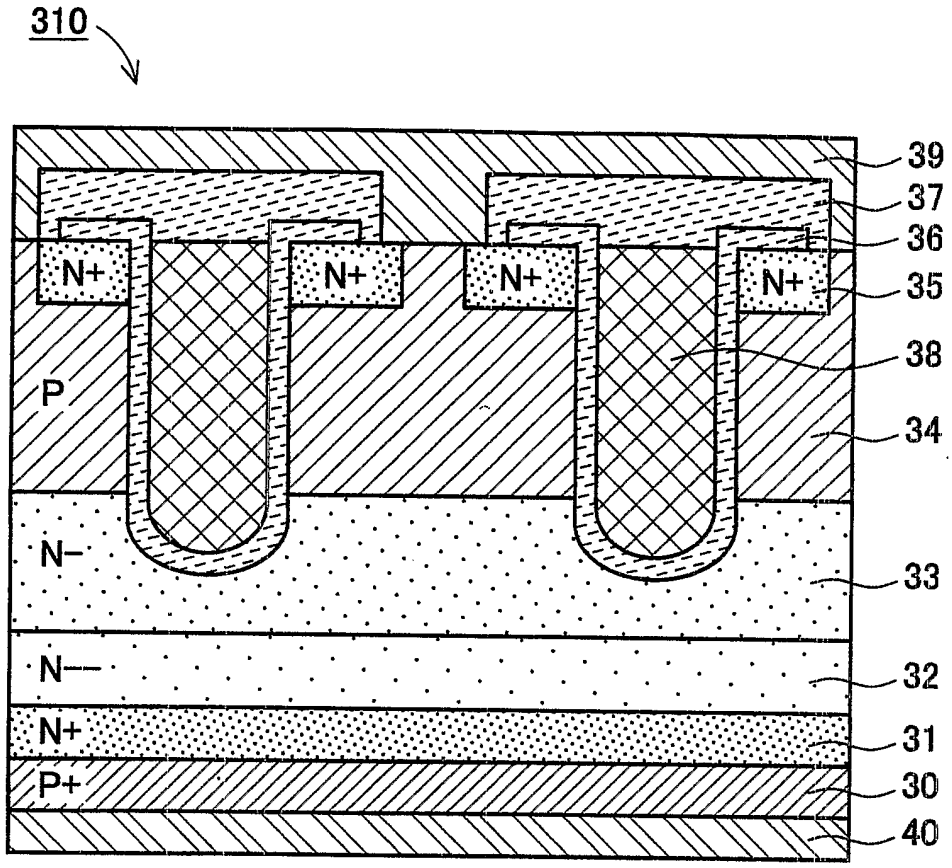
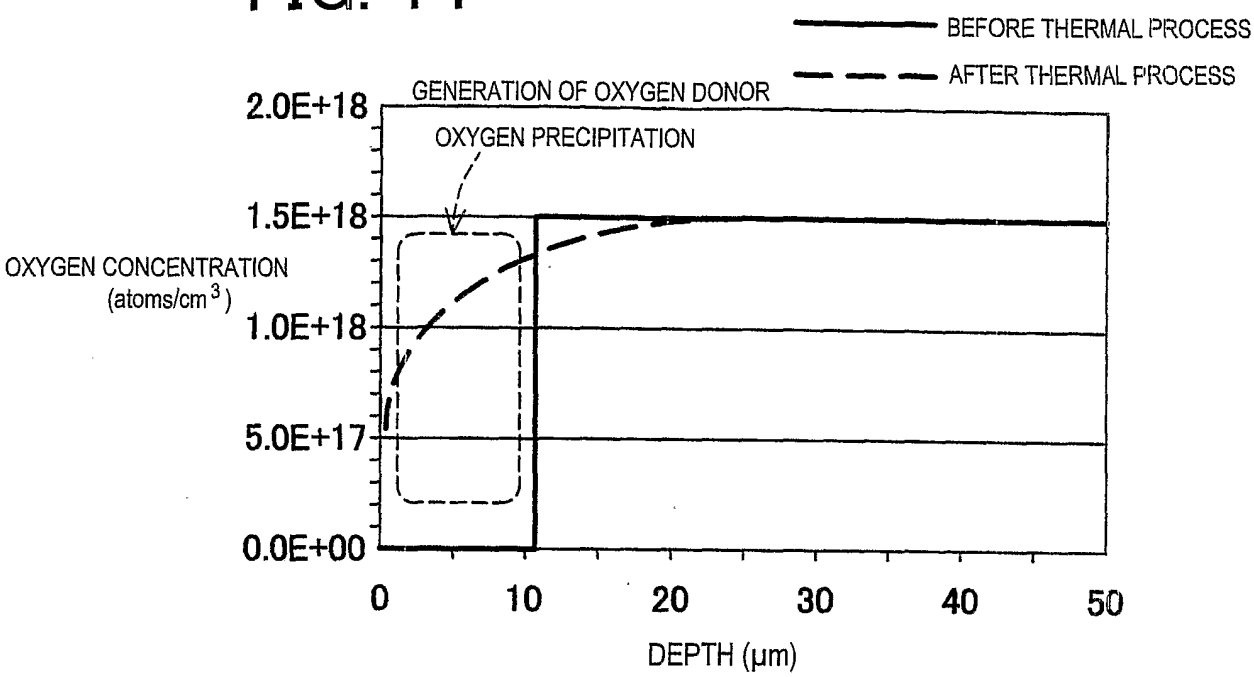


FIG. 14


BEFORE THERMAL PROCESS
AFTER THERMAL PROCESS
GENERATION OF OXYGEN DONOR
OXYGEN PRECIPITATION
OXYGEN CONCENTRATION (atoms/cm3)
2.0E+18
1.5E+18
1.0E+18
5.0E+17
0.0E+00
0
10
20
30
40
50
DEPTH (μm)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/JP2005/008337

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 C30B29/06 C30B15/00 H01L21/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 C30B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 6 565 652 B1 (KONONCHUK OLEG V ET AL) 20 May 2003 (2003-05-20) column 6, line 6 - line 49	1-7,9,10 8,11
Y	PATENT ABSTRACTS OF JAPAN vol. 1997, no. 09, 30 September 1997 (1997-09-30) & JP 09 115848 A (SONY CORP), 2 May 1997 (1997-05-02) abstract	8,11
A	PATENT ABSTRACTS OF JAPAN vol. 2003, no. 12, 5 December 2003 (2003-12-05) & JP 2003 286094 A (SUMITOMO MITSUBISHI SILICON CORP), 7 October 2003 (2003-10-07) cited in the application abstract	

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

'A' document defining the general state of the art which is not considered to be of particular relevance

'E' earlier document but published on or after the international filing date

'L' document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

'O' document referring to an oral disclosure, use, exhibition or other means

'P' document published prior to the international filing date but later than the priority date claimed

'T' later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

'X' document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

'Y' document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

'&' document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 July 2005	28/07/2005

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Cook, S

INTERNATIONAL SEARCH REPORT

International Application No
PCT/JP2005/008337

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 675 214 A (SUMITOMO SITIX CORPORATION) 4 October 1995 (1995-10-04) page 7, line 3 - line 10	1-11
A	PATENT ABSTRACTS OF JAPAN vol. 017, no. 551 (C-1117), 5 October 1993 (1993-10-05) & JP 05 155682 A (SHIN ETSU HANDOTAI CO LTD), 22 June 1993 (1993-06-22) abstract	1-11

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
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