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Liu et al.

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(54) **PIXEL CIRCUIT OUTPUTTING TIME DIFFERENCE DATA AND IMAGE DATA, AND OPERATING METHOD THEREOF**

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This patent is subject to a terminal disclaimer.

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(63) Continuation of application No. 17/401,554, filed on Aug. 13, 2021, now Pat. No. 11,706,542, which is a continuation-in-part of application No. 17/009,417, filed on Sep. 1, 2020, now Pat. No. 11,290,671.

(51) **Int. Cl.**

H04N 25/75	(2023.01)
H04N 25/589	(2023.01)
H04N 25/767	(2023.01)
H04N 25/77	(2023.01)
H04N 25/771	(2023.01)
H04N 25/78	(2023.01)

(52) **U.S. Cl.**

CPC ***H04N 25/75*** (2023.01); ***H04N 25/589*** (2023.01); ***H04N 25/767*** (2023.01); ***H04N 25/77*** (2023.01); ***H04N 25/771*** (2023.01); ***H04N 25/78*** (2023.01)

(58) **Field of Classification Search**

CPC H04N 25/75; H04N 25/589; H04N 25/767; H04N 25/77; H04N 25/771; H04N 25/78; H04N 25/44

See application file for complete search history.

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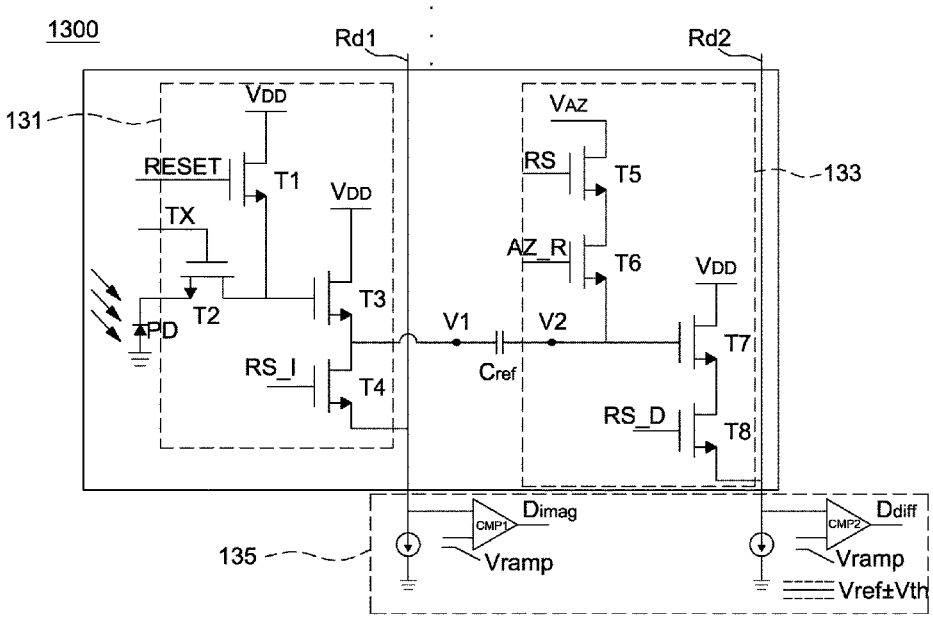
(57) **ABSTRACT**

There is provided a pixel circuit capable of outputting time difference data and image data, and including an image circuit and a difference circuit. The image circuit is used to record and output detected light energy of a first interval as the image data. The difference circuit is used to record and output a variation of detected light energy between the first interval and a second interval as the time difference data. The pixel circuit selects to output at least one of the time difference data and the image data.

18 Claims, 20 Drawing Sheets



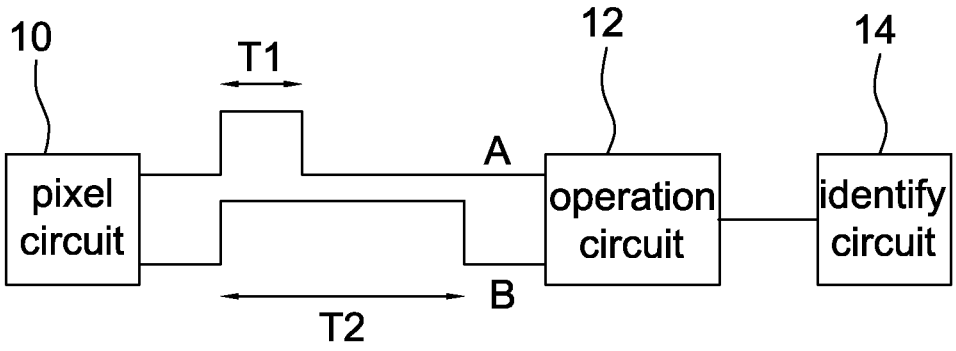

10
T1
12
14
A
pixel circuit
operation circuit
identify circuit
B
T2

FIG. 1

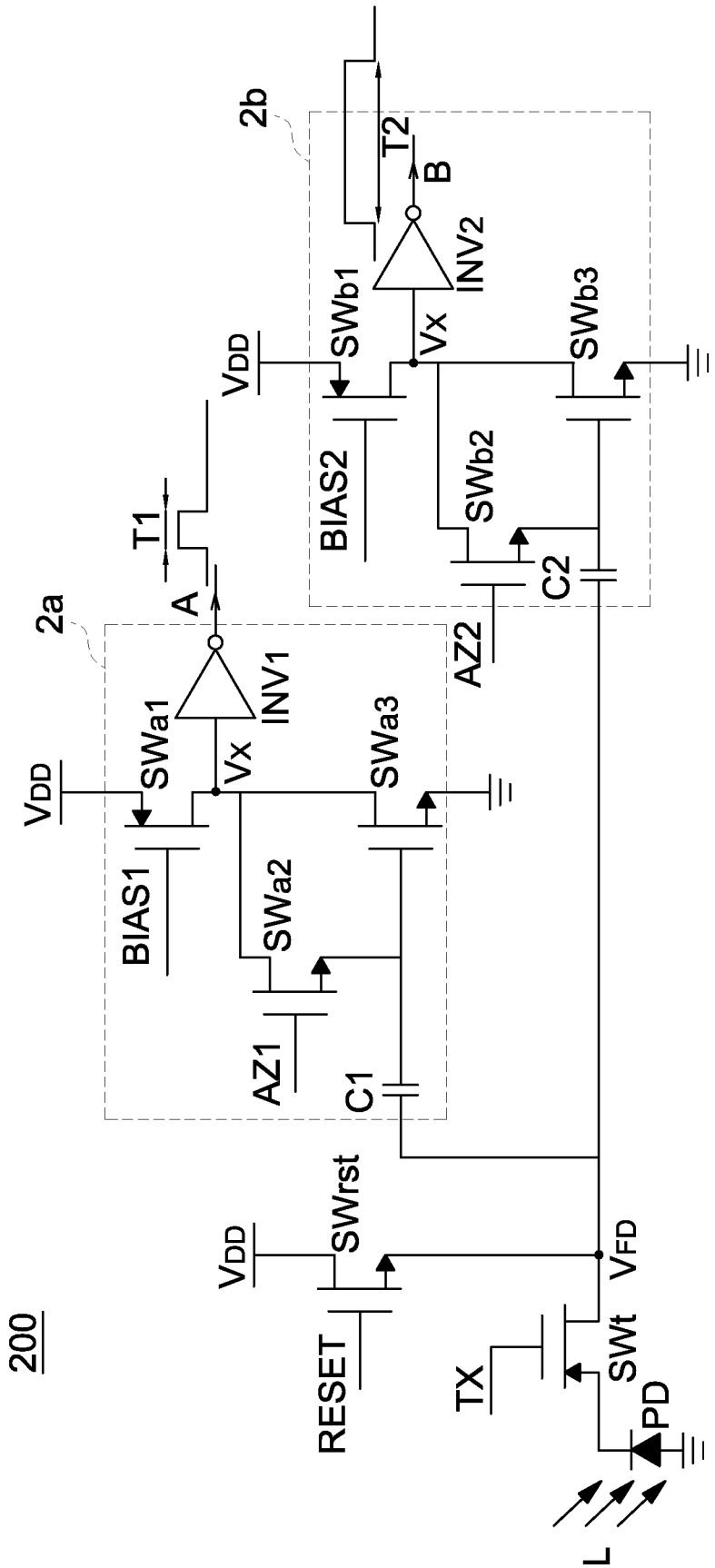

200
2a
2b
T1
T2
A
B
INV1
INV2
Vx
Vx
VDD
VDD
VDD
VDD
SWa1
SWa2
SWa3
SWb1
SWb2
SWb3
BIAS1
BIAS2
AZ1
AZ2
C1
C2
SWrst
RESET
TX
SWt
VFD
PD
L

FIG. 2

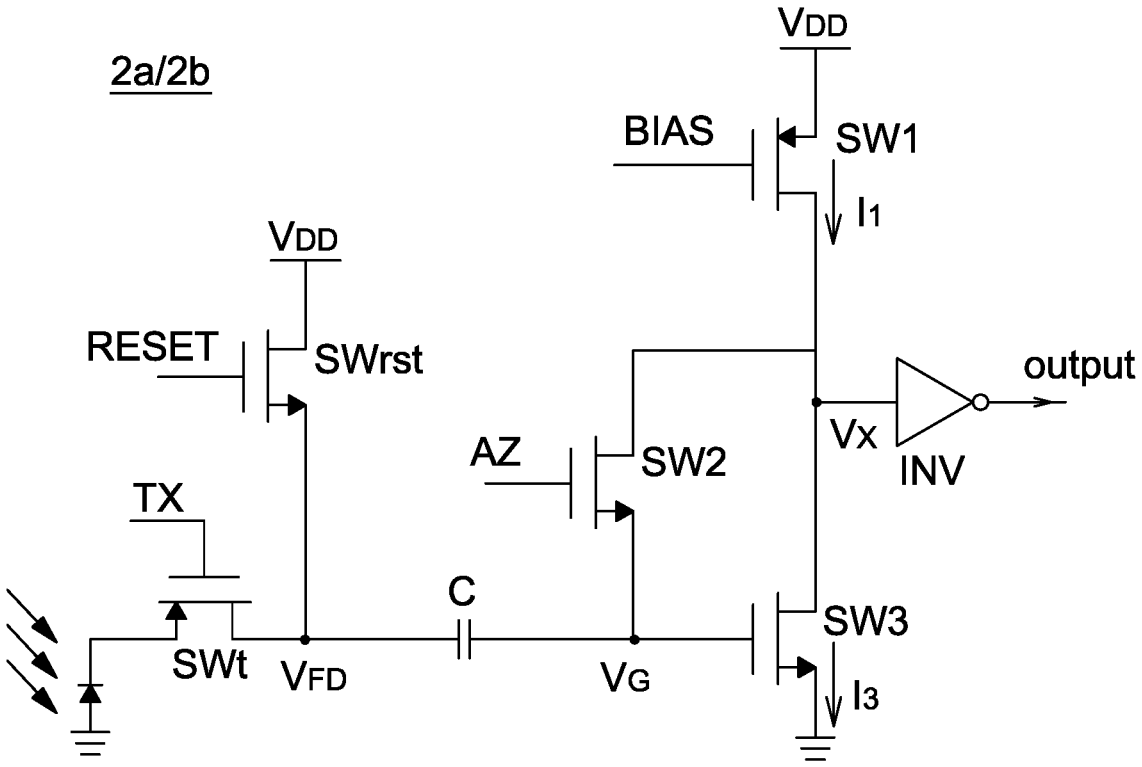

2a/2b
VDD
BIAS
SW1
I1
VDD
RESET
SWrst
output
Vx
INV
AZ
SW2
TX
C
SW3
SWt
VFD
VG
I3

FIG. 3

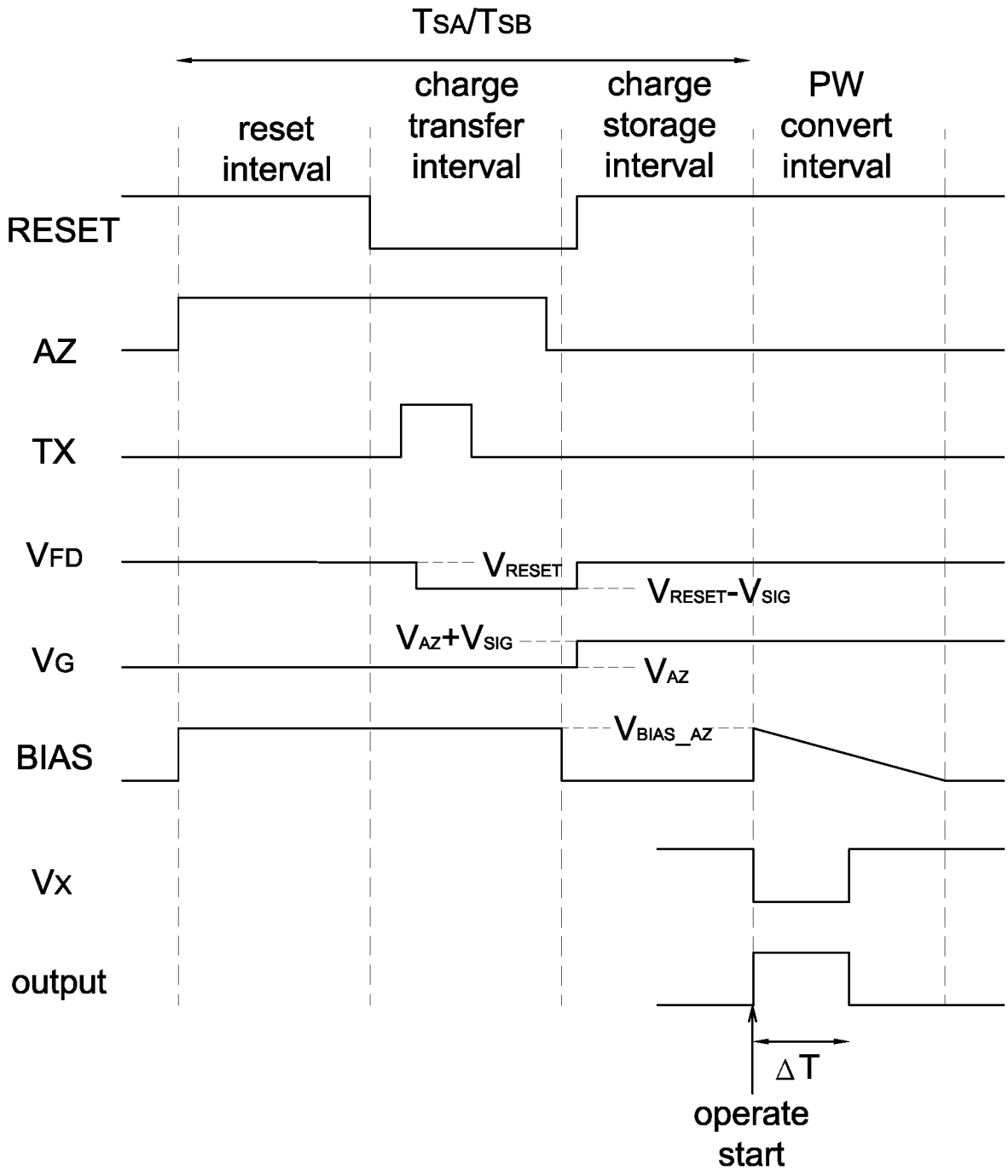

TSA/TSB
reset interval
charge transfer interval
charge storage interval
PW convert interval
RESET
AZ
TX
VFD
VRESET
VRESET-VSIG
VG
VAZ+VSIG
VAZ
BIAS
VBIAS_AZ
Vx
output
ΔT
operate start

FIG. 4A

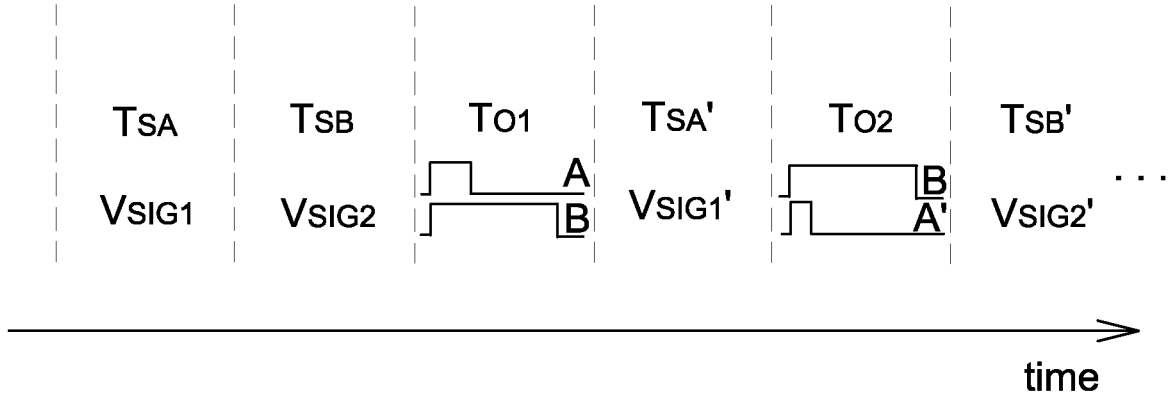

TSA
TSB
TO1
TSA'
TO2
TSB'
VSIG1
VSIG2
A
B
VSIG1'
B
A'
VSIG2'
. . .
time

FIG. 4B

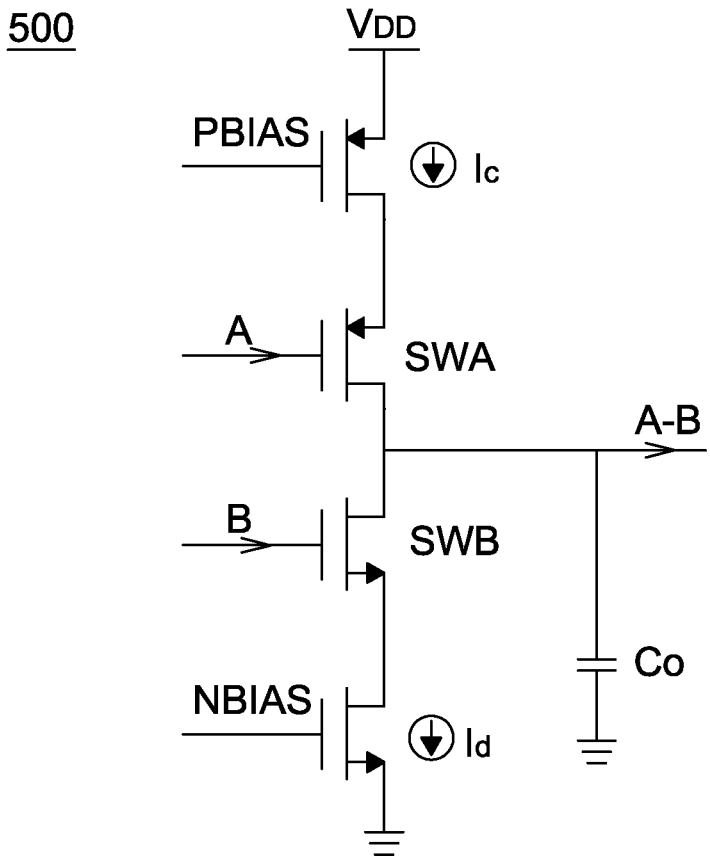

500
VDD
PBIAS
Ic
A
SWA
A-B
B
SWB
Co
NBIAS
Id

FIG. 5

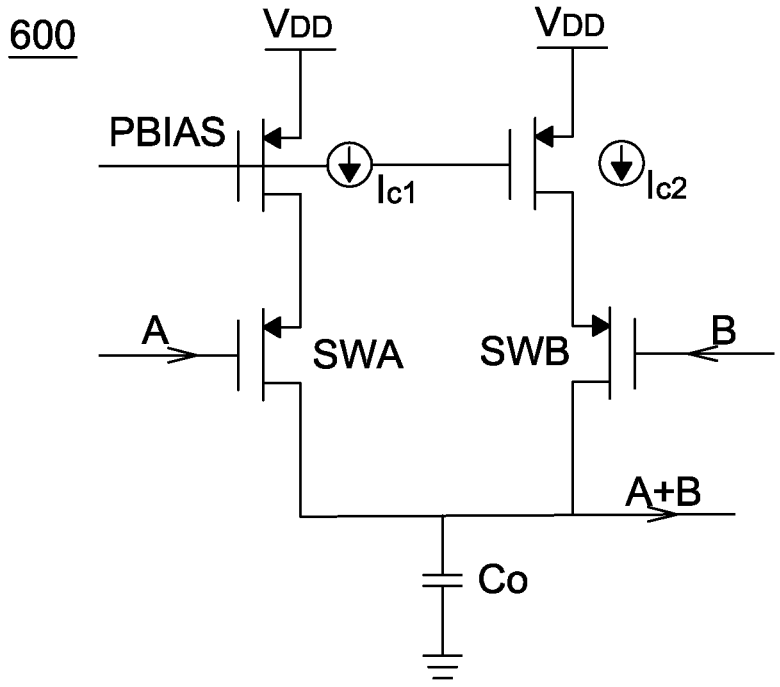

600
VDD
VDD
PBIAS
Ic1
Ic2
A
SWA
SWB
B
A+B
Co

FIG. 6

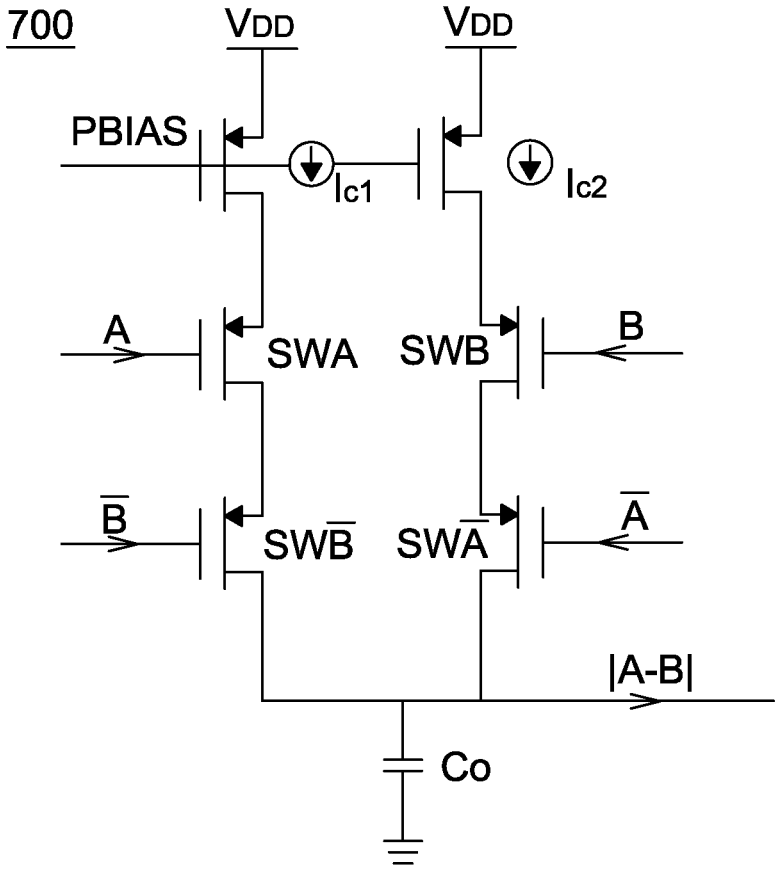

700
VDD
VDD
PBIAS
Ic1
Ic2
A
SWA
SWB
B
B̄
SWB̄
SWĀ
Ā
|A-B|
Co

FIG. 7

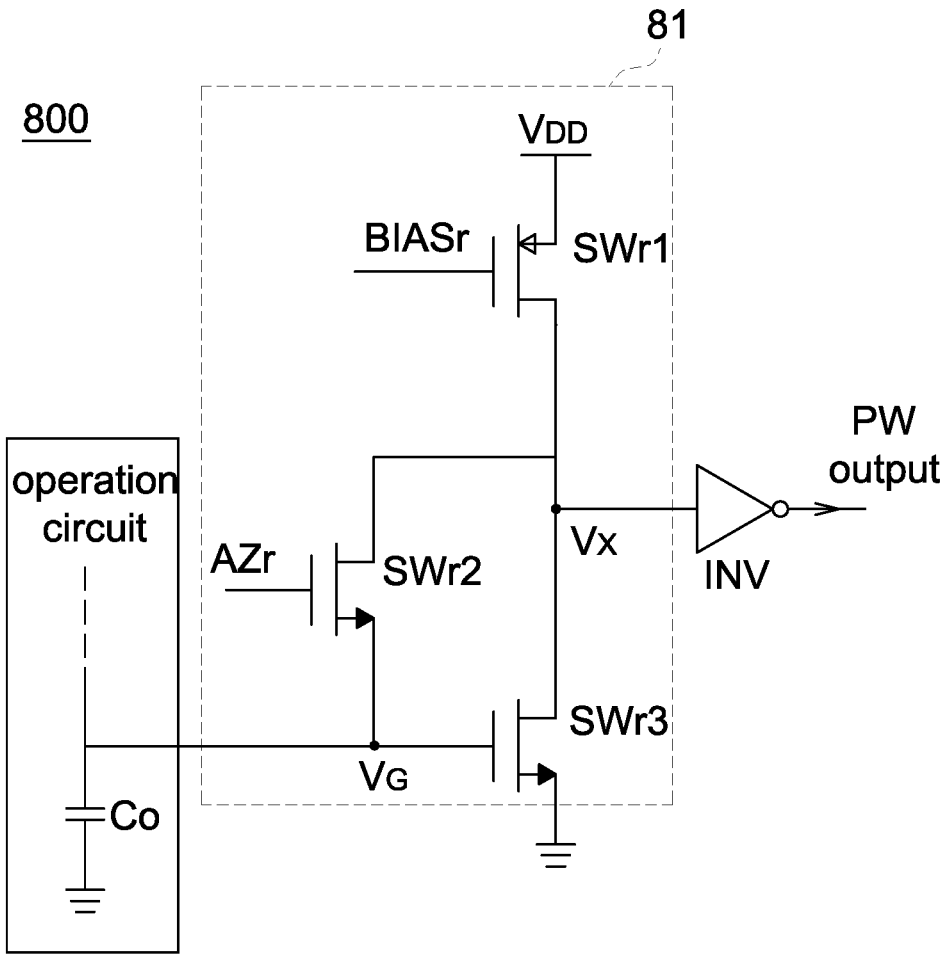

81
800
VDD
BIASr
SWr1
PW
output
operation
circuit
AZr
SWr2
Vx
INV
SWr3
VG
Co

FIG. 8

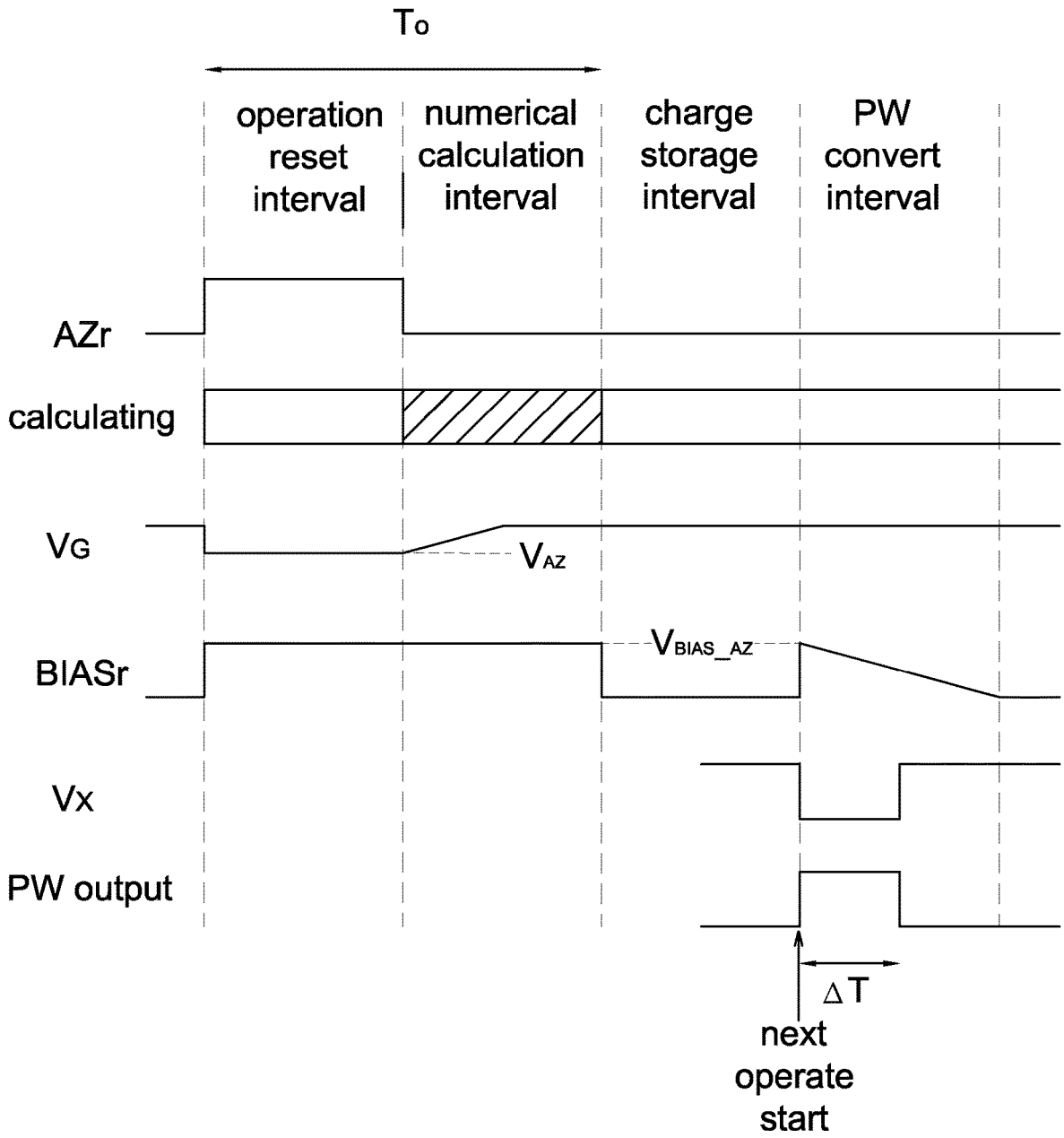

To
operation reset interval
numerical calculation interval
charge storage interval
PW convert interval
AZr
calculating
VG
VAZ
BIASr
VBIAS_AZ
Vx
PW output
ΔT
next operate start

FIG. 9

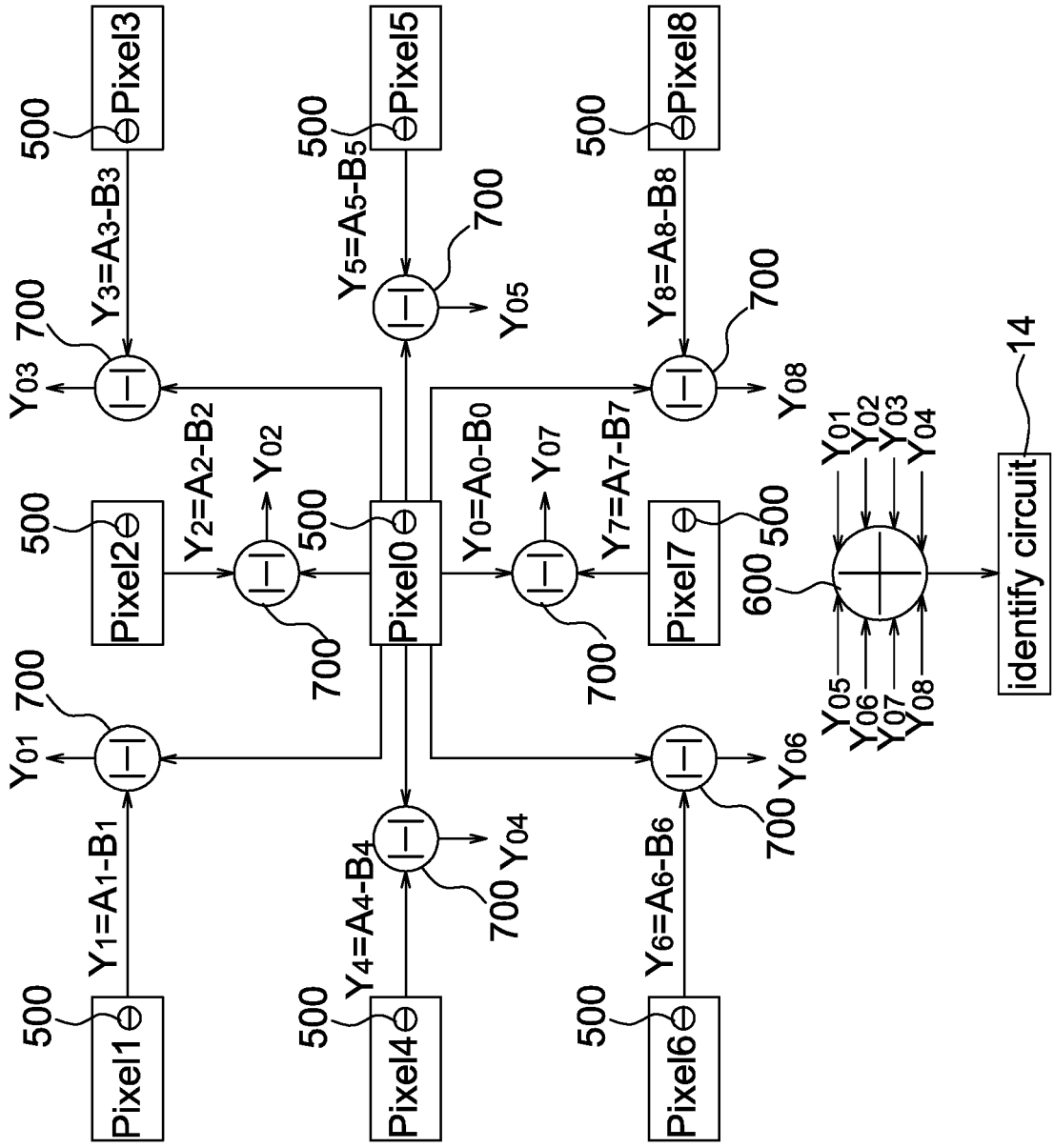

Pixel1
Pixel2
Pixel3
Pixel4
Pixel5
Pixel6
Pixel7
Pixel8
Pixel0
500
700
600
14
identify circuit
Y1=A1-B1
Y2=A2-B2
Y3=A3-B3
Y4=A4-B4
Y5=A5-B5
Y6=A6-B6
Y7=A7-B7
Y8=A8-B8
Y0=A0-B0
Y01
Y02
Y03
Y04
Y05
Y06
Y07
Y08

FIG. 10

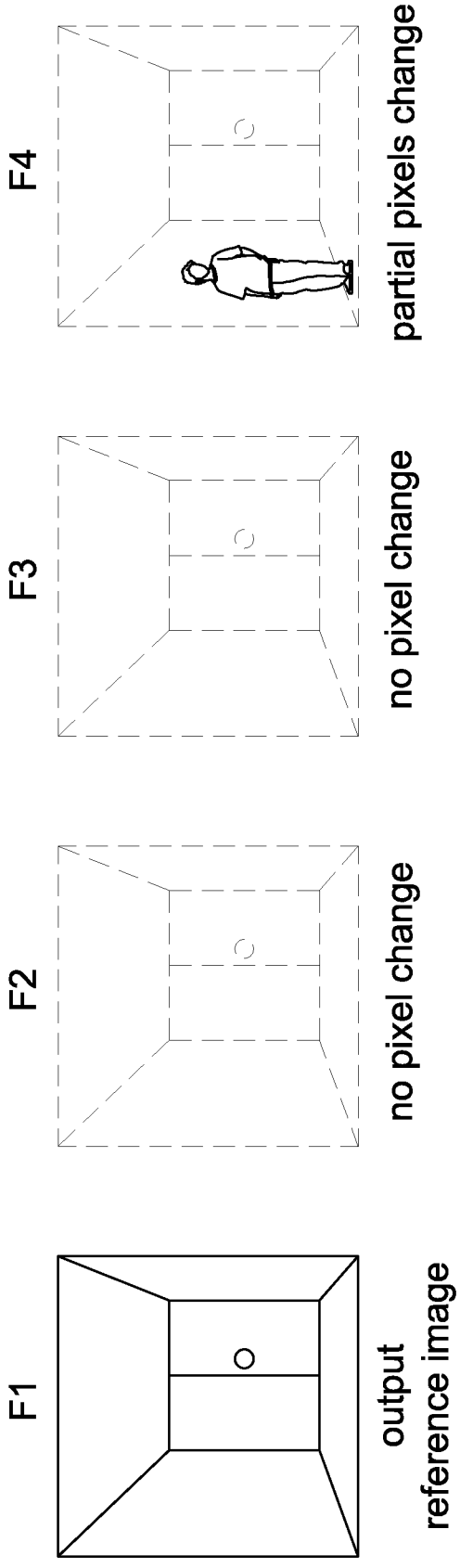

F4
partial pixels change
F3
no pixel change
F2
no pixel change
F1
output
reference image

FIG. 11

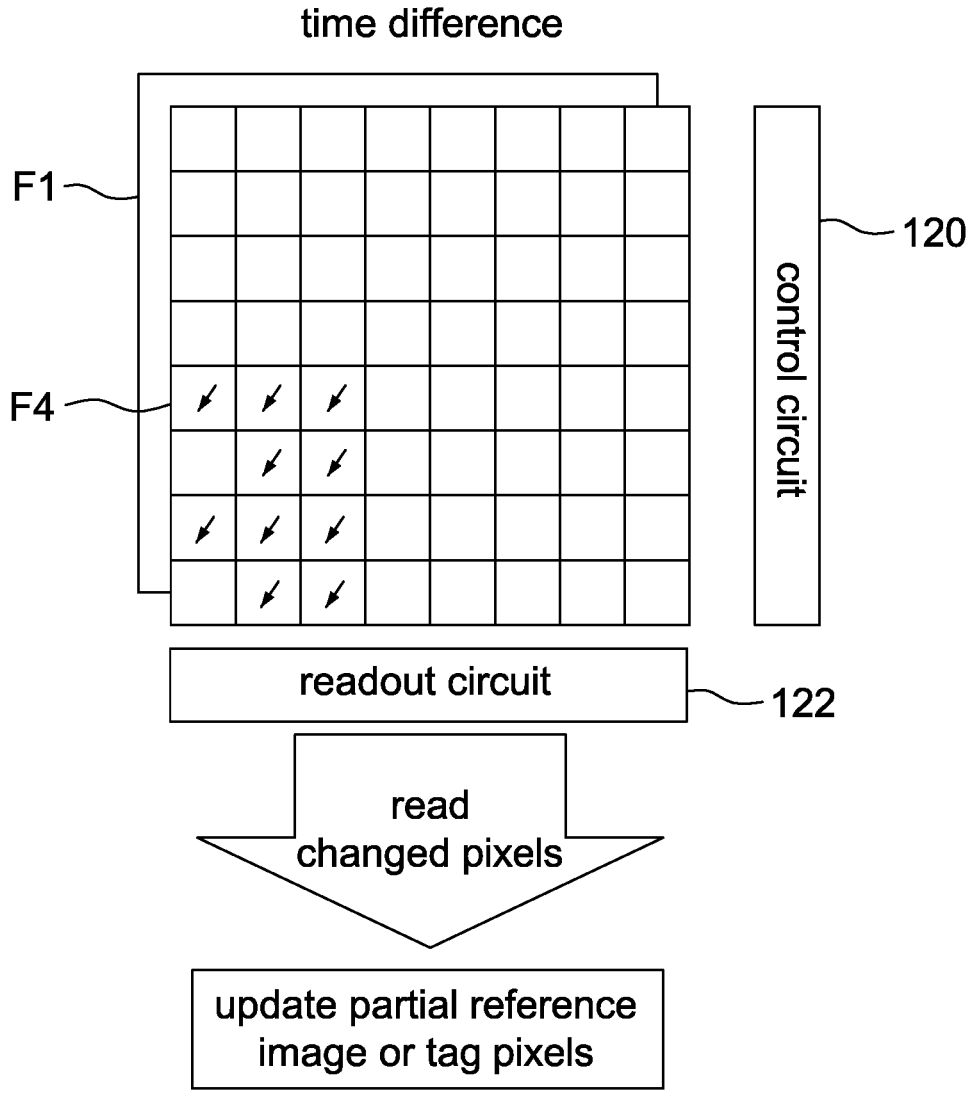

time difference
F1
F4
120
control circuit
readout circuit
122
read
changed pixels
update partial reference
image or tag pixels

FIG. 12

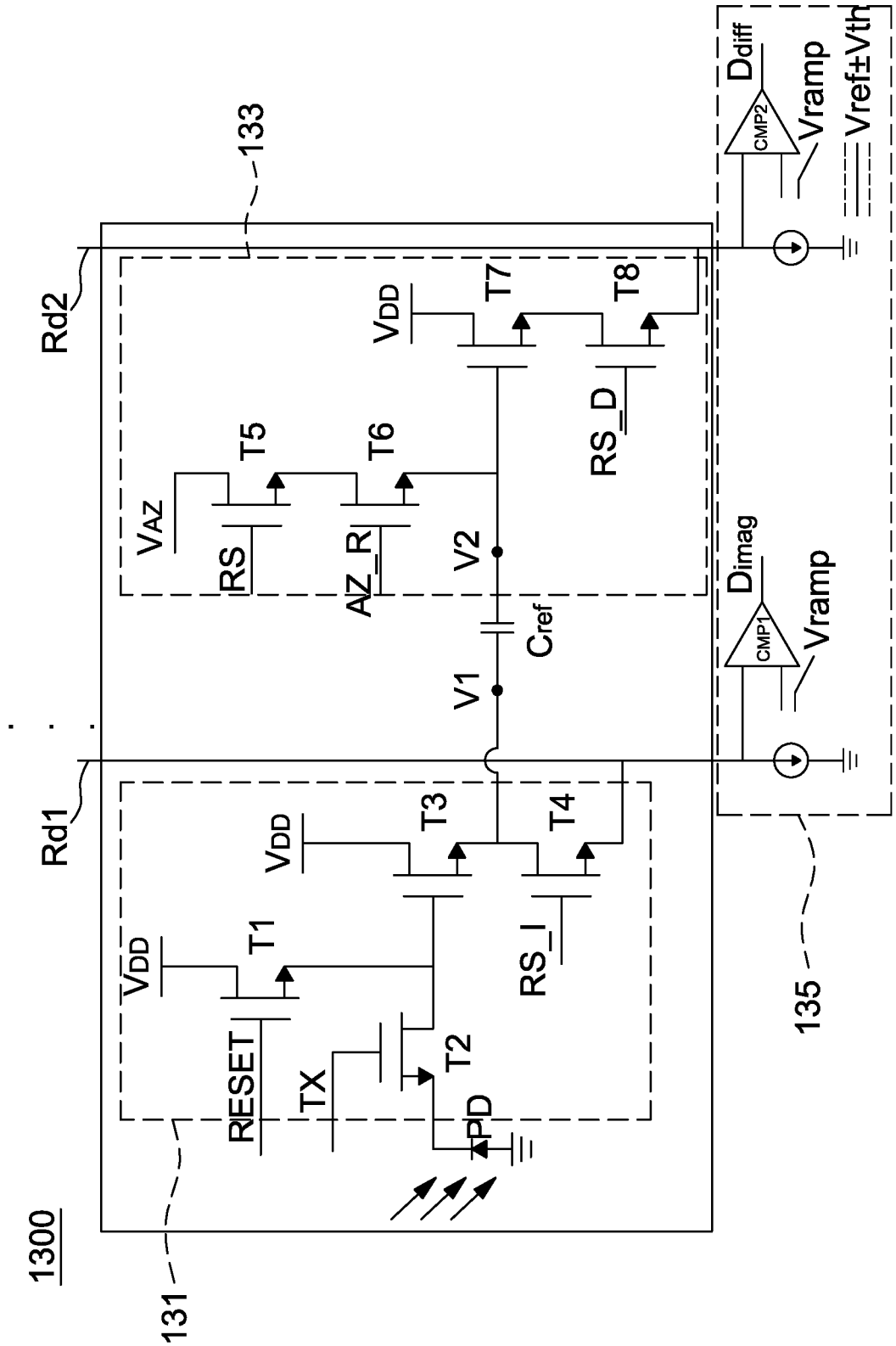

1300
131
133
135
Rd1
Rd2
VDD
T1
T2
T3
T4
T5
T6
T7
T8
RESET
TX
PD
RS_I
RS_D
RS
AZ_R
VAZ
V1
V2
Cref
Dimag
Ddiff
CMP1
CMP2
Vramp
Vramp
Vref±Vth

FIG. 13

	exposure	reset 1st node	charge transfer	read image data
transistorT1	Off	On	Off	Off
transistorT2	Off	Off	On	Off
transistorT4	Off	On	On	On
transistorT5	Off	Off	Off	Off
transistorT6	Off	Off	Off	Off
transistorT8	Off	Off	Off	Off
node V1	-	Vr	Vs	Vs
node V2	-	-	-	-

FIG. 14

	exposure & 1st charge transfer	reset 2nd node	exposure & 2nd charge transfer	read difference data
transistorT1	Off	Off	Off	Off
transistorT2	On	Off	On	Off
transistorT4	On	On	On	On
transistorT5	Off	On	Off	Off
transistorT6	Off	On	Off	Off
transistorT8	Off	On	Off	On
node V1	Vold	Vold	Vold + ΔV	Vold + ΔV
node V2	-	Vaz	Vaz + ΔV	Vaz + ΔV

FIG. 15

	exposure&2nd charge transfer	read difference data	reset 2nd node
T1	Off	Off	Off
T2	On	Off	Off
T4	On	On	On
T5	Off	Off	On
T6	Off	Off	On
T8	Off	On	On
V1	Vold + ΔV	Vold + ΔV	new Vold
V2	Vaz + ΔV	Vaz + ΔV	Vaz

FIG. 16A

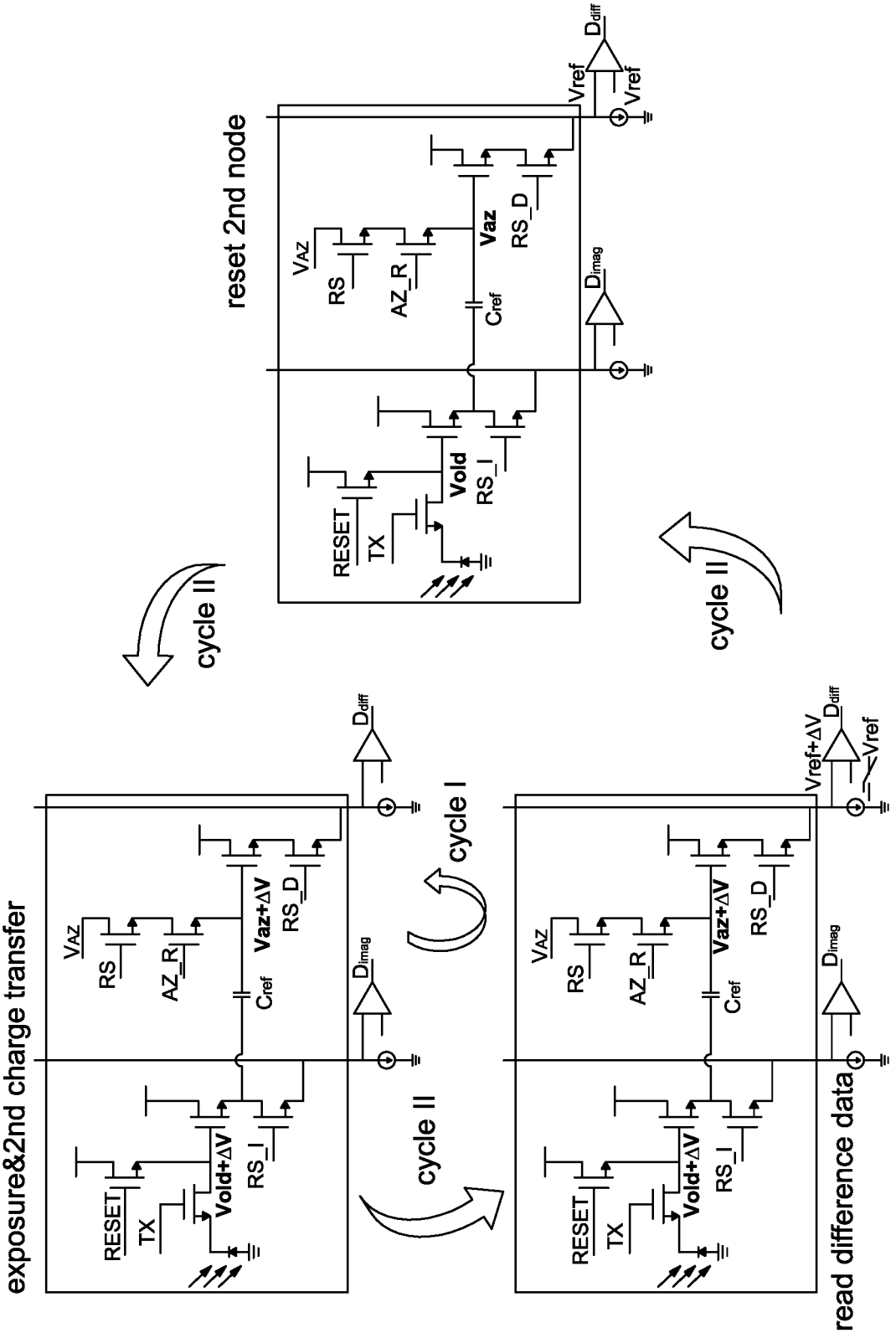

exposure&2nd charge transfer
reset 2nd node
read difference data
cycle I
cycle II
cycle II
cycle II
RESET
TX
Vold+ΔV
RS_I
VAZ
RS
AZ_R
Cref
Vaz+ΔV
RS_D
Dimag
Ddiff
Vref
Vref+ΔV
Vaz
Vold

FIG. 16B

	exposure	reset 1st node	charge transfer&check variation	read image data	reset 2nd node
T1	Off	On	Off	Off	Off
T2	Off	Off	Off	Off	Off
T4	Off	On	On	On	On
T5	Off	Off	Off	Off	On
T6	Off	Off	Off	Off	On
T8	Off	Off	On	Off	On
V1	-	Vr	Vold + ΔV	Vs	new Vold
V2	-	-	Vaz + ΔV	-	Vaz

FIG. 17A

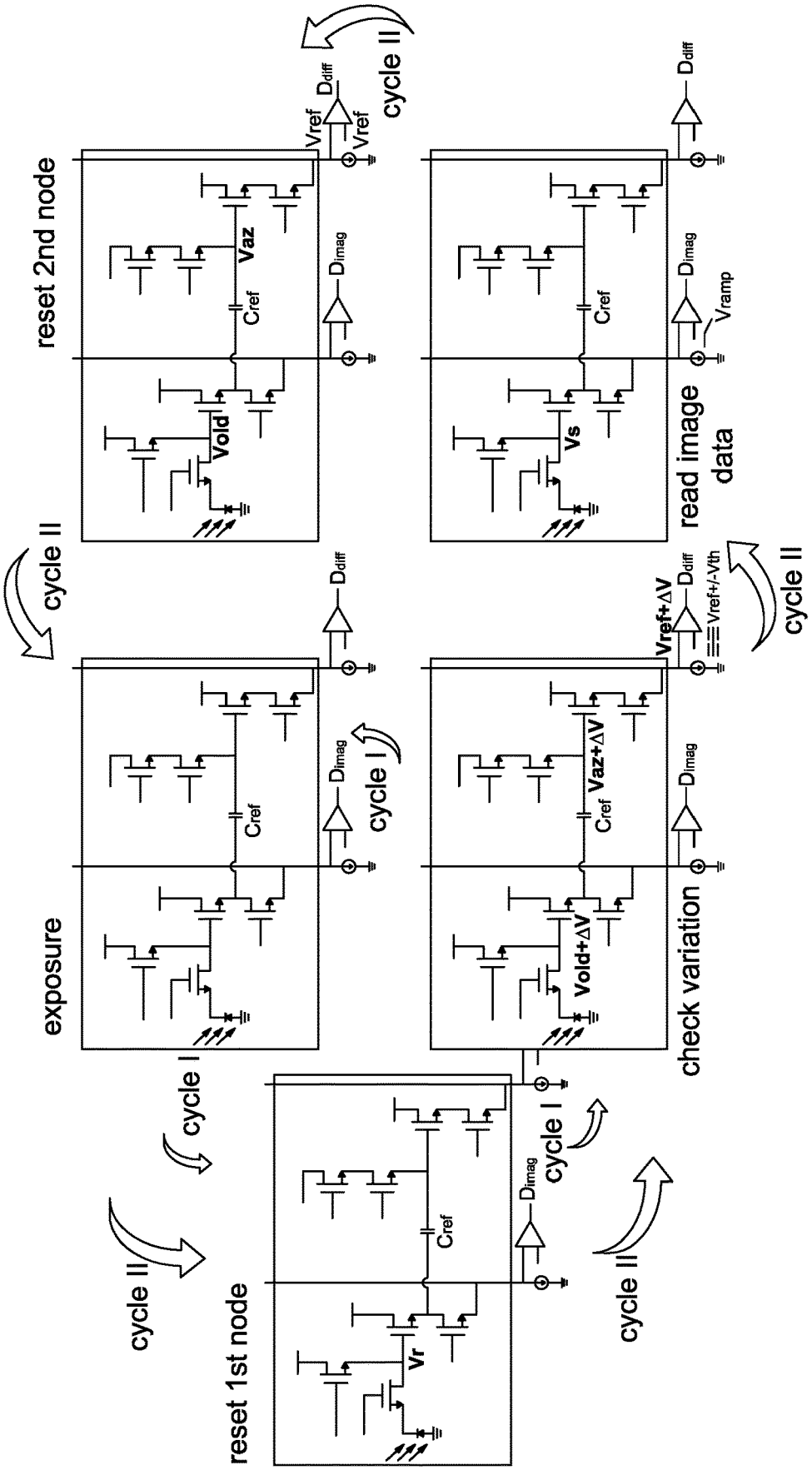

reset 2nd node
cycle II
Vref
Ddiff
Vref
Vaz
Cref
Dimag
Void
Vs
Vramp
read image data
exposure
cycle I
Vref+ΔV
Vref+/-Vth
Vaz+ΔV
Void+ΔV
check variation
reset 1st node
Vr

FIG. 17B

	exposure	charge transfer&check variation	read image data	reset 2nd node	reset 1st node
T1	Off	Off	Off	Off	On
T2	Off	Off	Off	Off	Off
T4	Off	On	On	On	On
T5	Off	Off	Off	On	Off
T6	Off	Off	Off	On	Off
T8	Off	On	Off	On	Off
V1	-	Vold + ΔV	Vs	new Vold	Vr
V2	-	Vaz + ΔV	-	Vaz	-

FIG. 18A

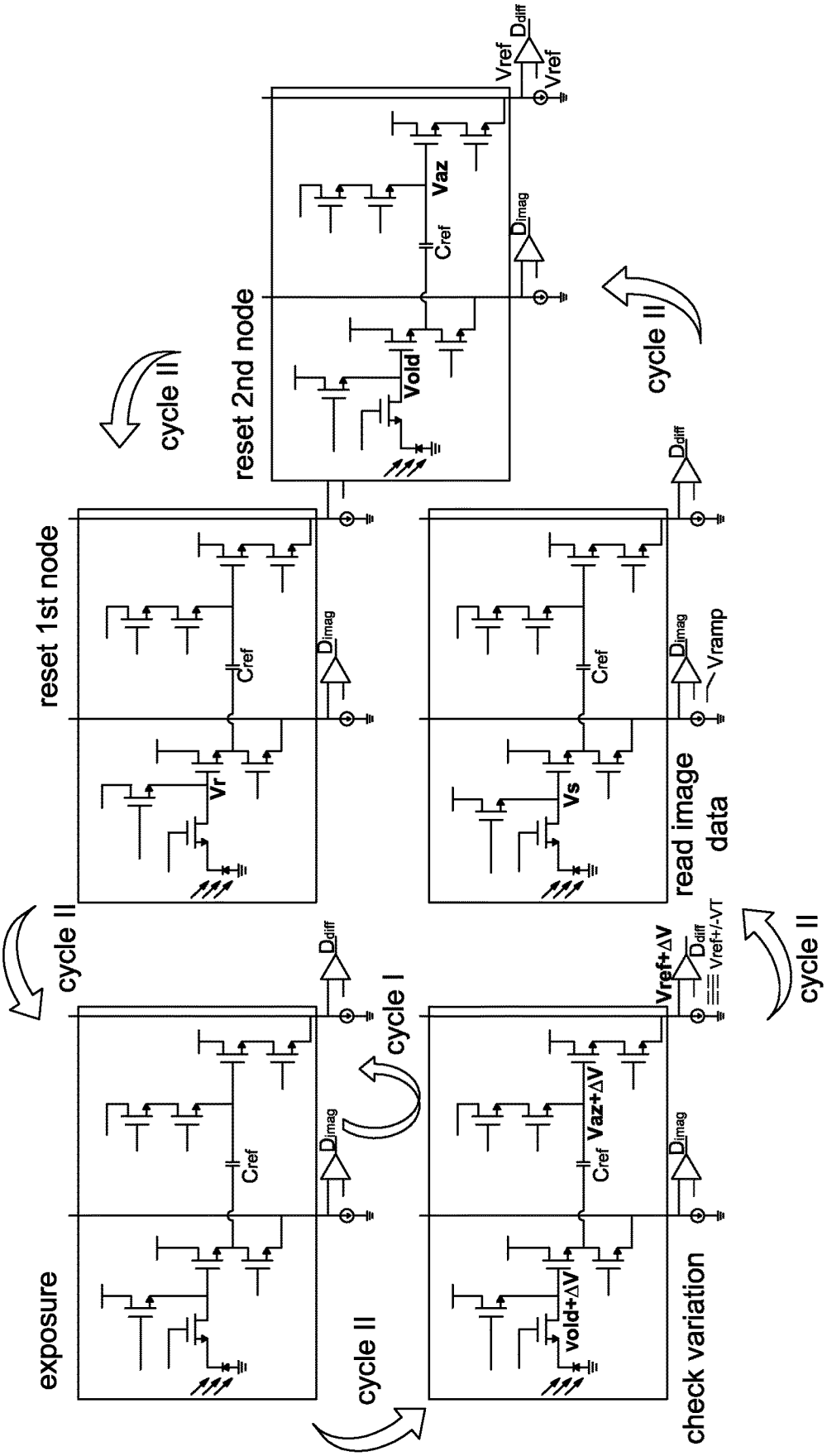

reset 2nd node
Vaz
Cref
Dimag
Vref
Ddiff
Vold
cycle II
reset 1st node
Vr
Vs
Vramp
read image data
Vref+ΔV
Vref+/-VT
Vaz+ΔV
Vold+ΔV
cycle I
exposure
check variation

FIG. 18B

PIXEL CIRCUIT OUTPUTTING TIME DIFFERENCE DATA AND IMAGE DATA, AND OPERATING METHOD THEREOF

CROSS REFERENCE TO RELATED APPLICATION

The present application is a continuation application of U.S. patent application Ser. No. 17/401,554 filed on, Aug. 13, 2021, which is a continuation-in-part application of U.S. patent application Ser. No. 17/009,417 filed on, Sep. 1, 2020, the disclosure of which is hereby incorporated by reference herein in its entirety.

To the extent any amendments, characterizations, or other assertions previously made (in this or in any related patent applications or patents, including any parent, sibling, or child) with respect to any art, prior or otherwise, could be construed as a disclaimer of any subject matter supported by the present disclosure of this application, Applicant hereby rescinds and retracts such disclaimer. Applicant also respectfully submits that any prior art previously considered in any related patent applications or patents, including any parent, sibling, or child, may need to be re-visited.

BACKGROUND

1. Field of the Disclosure

This disclosure generally relates to a pixel structure and, more particularly, to a pixel circuit capable of selecting to output time difference data and image data, and an operating method of a pixel array including the same.

2. Description of the Related Art

Nowadays, the optical sensor outputs voltage values to be converted to a digital image frame by an analog-to-digital converter, and then a processor of the optical sensor performs the following operation using the digital image frame, e.g., calculating displacement or performing motion detection.

However, in an optical sensor performing the operation in a digital backend thereof, the digital backend generally needs frame buffers to store the whole digital image frame. Generally, the optical sensor needs two frame buffers to store pixel data.

Accordingly, it is necessary to provide a pixel structure that performs various operations on pixel data at analog phase.

SUMMARY

The present disclosure provides a pixel circuit that represents detected light intensity using a pulse width, and performs the pixel-wise operation, including intra-pixel and inter-pixel operations, using pulse width signals.

The present disclosure provides a pixel structure including a photodiode, a storage capacitor, an image circuit, a difference circuit a first comparator, and a second comparator. The photodiode is configured to generate light energy. The storage capacitor has a first end and a second end. The image circuit is connected to the first end of the storage capacitor, and configured to output image data associated with the light energy generated in a first interval by the photodiode. The difference circuit is connected to the second end of the storage capacitor, and configured to output time difference data associated with a variation of the light energy generated between the first interval and a second interval by the photodiode. The first comparator is connected to the image circuit, and configured to output image data. The second comparator is connected to the difference circuit, and configured to output time difference data or a state-change signal.

The present disclosure further provides an operating method of a pixel circuit including the steps of: transferring a signal voltage, associated with the light energy generated in the first interval by the photodiode, to the first end of the storage capacitor; resetting the second end of the storage capacitor to a reset voltage and holding the signal voltage at the first end of the storage capacitor in a resetting interval; transferring a variation voltage, associated with the light energy generated in the second interval by the photodiode, to the first end of the storage capacitor to be added to the signal voltage to form the image data and coupled to the reset voltage to form the time difference data; outputting a state-change signal via the second comparator to read the image data via the first comparator upon the time difference data exceeding a predetermined voltage range; and not outputting the state-change signal and not reading the image data upon the time difference data not exceeding the predetermined voltage range.

The temporal circuit of the present disclosure is used to store detected light energy of different time intervals and to output detection signals of different pulse widths, wherein the pulse width is positively related to the detected light energy.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects, advantages, and novel features of the present disclosure will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings.

FIG. **1** is a schematic block diagram of a pixel structure of an optical sensor according to one embodiment of the present disclosure.

FIG. **2** is a circuit diagram of a pixel circuit according to one embodiment of the present disclosure.

FIG. **3** is a circuit diagram of a temporal circuit of a pixel circuit according to one embodiment of the present disclosure.

FIG. **4**A is an operational timing diagram of the temporal circuit in FIG. **3**.

FIG. **4**B is an operational timing diagram of the pixel circuit in FIG. **2**.

FIG. **5** is a circuit diagram of a subtraction circuit of a pixel circuit according to one embodiment of the present disclosure.

FIG. **6** is a circuit diagram of an addition circuit of a pixel circuit according to one embodiment of the present disclosure.

FIG. **7** is a circuit diagram of an absolute difference circuit of a pixel circuit according to one embodiment of the present disclosure.

FIG. **8** is a circuit diagram of a recursive circuit of a pixel circuit according to one embodiment of the present disclosure.

FIG. **9** is an operational timing diagram of the recursive circuit in FIG. **8**.

FIG. **10** is a schematic diagram of one application of a pixel circuit according to one embodiment of the present disclosure.

FIG. **11** is a schematic diagram of capturing image frames using an optical sensor including pixel circuits of the present disclosure.

FIG. **12** is a schematic diagram of a part of pixels of an image frame captured by an optical sensor including pixel circuits of the present disclosure having a light energy variation.

FIG. **13** is a circuit diagram of a pixel circuit according to one embodiment of the present disclosure.

FIG. **14** is a schematic diagram of the status of every element when the pixel circuit of the present disclosure outputs image data.

FIG. **15** is a schematic diagram of the status of every element when the pixel circuit of the present disclosure outputs time difference data.

FIGS. **16**A and **16**B are operational schematic diagrams of the pixel circuit of the present disclosure outputting time difference data.

FIGS. **17**A and **17**B are operational schematic diagrams of the pixel circuit of the present disclosure performing the event detection.

FIGS. **18**A and **18**B are other operational schematic diagrams of the pixel circuit of the present disclosure performing the event detection.

DETAILED DESCRIPTION OF THE EMBODIMENT

It should be noted that, wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

The present disclosure is related to a pixel circuit that performs pixel-wise analog operation. Every pixel outputs a detection signal having a pulse width corresponding to detected light energy. An operation circuit is used to perform the analog operation on the pulse width (PW) signals. The voltage value after the analog operation is further converted to a PW signal using a voltage-temporal conversion circuit at first and then a next analog operation is performed by the same or by another operation circuit. In this way, all data operation is accomplished in the analog phase without being converted to digital data at first.

Referring to FIG. **1**, it is a schematic block diagram of a pixel structure of an optical sensor (e.g., CMOS image sensor) according to one embodiment of the present disclosure. The pixel structure includes a pixel circuit **10** and an operation circuit **12**. The pixel circuit **10** is used to output detection signals of different time intervals, e.g., signals A and B in FIG. **1** indicating different detection signals detected within different time intervals. In the present disclosure, the detection signals A and B respectively indicate magnitude of light energy detected by the pixel circuit **10** using pulse widths T**1** and T**2**, wherein when the detected light energy is larger, the pulse width of the corresponding detection signals A or B is longer.

The operation circuit **12** includes any circuit used to perform the operation between signals, e.g., described by a subtraction circuit in FIG. **5**, an addition circuit in FIG. **6** and an absolute difference circuit in FIG. **7** herein, but not limited thereto. In a pixel array including multiple pixels, the operation circuit **12** is arranged inside each pixel to process data in the pixel or arranged between pixels to process data between pixels.

In some aspects, the pixel structure further includes an identify circuit **14**. The identify circuit **14** includes, for example, a comparator for comparing the output result of the operation circuit **21** with a predetermined threshold so as to identify an operating state of a device adopting the pixel structure of the present disclosure. For example, when the pixel structure of the present disclosure is adapted to a mouse device, the identify circuit **14** is used to identify whether the mouse device is lifted up by a user. The output result of the operation circuit **12** indicates a brightness variation. When the identify circuit **14** identifies that the brightness variation is larger than or smaller than a brightness threshold, the mouse device is identified to be lifted by the user. The identify circuit **14** then outputs a control signal to perform corresponding controls, e.g., turning off the light source and/or not outputting displacement signals, but not limited to.

Please referring to FIG. **2**, it is a circuit diagram of a pixel circuit **200** according to one embodiment of the present disclosure. The pixel circuit **200** is used to output pulse width (PW) signals A and B, i.e. detection signals. The pixel circuit **200** includes a photodiode PD, a transfer transistor SWt, a reset transistor SWrst, a first temporal circuit **2***a* and a second temporal circuit **2***b* all connected to a node V_{FD}.

The photodiode PD is used to generate light energy according to the light L being received. The light energy is respectively stored in the first temporal circuit **2***a* and the second temporal circuit **2***b* within different time intervals (e.g., controlled by a control signal TX). In the present disclosure, in addition to storing light energy detected within different time intervals, the first temporal circuit **2***a* and the second temporal circuit **2***b* further respectively convert the stored light energy into detection signals A and B having corresponding pulse widths (e.g., T**1** and T**2**) for the operation circuit **12** to perform analog operation. The first temporal circuit **2***a* and the second temporal circuit **2***b* have identical circuit arrangement only being operated within different time intervals.

The first temporal circuit **2***a* stores first light energy (e.g., referring to V_{SIG1} shown in FIG. **4**B), generated by the photodiode PD within a first interval (e.g., referring to T_{SA} shown in FIG. **4**B), and outputs a first detection signal A having a first pulse width T**1** according to the first light energy V_{SIG1} within an operation interval (e.g., referring to T_{O1} shown in FIG. **4**B).

The second temporal circuit **2***b* stores second light energy (e.g., referring to V_{SIG2} shown in FIG. **4**B) generated by the photodiode PD within a second interval (e.g., referring to T_{SB} shown in FIG. **4**B), and outputs a second detection signal B having a second pulse width T**2** according to the second light energy V_{SIG2} within the operation interval T_{O1}. It is appreciated that lengths of T**1** and T**2** in drawings are only intended to illustrate but not to limit the present disclosure.

The reset transistor SWrst is coupled between a voltage source V_{DD} and the node V_{FD}, and used to reset the first temporal circuit **2***a* in the first interval T_{SA} and reset the second temporal circuit **2***b* in the second interval T_{SB}.

The transfer transistor SWt is coupled between the photodiode PD and the node V_{FD}, and used to transfer the first light energy V_{SIG1} to be stored into the first temporal circuit **2***a* in the first interval T_{SA} and transfer the second light energy V_{SIG2} to be stored into the second temporal circuit **2***b* in the second interval T_{SB}. In this way, the pixel circuit **200** stores detected light energy of different time intervals to indicate the variation of detected light with time.

In some aspects, the first temporal circuit **2***a* further includes a first inverter INV**1** coupled between an output terminal of the first temporal circuit **2***a* and the operation circuit **12**, and the first inverter INV**1** is used to invert a phase of the first detection signal A; the second temporal

circuit **2***b* further includes a second inverter INV**2** coupled between an output terminal of the second temporal circuit **2***b* and the operation circuit **12**, and the second inverter INV**2** is used to invert a phase of the second detection signal B. In other aspects, the first inverter INV**1** and the second inverter INV**2** are arranged in the operation circuit **12** instead of being arranged in the first temporal circuit **2***a* and the second temporal circuit **2***b*.

Please referring to FIGS. **3** and **4**A, FIG. **3** is a circuit diagram of the temporal circuit (e.g., **2***a* and **2***b*) of a pixel circuit according to one embodiment of the present disclosure; and FIG. **4**A is an operational timing diagram of the temporal circuit **2***a*/**2***b* in FIG. **3**. It should be mentioned that although FIG. **2** shows that a single pixel circuit includes two temporal circuits, but the present disclosure is not limited thereto. In other aspects, each pixel circuit includes a single temporal circuit as shown in FIG. **3** to output a PW signal A or B.

In the present disclosure, operation of the temporal circuits **2***a* and **2***b* in FIG. **2** is described using FIGS. **3** and **4**A.

The temporal circuits **2***a* and **2***b* respectively include a storage capacitor C, a first transistor SW**1**, a second transistor SW**2** and a third transistor SW**3**. The storage capacitors and the first to third transistors are indicated by different reference numerals in FIG. **2** to indicate belonging to different temporal circuits.

A first end of the storage capacitor C (shown as a first capacitor C**1** in the first temporal circuit **2***a* and as a second capacitor C**2** in the second temporal circuit **2***b*) is coupled to the reset transistor SWrst. The storage capacitor C is used to store light energy generated by the photodiode PD, e.g., the first light energy V_{SIG1} or the second light energy V_{SIG2}.

The first transistor SW**1** (shown as SWa**1** in the first temporal circuit **2***a* and as SWb**1** in the second temporal circuit **2***b*) is coupled between the voltage source V_{DD} and a node Vx, and is controlled by a control signal BIAS (shown as BIAS**1** in the first temporal circuit **2***a* and as BIAS**2** in the second temporal circuit **2***b*) to convert the stored light energy to a detection signal, e.g., the first detection signal A or the second detection signal B.

The second transistor SW**2** (shown as SWa**2** in the first temporal circuit **2***a* and as SWb**2** in the second temporal circuit **2***b*) is coupled between the storage capacitor C and the first transistor SW**1**, and controlled by a control signal AZ (shown as AZ**1** in the first temporal circuit **2***a* and as AZ**2** in the second temporal circuit **2***b*). In the first interval T_{SA}, the second transistor SWb**2** is not conducted to avoid changing the stored energy in the second capacitor C**2**; and in the second interval T_{SB}, the first transistor SWa**2** is not conducted to avoid changing the stored energy in the first capacitor C**1**.

The third transistor SW**3** (shown as SWa**3** in the first temporal circuit **2***a* and as SWb**3** in the second temporal circuit **2***b*) is coupled between a second end of the storage capacitor C and a ground voltage.

Please referring to FIG. **4**A again, it shows that operation of the temporal circuit **2***a*/**2***b* includes a reset interval, a charge transfer interval, a charge storage interval and a pulse width (PW) convert interval. In the reset interval, control signals BIAS, RESET and AZ are respectively at a high voltage level to reset charges on the storage capacitor C, e.g., a voltage of the node V_{FD} being reset to V_{RESET} (e.g., equal to V_{DD}) and a voltage of the node V_G being reset to V_{AZ}. In the charge transfer interval, the control signal RESET is changed to a low voltage level, and when the control signal TX is changed to a high voltage level, the light energy V_{SIG} detected by the photodiode PD is transferred to the node V_{FD} via the transfer transistor SWt to cause the voltage thereon to decrease to $V_{RESET}-V_{SIG}$, wherein V_{SIG} indicates the detected light energy. In the charge storage interval, the control signal RESET is changed to the high voltage level again and the control signals BIAS and AZ are changed to low voltage levels to store the light energy V_{SIG} to the node V_G to cause the voltage thereon to increase to $V_{AZ}+V_{SIG}$. Meanwhile, if the control signal AZ is kept at the low voltage level to turn off the second transistor SW**2**, charges stored in the storage capacitor C are substantially kept constant.

In FIG. **4**A, the reset interval, the charge transfer interval and the charge storage interval as a whole is used as an energy storage interval T_{SA} of the first temporal circuit **2***a* or an energy storage interval T_{SB} of the second temporal circuit **2***b*. Before the operation circuit **12** starts to operate, the first temporal circuit **2***a* and the second temporal circuit **2***b* sequentially store light energy detected by the photodiode PD. As shown in FIG. **4**A, till the PW convert interval is entered after the operation starts, the first light energy V_{SIG1} in the first temporal circuit **2***a* is converted to the first detection signal A and the second light energy V_{SIG2} in the second temporal circuit **2***b* is converted to the second detection signal B.

In the PW convert interval, the control signal BIAS uses a ramp signal having the voltage level decreasing with time. When the control signal BIAS starts at a high voltage level (e.g., V_{BIAS_AZ}), the current I**1** flowing through the first transistor SW**1** is smaller than the current I**3** flowing through the third transistor SW**3** to cause an output voltage of Vx to have a low voltage level. With the level decreasing of the control signal BIAS, the current I**1** is increasing correspondingly, and when the current I**1** is substantially identical to the current I**3**, the output voltage of Vx changes to a high voltage level to form a negative PW signal. After the output voltage of Vx passes an inverter INV, a positive PW signal is generated as shown in FIG. **4**A, wherein a pulse width ΔT is positively related to the light energy V_{SIG}. In this way, the temporal circuits **2***a* and **2***b* of the present disclosure convert light energy detected by the photodiode PD to a timing signal to be operated by the operation circuit **12**.

Please referring to FIG. **4**B, it is an operational timing diagram of the pixel circuit **200** in FIG. **2**. The first temporal circuit **2***a* stores first light energy V_{SIG1} in the first capacitor C**1** in the first interval (e.g., the energy storage interval T_{SA}) using the operation of FIG. **4**A. The second temporal circuit **2***b* stores second light energy V_{SIG2} in the second capacitor C**2** in the second interval (e.g., the energy storage interval T_{SB}) using the operation of FIG. **4**A. Next, in the first operation interval T_{O1}, the first temporal circuit **2***a* uses a ramp signal having the voltage level decreasing with time as the control signal BIAS**1** to convert the first light energy V_{SIG1} into a first detection signal A; meanwhile, the second temporal circuit **2***b* uses a ramp signal having the voltage level decreasing with time as the control signal BIAS**2** to convert the second light energy V_{SIG2} into a second detection signal B. Preferably, the ramp signals BIAS**1** and BIAS**2** are substantially in-phase to generate detection signals A and B substantially at the same time, but not limited thereto. It is possible that detection signals A and B are generated sequentially depending on the operation of the operation circuit **12**. The operation circuit **12** performs the numerical calculation on the first detection signal A and the second detection signal B in the first operation interval T_{O1}, e.g., the summation, subtraction and absolute differencing given in the present disclosure, but the present disclosure is not limited to these operations.

As shown in FIG. **4**B, in the first operation interval T_{O1}, the first interval T_{SA} for storing the first light energy V_{SIG1} is prior to the second interval T_{SB} for storing the second light energy V_{SIG2}.

In one aspect, after the first operation interval T_{O1} is over, the second temporal circuit **2***b* continuously holds the second light energy V_{SIG2}, but the first temporal circuit **2***a* stores a next first light energy V_{SIG1}' in the first capacitor C**1** in a next energy storage interval T_{SA}' also using the operation of FIG. **4**A. Next, in a second operation interval T_{O2}, the first temporal circuit **2***a* uses a ramp signal having the voltage level decreasing with time as the control signal BIAS**1** to convert the first light energy V_{SIG1}' into a first detection signal A'; meanwhile, the second temporal circuit **2***b* uses a ramp signal having the voltage level decreasing with time as the control signal BIAS**2** to convert the second light energy V_{SIG2} into a second detection signal B, which is substantially identical to that generated in the first operation interval T_{O1}. The operation circuit **12** performs the numerical calculation on the first detection signal A' and the second detection signal B in the second operation interval T_{O2}. In the second operation interval T_{O2}, the first interval T_{SA}' for storing the first light energy V_{SIG1}' is behind the second interval T_{SB} for storing the second light energy V_{SIG2}.

In the next energy storage interval, the first light energy V_{SIG1}' in the first temporal circuit **2***a* is maintained, but the second light energy in the second temporal circuit **2***b* is updated to V_{SIG2}'. By alternatively updating the light energy stored in the first temporal circuit **2***a* and the second temporal circuit **2***b* as shown in FIG. **4**B, it is possible to perform the numerical calculation on signals of different time intervals.

Please referring to FIG. **5**, it is a circuit diagram of a subtraction circuit **500** according to one embodiment of the present disclosure, which has two inputs respectively coupled to the first temporal circuit **2***a* and the second temporal circuit **2***b* to respectively receive a first detection signal A having a first pulse width T**1** and a second detection signal B having a second pulse width T**2**. The subtraction circuit **500** includes an operation capacitor Co and cascaded first operation transistor SWA and second operation transistor SWB, wherein the operation capacitor Co is connected between the first operation transistor SWA and the second operation transistor SWB. The first operation transistor SWA is used as a switch to control a charging interval of a first current Ic to charge the operation capacitor Co according to the first pulse width T**1**; and the second operation transistor SWB is used as a switch to control a discharging interval of a second current Id to discharge the operation capacitor Co according to the second pulse width T**2**, wherein the first current Ic is substantially identical to the second current Id. In this way, the subtraction circuit **500** performs the numerical calculation of A-B. It is appreciated that when the subtraction circuit **500** performs the numerical calculation of B-A, gates of the first operation transistor SWA and the second operation transistor SWB receive opposite input signals, e.g., implemented by using a switching device or a multiplexer.

Please referring to FIG. **6**, it is a circuit diagram of an addition circuit **600** according to one embodiment of the present disclosure, which has two inputs respectively coupled to the first temporal circuit **2***a* and the second temporal circuit **2***b* to respectively receive a first detection signal A having a first pulse width T**1** and a second detection signal B having a second pulse width T**2**. The addition circuit **600** includes an operation capacitor Co and a first operation transistor SWA and a second operation transistor SWB connected in parallel, wherein the operation capacitor Co is connected between the first operation transistor SWA and the second operation transistor SWB. The first operation transistor SWA is used as a switch to control a first charging interval of a first current Ic**1** to charge the operation capacitor Co according to the first pulse width T**1**; and the second operation transistor SWB is used as a switch to control a second charging interval of a second current Ic**2** to charge the operation capacitor Co according to the second pulse width T**2**, wherein the first current Ic**1** is substantially identical to the second current Ic**2**. In this way, the addition circuit **600** performs the numerical calculation of A+B.

Referring to FIG. **7**, it is a circuit diagram of an absolute difference circuit **700** according to one embodiment of the present disclosure, which has two input sets respectively coupled to the first temporal circuit **2***a* and the second temporal circuit **2***b* to respectively receive first detection signals A and Abar having a first pulse width T**1** and second detection signals B and Bbar having a second pulse width T**2**, wherein Abar and Bbar are generated from A and B using the inverter or vice versa. When the first pulse width T**1** is larger than the second pulse width T**2**, the first input set (including operation transistors SWA and SWBbar) receives the pulse width signals A and Bbar to control a first charging interval of a first current Ic**1** to charge the operation capacitor Co. When first pulse width T**1** is smaller than the second pulse width T**2**, the second input set (including operation transistors SWB and SWAbar) receives the pulse width signals B and Abar to control a second charging interval of a second current Ic**2** to charge the operation capacitor Co. In this way, the absolute difference circuit **700** performs the numerical calculation of |A−B|.

Although the current sources in FIGS. **5**-**7** are shown to be implemented by controlling a transistor using a control signal PBIAS, but the present disclosure is not limited thereto. Other current sources may be used.

Please referring to FIG. **8**, it is a circuit diagram of a recursive circuit **800** of a pixel circuit according to one embodiment of the present disclosure. The recursive circuit **800** is coupled to the operation circuit **12** and used to control the operation timing of the operation circuit **12** and convert the operation result (i.e. charges stored in the operation capacitor Co) into a pulse width signal again for the next operation, e.g., the PW output of the recursive circuit **800** being coupled to one signal input of the operation circuit **12** as the signal A or B in FIGS. **5** to **7**.

The recursive circuit **800** includes a first recursive transistor SWr**1**, a second recursive transistor SWr**2** and a third recursive transistor SWr**3**, which have identical connection as the first transistor SW**1**, the second transistor SW**2** and the third transistor SW**3** in FIG. **3**.

In FIG. **8**, the circuit in a dashed block **81** is referred to a voltage-temporal conversion circuit which is used to convert a voltage on the operation capacitor Co to a PW signal similar to A and B, wherein the operation capacitor Co in FIG. **8** is the operation capacitor Co in FIGS. **5** to **7**.

Please referring to FIG. **9** together, it is an operational timing diagram of the recursive circuit **800** in FIG. **8**. Before the operation capacitor Co starts to perform the numerical calculation on the detection signal A from the first temporal circuit **2***a* and the second detection signal B from the second temporal circuit **2***b*, the operation capacitor Co is reset at first. In the operation reset interval, control signals AZr and BIASr are respectively changed to a high voltage level for resetting a voltage of the operation capacitor Co to V_{AZ}. In this aspect, the second recursive transistor SWr**2** is used as an operation reset transistor so as to reset the voltage of the

operation capacitor Co in the operation reset interval. In the numerical calculation interval (e.g., slant-lines region), the control signal AZr is changed to a low voltage level and the operation result of the operation circuit **12** is stored in the operation capacitor Co to change a voltage thereon, wherein magnitude of the voltage change is corresponding to the operation result. Next, in the charge storage interval, the operation capacitor Co holds the voltage thereon. Till a next operation starts, the voltage-temporal conversion circuit **81** converts the calculated voltage to a PW signal for the operation of the operation circuit **12**. The operations of the charge storage interval and the PW convert interval of the recursive circuit **800** are similar to those of the charge storage interval and the PW convert interval in FIG. **4**A, e.g., using a ramp signal to generate the PW signal, and thus details thereof are not repeated herein.

In one aspect, the recursive circuit **800** further includes an inverter INV to invert a phase of the outputted PW signal. However, when the operation circuit **12** includes an inverter therein, the recursive circuit **800** does not include the inverter INV.

In the present disclosure, the PW convert interval of FIG. **4**A as well as the operation reset interval and the numerical calculation interval of FIG. **9** as a whole is referred to an operation interval T_O herein, wherein the operation reset interval of FIG. **9** is performed in parallel with or behind the PW convert interval of FIG. **4**A.

It is appreciated that if there is no next operation after the recursive circuit **800**, the recursive circuit **800** directly provides (e.g., controlled by a switching device) the calculated voltage on the operation capacitor Co to the identify circuit **14** for identification, e.g., compared with a reference voltage using a comparator.

The circuit in FIG. **8** is called recursive circuit because the operation result of the operation circuit **12** may be stored and then converted to a PW signal multiple times by the recursive circuit **800** to perform multiple recursive operations. That is, the operation circuit **12** not only calculates the detected result of the photodiode PD, but also calculates the operation result thereof with the operation result of other pixels.

In this way, by using the pixel circuit **200** of FIG. **2** in conjunction with the recursive circuit **800** of FIG. **8**, it is possible to perform various pixel-wise operations on the pixel data for various applications. The identify circuit **14** performs various identifications according to a final operation result of the pixel circuit **20** and the recursive circuit **800**, e.g., identifying the lift-up of a navigation device, calculating the navigation vector, performing image recognition, categorizing images, performing motion detection and performing multi-layer neural network so as to realize the pixel structure with pixel-wise operation.

For example referring to FIG. **10**, it is a schematic diagram of one application of the pixel circuit of the present disclosure that performs the motion detection (e.g., adapted to a security system). A pixel array of a camera includes multiple pixels arranged in an array. The identify circuit **14** performs the motion detection according to 9 adjacent pixels, including pixel 0 to pixel 8, wherein the pixel 0 is a central pixel of pixel 1 to pixel 8. In this aspect, the pixels 0 to 8 respectively include the pixel circuit **200** in FIG. **2** and/or at least one operation circuit **12**.

As mentioned above, pixels 0 to 8 respectively generate a first detection signals A**0** to A**8** and second detection signals B**0** to B**8**. After the subtraction circuit **500** (e.g., included in the pixel circuit of pixels 0 to 8, but not limited to) performs the numerical calculation on the first detection signals A**0** to A**8** and the second detection signal B**0** to B**8** of the pixels 0 to 8, the subtracted result Y**0** to Y**8** are obtained and stored in the corresponding operation capacitor Co (e.g., shown in FIG. **8**), wherein Y**0** to Y**8** indicate that each of pixels 0 to 8 performs the temporal difference operation on detected signals obtained in different detection intervals to represent the brightness variation detected by every pixel.

Next, after converting Y**0** to Y**8** to PW signals using the recursive circuit **800**, the absolute difference circuit **700** performs the numerical calculation of absolute differencing between Y**0** and Y**1**, Y**0** and Y**2** . . . Y**0** and Y**8** to obtain Y**01** to Y**08**, wherein Y**01** to Y**08** indicate that the pixel array performs the spatial difference operation between different pixels, and Y**01** to Y**08** contain the operation result of both the temporal difference and spatial difference.

Finally, Y**01** to Y**08** are summed by the addition circuit **600**. Similarly, Y**01** to Y**08** are firstly stored in the corresponding operation capacitor Co, and then converted to PW signals by the voltage-temporal conversion circuit **81** for the summation of the addition circuit **600**.

In one aspect, the addition circuit **600** includes two inputs as shown in FIG. **6**, and the addition circuit each time performs the summation of two of Y**01** to Y**08** that is stored and voltage-temporal converted, and then summed with another one of the rest of Y**01** to Y**08** till all of Y**01** to Y**08** is added together.

In another aspect, the addition circuit includes 8 inputs and uses the pulse widths associated with Y**01** to Y**08** to control the charging intervals of respective current sources as a way of adding Y**01** to Y**08** together.

The identify circuit **14** receives a summation of the addition circuit **600**, and compares the summation with a predetermined threshold (e.g., using a comparator). When the summation of Y**01** to Y**08** is larger than or equal to the predetermined threshold, it means that a motion is detected. The identify circuit **14** then outputs a control signal to perform corresponding controls, e.g., turning on a light source, starting to record images or increasing image capture frequency.

In another aspect, the identify circuit **14** receives a summation of the temporal differences Y**0** to Y**8** (e.g., Y**0** to Y**8** directly outputted to the addition circuit **600** from pixels 0 to 8). When the summation is larger than or smaller than (determined according to the light source arrangement) a brightness threshold, it means that a mouse device is lifted up by a user.

It is appreciated that although FIG. **10** uses 9 neighboring pixels to detect the temporal and spatial brightness variation to perform the motion detection or lift-up detection, the present disclosure is not limited thereto. The identify circuit **14** uses a proper number of pixels to detect the temporal and spatial brightness variation, e.g., the proper number being determined according to environment to be detected and a size of pixel array.

In the above embodiments, two temporal circuits are arranged in the pixel circuit to alternatively output a detected signal having a pulse width corresponding to the latest light energy detected in successive exposure intervals.

In the embodiments below, a pixel circuit (e.g., indicated by **1300** in FIG. **13**) selects to output image data, time difference data or a state-change signal according to control signals of a control circuit (e.g., indicated by **120** in FIG. **12**) and an input signal of a comparator is further provided.

Please refer to FIG. **11**, it shows four image frames F**1** and F**4** successively captured by an optical sensor which includes the pixel circuit **1300** of the present disclosure. For

example, the image frame F1 is the first image frame captured when the optical sensor is activated or woken up, and pixel data of all pixel circuits **1300** (e.g., each rectangle in FIG. **12** indicating one pixel) is readout to form one reference image to be stored in a backend circuit or device. In capturing the image frames F2 and F3 by the optical sensor, if an analog circuit (e.g., arranged in a sensor chip or in the optical sensor) identifies that no pixel has a change (i.e. not detecting enough light energy variation, e.g., ΔV<variation threshold as mentioned below) according to a state-change signal or time difference data outputted by each pixel circuit **1300**, the optical sensor does not output image data of the image frames F2 and F3.

In capturing the image frame F4, when the analog circuit identifies that a part of pixels have a change (e.g., a part of pixel circuits **1300** detecting a human body) according to the state-change signal or time difference data outputted by each pixel circuit **1300**, the readout circuit **122** then reads gray levels of the part of pixels having a change as the image data.

That is, in the image frames F1 to F4 of FIG. **11**, only pixel circuits corresponding to solid lines output image data to backend circuit or device.

Please refer to FIG. **12**, it shows that only pixel circuits **1300** indicated by an arrow detect light energy variation between the image frames F1 and F4, as mentioned above no light energy variation being detected between F1 and F2 or between F1 and F3. Therefore, the readout circuit **122** only reads image data of the pixel circuits **1300** indicated by an arrow in FIG. **12**. The backend circuit or device (e.g., host) updates the stored reference image therein according to the read image data or tags the pixels indicated by an arrow in FIG. **12**, wherein how the backend circuit or device using the image data, time difference data or state-change signal outputted by every pixel circuit **1300** is determined according to different applications, and is not limited to those mentioned herein.

Please refer to FIG. **13**, it is a circuit diagram of a pixel circuit **1300** according to one embodiment of the present disclosure. The pixel circuit **1300** includes a photodiode PD, a storage capacitor Cref, an image circuit **131**, a difference circuit **133** and a sharing circuit **135**, wherein the sharing circuit **135** is shared by the pixel circuit **1300** with other pixel circuits, which are multiple pixel circuits at a same column of a pixel array (e.g., pixel array corresponding to image frames F1 and F4 in FIG. **12**) as the pixel circuit **1300**.

It should be mentioned that although the image circuit **131** and the difference circuit **133** both output voltage values, the voltage value outputted by the image circuit **131** is image data associated with light energy generated in a first interval (e.g., T_{SA} of FIG. **4**B) by the photodiode PD; and the voltage value outputted by the difference circuit **133** is time difference data associated with a variation of light energy generated between the first interval T_{SA} and a second interval (e.g., T_{SB} of FIG. **4**B) by the photodiode PD. That is, in the present disclosure, the image data is referred to detected light energy of the photodiode PD in a single exposure interval, and the time difference data is referred to a difference or variation of detected light energy of the photodiode PD between two exposure intervals. Accordingly, the pixel circuit **1300** is able to perform the time difference detection or simply output pixel data.

The storage capacitor Cref has a first end (e.g., left end in FIG. **13**) connected to a first node V1, and a second end (e.g., right end in FIG. **13**) connected to a second node V2.

The image circuit **131** is connected to the first end of the storage capacitor Cref and is a 4-transistor pixel circuit, e.g., including a first reset transistor T1, a transfer transistor T2, a first source follower T3 and a first output transistor T4, which are all NMOS transistors.

The transfer transistor T2 is connected between the photodiode PD and the first end of the storage capacitor Cref, and is used to transfer light energy generated by the photodiode PD to the storage capacitor Cref according to a control signal TX.

The first reset transistor T1 has a source connected between the transfer transistor T2 and the first end of the storage capacitor Cref and has a drain connected to a voltage source V_{DD}. The first reset transistor T1 is conducted to reset a voltage at the first node V1 according to a control signal RESET.

The first output transistor T4 is connected between the first end of the storage capacitor Cref and a first readout line Rd1, and is used to output the voltage at the first node V1 to the first readout line Rd1 according to a control signal RS_I, wherein the first readout line Rd1 connects multiple pixel circuits at the same column of a pixel array as the pixel circuit **1300**.

The control signals TX, RESET and RS_I are generated, for example, by the control circuit **120**. For example, the control circuit **120** controls the pixel array to acquire an image frame using the rolling shutter.

The first source follower T3 is connected between the transfer transistor T2 and the first end of the storage capacitor Cref, and is used to losslessly buffer light energy of the photodiode PD to the storage capacitor Cref.

The difference circuit **133** is connected to the second end of the storage capacitor Cref, and includes a row selection transistor T5, a second reset transistor T6, a second source follower T7 and a second output transistor T8, which are all NMOS transistors.

The row selection transistor T5 is connected between a reset voltage V_{AZ} and the second reset transistor T6, and is conducted according to a row selection signal RS, which is used to determine the row of a pixel array being triggered.

The second reset transistor T6 is cascaded to the row selection transistor T5 via a drain thereof, and has a source connected between the second end of the storage capacitor Cref and the second output transistor T8, and is used to reset the second end of the storage capacitor Cref to a reset voltage Vaz according to a control signal AZ_R, which is used to determine the column of a pixel array being triggered.

The second output transistor T8 is connected between the second end of the storage capacitor Cref and a second readout line Rd2, and is used to output a voltage at the second node V2 to the second readout line Rd2 according to a control signal RS_D, wherein the second readout line Rd2 connects multiple pixel circuits at the same column of a pixel array as the pixel circuit **1300**.

The row selection signal RS, as well as the control signals AZ_R and RS_D are generated, for example, by the control circuit **120**.

The second source follower T7 is connected between the second end of the storage capacitor Cref and the second output transistor T8, and is used to losslessly buffer a voltage at the second node V2 to the second readout line Rd2.

The sharing circuit **135** includes a first comparator CMP1 and a second comparator CMP2.

One input terminal of the first comparator CMP1 is connected to the first readout line RD1, and the first comparator CMP1 is used to output image data D_{imag}. For example, the first comparator CMP1 is used to compare a voltage at the first end of the storage capacitor Cref with a ramp signal Vramp to output the image data D_{imag}. For

example, a single slop ADC is used to generate magnitude of the image data D_{imag}, wherein the operation of the single slop ADC is known to the art, and thus details thereof are not described herein. The first comparator CMP**1** is shared by the pixel circuit **131** with other pixel circuits via the first readout line Rd**1**.

One input terminal of the second comparator CMP**2** is connected to the second readout line RD**2**, and the second comparator CMP**2** is used to output time difference data D_{diff} or a state-change signal. The second comparator CMP**2** is used to compare a voltage at the second end of the storage capacitor Cref with a ramp signal Vramp to output the time difference data D_{diff}. Or, the second comparator CMP**2** is used to sequentially compare a voltage at the second end of the storage capacitor Cref with an upper threshold voltage (e.g. Vref+Vth) and a lower threshold voltage (e.g., Vref−Vth) to output a state-change signal. More specifically, when the voltage at the second node V**2** does not exceed a range of Vref±Vth (or called variation threshold), it means that the pixel circuit **1300** does not detect enough light energy variation such that the state-change signal is not generated; whereas when the voltage at the second node V**2** exceeds the range of Vref±Vth, it means that the pixel circuit **1300** detects enough light energy variation such that the state-change signal is generated, e.g., pixels indicated by an arrow in FIG. **12**. The second comparator CMP**2** is shared by the difference circuit **133** with other pixel circuits via the second readout line Rd**2**.

In the present disclosure, the state-change signal is sometimes called the time difference data which indicates whether light energy between a first interval and a second interval has enough variation to have the pixel change, as shown in FIGS. **11** and **12**.

Please refer to FIG. **14**, it is a first operation mode of a pixel circuit **1300** according to one embodiment of the present disclosure, in which the pixel circuit **1300** outputs image data D_{imag}. For example, the first operation mode is a mode for a 4-T pixel circuit to output image data, and includes an exposure interval in first column, a reset interval in second column, a charge transfer interval in third column and a readout interval in fourth column of FIG. **14**.

The exposure interval is an interval to expose the photodiode PD, and all transistors are not conducted.

The reset interval is to reset a voltage at the first node V**1** to Vr by conducting the transistors T**1** and T**4**.

The charge transfer interval is to transfer detected light energy of the photodiode PD to the storage capacitor Cref by conducting the transistors T**2** and T**4** such that the voltage at the first node changes to Vs containing charges dumped from the photodiode PD.

The readout interval is to couple the voltage Vs at the first node V**1** to an input terminal of the first comparator CMP**1** by conducting the transistor T**4**. The voltage Vs is compared with a ramp signal Vramp to output image data D_{imag}.

In the first operation mode, all transistors in the difference circuit **133** are not conducted. It is seen from FIG. **14** that the transistors T**5**, T**6** and T**8** are not conducted in every interval. The transistors T**3** and T**7** are used as source followers instead of switching devices.

Please refer to FIG. **15**, it is a second operation mode of a pixel circuit **1300** according to one embodiment of the present disclosure, in which the pixel circuit **1300** outputs time difference data D_{diff}. The second operation mode includes a first charge transfer interval in first column, a reset interval in second column, a second charge transfer interval in third column and a readout interval in fourth column of FIG. **15**.

The first charge transfer interval is to transfer detected light energy of the photodiode PD in a first interval to the first node V**1** to form a voltage Vold, wherein the first charge transfer interval of FIG. **15** actually includes operating results of the exposure interval, the reset interval and the charge transfer interval of FIG. **14**, i.e. Vold=Vs. For simplification, FIG. **15** only shows the charge transfer interval.

The reset interval is to reset a voltage at the second node V**2** to Vaz by conducting the transistors T**5**, T**6** and T**8**. Meanwhile, in order not to change the voltage Vold at the first node V**1**, the transistor T**4** is also conducted.

The second charge transfer interval is to transfer detected light energy of the photodiode PD in a second interval to the first node V**1** to form a voltage Vold+ΔV, wherein the second charge transfer interval in FIG. **15** actually includes operating results of the exposure interval and charge transfer interval of FIG. **14**. Meanwhile, since the transistors T**5**, T**6** and T**8** are not conducted, the voltage at the second node V**2** also has a voltage variation ΔV to become Vaz+ΔV.

Because the image circuit **131** is to generate a variation of detected light energy between the first interval and the second interval, the image circuit **131** is not reset between the first interval and the second interval, or between the first charge transfer and the second charge transfer.

The readout interval is to couple the voltage Vaz+ΔV at the second node V**2** to an input terminal of the second comparator CMP**2** by conducting the transistor T**8**. The voltage Vaz+ΔV is compared with a ramp signal Vramp to generate time difference data D_{diff}. The time difference data D_{diff} is also the digital data generated by the single slope ADC. In one aspect, the voltage Vold+ΔV at the first node V**1** is coupled to an input terminal of the first comparator CMP**1** by conducting the transistor T**4**, and the voltage Vold+ΔV is compared with a ramp signal Vramp to output image data.

Please refer to FIGS. **16**A and **16**B, it is a third operation mode of a pixel circuit **1300** according to one embodiment of the present disclosure, in which an analog circuit of the optical sensor identifies whether to output time difference data D_{diff} to backend circuit or device according to the time difference data D_{diff} of the difference circuit **133**.

It should be mentioned that the second charge transfer interval in first column of FIG. **16**A is the second charge transfer interval of FIG. **15**. That is, before the second charge transfer interval, the third operation mode further includes the first charge transfer interval and the reset interval of FIG. **15**, and FIGS. **16**A and **16**B mainly show the operation of a cycle I and a cycle II for simplification purposes.

The cycle I of FIG. **16**B is to identify (e.g., by analog circuit) that whether the time difference data D_{diff} exceeds a variation threshold. As mentioned above, the present disclosure is to identify magnitude of the time difference data D_{diff} according to the conversion result of the single slope ADC.

In the read difference data interval in second column, if the time difference data D_{diff} does not exceed a predetermined variation threshold, the process returns to the second charge transfer interval to accumulate the voltage variation of a next exposure interval, e.g., the voltage at the first node V**1** changes from Vold+ΔV to Vold+2ΔV or Vold+ΔV+ΔV'.

In the read difference data interval, if the time difference data D_{diff} exceeds the predetermined variation threshold, the cycle II is performed, i.e. resetting the second node V**2** as in third column of FIG. **16**A after reading the time difference data D_{diff}. The voltage at the second node V**2** is reset to Vaz, and the voltage at the first node is changed to Vold (FIG. **16**A showing new Vold since it is formed within different time interval).

In the third operation mode, the analog circuit identifies whether to output time difference data D_{diff} according to magnitude of the time difference data D_{diff}. The time difference data D_{diff} outputted in the read difference data interval is sent to the backend circuit or device, which uses the time difference data D_{diff} in different ways according to different requirements.

Please refer to FIGS. **17**A and **17**B, it is a fourth operation mode of a pixel circuit **1300** according to one embodiment of the present disclosure, in which an analog circuit of the optical sensor identifies whether to control the image circuit **131** to output image data according to whether the difference circuit **133** outputs a state-change signal. It should be mentioned that some operation intervals of FIGS. **17**A and **17**B may include other operations, but for simplification purposes, only representative operation intervals are shown in FIGS. **17**A and **17**B.

As mentioned above, the analog circuit identifies whether a state change occurs in an output signal of the second comparator CMP**2**, which sequentially compares the time difference data D_{diff} (i.e. voltage at the second node V**2**) with an upper threshold voltage Vref+Vth and a lower threshold voltage Vref−Vth.

The exposure interval in first column and the reset first node interval in second column of FIG. **17**A are identical to those of FIG. **14**, and thus details thereof are not repeated herein. The charge transfer & check variation interval in third column of FIG. **17**A includes the first charge transfer interval, the reset second node interval and the second charge transfer interval of FIG. **15** to cause a voltage at the first node V**1** to change to Vold+ΔV, and a voltage at the second node V**2** to change to Vaz+ΔV. Then, the second comparator CMP**2** compares the Vref+ΔV (i.e. time difference data Vaz+ΔV passing T**7** and T**8**) with the upper threshold voltage Vref+Vth and the lower threshold voltage Vref−Vth.

If the second comparator CMP**2** fails to output a state-change signal (i.e. time difference data not exceeding variation threshold), the pixel circuit **1300** does not output image data D_{imag}. That is, in FIG. **17**B, if the second comparator CMP**2** does not output a state-change signal, the process enters a cycle I to perform a new exposure, and the readout circuit **122** does not read image data of the pixel circuit **1300**, e.g., pixels not indicated by an arrow in FIG. **12**.

The cycle I is to repeatedly perform the intervals of exposure, reset first node and check variation, and the second end of the storage capacitor Cref (i.e. second node V**2**) is not reset before a next exposure interval.

When the second comparator CMP**2** outputs a state-change signal (i.e. time difference data exceeding variation threshold), a cycle II is entered. In the cycle II, the readout circuit **122** reads image data D_{imag} (e.g., shown as Vs) of the image circuit **1300**. As mentioned above, the conversion result of the single slope ADC is treated as the image data D_{imag} by the backend circuit or device. Then, a new exposure is performed after resetting the second node V**2**.

In the fourth operation mode, the cycle II is to repeatedly perform intervals of the exposure, reset first node, check variation, read image data and reset second node. The control of transistors in every interval is shown in FIG. **17**A.

Please refer to FIGS. **18**A and **18**B, it is a fifth operation mode of a pixel circuit **1300** according to one embodiment of the present disclosure, in which an analog circuit arranged in the optical sensor identifies whether to control the image circuit **131** to output image data D_{imag} according to whether the difference circuit **133** outputs a state-change signal.

The fifth operation mode also includes intervals of the exposure in first column, check variation in second column, read image data in third column, reset second node in fourth column and reset first node in fifth column. The difference from the fourth operation mode is that in the fifth operation mode the reset first node is executed in the cycle II, i.e. the first end of the storage capacitor Cref (i.e. first node V**1**) is reset only when the second comparator CMP**2** outputs a state-change signal. Other parts are similar to the fourth operation mode.

In the fifth operation mode, the cycle I repeatedly performing intervals of the exposure and check variation; and the cycle II repeatedly performing intervals of the exposure, check variation, read pixel data, reset second node and reset first node. The control of transistors in every interval is shown in FIG. **18**A.

It should be mentioned that for simplification purposes, FIGS. **17**B and **18**B omits control signals, which are already shown in FIGS. **13** and **16**B.

The present disclosure further provides an operating method of a pixel array (e.g., referring to FIG. **12**) including multiple pixel circuits **1300** of FIG. **13**, including the steps of:

Step **1**: The analog circuit identifies whether the time difference data D_{diff} of every pixel circuit **1300** of a pixel array exceeds a variation threshold (i.e. a range of ±Vth). In one aspect, the analog circuit identifies according to the time difference data D_{diff} read in FIG. **16**B. In another aspect, the analog circuit identifies according to the check variation of FIGS. **17**B and **18**B, i.e. sequentially comparing, by the second comparator CMP**2**, the time difference data D_{diff} with an upper threshold Vref+Vth and a lower threshold Vref−Vth to identify whether an output signal from the second comparator CMP**2** has a state change so as to identify whether the variation threshold is exceeded.

Step **2**: When the time difference data D_{diff} of all of the pixel circuits **1300** of the pixel array does not exceed the variation threshold, the pixel array does not output image data D_{imag}, e.g., FIG. **11** showing that image frames F**2** and F**3** do not have pixel change such that the image data D_{imag} corresponding to the image frames F**2** and F**3** is not outputted to backend circuit or device.

Step **3**: When the time difference data D_{diff} of a part of pixel circuits **1300** of the pixel array exceeds the variation threshold, only the part of pixel circuits **1300** output the image data D_{imag}, e.g., FIG. **11** showing that only pixels indicated by an arrow output image data D_{imag} (e.g., executing cycle II in FIGS. **17**B and **18**B), but the rest pixels do not output image data D_{imag} (e.g., executing cycle I in FIGS. **17**B and **18**B).

The image data D_{imag} outputted by the part of pixel circuits **1300** is used to update a reference image stored in the backend circuit or device, and the backend circuit or device may tag the part of pixel circuits in the pixel array. As mentioned above, the backend circuit or device uses the time difference data D_{diff}, state-change signal and image data D_{imag} according to different applications.

As mentioned above, in the conventional optical sensor, pixel data is converted to digital data at first, and then the digital data is operated by the digital backend such that frame buffers are required to temporarily store frame data. Accordingly, the present disclosure further provides a pixel circuit that outputs pulse width signals for the analog operation (e.g., FIG. **2** and FIGS. **5** to **7**). The pixel circuit outputs, within an operation interval, the PW signals corresponding to different detecting intervals for the analog

operation of an operation circuit so as to realize the objective of the pixel-wise operation of pixel data.

Although the disclosure has been explained in relation to its preferred embodiment, it is not used to limit the disclosure. It is to be understood that many other possible modifications and variations can be made by those skilled in the art without departing from the spirit and scope of the disclosure as hereinafter claimed.

What is claimed is:

1. A pixel circuit, comprising:

a photodiode, configured to generate light energy;

a storage capacitor, having a first end and a second end;

an image circuit, connected to the first end of the storage capacitor, and configured to output image data associated with the light energy generated in a first interval by the photodiode; and

a difference circuit, connected to the second end of the storage capacitor, and configured to output time difference data associated with a variation of the light energy generated between the first interval and a second interval by the photodiode;

a first comparator, connected to the image circuit, and configured to output image data; and

a second comparator, connected to the difference circuit, and configured to output time difference data or a state-change signal.

2. The pixel circuit as claimed in claim **1**, wherein

the first comparator and the second comparator are shared by the image circuit with other pixel circuits,

wherein said other pixel circuits are multiple pixel circuits at a same column of a pixel array as the pixel circuit.

3. The pixel circuit as claimed in claim **2**, wherein

the first comparator is configured to compare a voltage at the first end of the storage capacitor with a ramp signal to generate the image data, and

the second comparator is configured to compare a voltage at the second end of the storage capacitor with a ramp signal to generate the time difference data.

4. The pixel circuit as claimed in claim **2**, wherein the second comparator is configured to sequentially compare a voltage at the second end of the storage capacitor with an upper threshold voltage and a lower threshold voltage to generate the state-change signal.

5. The pixel circuit as claimed in claim **4**, wherein the image circuit is configured not to output the image data when the second comparator does not generate the state-change signal.

6. The pixel circuit as claimed in claim **4**, wherein the second end of the storage capacitor is not reset before a next exposure interval when the second comparator does not generate the state-change signal.

7. The pixel circuit as claimed in claim **4**, wherein the first end of the storage capacitor is still reset when the second comparator does not generate the state-change signal.

8. The pixel circuit as claimed in claim **4**, wherein the first end of the storage capacitor is reset only when the second comparator generates the state-change signal.

9. The pixel circuit as claimed in claim **1**, wherein the image circuit comprises:

a first output transistor, connected between the first end of the storage capacitor and a first readout line;

a transfer transistor, connected between the photodiode and the first end of the storage capacitor, and

a first reset transistor, having a source connected between the transfer transistor and the first end of the storage capacitor.

10. The pixel circuit as claimed in claim **1**, wherein the difference circuit comprises:

a second output transistor, connected between the second end of the storage capacitor and a second readout line;

a second reset transistor, having a source connected between the second end of the storage capacitor and the second output transistor; and

a row selection transistor, cascaded with the second reset transistor.

11. An operating method of the pixel circuit as claimed in claim **1**, the operating method comprising:

transferring a signal voltage, associated with the light energy generated in the first interval by the photodiode, to the first end of the storage capacitor;

resetting the second end of the storage capacitor to a reset voltage and holding the signal voltage at the first end of the storage capacitor in a resetting interval;

transferring a variation voltage, associated with the light energy generated in the second interval by the photodiode, to the first end of the storage capacitor to be added to the signal voltage to form the image data and coupled to the reset voltage to form the time difference data;

outputting a state-change signal via the second comparator to read the image data via the first comparator upon the time difference data exceeding a predetermined voltage range; and

not outputting the state-change signal and not reading the image data upon the time difference data not exceeding the predetermined voltage range.

12. The operating method as claimed in claim **11**, wherein the image circuit is not reset between the first interval and the second interval.

13. The operating method as claimed in claim **11**, wherein upon the time difference data not exceeding the predetermined voltage range, the operating method further comprises:

transferring another variation voltage, associated with the light energy generated in a third interval by the photodiode, to the first end of the storage capacitor to be accumulated to the image data to form new image data and coupled to the time difference data to form new time difference data.

14. The operating method as claimed in claim **13**, wherein the image circuit and the difference circuit are not reset between the second interval and the third interval.

15. The operating method as claimed in claim **13**, further comprising:

sequentially resetting a second node connected to the second end of the storage capacitor and a first node connected to the first end of the storage capacitor after the image data is read.

16. The operating method as claimed in claim **11**, wherein upon the time difference data not exceeding the voltage range, the operating method further comprises:

performing a new round of the transferring a signal voltage, the resetting the second end of the storage capacitor and the transferring a variation voltage.

17. The operating method as claimed in claim **16**, further comprising:

resetting a second node connected to the second end of the storage capacitor after the image data is read.

18. The operating method as claimed in claim **11**, further comprising:

resetting a second node connected to the second end of the storage capacitor after the time difference data is read.

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