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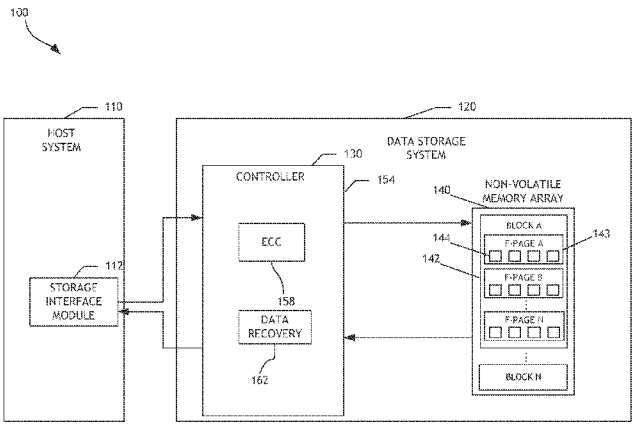


FIGURE 1

(57) Abstract: In some embodiments of the present invention, a data storage system includes a controller and a non-volatile memory array having a plurality of memory pages. The controller performs a method that efficiently resolves the lower page corruption problem. In one embodiment, the method selects programmed lower page(s) for which paired upper page(s) have not been programmed, reads data from those selected lower page(s), corrects the read data, and reprograms the read data into those lower page(s). Since the number of lower pages in this condition is typically low (e.g., several pages in a block with hundreds or thousands of pages), this is a much more efficient method than reprogramming the entire block, in another embodiment, a similar reprogramming method is applied as a data recovery scheme in situations in which only lower pages are programmed (e.g., SLC memory, MLC memory in SLC mode, etc.).

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# SYSTEM AND METHOD FOR LOWER PAGE DATA RECOVERY IN A SOLID STATE DRIVE

## BACKGROUND

### Technical Field

This disclosure relates to data storage systems, such as solid state drives, for computer systems. More particularly, the disclosure relates to lower page data recovery.

### Description of the Related Art

Memory arrays with multi-level cell (MLC) NAND media are now commonplace in solid state drives (SSDs). MLC allows multiple possible states to exist in a single memory cell, thereby enabling the storing of more than one bit of information per cell (e.g., 2, 3, 4 or more). For example, in a 2-bit-per cell MLC flash, 4 possible states (4 voltage (Vt) levels) are possible which enable storage of 2 bits. Based on the data the memory cells are going to store and the coding for different states, the cells are programmed to 4 possible and distinctive Vt zones. Typically, data stored in lower pages and upper pages are logically paired together, with the lower pages being programmed first.

## BRIEF DESCRIPTION OF THE DRAWINGS

Systems and methods that embody the various features of the invention will now be described with reference to the following drawings, in which:

Figure 1 illustrates a storage system that reprograms data according to one embodiment of the invention.

Figures 2A and 2B show the voltage distribution of memory cells to illustrate the factors that contribution to lower page corruption and a solution according to one embodiment of the invention.

Figure 3 is a flow diagram showing a method of reprogramming according to one embodiment of the invention.

Figures 4A-4B and 5 show the different memory cell configuration in which open lower pages may be selected for reprogramming according to embodiments of the invention.

Figure 6 is a flow diagram illustrating a process of reprogramming lower page programmed only cells according to one embodiment of the invention.

## DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

While certain embodiments are described, these embodiments are presented by way of example only, and are not intended to limit the scope of protection. Indeed, the novel methods and systems described herein may be embodied in a variety of other forms. Furthermore, various omissions, substitutions, and changes in the form of the methods and systems described herein may be made without departing from the scope of protection.

### Overview

In MLC flash memory, even though the lower pages and upper pages are physically paired, they are generally decoupled in programming. The data stored in lower pages and upper pages can be programmed at different time and from different sources. There are often cases where the upper pages are programmed much later and at different temperature. Most time, there are no problems for this programming scheme. However, various factors including temperature and aging effects of the memory cells can degrade retention of the data in the cells and may lead to the problem of lower page corruption when the storage system attempts to program the upper page.

One way to overcome the lower page corruption problem is to move the old data of the entire open block to another new address when there is a need to program the upper page. In this manner, the lower page and upper page are programmed at the same time under the similar condition. However, this method is inefficient.

In some embodiments of the present invention, a data storage system includes a controller and a non-volatile memory array having a plurality of memory pages. The controller performs a method that may require less system load while still preventing the lower page corruption problem discussed above. In one embodiment, the method selects programmed lower page(s) for which paired upper page(s) have not been programmed, reads data from those selected lower page(s), corrects the read data, and reprograms the read data into those lower page(s). Since the number of lower pages in this condition is typically low (e.g., several pages

in a block with hundreds or thousands of pages), this is a much more efficient method than reprogramming the entire block. In another embodiment, a similar reprogramming method is applied as a data recovery scheme in situations in which only lower pages are programmed (e.g., SLC (single-level cell) memory, MLC memory in SLC mode, etc.).

System Overview

Fig. 1 illustrates a storage system 120 that performs reprogramming for data recovery according to one embodiment of the invention. As is shown, a storage system 120 (e.g., solid state drive, hybrid hard drive, etc.) includes a controller 130 and a non-volatile memory array 140, which includes one or more blocks of memory storage, identified as Block "A" 142 through Block "N". Each block includes flash pages (F-pages). For example, Block A 142 of Figure 1 includes F-pages identified as F-pages A 153, B, through N. In some embodiments, each "F-page" is a smallest grouping of memory cells in the non-volatile memory array 140 that can be programmed in a single operation or as a unit. Further, each F-page includes error correcting code pages (E-pages). In the illustrated embodiment, each F-page includes four E-pages that are illustrated as four boxes, including E-page 144. Other embodiments may use F-pages or E-pages that are defined differently or each F-page may include greater or fewer than four E-pages.

The controller 130 can receive data and/or storage access commands from a storage interface module 112 (e.g., a device driver) in a host system 110. Storage access commands communicated by the storage interface 112 can include write and read commands issued by the host system 110. The commands can specify a logical block address in the storage system 120, and the controller 130 can execute the received commands in the non-volatile memory array 140. In a hybrid hard drive, data may be stored in magnetic media storage component (not shown in Fig. 1) in addition to the non-volatile memory array 140.

In one embodiment, the controller 130 includes an ECC module 158. In one embodiment, the ECC module 158 handles error correction of data read from the memory array 140. In one embodiment, it encodes data to be written to memory pages, such as E-pages, of the non-volatile memory array 140 and decodes the data when they are read out. The controller 130 in one embodiment also includes a data

recovery module 162 which performs the reprogramming methods in accordance with one or more embodiments of the invention, as further described below.

Voltage Distribution Illustration

Figures 2A and 2B show the voltage distribution of memory cells to illustrate the factors that contribution to lower page corruption and a solution according to one embodiment of the invention. Figure 2A shows the voltage distribution of MLC memory cells in which only the lower pages have been programmed. Line 200 shows the voltage distribution at the point of initial programming. Line 202 shows the voltage distribution after some time has lapsed. In Figure 2A, those cells have undergone a testing process where they are heated to simulate a time lapse of approximately 12.6 months at 40 °C. It can be seen that the distribution has drifted to the left on the voltage scale, such that some cells are now in the error region 208. These cells, if read, would likely result in a different bit value than the initial programmed value, because their voltage level is now below threshold 206. Thus these hundreds of bits are now in error. Line 204 shows the distribution after the cells have been reprogrammed in according to one or more embodiments of the invention. The distribution is now nearly identical to the distribution at the time of initial programming, and the failing bit count (FBC) is zero.

Figure 2B shows the voltage distribution of MLC memory cells in which both the lower and upper pages have been programmed. This graph does not show the effect of the voltage drifts. Rather, it illustrates two scenarios. First, line 210 shows the voltage distribution of the Vt states of the cells in which both the upper and lower pages are programmed at the same time or nearly the same time. This would be considered an ideal condition since there is little to no time lapsed, and little to no temperature differences between the two programming. However, this is not always how the cells are programmed. If the upper page is programmed at a different time and/or temperature than the lower page, the lower page corruption problem can occur. However, the reprogramming of the lower page reduces the risk of this problem. Line 212 shows the voltage distribution after the cells have been reprogrammed according to one or more embodiments of the invention. As shown, after reprogramming all three states are aligned very closely to the distribution

shown in line 210, which, as mentioned above reflects the distribution of cells where upper and lower pages have been programmed at the same or nearly the same time.

Reprogramming

Figure 3 is a flow diagram showing a method 250 of reprogramming according to one embodiment of the invention. The method 250 may be executed as part of a start-up sequence, on a periodic basis, or on an as-needed basis. In one embodiment, the method 250 is performed by the controller 130 shown in Figure 1. At block 255, the method selects programmed lower page(s) with paired upper pages that are not programmed. These lower page(s) may be referred to as "open" lower pages. For example, the method may select such pages from one or more "open" blocks in which data is currently being programmed. To illustrate further, if the method 250 is executed as part of a start-up sequence, such open blocks may be blocks that were being programmed when the storage system was last shut down, and they have not been closed since their capacity have not been filled. Since the system is likely to resume programming in these open blocks, the lower page corruption problem may occur in these open lower page(s). Therefore, in one embodiment, the method selects such open lower pages for reprogramming.

At block 260, the data from the selected lower pages are read, and then the read data is corrected (e.g., through the application of Error Correction Code (ECC)) at block 265. Then, at block 270, the corrected data is reprogrammed back to the selected lower pages. As previously shown in Figure 2A, the voltage distribution of the cells in these lower pages now closely resembles the distribution when they were initially programmed. Thus, when their paired upper pages are programmed, the lower page corruption problem can be avoided.

Selecting Lower Pages

Figures 4A-4B and 5 show the different memory cell configuration in which open lower pages may be selected. In Figure 4A, an MLC configuration is presented and pages 0-7 are shown. The "U" denotes an upper page and the "L" denotes a lower page. From top to bottom, the horizontal lines represent word lines, and they are labeled (between Figures 4A and 4B) WL (Word Line) 0, WL 1, WL 2, and so on.

The page number denotes the order in which pages are programmed. Here, pages 0-7 have been programmed. Page 0, a lower page in WL 0 is first

programmed, and then page 1, a lower page in the same WL 0 is programmed, and so on. Note that page 0 is paired with upper page 4, and page 1 is paired with upper page 5, and so on. In this programming sequence, pages 2, 3, 6, and 7 are open lower pages that do not have their paired upper pages programmed. In one embodiment, if the controller finds the state of the memory as shown in Figure 4A, these pages will be selected for reprogramming, for example, according to the method shown in Figure 2. In this typical configuration, there is a maximum of 4 such open pages at a given time. Thus, to reprogram these open pages is much more efficient than reprogram data from the entire memory block. In one embodiment, these open pages may be flagged (e.g., through metadata) by the controller as part of a shutdown sequence, so that any such open lower pages in open blocks can be quickly identified at start-up. If the indication for such open lower pages is not available (e.g., a previous ungraceful/unexpected shutdown has occurred or the system does not support marking such pages), the controller may perform scanning through the memory blocks to locate such open lower pages.

Figure 4B shows the same memory cells after the programming of pages 8 and 9. In the current example, just before pages 8 and 9 are programmed, a reprogram has taken place to read out data from pages 2 and 3, the corrected data is reprogrammed back to pages 2 and 3. Thus, lower page corruption of pages 2 and 3 can be avoided when pages 8 and 9 are programmed. With pages 8 and 9 programmed, pages 2 and 3 are no longer open. If the system shut downs at this point, at the next start-up the controller may select pages 6 and 7 for reprogramming.

Figure 5 shows another MLC configuration in which each cell is configured to encode 3 bits. This configuration is commonly referred to as TLC (Three-Level Cell) memory. The same notations apply here as with Figures 4A-4B. The programmed pages are labeled pages 0-11 with U and L designations and the word lines are labeled accordingly. Here, each lower page is paired with two upper pages. For example, page 0 is paired with upper pages 4 and 10. Pages 2, 3, 6, and 7 are open lower pages. Accordingly to one embodiment, if the controller finds the memory in this illustrated state, these pages would be selected for reprogramming. Note that pages 2 and 3 are considered open pages even though they are already paired with programmed upper pages 8 and 9. This is because each of pages 2 and 3 has one more upper page to be programmed. Again, reprogramming these few open pages is more efficient than reprogramming the entire block of memory.

Lower Page Only Reprogramming

Figure 6 is a flow diagram illustrating a process of reprogramming lower page programmed only cells according to one embodiment of the invention. Another situation the lower page recovery program may be useful is where only lower pages are programmed for data storage. Typically these pages are in memory blocks that have been designated to operate in a lower page only or SLC mode. Alternatively, the same scenario can occur in SLC memory. Because the upper pages are not programmed, lower page corruption problem does not occur. However, there are instances where reprogramming may nonetheless be useful to preserve data integrity. For example, in one embodiment, when the storage system finds that the data are close to some predefined criteria, recovery program may be then applied to bring the programmed voltage level back up to where it is supposed to be.

In Figure 6, the method 600 may be performed by the controller 130. The method starts at block 610 where one or more data integrity conditions are checked. Error rate such as bit failure rate and/or error correction effort applied (e.g., in the LDPC decoding and/or RAID recovery) from recent reads may be indications of the data integrity condition. The rates/conditions may be obtained from reads that are performed as part of a scanning process. In addition, other useable indications of integrity condition may include program erase cycle counter values and time lapsed approximated by voltage reference drift measured in reference pages/blocks. These conditions may be compared against a threshold metric at block 315, and when certain pre-defined conditions for triggering recovery are met, the method goes to block 320 to read data from these pages where only lower page are programmed. The read data is corrected (e.g., through the application of ECC) at block 325. Then at block 330 the corrected data is reprogrammed back to the pages. As previously shown in Figure 2A, the voltage distribution of the cells in these pages now closely resembles the distribution when they were initially programmed.

Other Variations

Those skilled in the art will appreciate that in some embodiments, other approaches and methods can be used. For example, if multi-pass programming is allowed for upper pages by finite-state machine on NAND flash chips, it is also possible to apply the methods in the various embodiments for upper page data

recovery. For example, some upper pages may be causing an amount of errors that is near the correction limit of the ECC and may benefit from reprogramming to move the voltage levels to near the original programmed levels. In addition, the non-volatile memory array 140 can be implemented using memory devices other than NAND flash memory devices. Other types of solid-state memory devices can alternatively be used, such as array of flash integrated circuits, Chalcogenide RAM (C-RAM), Phase Change Memory (PC-RAM or PRAM), Programmable Metallization Cell RAM (PMC-RAM or PMCm), Ovonic Unified Memory (OUM), Resistance RAM (RRAM), NOR memory, EEPROM, Ferroelectric Memory (FeRAM), Magnetoresistive RAM (MRAM), other discrete NVM (non-volatile memory) chips, or any combination thereof. In one embodiment, the non-volatile memory array 140 preferably includes multi-level cell (MLC) devices having multi-level cells capable of storing more than a single bit of information, although single-level cell (SLC) memory devices or a combination of SLC and MLC devices may be used. In one embodiment, the storage system 120 can include other memory modules, such as one or more magnetic memory modules. The storage system 120 can further include other types of storage media, such as magnetic storage. Accordingly, the scope of the present disclosure is intended to be defined only by reference to the appended claims.

While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the protection. Indeed, the novel methods and systems described herein may be embodied in a variety of other forms. Furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the protection. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the protection. For example, the systems and methods disclosed herein can be applied to hybrid hard drives and the like. In addition, other forms of storage (e.g., DRAM or SRAM, battery backed-up volatile DRAM or SRAM devices, EPROM, EEPROM memory, etc.) may additionally or alternatively be used. As another example, the various components illustrated in the figures may be implemented as software and/or firmware on a processor, ASIC/FPGA, or dedicated hardware. Also, the features and attributes of the specific embodiments disclosed above may be combined in different ways to form additional embodiments, all of

which fall within the scope of the present disclosure. Although the present disclosure provides certain preferred embodiments and applications, other embodiments that are apparent to those of ordinary skill in the art, including embodiments which do not provide all of the features and advantages set forth herein, are also within the scope of this disclosure. Accordingly, the scope of the present disclosure is intended to be defined only by reference to the appended claims.

WHAT IS CLAIMED IS:

1. A solid-state storage system, including:

a non-volatile memory array including a plurality of memory blocks, each memory block including lower memory pages paired with upper memory pages; and

a controller configured to:

select, from the memory blocks, a programmed lower memory page that has a paired upper memory page that has not been programmed;

read data from the selected lower memory page;

apply error correction to the read data to generated corrected data; and

program the corrected data to the selected lower memory page.

2. The solid-state storage system of claim 1, wherein the non-volatile memory array comprises multi-level memory (MLC) cells.

3. The solid-state storage system of claim 1, wherein the controller is configured to select the programmed lower memory page from an open memory block of the memory blocks.

4. A solid-state storage system, including:

a non-volatile memory array including a plurality of memory blocks, each including a plurality of memory pages; and

a controller configured to:

determine whether a state of the storage system meets a pre-defined condition to initiate data recovery;

in response to determining that the state of the storage system meets a pre-defined condition to initiate data recovery, select, from the memory blocks, a memory page from a memory block;

read data from the selected memory page;

apply error correction to the read data to generated corrected data; and

program the corrected data to the selected memory page.

5. The solid-state storage system of claim 4, wherein the state of the storage system includes a state of a memory page in a reference memory block.

6. The solid-state storage system of claim 5, wherein the state of the memory page in the reference memory block comprises a failure bit rate.

7. The solid-state storage system of claim 6, wherein failure bit rate is used to approximate time lapsed since last programmed.

8. The solid-state storage system of claim 6, wherein the state of the storage system includes a failure bit rate that is obtained from a scanning process.

9. The solid-state storage system of claim 4, wherein the non-volatile memory array comprises multi-level memory (MLC) cells and the memory page is in a memory block that is lower-page only programmed.

10. The solid-state storage system of claim 4, wherein the non-volatile memory array comprises single-level memory (SLC) cells.

11. The solid-state storage system of claim 4, wherein the controller is configured to determine whether the state of the storage system meets the pre-defined condition to initiate data recovery as part of a startup sequence.

12. A method of preserving data integrity in a solid-state storage system that includes a non-volatile memory array including a plurality of memory blocks, each including a plurality of memory pages, the method including:

selecting, from the memory blocks, a programmed lower memory page that has a paired upper memory page that has not been programmed;

reading data from the selected lower memory page;

applying error correction to the read data to generated corrected data; and

programming the corrected data to the selected lower memory page.

13. The method of claim 12, wherein the non-volatile memory array comprises multi-level memory (MLC) cells.

14. The method of claim 12, wherein selecting comprises selecting the programmed lower memory page from an open memory block of the memory blocks.

15. A method of preserving data integrity in a solid-state storage system that includes a non-volatile memory array including a plurality of memory blocks, each including a plurality of memory pages, the method including:

determining whether a state of the storage system meets a pre-defined condition to initiate data recovery;

in response to determining that the state of the storage system meets a pre-defined condition to initiate data recovery, selecting, from the memory blocks, a memory page from a memory block;

reading data from the selected memory page;

applying error correction to the read data to generated corrected data; and

programming the corrected data to the selected memory page.

16. The method of claim 15, wherein the state of the storage system includes a state of a memory page in a reference memory block.

17. The method of claim 16, wherein the state of the memory page in the reference memory block comprises a failure bit rate.

18. The method of claim 17, wherein failure bit rate is used to approximate time lapsed since last programmed.

19. The method of claim 17, wherein the state of the storage system includes a failure bit rate that is obtained from a scanning process.

20. The method of claim 15, wherein the non-volatile memory array comprises multi-level memory (MLC) cells and the memory page is in a memory block that is lower-page only programmed.

21. The method of claim 15, wherein the non-volatile memory array comprises single-level memory (SLC) cells.

22. The method of claim 15, wherein determining whether the state of the storage system meets the pre-defined condition to initiate data recovery is performed as part of a startup sequence.

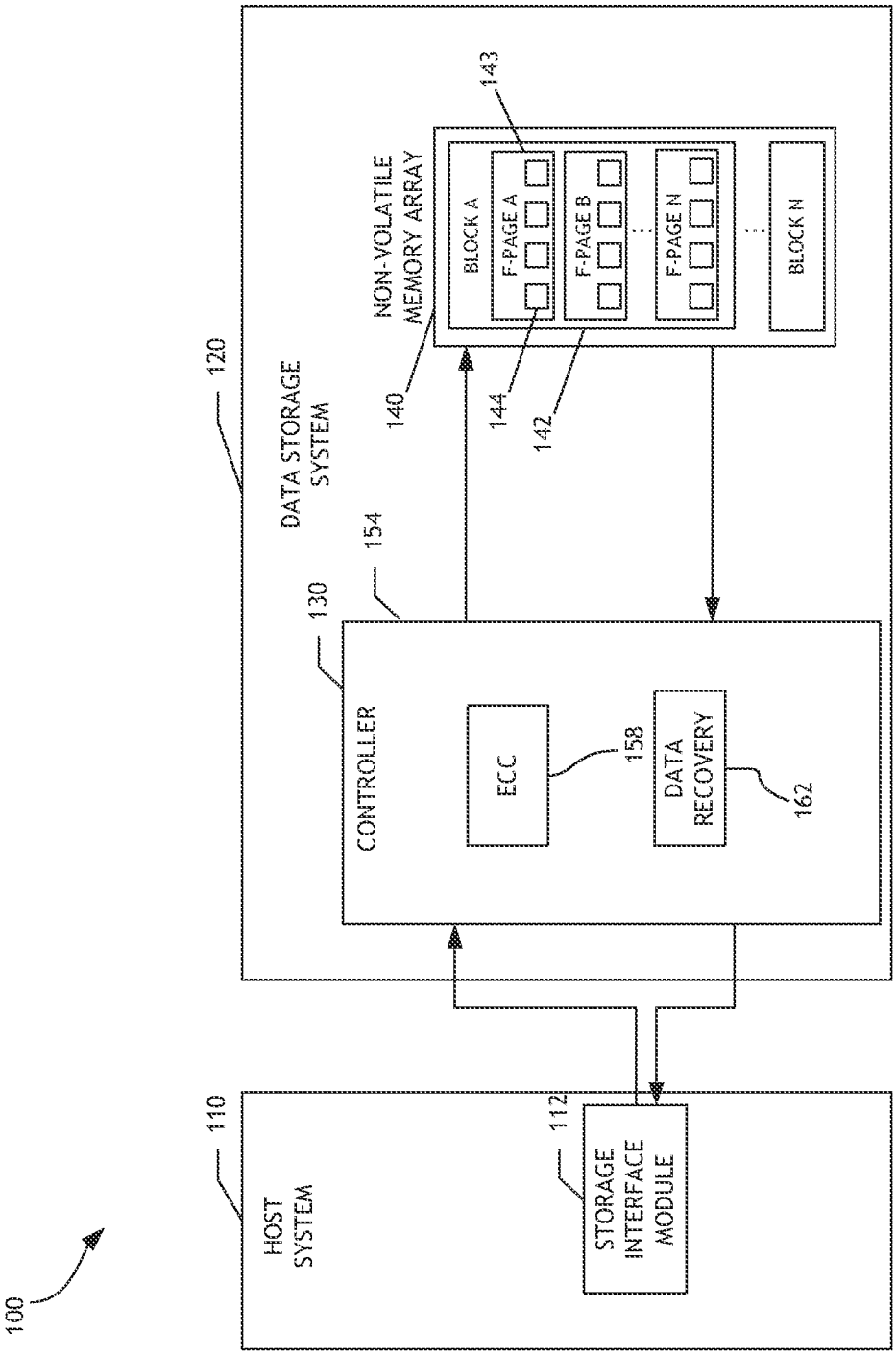
100
HOST SYSTEM
110
STORAGE INTERFACE MODULE
112
DATA STORAGE SYSTEM
120
CONTROLLER
130
154
ECC
158
DATA RECOVERY
162
NON-VOLATILE MEMORY ARRAY
140
143
BLOCK A
F-PAGE A
F-PAGE B
F-PAGE N
BLOCK N
144
142

FIGURE 1

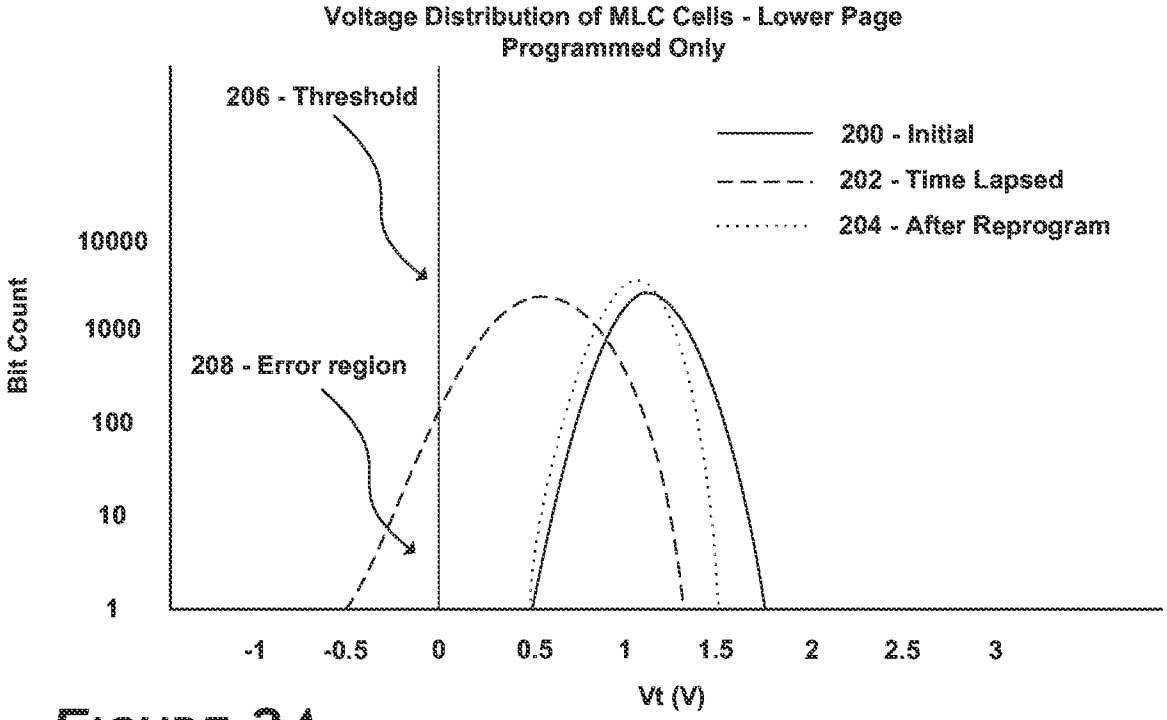


FIGURE 2A

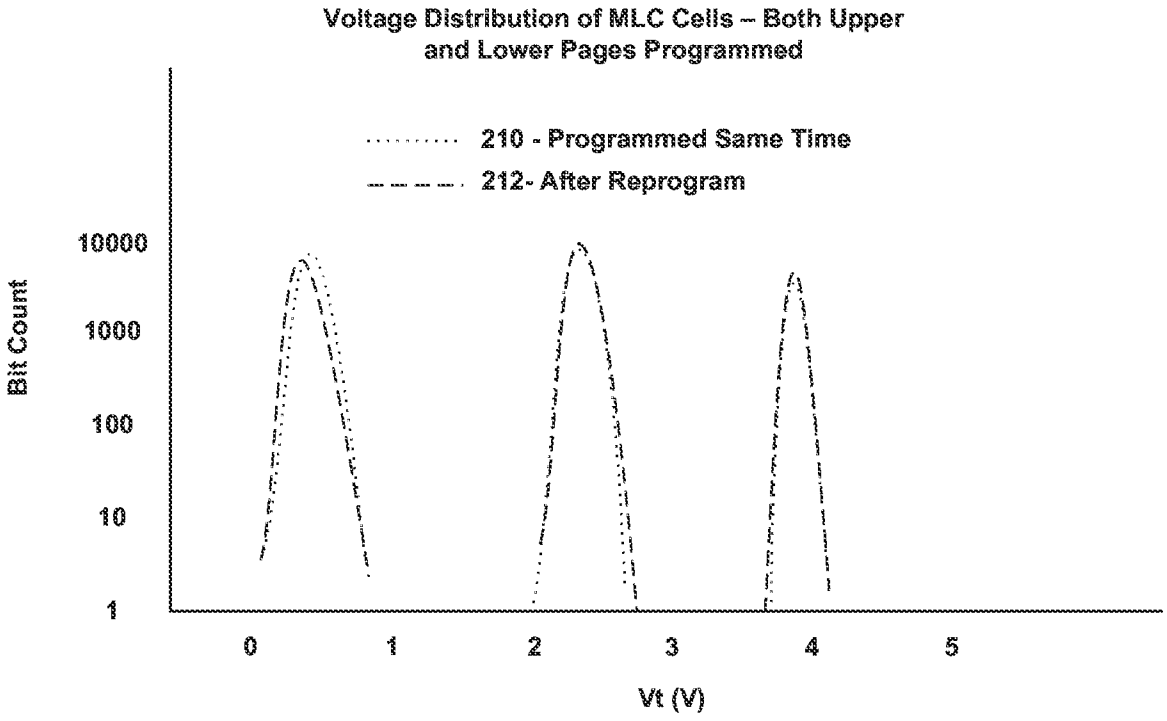


FIGURE 2B

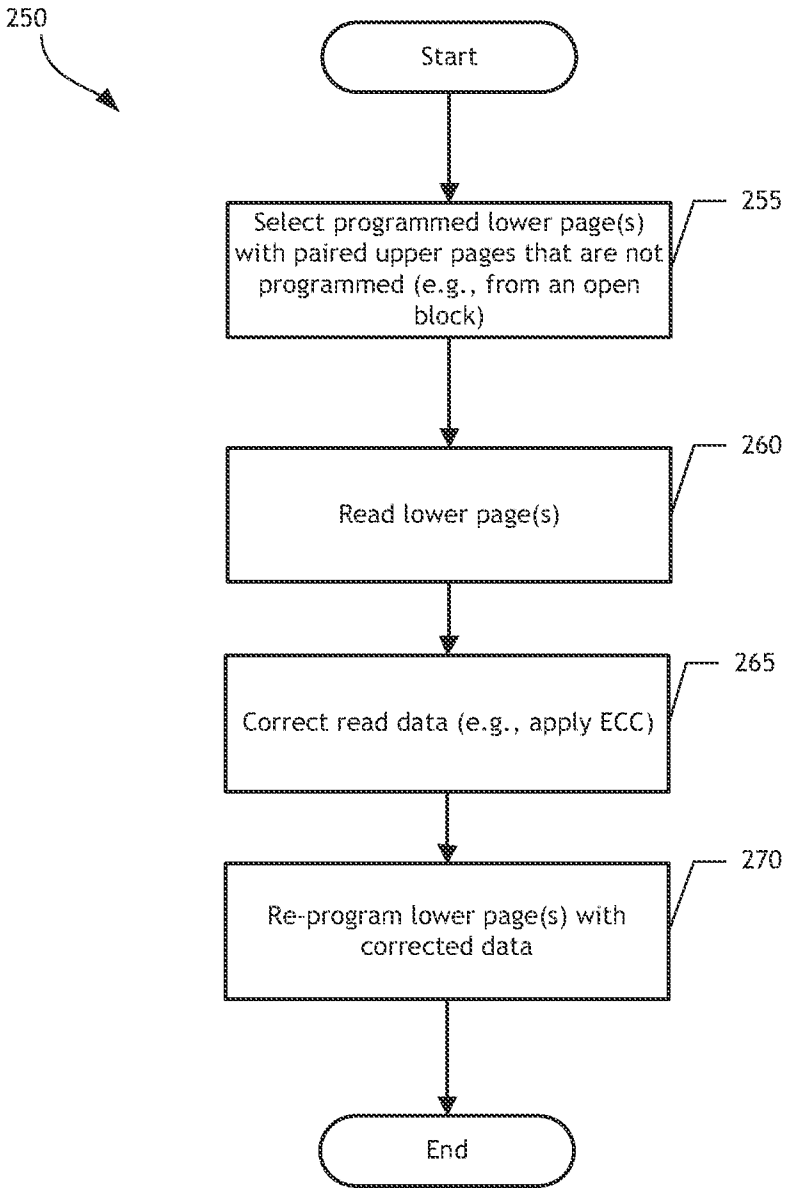
250
Start
Select programmed lower page(s) with paired upper pages that are not programmed (e.g., from an open block)
255
Read lower page(s)
260
Correct read data (e.g., apply ECC)
265
Re-program lower page(s) with corrected data
270
End

FIGURE 3

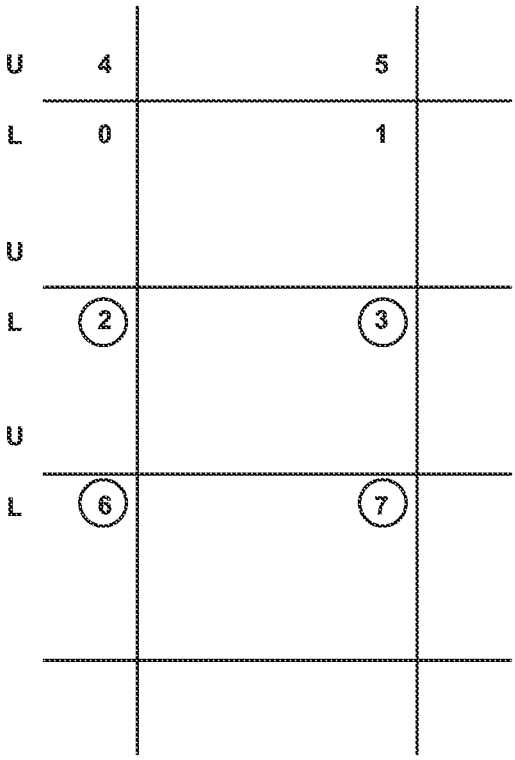


FIGURE 4A

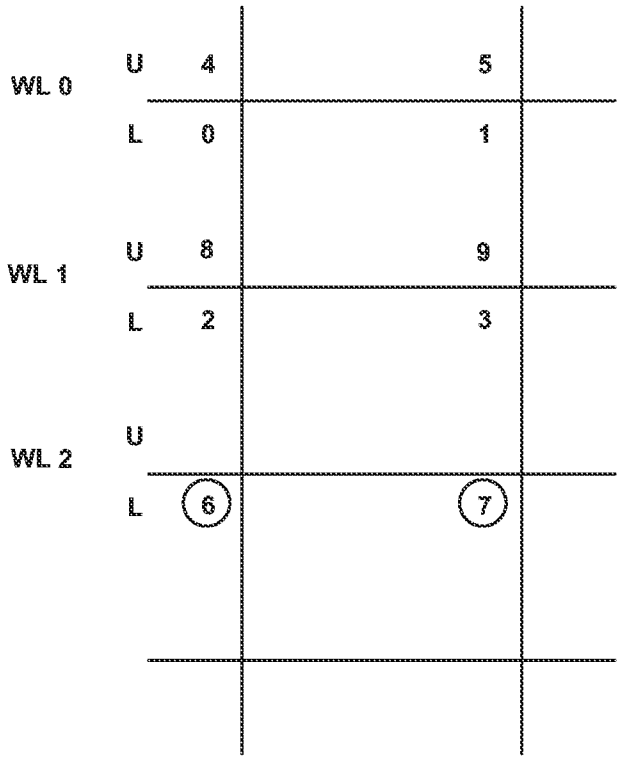


FIGURE 4B

◯ = open lower page

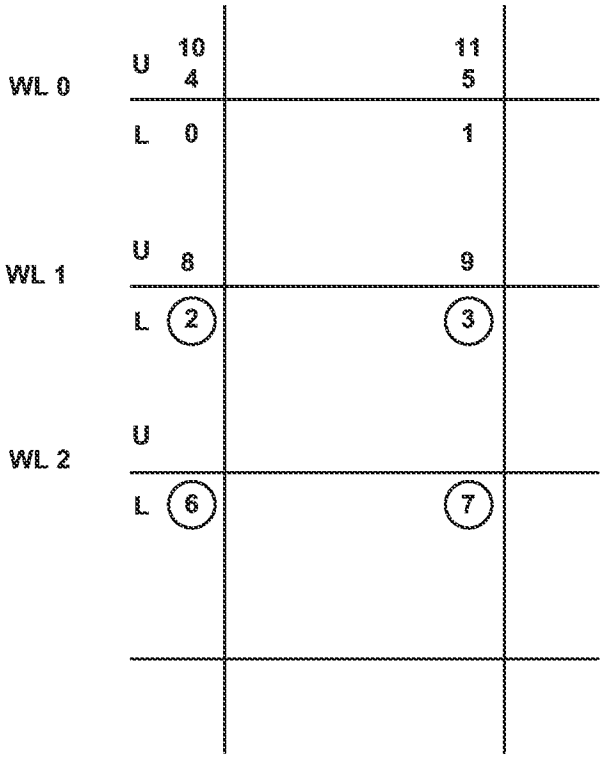


FIGURE 5

◯ = open lower page

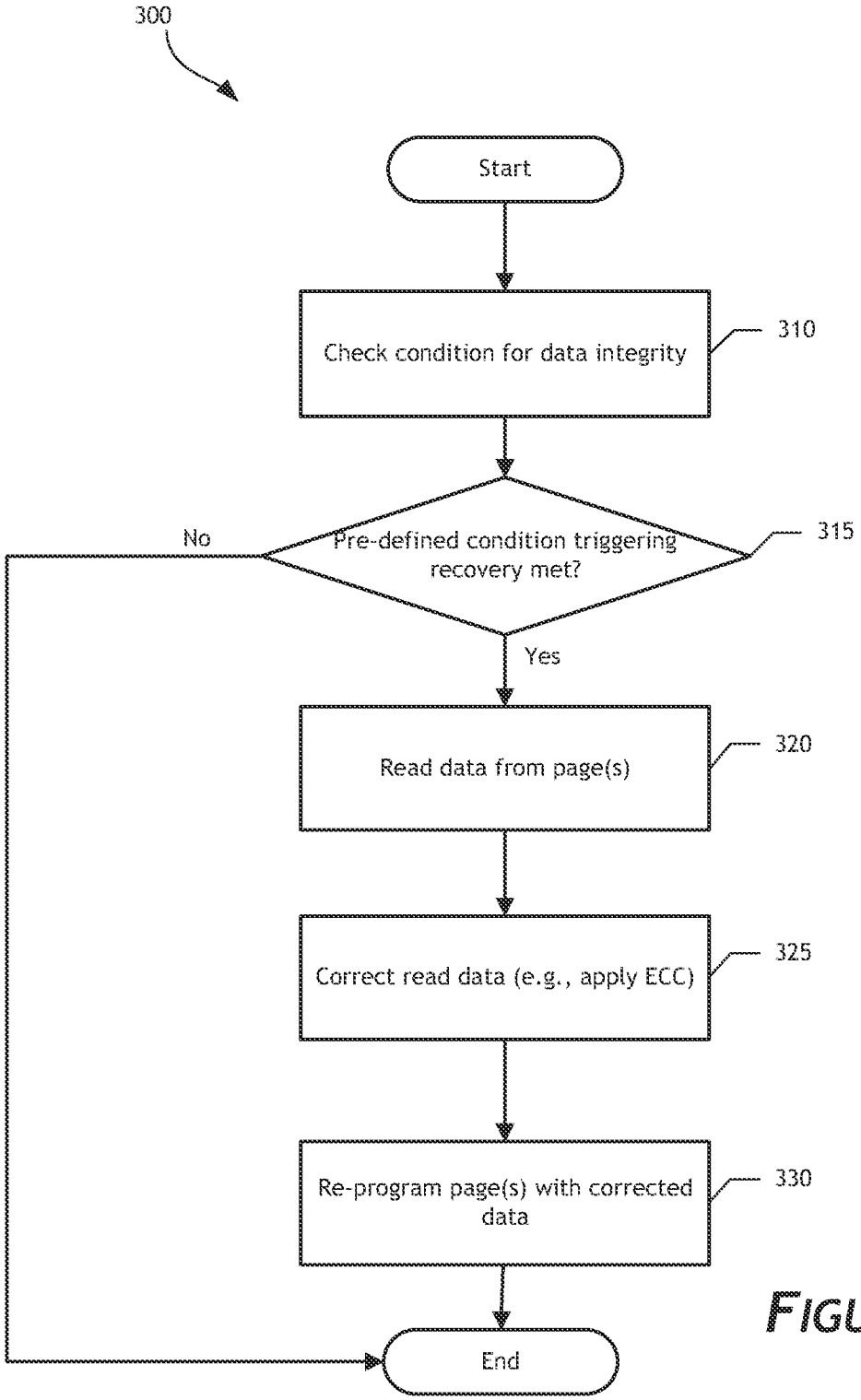
300
Start
Check condition for data integrity
310
Pre-defined condition triggering recovery met?
315
No
Yes
Read data from page(s)
320
Correct read data (e.g., apply ECC)
325
Re-program page(s) with corrected data
330
End

FIGURE 6

**INTERNATIONAL SEARCH REPORT**

International application No.
**PCT/US2013/061608**

**A. CLASSIFICATION OF SUBJECT MATTER**

**G06F 12/16(2006.01)i, G06F 11/08(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)
G06F 12/16; H03M 13/05; G11C 16/04; G06F 11/10; G06F 11/14; G06F 12/00; G06F 12/08; G06F 11/08

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: lower page, upper page, non-volatile memory, data recovery, error correction, and similar terms.

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A | US 2012-0054582 A1 (BYOM, MATTHEW et al.) 01 March 2012<br>See paragraphs [0032]-[0047] and [0061]-[0074]; claim 9; and figures 2 and 6. | 1-22 |
| A | US 2010-0318839 A1 (AVILA, CHRIS NGA YEE et al.) 16 December 2010<br>See paragraphs [0033]-[0037] and [0049]; claims 1 and 12; and figures 3 and 8. | 1-22 |
| A | US 2011-0202710 A1 (ZHAO, QUN et al.) 18 August 2011<br>See paragraphs [0018]-[0028]; claim 1; and figures 1-3. | 1-22 |
| A | US 2008-0177934 A1 (YU, JAE-SUNG et al.) 24 July 2008<br>See paragraphs [0058]-[0081] and [0104]-[0120]; claim 15; and figures 3-4 and 7. | 1-22 |
| A | US 2010-0246260 A1 (KANG, DONGKU) 30 September 2010<br>See paragraphs [0089]-[0094] and [0113]-[0122]; claim 14; and figures 5 and 10. | 1-22 |
| A | US 2010-0157675 A1 (SHALVI, OFIR et al.) 24 June 2010<br>See paragraphs [0058]-[0083]; claim 17; and figures 1-2. | 1-22 |

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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| Date of the actual completion of the international search | Date of mailing of the international search report |
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**INTERNATIONAL SEARCH REPORT**

Information on patent family members

International application No.
**PCT/US2013/061608**

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