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(54) Title: METHOD AND SYSTEM FOR MONITORING AND SELF-RECOVERY OF RADIO UNIT

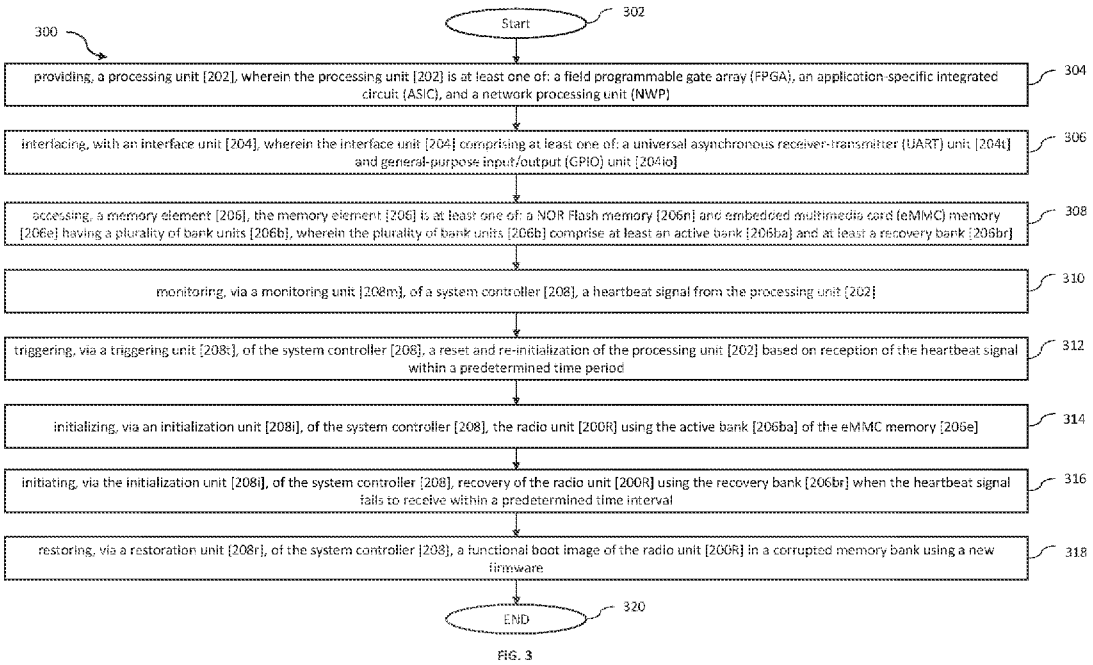


FIG. 3

(57) Abstract: The present disclosure relates to a method and a system for automatic monitoring and self-recovery of a radio unit in a 5G radio network The disclosure encompasses providing a processing unit [202] as one of a FPGA, an ASIC, and a NWP; interfacing, with an interface unit [204] comprising at least one of: a UART unit [204t] and GPIO unit [204io]; accessing, a memory element [206] as one of a NOR Flash memory [206n] and embedded multimedia card (eMMC) memory [206e] having a plurality of bank units [206b]; monitoring a heartbeat signal; triggering a reset and re- initialization based on reception of the heartbeat signal; initializing the radio unit [200r]; initiating recovery of the radio unit [200r] when the heartbeat signal fails; and restoring a functional boot image of the radio unit [200r] using a new firmware.

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METHOD AND SYSTEM FOR MONITORING AND SELF-RECOVERY OF RADIO UNIT

FIELD OF INVENTION

[0001] Embodiments of the present disclosure generally relate to network performance management systems. More particularly, embodiments of the present disclosure relate to monitoring and self-recovery of a radio unit in a 5G radio network.

BACKGROUND

[0002] The following description of the related art is intended to provide background information pertaining to the field of the disclosure. This section may include certain aspects of the art that may be related to various features of the present disclosure. However, it should be appreciated that this section is used only to enhance the understanding of the reader with respect to the present disclosure, and not as admissions of the prior art.

[0003] Wireless communication technology has rapidly evolved over the past few decades, with each generation bringing significant improvements and advancements. The first generation of wireless communication technology was based on analog technology and offered only voice services. However, with the advent of the second generation (2G) technology, digital communication and data services became possible, and text messaging was introduced. 3G technology marked the introduction of high-speed internet access, mobile video calling, and location-based services. The fourth generation (4G) technology revolutionized wireless communication with faster data speeds, better network coverage, and improved security. Currently, the fifth generation (5G) technology is being deployed, promising even faster data speeds, low latency, and the ability to connect multiple devices simultaneously. With each generation, wireless communication technology has become more advanced, sophisticated, and capable of delivering more services to its users.

[0004] Automatic monitoring and self-recovery systems play a crucial role in ensuring the reliability and stability of 5G radio networks. However, they do have certain limitations that need to be considered.

[0005] Firstly, in the current existing solutions, 5G radio networks operate in a highly complex environment with numerous network elements, including base stations, small cells, and user devices. This complexity introduces challenges for automatic monitoring and self-recovery systems. The sheer volume of network components and their interconnectedness make it difficult to accurately detect and diagnose issues. Some problems may go unnoticed or may be misdiagnosed, leading to inadequate self-recovery measures. The complexity of the network environment also increases the time required for recovery, potentially impacting service quality and user experience.

[0006] Further, in the current existing solutions, automatic monitoring systems rely on real-time data and analytics to identify anomalies and potential issues. However, these systems often lack the ability to understand the contextual information surrounding the detected problems. They may detect performance degradation or service interruptions but may fail to determine the underlying cause or impact on end-users. Without a comprehensive understanding of the context, self-recovery mechanisms may be limited in their effectiveness. It becomes challenging to differentiate between transient issues that can be resolved automatically and more critical problems requiring human intervention.

[0007] Furthermore, in the current existing solutions while self-recovery mechanisms in 5G radio networks can handle certain types of faults and failures, their scope is often limited. They are designed to address specific predefined scenarios and may not cover all potential failure modes. Complex and uncommon issues that fall outside the predefined parameters may require manual intervention from network operators or engineers. Additionally, self-recovery mechanisms may focus primarily on restoring network connectivity rather than addressing underlying performance issues or optimizing resource allocation. This limitation can impact the network's ability to adapt to dynamic conditions and optimize performance for different user demands.

[0008] Thus, there exists an imperative need in the art to provide a method and system for monitoring and self-recovery of radio unit.

SUMMARY

[0009] This section is provided to introduce certain aspects of the present disclosure in a simplified form that are further described below in the detailed description. This summary is not intended to identify the key features or the scope of the claimed subject matter.

[0010] An aspect of the present disclosure may relate to a method for monitoring and self-recovery of a radio unit in a 5G radio network. The method comprises providing, a processing unit. The processing unit may be at least one of: a field programmable gate array (FPGA), an application-specific integrated circuit (ASIC), and a network processing unit (NWP). The method further comprises interfacing, with an interface unit. The interface unit may comprise at least one of: a universal asynchronous receiver-transmitter (UART) unit and general-purpose input/output (GPIO) unit. The method further comprises accessing, a memory element. The memory element may be at least one of: a NOR Flash memory and embedded multimedia card (eMMC) memory having a plurality of bank units. The plurality of bank units may comprise at least an active bank and at least a recovery bank. The method further comprises monitoring, via a monitoring unit of a system controller, a heartbeat signal from the processing unit. The method further comprises triggering, via a triggering unit of the system controller, a reset and re-initialization of the processing unit based on reception of the heartbeat signal within a predetermined time period. The method further comprises initializing, via an initialization unit of the system controller, the radio unit using the active bank of the eMMC memory. The method further comprises initiating, via the initialization unit of the system controller, recovery of the radio unit using the recovery bank when the heartbeat signal fails to be received within a predetermined time interval. Thereafter, the method also comprises restoring, via a restoration unit of the system controller, a functional boot image of the radio unit in a corrupted memory bank using a new firmware.

[0011] In an exemplary aspect of the present disclosure, the method further comprises storing the functional boot image and a root file system by forming a connection between the processing unit and the memory element.

[0012] In an exemplary aspect of the present disclosure, the heartbeat signal comprises a continuous signal on the GPIO unit.

[0013] In an exemplary aspect of the present disclosure, the eMMC memory is partitioned into two primary bank units of the plurality of bank units, the two primary bank units being configured to have a respective firmware image each.

[0014] In an exemplary aspect of the present disclosure, each of the primary bank units is sub-divided into at least four partitions. It is to be noted that the at least four partitions are configured

to carry critical configuration for individual sub-sections of the processing unit. It is further noted that the individual sub-sections are configured to be executed sequentially.

[0015] Another aspect of the present disclosure may relate to a system for monitoring and self-recovery of a radio unit in a 5G radio network. The system comprises a processing unit which may be at least one of: a field programmable gate array (FPGA), an application-specific integrated circuit (ASIC) and a network processing unit (NWP). The system further comprises an interface unit that further comprises at least one of: a universal asynchronous receiver-transmitter (UART) unit and a general-purpose input/output (GPIO) unit. The system further comprises a memory element that may be at least one of: a NOR Flash memory and an embedded multimedia card (eMMC) memory with a plurality of bank units. The plurality of bank units may comprise at least an active bank and a recovery bank. The system further comprises a system controller configured to monitor, via a monitoring unit, a heartbeat signal from the processing unit. The system controller is further configured to trigger, via a triggering unit, a reset and re-initialization of the processing unit based on reception of the heartbeat signal within a predetermined time period. The system controller is further configured to initialize, via an initialization unit, the radio unit using the active bank of the eMMC memory. The system controller is further configured to initiate, via the initialization unit, recovery of the radio unit using the recovery bank when the heartbeat signal fails to be received within a predetermined time interval. Furthermore, the system controller is further configured to restore, via a restoration unit, a functional boot image of the radio unit in a corrupted memory bank using a new firmware.

[0016] The present disclosure further discloses a non-transitory computer readable storage medium storing instructions for monitoring and self-recovery of a radio unit in a 5G radio network, the instructions include executable code which, when executed by one or more units of a system, causes a system controller [208] to: monitor, via a monitoring unit [208m], a heartbeat signal from a processing unit [202]. Further, the instructions include executable code, which when executed causes a triggering unit [208t] to trigger a reset and re-initialization of the processing unit [202] based on reception of the heartbeat signal within a predetermined time period. Further, the instructions include executable code, which when executed causes an initialization unit [208i] to initialize the radio unit [200r] using an active bank [206ba] of an eMMC memory [206e]. Further, the instructions include executable code, which when executed causes the initialization unit [208i] to initiate recovery of the radio unit [200r] using a recovery bank [206br] when the heartbeat signal fails to be received within a predetermined time interval. Further, the instructions include

executable code, which when executed causes a restoration unit [208r] to restore a functional boot image of the radio unit [200r] in a corrupted memory bank using a new firmware.

OBJECTS OF THE DISCLOSURE

[0017] Some of the objects of the present disclosure, which at least one embodiment disclosed herein satisfies are listed herein below.

[0018] One primary object of the disclosure is to auto-recover a radio system in case of firmware failure or crash.

[0019] An object of the disclosure is to provide a unique hardware system using low-cost microcontroller unit (MCU) which detects the radio unit fault while measuring heartbeat of the ASICs/FPGA/Network Processors (NWP) in a 5G communication network.

[0020] Another object of the disclosure is to recover the radio unit from stuck or hung state during the data transmission in the 5G network.

[0021] Another object of the disclosure is to enhance the radio unit recovery in case of software crash.

[0022] Yet another object of the proposed disclosure is to enable a failure recovery system in 5G Radios that responds during run time upon detecting an abnormal fault in the system.

DESCRIPTION OF THE DRAWINGS

[0023] The accompanying drawings, which are incorporated herein, and constitute a part of this disclosure, illustrate exemplary embodiments of the disclosed methods and systems in which like reference numerals refer to the same parts throughout the different drawings. Components in the drawings are not necessarily to scale, emphasis instead being placed upon clearly illustrating the principles of the present disclosure. Also, the embodiments shown in the figures are not to be construed as limiting the disclosure, but the possible variants of the method and system according to the disclosure are illustrated herein to highlight the advantages of the disclosure. It will be appreciated by those skilled in the art that disclosure of such drawings includes disclosure of electrical components or circuitry commonly used to implement such components.

[0024] FIG. 1 illustrates an exemplary block diagram of a computing device upon which the features of the present disclosure may be implemented in accordance with exemplary implementation of the present disclosure.

[0025] FIG. 2 illustrates an exemplary block diagram of a system for monitoring and self-recovery of a radio unit in a 5G radio network, in accordance with exemplary implementations of the present disclosure.

[0026] FIG. 3 illustrates a method flow diagram for monitoring and self-recovery of a radio unit in a 5G radio network, in accordance with exemplary implementations of the present disclosure.

[0027] FIG. 4A illustrates an exemplary auto-recovery system architecture, in accordance with exemplary embodiments of the present disclosure.

[0028] FIG. 4B illustrates an exemplary example of bootable memory element partition architecture, in accordance with exemplary embodiments of the present disclosure.

[0029] The foregoing shall be more apparent from the following more detailed description of the disclosure.

DETAILED DESCRIPTION

[0030] In the following description, for the purposes of explanation, various specific details are set forth in order to provide a thorough understanding of embodiments of the present disclosure. It will be apparent, however, that embodiments of the present disclosure may be practiced without these specific details. Several features described hereafter may each be used independently of one another or with any combination of other features. An individual feature may not address any of the problems discussed above or might address only some of the problems discussed above.

[0031] The ensuing description provides exemplary embodiments only, and is not intended to limit the scope, applicability, or configuration of the disclosure. Rather, the ensuing description of the exemplary embodiments will provide those skilled in the art with an enabling description for implementing an exemplary embodiment. It should be understood that various changes may be

made in the function and arrangement of elements without departing from the spirit and scope of the disclosure as set forth.

[0032] Specific details are given in the following description to provide a thorough understanding of the embodiments. However, it will be understood by one of ordinary skill in the art that the embodiments may be practiced without these specific details. For example, circuits, systems, processes, and other components may be shown as components in block diagram form in order not to obscure the embodiments in unnecessary detail.

[0033] Also, it is noted that individual embodiments may be described as a process which is depicted as a flowchart, a flow diagram, a data flow diagram, a structure diagram, or a block diagram. Although a flowchart may describe the operations as a sequential process, many of the operations may be performed in parallel or concurrently. In addition, the order of the operations may be re-arranged. A process is terminated when its operations are completed but could have additional steps not included in a figure.

[0034] The word "exemplary" and/or "demonstrative" is used herein to mean serving as an example, instance, or illustration. For the avoidance of doubt, the subject matter disclosed herein is not limited by such examples. In addition, any aspect or design described herein as "exemplary" and/or "demonstrative" is not necessarily to be construed as preferred or advantageous over other aspects or designs, nor is it meant to preclude equivalent exemplary structures and techniques known to those of ordinary skill in the art. Furthermore, to the extent that the terms "includes," "has," "contains," and other similar words are used in either the detailed description or the claims, such terms are intended to be inclusive—in a manner similar to the term "comprising" as an open transition word—without precluding any additional or other elements.

[0035] As used herein, a "processing unit" or "processor" or "operating processor" or "microcontroller unit" includes one or more processors, wherein processor refers to any logic circuitry for processing instructions. A processor may be a general-purpose processor, a special purpose processor, a conventional processor, a digital signal processor, a plurality of microprocessors, one or more microprocessors in association with a (Digital Signal Processing) DSP core, a controller, a microcontroller, Application Specific Integrated Circuits, Field Programmable Gate Array circuits, any other type of integrated circuits, etc. The processor may perform signal coding data processing, input/output processing, and/or any other functionality that

enables the working of the system according to the present disclosure. More specifically, the processor or processing unit is a hardware processor.

[0036] As used herein, "a user equipment", "a user device", "a smart-user-device", "a smart-device", "an electronic device", "a mobile device", "a handheld device", "a wireless communication device", "a mobile communication device", "a communication device" may be any electrical, electronic and/or computing device or equipment, capable of implementing the features of the present disclosure. The user equipment/device may include, but is not limited to, a mobile phone, smart phone, laptop, a general-purpose computer, desktop, personal digital assistant, tablet computer, wearable device or any other computing device which is capable of implementing the features of the present disclosure. Also, the user device may contain at least one input means configured to receive an input from at least one of a transceiver unit, a processing unit, a storage unit, a detection unit and any other such unit(s) which are required to implement the features of the present disclosure.

[0037] As used herein, "storage unit" or "memory unit" refers to a machine or computer-readable medium including any mechanism for storing information in a form readable by a computer or similar machine. For example, a computer-readable medium includes read-only memory ("ROM"), random access memory ("RAM"), magnetic disk storage media, optical storage media, flash memory devices or other types of machine-accessible storage media. The storage unit stores at least the data that may be required by one or more units of the system to perform their respective functions.

[0038] As used herein "interface" or "user interface refers to a shared boundary across which two or more separate components of a system exchange information or data. The interface may also be referred to a set of rules or protocols that define communication or interaction of one or more modules or one or more units with each other, which also includes the methods, functions, or procedures that may be called.

[0039] All modules, units, components used herein, unless explicitly excluded herein, may be software modules or hardware processors, the processors being a general-purpose processor, a special purpose processor, a conventional processor, a digital signal processor (DSP), a plurality of microprocessors, one or more microprocessors in association with a DSP core, a controller, a microcontroller, Application Specific Integrated Circuits (ASIC), Field Programmable Gate Array circuits (FPGA), any other type of integrated circuits, etc.

[0040] As used herein the transceiver unit include at least one receiver and at least one transmitter configured respectively for receiving and transmitting data, signals, information or a combination thereof between units/components within the system and/or connected with the system.

[0041] As discussed in the background section, the current known solutions have several shortcomings. The present disclosure aims to overcome the above-mentioned and other existing problems in this field of technology by providing method and system of monitoring and self-recovery of a radio unit in a 5G radio network.

[0042] As used herein, a radio unit refers to a component of a telecommunications network, specifically designed to handle wireless communications within a 5G radio network. It is responsible for transmitting and receiving radio signals between user devices and the network infrastructure. The radio unit includes various processing units such as ASICs, FPGAs, or network processors, interfaces like UART and GPIO, and memory elements such as NOR Flash or eMMC memory.

[0043] As used herein, general-purpose input/output (GPIO) refers to a type of pin found on an integrated circuit or microcontroller that can be configured by the user to function either as an input or an output, enabling interaction with various electronic components and peripherals. GPIO pins can be programmed to read signals from sensors, buttons, or other devices, and to send control signals to actuators, LEDs, or other circuit elements, thereby providing flexibility and control in a wide range of applications.

[0044] As used herein, application-specific integrated circuit (ASIC) refers to a type of integrated circuit (IC) that is custom-designed for a specific application or purpose rather than for general-purpose use. Unlike standard ICs, which can perform a wide range of functions, ASICs are tailored to meet particular requirements of a specific device or system, offering optimized performance, lower power consumption, and increased efficiency for that specific task.

[0045] As used herein, field programmable gate array (FPGA) refers to a type of integrated circuit that can be configured by the user after manufacturing. Unlike fixed-function chips, FPGAs are designed to be programmed with custom logic and functionality to suit specific applications. This flexibility allows for rapid prototyping, iterative design, and deployment in a wide range of industries, including telecommunications, automotive, and consumer electronics. The FPGA

consists of an array of programmable logic blocks and interconnects that can be reconfigured to perform complex computational tasks efficiently.

[0046] As used herein, network processing unit (NWP) refers to a specialized microprocessor designed to handle network communications and data packet processing tasks at high speeds. NWPs are optimized for tasks such as routing, switching, load balancing, and firewall operations, ensuring efficient data flow within a network.

[0047] As used herein, universal asynchronous receiver-transmitter (UART) refers to a hardware communication protocol that allows asynchronous serial communication between devices. It converts parallel data from a microcontroller into serial form for transmission and vice versa for received data. UART is widely used for short-distance, low-speed, and low-cost data exchange between computer and peripheral devices, enabling seamless data transfer without the need for synchronized clocks.

[0048] As used herein, embedded multimedia card (eMMC) refers to an integrated data storage solution that combines flash memory and a flash memory controller within a single package. eMMC provides a standardized interface for simplifying the design and integration process in electronic devices. It is commonly used in mobile phones, tablets, and other compact devices to store operating systems, applications, and user data, offering a balance of performance, reliability, and cost-effectiveness.

[0049] As used herein, network processing unit (NWP) refers to a specialized microprocessor designed to handle data packet processing tasks in a network. Unlike general-purpose processors, NWPs are optimized for network operations, such as routing, switching, and managing network traffic efficiently. The NWP offload these tasks from the main CPU, allowing for higher throughput and reduced latency in network communications. NWPs are integral in managing the complex data flows of modern networks, ensuring fast, reliable, and secure data transmission across various network infrastructures.

[0050] As used herein, NOR Flash memory refers to a type of non-volatile storage technology that retains data without the need for a power supply, characterized by its ability to randomly access individual memory locations. The NOR Flash memory is known for its fast read speeds, making it ideal for applications requiring quick access to data, such as in embedded systems and firmware storage. NOR Flash memory structures its cells in a way that enables direct read operations, similar

to traditional ROM, providing reliable and durable storage for critical system code and configurations.

[0051] As used herein, recovery bank refers to a designated partition within the eMMC memory that stores a backup firmware image. This backup is utilized when the primary firmware in the active bank becomes corrupted or fails, enabling the system to automatically switch to the recovery bank to restore functionality. The recovery bank ensures continuity and reliability by providing an alternative firmware image for system recovery, thereby minimizing downtime and the need for manual intervention.

[0052] As used herein, active bank refers to the primary partition within the eMMC memory that contains the default firmware image and is responsible for the initial boot and normal operation of the radio unit. This active bank is the main operational segment that the system controller uses to initialize and run the device unless a fault or crash is detected, at which point the system may switch to a recovery bank for restoration purposes.

[0053] As used herein, firmware refers to a specific class of computer software that provides low-level control for a device's hardware. It is typically embedded directly into the device's non-volatile memory, such as ROM, flash memory, or EEPROM, and serves as the essential intermediary that allows hardware components to interact seamlessly with higher-level software. Unlike regular software, firmware is often designed to be more resilient and is updated less frequently, providing a stable foundation for the device's operations.

[0054] FIG. 1 illustrates an exemplary block diagram of a computing device [100] upon which the features of the present disclosure may be implemented in accordance with exemplary implementation of the present disclosure. In an implementation, the computing device [100] may also implement a method for monitoring and self-recovery of a radio unit in a 5G radio network utilising the system. In another implementation, the computing device [100] itself implements the method for monitoring and self-recovery of a radio unit in a 5G radio network using one or more units configured within the computing device [100], wherein said one or more units are capable of implementing the features as disclosed in the present disclosure.

[0055] The computing device [100] may include a bus [102] or other communication mechanism for communicating information, and a processor [104] coupled with the bus [102] for processing information. The processor [104] may be, for example, a general-purpose microprocessor. The

computing device [100] may also include a main memory [106], such as a random-access memory (RAM), or other dynamic storage device, coupled to the bus [102] for storing information and instructions to be executed by the processor [104]. The main memory [106] also may be used for storing temporary variables or other intermediate information during execution of the instructions to be executed by the processor [104]. Such instructions, when stored in non-transitory storage media accessible to the processor [104], render the computing device [100] into a special-purpose machine that is customized to perform the operations specified in the instructions. The computing device [100] further includes a read only memory (ROM) [108] or other static storage device coupled to the bus [102] for storing static information and instructions for the processor [104].

[0056] A storage device [110], such as a magnetic disk, optical disk, or solid-state drive is provided and coupled to the bus [102] for storing information and instructions. The computing device [100] may be coupled via the bus [102] to a display [112], such as a cathode ray tube (CRT), Liquid crystal Display (LCD), Light Emitting Diode (LED) display, Organic LED (OLED) display, etc. for displaying information to a computer user. An input device [114], including alphanumeric and other keys, touch screen input means, etc. may be coupled to the bus [102] for communicating information and command selections to the processor [104]. Another type of user input device may be a cursor controller [116], such as a mouse, a trackball, or cursor direction keys, for communicating direction information and command selections to the processor [104], and for controlling cursor movement on the display [112]. This input device typically has two degrees of freedom in two axes, a first axis (e.g., x) and a second axis (e.g., y), that allow the device to specify positions in a plane.

[0057] The computing device [100] may implement the techniques described herein using customized hard-wired logic, one or more ASICs or FPGAs, firmware and/or program logic which in combination with the computing device [100] causes or programs the computing device [100] to be a special-purpose machine. According to one implementation, the techniques herein are performed by the computing device [100] in response to the processor [104] executing one or more sequences of one or more instructions contained in the main memory [106]. Such instructions may be read into the main memory [106] from another storage medium, such as the storage device [110]. Execution of the sequences of instructions contained in the main memory [106] causes the processor [104] to perform the process steps described herein. In alternative implementations of the present disclosure, hard-wired circuitry may be used in place of or in combination with software instructions.

[0058] The computing device [100] also may include a communication interface [118] coupled to the bus [102]. The communication interface [118] provides a two-way data communication coupling to a network link [120] that is connected to a local network [122]. For example, the communication interface [118] may be an integrated services digital network (ISDN) card, cable modem, satellite modem, or a modem to provide a data communication connection to a corresponding type of telephone line. As another example, the communication interface [118] may be a local area network (LAN) card to provide a data communication connection to a compatible LAN. Wireless links may also be implemented. In any such implementation, the communication interface [118] sends and receives electrical, electromagnetic or optical signals that carry digital data streams representing various types of information.

[0059] The computing device [100] can send messages and receive data, including program code, through the network(s), the network link [120] and the communication interface [118]. In the Internet example, a server [130] might transmit a requested code for an application program through the Internet [128], the ISP [126], the local network [122], host [124] and the communication interface [118]. The received code may be executed by the processor [104] as it is received, and/or stored in the storage device [110], or other non-volatile storage for later execution.

[0060] Referring to **FIG. 2**, an exemplary block diagram of a system [200a] for monitoring and self-recovery of a radio unit [200r] in a 5G radio network, is shown, in accordance with the exemplary implementations of the present disclosure. The system [200a] comprises at least one processing unit [202]. The processing unit [202] may corresponds to at least one of, but not limited only to a field programmable gate array (FPGA), an application-specific integrated circuit (ASIC) or a network processing unit (NWP). The system [200a] may further include at least one interface unit [204]. The interface unit [204] further comprises at least one of, but not limited only to a universal asynchronous receiver-transmitter (UART) unit [204t] and a general-purpose input/output (GPIO) unit [204io]. The system [200a] may further include at least one memory element [206]. The memory element includes at least one of a NOR Flash memory [206n], and embedded multimedia card (eMMC) memory [206e]. The eMMC memory [206e] includes a plurality of bank units [206b]. The plurality of bank units further includes at least an active bank [206ba] and a recovery bank [206br]. The system [200a] further includes at least one system controller [208]. The system controller [208] comprises a monitoring unit [208m], a triggering unit [208t], an initialization unit [208i] and a restoration unit [208r] Also, all of the components/ units of the system [200a] are assumed to be connected to each other unless otherwise indicated below. As shown in the figures all units shown within the system should also be assumed to be connected

to each other. Also, in FIG. 2 only a few units are shown, however, the system [200a] may comprise multiple such units or the system [200a] may comprise any such numbers of said units, as required to implement the features of the present disclosure. Further, in an implementation, the system [200a] may be present in a radio unit [200r] to implement the features of the present disclosure. In another implementation, the system [200a] may reside in a server or a network entity.

[0061] The system [200a] is configured for monitoring and self-recovery of a radio unit [200r] in a 5G radio network, with the help of the interconnection between the components/units of the system [200a].

[0062] The processing unit [202] may be the FPGA, ASIC and the NWP. In an exemplary embodiment of the present disclosure, the processing unit [202] is connected to the memory element [206] to store the functional boot image and a root file system. The connection allows the processing unit [202] to access the necessary software and configuration data required for its operation, ensuring that it can boot up correctly and perform its functions reliably. The memory element [206] provides a secure and efficient storage solution for the software components, enabling seamless initialization and operation of the processing unit [202]. The processing unit [202] as the FPGA may include a type of integrated circuit (IC) which is programmed to work in 5G communication network for real-time processing, enhancing data throughput, reducing latency, updates and optimizations along with complex signal processing. The processing unit [202] as the FPGA may include customized IC/ chips for a particular application or task such as but not limited to encoding/decoding, signal modulation etc.

[0063] The interface unit [204] comprising the UART unit [204t] and GPIO unit [204io]. The UART unit [204t] may be used for serial communication over the communication network. The UART unit [204t] often transmits bits asynchronously, which is why they are beneficial in low-speed reliable communication between network devices. The low-speed reliable communication often involves control and status information of the network devices rather than the actual messages. The GPIO unit [204io] may include an interfacing general purpose pin on an IC for control signals and status monitoring such as changing the state of network hardware devices, reading the state of switches etc.

[0064] The memory element [206] may be the NOR Flash memory [206n] and the embedded multimedia card (eMMC) memory [206e] with the plurality of bank units [206b]. The NOR flash memory [206n] here refers to a fast random-access memory made using NOR gate. The NOR flash

memory [206n] is used to store firmware, boot code and configuration data. This type of memory is effective for booting and startup process. The NOR flash memory [206n] is used for faster data allocation. While the eMMC memory [206e] refers to an integrated non-volatile memory made using NAND gated flash that are used for storing operating system, application, and data logs on the network devices in a 5G communication network.

[0065] The plurality of bank units [206b] may comprise at least an active bank [206ba] and a recovery bank [206br].

[0066] In an exemplary embodiment of the present disclosure, the eMMC memory [206e] having plurality of bank units (such as two primary bank units of the plurality of bank units [206b]). The two primary bank units are the active bank [207ba] and the recovery bank [206br] which are being configured to have respective firmware image each. The firmware refers to a small set of machine instructions that is responsible for allowing the hardware to function and communicate with other devices in the communication network. Similarly, the firmware image here refers to a small binary file of the radio unit [200r] that can be booted to operate radio unit [200r], thereby handling data transmission by fixing bugs in the firmware code.

[0067] In an exemplary embodiment of the present disclosure, each of the primary bank units is sub-divided into at least four partitions designed to carry critical configuration for individual sub-sections of the processing unit [202]. It is further noted that the individual sub-sections are configured to be executed sequentially. The individual sub-sections of at least four partitions are configured to be executed sequentially, such that each sub-section of the processing unit [202] receives its specific configuration in a structured and orderly manner. This subdivision and sequential execution enhance the reliability and efficiency of the system, as it ensures that all necessary configurations are correctly applied to the processing unit, thereby minimizing the risk of errors and improving overall performance.

[0068] The system controller [208] is configured to monitor, via the monitoring unit [208m], a heartbeat signal from the processing unit [202]. The heartbeat signal acts as a regular indicator of the processing unit's status, allowing the system controller to detect any abnormalities or failures in real-time. By monitoring this signal, the system controller [208] can promptly identify if the processing unit [202] is functioning correctly or if there are any issues that require intervention, thereby enhancing the reliability and stability of the overall system.

[0069] In an exemplary embodiment of the present disclosure, the heartbeat signal comprises a continuous signal on the GPIO unit [204io]. The system controller [208] can receive the heartbeat signal either as a recurring polling message, which is a regular check or request for status, or as a steady, uninterrupted signal on the General-Purpose Input/Output (GPIO) unit [204io]. The system controller [208] can thus monitor the operational status of the processing unit [202] through different communication techniques, providing flexibility and robustness in detecting and responding to potential issues.

[0070] The system controller [208] is further configured to trigger, via the triggering unit [208t], a reset and re-initialization of the processing unit [202] based on reception of the heartbeat signal within a predetermined time period. The predefined time period may include a duration of particular time interval (for e.g., 5 seconds). If the heartbeat signal is received within a predetermined time period, such as 5 seconds, the system controller [208] will trigger a reset and re-initialization of the processing unit [202] via the triggering unit [208t]. This mechanism helps in maintaining the functionality of the processing unit by automatically restarting it if the signal is not detected within the specified interval, thereby addressing potential system faults or hangs promptly and effectively.

[0071] The system controller [208] is further configured to initialize, via an initialization unit [208i], the radio unit [200r] using the active bank [206ba] of the eMMC memory [206e]. The process involves accessing the active bank [206ba] of the eMMC memory [206e], which contains the necessary firmware and configuration data. By initializing the radio unit with this active bank, the system controller [208] ensures that the radio unit [200r] is loaded with the most current and functional software, enabling it to operate efficiently and effectively within the network. This initialization process is crucial for maintaining the reliability and performance of the radio unit.

[0072] The system controller [208] is further configured to initiate, via the initialization unit [208i], recovery of the radio unit [200r] using the recovery bank [206br] when the heartbeat signal fails to be received within a predetermined time interval. The recovery mechanism facilitates in ensuring that in the event of a system fault or failure, where the regular heartbeat signal is not detected within the specified time frame, the system can automatically switch to the recovery bank. This allows the radio unit to reboot with a backup firmware, thereby restoring its functionality and minimizing downtime or disruption in service.

[0073] The system controller [208] is further configured to restore, via the restoration unit [208r], a functional boot image of the radio unit [200r] in a corrupted memory bank using a new firmware. For example, if a firmware update or unexpected event corrupts the memory bank of the radio unit, the restoration unit [208r] will detect the issue and use a new firmware to overwrite the corrupted data. The radio unit [200r] can recover and operate normally without requiring manual intervention. By restoring a functional boot image with the latest firmware, the system controller [208] ensures that the radio unit is always equipped with a reliable and up-to-date operating environment, thus minimizing downtime and maintaining consistent performance. For example, if the active bank [206ba] of the eMMC memory [206e] becomes corrupted during a failed update, the system controller will use the new firmware stored in the restoration unit to rewrite the active bank, effectively restoring the radio unit to a functional state.

[0074] Thereafter, the system controller [208] is configured to initiate recovery from the recovery bank if the heartbeat signal is not received within a further configured time interval; and communicate with an element management system (EMS) [not shown] to obtain and push a new firmware for restoring a functional boot image in a corrupted memory bank. It is important to note that the EMS is tool responsible for controlling the alarms. The EMS gives the signal to the network about the system controller [208] not working properly. The EMS is responsible for catering to the number of the components (such as gNodeB, etc.) in the communication network. The EMS is also known as Equipment Management System (EMS) and can vary in nomenclature among different telecom operators. Further, the functional boot image may refer to a primary boot image which performs the attach and detach of the files related to the booting. Also, the functional boot image is the file from where all the subsequent boot images (such as backup images, etc.) are created.

[0075] The heartbeat signals/heartbeat is identified through periodic status messages that are exchanged between the various network components for monitoring network activity. The heartbeat is indicative of the fact that the components in the network are carrying out their intended function as per the functional boot image. The heartbeat goes to a microcontroller unit (MCU) [not shown], a standalone system having own power supply and operating system other than the network components in the network. If heartbeat is not received for a certain duration, then system controller will initiate a recovery signal which will perform following actions:

[0076] Reset and Re-initialize the ASIC/FPGA/NWP so that it will start from the boot process. At first it will initialize using the active bank of eMMC memory.

[0077] If heartbeat is not received till the configured time interval (which changes from product to product) then system controller will initiate another recovery/reset signal which will perform the system recovery from the recovery bank. The configured time interval is the predefined period defined by the user between two successive heartbeat signals. The configured time interval may be based on a network performance parameter(s) which enables monitoring the network performance. This will recover the system if there is software crash also and image on the active bank is corrupted.

[0078] Once recovered the radio will communicate with the EMS which will push the new firmware to restore a functional boot image in the corrupted memory bank.

[0079] A person skilled in the art would appreciate that the above listed features are only exemplary and does not limit the present disclosure in any possible manner. In an exemplary implementation, the features listed above may be considered to be in the order of their importance.

[0080] Referring to FIG. 3, an exemplary method flow diagram [300] for monitoring and self-recovery of a radio unit in a 5G radio network, in accordance with exemplary implementations of the present disclosure is shown. In an implementation the method [300] is performed by the system [200a]. Further, in an implementation, the system [200a] may be present in a server device to implement the features of the present disclosure. Also, as shown in Figure 4, the method [300] starts at step [302].

[0081] At step [304], the method [300] comprises providing, a processing unit [202]. The processing unit [202] may be at least one of: a field programmable gate array (FPGA), an application-specific integrated circuit (ASIC), and a network processing unit (NWP). An FPGA, for example, offers flexibility as it can be reprogrammed post-manufacturing to adapt to different tasks and protocols, making it ideal for high-speed data processing in a 5G radio network. An ASIC is a customized chip designed for specific applications, such as efficient signal processing, providing high performance with low power consumption. Further, the NWP is configured for managing network traffic, ensuring efficient data routing and protocol handling within the network. By incorporating a processing unit [202] that could be any of these advanced components, the method [300] ensures the system can capitalize on the unique strengths of each type, leading to optimized performance and adaptability in various scenarios.

[0082] At step [306], the method [300] comprises interfacing, with an interface unit [204]. The interface unit [204] may comprise at least one of: a universal asynchronous receiver-transmitter (UART) unit [204t] and general-purpose input/output (GPIO) unit [204io]. he UART unit [204t] may be used for serial communication over the communication network. The UART unit [204t] often transmits bits asynchronously, which is why they are beneficial in low-speed reliable communication between network devices. The low-speed reliable communication often involves control and status information of the network devices rather than the actual messages. The GPIO unit [204io] may include an interfacing general purpose pin on an IC for control signals and status monitoring such as changing the state of network hardware devices, reading the state of switches etc.

[0083] At step [308], the method [300] comprises accessing, a memory element [206]. The memory element [206] may be at least one of: a NOR Flash memory [206n] and embedded multimedia card (eMMC) memory [206e] having a plurality of bank units [206b]. The NOR flash memory [206n] here refers to a fast random-access memory made using NOR gate. The NOR flash memory [206n] is used to store firmware, boot code and configuration data. This type of memory is effective for booting and startup process. The NOR flash memory [206n] is used for faster data allocation. While the eMMC memory [206e] refers to an integrated non-volatile memory made using NAND gated flash that are used for storing operating system, application, and data logs on the network devices in a 5G communication network. The plurality of bank units [206b] may comprise at least an active bank [206ba] and at least a recovery bank [206br].

[0084] In an exemplary aspect of the present disclosure, in the disclosed method [300], the eMMC memory [206e] is partitioned into two primary bank units of the plurality of bank units [206b], the two primary bank units being configured to have a respective firmware image each.

[0085] In an exemplary aspect of the present disclosure, in the disclosed method [300], each of the primary bank units is sub-divided into at least four partitions designed to carry critical configuration for individual sub-sections of the processing unit [202]. It is further noted that the individual sub-sections are configured to be executed sequentially.

[0086] At step [310], the method [300] comprises monitoring, via a monitoring unit [208m], of a system controller [208], a heartbeat signal from the processing unit [202]. The heartbeat signal acts as a regular indicator of the processing unit's status, allowing the system controller to detect any abnormalities or failures in real-time. By monitoring this signal, the system controller [208]

can promptly identify if the processing unit [202] is functioning correctly or if there are any issues that require intervention, thereby enhancing the reliability and stability of the overall system.

[0087] In an exemplary aspect of the present disclosure, in the disclosed method, the heartbeat signal comprises a continuous signal on the GPIO unit [204io]. It is to be noted that the GPIO unit [204io] handles both incoming and outgoing signals. The continuous signal on the GPIO unit [204io] is indicative of a consistent, uninterrupted and steady state of the signal from/to the GPIO unit [204io].

[0088] At step [312], the method [300] comprises triggering, via a triggering unit [208t] of the system controller [208], a reset and re-initialization of the processing unit [202] based on reception of the heartbeat signal within a predetermined time period. It is to be noted that reset including making the default state of the processing unit [202] in the system controller [208] again. While the re-initialisation includes but not limited to restarting the processing unit [202]. If the heartbeat signal is received within a predetermined time period, such as 5 seconds, the system controller [208] will trigger a reset and re-initialization of the processing unit [202] via the triggering unit [208t]. This mechanism helps in maintaining the functionality of the processing unit by automatically restarting it if the signal is not detected within the specified interval, thereby addressing potential system faults or hangs promptly and effectively.

[0089] At step [314], the method [300] comprises initializing, via an initialization unit [208i] of the system controller [208], the radio unit [200r] using the active bank [206ba] of the eMMC memory [206e]. The process involves accessing the active bank [206ba] of the eMMC memory [206e], which contains the necessary firmware and configuration data. By initializing the radio unit with this active bank, the system controller [208] ensures that the radio unit [200r] is loaded with the most current and functional software, enabling it to operate efficiently and effectively within the network. This initialization process is crucial for maintaining the reliability and performance of the radio unit.

[0090] At step [316], the method [300] comprises initiating, via the initialization unit [208i] of the system controller [208], recovery of the radio unit [200r] using the recovery bank [206br] when the heartbeat signal fails to be received within a predetermined time interval. The recovery mechanism facilitates in ensuring that in the event of a system fault or failure, where the regular heartbeat signal is not detected within the specified time frame, the system can automatically

switch to the recovery bank. This allows the radio unit to reboot with a backup firmware, thereby restoring its functionality and minimizing downtime or disruption in service.

[0091] At step [318], the method [300] comprises restoring, via a restoration unit [208r] of the system controller [208], a functional boot image of the radio unit [200r] in a corrupted memory bank using a new firmware. For example, if a firmware update or unexpected event corrupts the memory bank of the radio unit, the restoration unit [208r] will detect the issue and use a new firmware to overwrite the corrupted data. The radio unit [200r] can recover and operate normally without requiring manual intervention. By restoring a functional boot image with the latest firmware, the system controller [208] ensures that the radio unit is always equipped with a reliable and up-to-date operating environment, thus minimizing downtime and maintaining consistent performance. For example, if the active bank [206ba] of the eMMC memory [206e] becomes corrupted during a failed update, the system controller will use the new firmware stored in the restoration unit to rewrite the active bank, effectively restoring the radio unit to a functional state.

[0092] Thereafter, the method [300] terminates at step [320].

[0093] In an exemplary aspect of the present disclosure, the method [300] further comprises storing the functional boot image and a root file system by forming a connection between the processing unit [202] and the memory element [206].

[0094] Referring to FIG. 4A, an exemplary auto-recovery system [400] architecture is shown, in accordance with the exemplary embodiments of the present disclosure. The system [400] comprises a microcontroller/ processing unit which is connected to/ which itself is at least one of: a Field Programmable Gate Array (FPGA)/ Application-specific Integrated circuit (ASIC)/ Network Processors (NWP) [402]. In an implementation, the system [400] comprises a heartbeat monitor toggle unit [408m] and a system controller [408] that may be connected to each FPGA/ASIC/NWP. In another implementation, an interface [not shown] accessible may be Universal Asynchronous receiver- transmitter (UART) [not shown] and General-Purpose Input/Output (GPIO) [not shown].

[0095] Now, each FPGA may be connected to NOR Flash memory [406n] and/or Embedded Multimedia Card (eMMC) memory [406e], but the present disclosure is not limited thereto, that may carry a bootable image and a root file system. In an implementation, a firmware image may be stored in a plurality of memories.

[0096] Next, a system controller [408] may dynamically monitor a heartbeat of each ASIC/FPGA/NWP. Further, the heartbeat may be a continuous signal on one of the GPIO. The system controller [408] may be associated with the heartbeat monitor toggle unit [408m]. The heartbeat monitor toggle unit [408m] may enable or disable monitoring of the heartbeat. Now, if the heartbeat may not be received for a certain duration, then the system controller [408] may initiate a recovery signal that may perform the following actions. Firstly, the system [400] may be configured to reset and re-initialize the ASIC/FPGA/NWP so that the system [400] may start from the boot process. At first, the system [400] may initialize using an active bank [not shown] of the eMMC memory [406e], where the eMMC memory [406e] may comprises a set of bank units [not shown], where the set of bank units [not shown] may be one of the active bank and a recovery bank [not shown]. In an event, the heartbeat may not be received till a configured time interval then, the system controller [408] may initiate another recovery/reset signal that may perform the system [400] recovery from the recovery bank. Now, the system [400] may experience a software crash and an image on the active bank may be corrupted. Further, once recovered the radio unit [not shown] in the 5G communication network may communicate with EMS that may push a new firmware to restore a functional boot image in a corrupted memory bank.

[0097] Referring to FIG. 4B, that illustrates an exemplary architecture of bootable memory element [406] partition, in accordance with exemplary embodiments of the present disclosure. The bootable memory element [406] partition may include a designated section of the boot file that point to a root file for booting. The bootable memory element [406] partition enables one to access the boot files. The eMMC memory [406e] may include a plurality of bank units [not shown] that can be divided into two bank units, i.e., Bank 1 [406ba] being an active bank, and Bank 2 [406br] being a recovery bank as also shown in FIG. 2. The bank unit here refers to a unit comprising various accumulative memory locations (also known as an array) as a single unit. Each bank unit may have a respective firmware image. Further, each bank units may be sub-divided into at least four partitions that carry critical configuration for sub-section of individual ASIC/NWP/FPGA. It is further noted that these individual sub-sections of ASIC/ NWP/ FPGA are executed sequentially. Furthermore, the Bank 1 [406ba] may have the default firmware image and Bank 2 [406br] may carry the recovery firmware image that may be used when the system [400] crash may be detected. Also, a memory flag may be maintained to direct each of the processing unit i.e., ASIC/NWP/FPGA [402] to the firmware image bank. During the process of firmware update, the flag may be updated and accordingly the recovery bank/ Bank 2 [406br] having recovery image bank may switch.

[0098] The present disclosure further discloses a non-transitory computer readable storage medium storing instructions for monitoring and self-recovery of a radio unit in a 5G radio network, the instructions include executable code which, when executed by one or more units of a system, causes a system controller [208] to: monitor, via a monitoring unit [208m], a heartbeat signal from a processing unit [202]. The processing unit [202] is provided in at least one of: a field programmable gate array (FPGA), an application-specific integrated circuit (ASIC), and a network processing unit (NWP). Further, the instructions include executable code, which when executed causes a triggering unit [208t] to trigger a reset and re-initialization of the processing unit [202] based on reception of the heartbeat signal within a predetermined time period. Further, the instructions include executable code, which when executed causes an initialization unit [208i] to initialize the radio unit [200r] using an active bank [206ba] of an eMMC memory [206e]. Further, the instructions include executable code, which when executed causes the initialization unit [208i] to initiate recovery of the radio unit [200r] using a recovery bank [206br] when the heartbeat signal fails to be received within a predetermined time interval. Further, the instructions include executable code, which when executed causes a restoration unit [208r] to restore a functional boot image of the radio unit [200r] in a corrupted memory bank using a new firmware.

[0099] Further, in accordance with the present disclosure, it is to be acknowledged that the functionality described for the various the components/units can be implemented interchangeably. While specific embodiments may disclose a particular functionality of these units for clarity, it is recognized that various configurations and combinations thereof are within the scope of the disclosure. The functionality of specific units as disclosed in the disclosure should not be construed as limiting the scope of the present disclosure. Consequently, alternative arrangements and substitutions of units, provided they achieve the intended functionality described herein, are considered to be encompassed within the scope of the present disclosure.

[0100] It should be noted that the terms "first", "second", "primary", "secondary", "target" and the like, herein do not denote any order, ranking, quantity, or importance, but rather are used to distinguish one element from another.

[0101] As is evident from the above, the present disclosure provides a technically advanced solution for monitoring and self-recovery of a radio unit in a 5G radio network by enabling to recover system from stuck or hung state. Further, the proposed solution employs partitioning of firmware storage memory into two banks and providing the capability in the system to change the

banks which enables auto recovery in the system in case of firmware crash. The present solution thus enhances the recovery of the radio unit in the 5G communication network thereby helps in minimizing and eventually eliminating the physical visit by the infrastructural personnel to restore the site which will reduce the operational expenditure (OPEX) of the 5G communication network.

[0102] While considerable emphasis has been placed herein on the disclosed implementations, it will be appreciated that many implementations can be made and that many changes can be made to the implementations without departing from the principles of the present disclosure. These and other changes in the implementations of the present disclosure will be apparent to those skilled in the art, whereby it is to be understood that the foregoing descriptive matter to be implemented is illustrative and non-limiting.

We Claim:

1. A method [300] for monitoring and self-recovery of a radio unit [200r] in a 5G radio network, the method [300] comprising the steps of:

providing, a processing unit [202], wherein the processing unit [202] is at least one of: a field programmable gate array (FPGA), an application-specific integrated circuit (ASIC), and a network processing unit (NWP);

interfacing, with an interface unit [204], wherein the interface unit [204] comprising at least one of: a universal asynchronous receiver-transmitter (UART) unit [204t] and general-purpose input/output (GPIO) unit [204io];

accessing, a memory element [206], the memory element [206] is at least one of: a NOR Flash memory [206n] and embedded multimedia card (eMMC) memory [206e] having a plurality of bank units [206b], wherein the plurality of bank units [206b] comprise at least an active bank [206ba] and at least a recovery bank [206br];

monitoring, via a monitoring unit [208m] of a system controller [208], a heartbeat signal from the processing unit [202];

triggering, via a triggering unit [208t] of the system controller [208], a reset and re-initialization of the processing unit [202] based on reception of the heartbeat signal within a predetermined time period;

initializing, via an initialization unit [208i] of the system controller [208], the radio unit [200r] using the active bank [206ba] of the eMMC memory [206e];

initiating, via the initialization unit [208i] of the system controller [208], recovery of the radio unit [200r] using the recovery bank [206br] when the heartbeat signal fails to be received within a predetermined time interval; and

restoring, via a restoration unit [208r] of the system controller [208], a functional boot image of the radio unit [200r] in a corrupted memory bank using a new firmware.

2. The method [300] as claimed in claim 1, further comprises storing at least one of: the functional boot image and a root file system by forming a connection between the processing unit [202] and the memory element [206].

3. The method [300] as claimed in claim 1, wherein the heartbeat signal comprises a continuous signal on the GPIO unit [204io].

4. The method [300] as claimed in claim 1, wherein the eMMC memory [206e] is partitioned into two primary bank units of the plurality of bank units [206b], the two primary bank units being configured to have respective firmware image each.

5. The method [300] as claimed in claim 4, wherein each of the primary bank units is sub-divided into at least four partitions, wherein the at least four partitions being configured to carry critical configuration for individual sub-sections of the processing unit [202], and wherein the individual sub-sections are configured to be executed sequentially.

6. A system [200a] for monitoring and self-recovery of a radio unit [200r] in a 5G radio network, the system [200] comprising:

a processing unit [202], the processing unit [202] is at least one of: a field programmable gate array (FPGA), an application-specific integrated circuit (ASIC), and a network processing unit (NWP);

an interface unit [204] comprising at least one of: a universal asynchronous receiver-transmitter (UART) unit [204t] and a general-purpose input/output (GPIO) unit [204io];

a memory element [206], the memory element [206] is at least one of: a NOR Flash memory [206n] and an embedded multimedia card (eMMC) memory [206e] with a plurality of bank units [206b], wherein the plurality of bank units [206b] comprise at least an active bank [206ba] and a recovery bank [206br]; and

a system controller [208] configured to:

monitor, via a monitoring unit [208m], a heartbeat signal from the processing unit [202];

trigger, via a triggering unit [208t], a reset and re-initialization of the processing unit [202] based on reception of the heartbeat signal within a predetermined time period;

initialize, via an initialization unit [208i], the radio unit [200r] using the active bank [206ba] of the eMMC memory [206e];

initiate, via the initialization unit [208i], recovery of the radio unit [200r] using the recovery bank [206br] when the heartbeat signal fails to be received within a predetermined time interval; and

restore, via a restoration unit [208r], a functional boot image of the radio unit [200r] in a corrupted memory bank using a new firmware.

7. The system [200a] as claimed in claim 6, wherein the processing unit [202] is connected to the memory element [206] to store the functional boot image and a root file system.

8. The system [200a] as claimed in claim 6, wherein the heartbeat signal is a continuous signal on the GPIO unit [204io].

9. The system [200a] as claimed in claim 6, wherein the eMMC memory [206e] is partitioned into two primary bank units of the plurality of bank units [206b], the two primary bank units being configured to have respective firmware image each.

10. The system [200a] as claimed in claim 9, wherein each of the primary bank units is sub-divided into at least four partitions, wherein the at least four partitions being configured to carry critical configuration for individual sub-sections of the processing unit [202], and wherein the individual sub-sections of the processing unit [202] are configured to be executed sequentially.

11. A non-transitory computer readable storage medium storing instructions for monitoring and self-recovery of a radio unit [200r] in a 5G radio network, the instructions include executable code which, when executed by one or more units of a system [200a], causes:

- a system controller [208] of the system [200a] to:
    - monitor, via a monitoring unit [208m], a heartbeat signal from a processing unit [202];
    - trigger, via a triggering unit [208t], a reset and re-initialization of the processing unit [202] based on reception of the heartbeat signal within a predetermined time period;
    - initialize, via an initialization unit [208i], the radio unit [200r] using the active bank [206ba] of the eMMC memory [206e];
    - initiate, via the initialization unit [208i], recovery of the radio unit [200r] using a recovery bank [206br] when the heartbeat signal fails to be received within a predetermined time interval; and
    - restore, via a restoration unit [208r], a functional boot image of the radio unit [200r] in a corrupted memory bank using a new firmware.

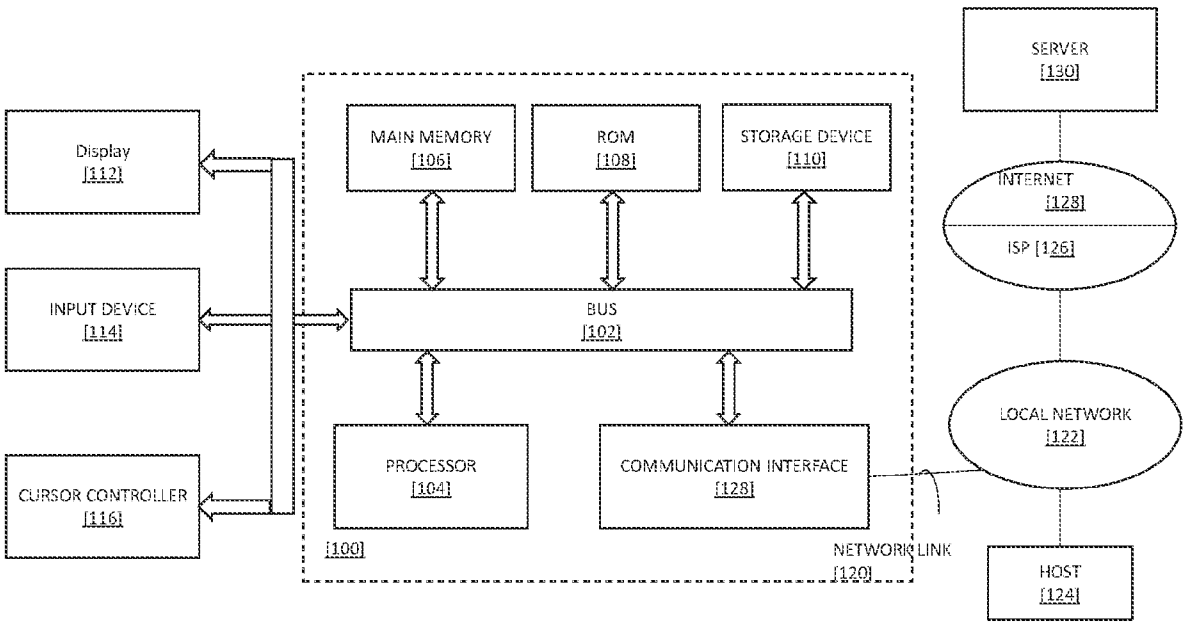

SERVER
[130]
Display
[112]
MAIN MEMORY
[106]
ROM
[108]
STORAGE DEVICE
[110]
INTERNET
[128]
ISP [126]
INPUT DEVICE
[114]
BUS
[102]
LOCAL NETWORK
[122]
CURSOR CONTROLLER
[116]
PROCESSOR
[104]
COMMUNICATION INTERFACE
[128]
[100]
NETWORK LINK
[120]
HOST
[124]

FIG. 1

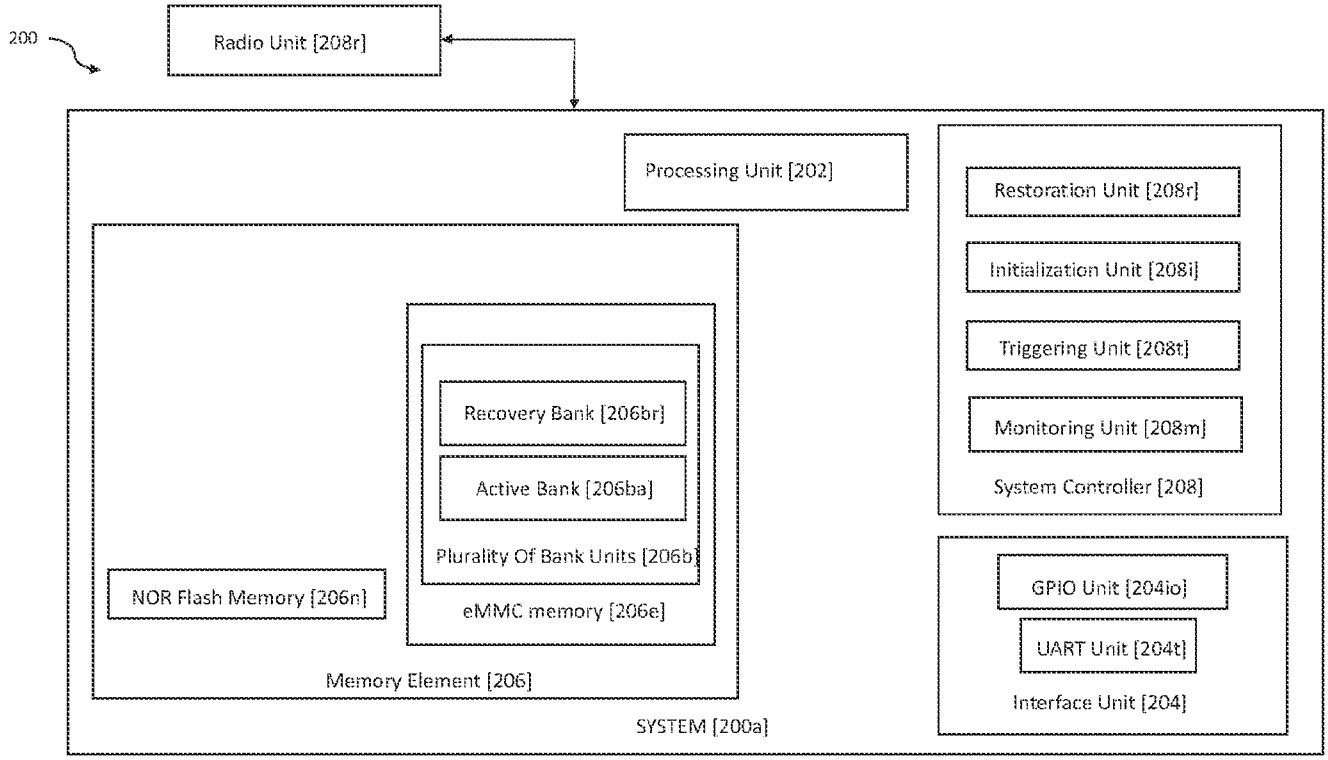

200
Radio Unit [208r]
Processing Unit [202]
Restoration Unit [208r]
Initialization Unit [208i]
Triggering Unit [208t]
Monitoring Unit [208m]
System Controller [208]
Recovery Bank [206br]
Active Bank [206ba]
Plurality Of Bank Units [206b]
eMMC memory [206e]
NOR Flash Memory [206n]
Memory Element [206]
GPIO Unit [204io]
UART Unit [204t]
Interface Unit [204]
SYSTEM [200a]

FIG. 2

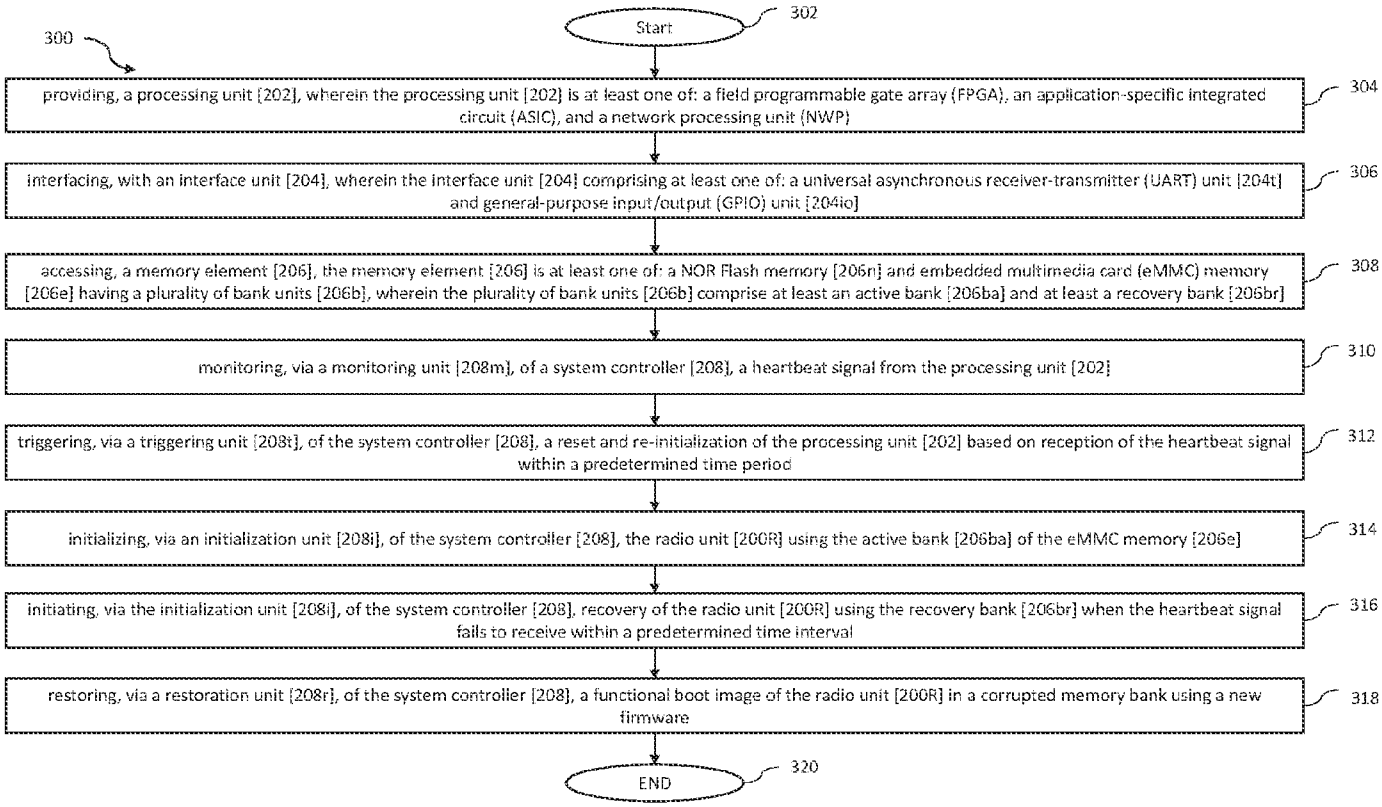

300
Start
302
providing, a processing unit [202], wherein the processing unit [202] is at least one of: a field programmable gate array (FPGA), an application-specific integrated circuit (ASIC), and a network processing unit (NWP)
304
interfacing, with an interface unit [204], wherein the interface unit [204] comprising at least one of: a universal asynchronous receiver-transmitter (UART) unit [204t] and general-purpose input/output (GPIO) unit [204io]
306
accessing, a memory element [206], the memory element [206] is at least one of: a NOR Flash memory [206n] and embedded multimedia card (eMMC) memory [206e] having a plurality of bank units [206b], wherein the plurality of bank units [206b] comprise at least an active bank [206ba] and at least a recovery bank [206br]
308
monitoring, via a monitoring unit [208m], of a system controller [208], a heartbeat signal from the processing unit [202]
310
triggering, via a triggering unit [208t], of the system controller [208], a reset and re-initialization of the processing unit [202] based on reception of the heartbeat signal within a predetermined time period
312
initializing, via an initialization unit [208i], of the system controller [208], the radio unit [200R] using the active bank [206ba] of the eMMC memory [206e]
314
initiating, via the initialization unit [208i], of the system controller [208], recovery of the radio unit [200R] using the recovery bank [206br] when the heartbeat signal fails to receive within a predetermined time interval
316
restoring, via a restoration unit [208r], of the system controller [208], a functional boot image of the radio unit [200R] in a corrupted memory bank using a new firmware
318
END
320

FIG. 3

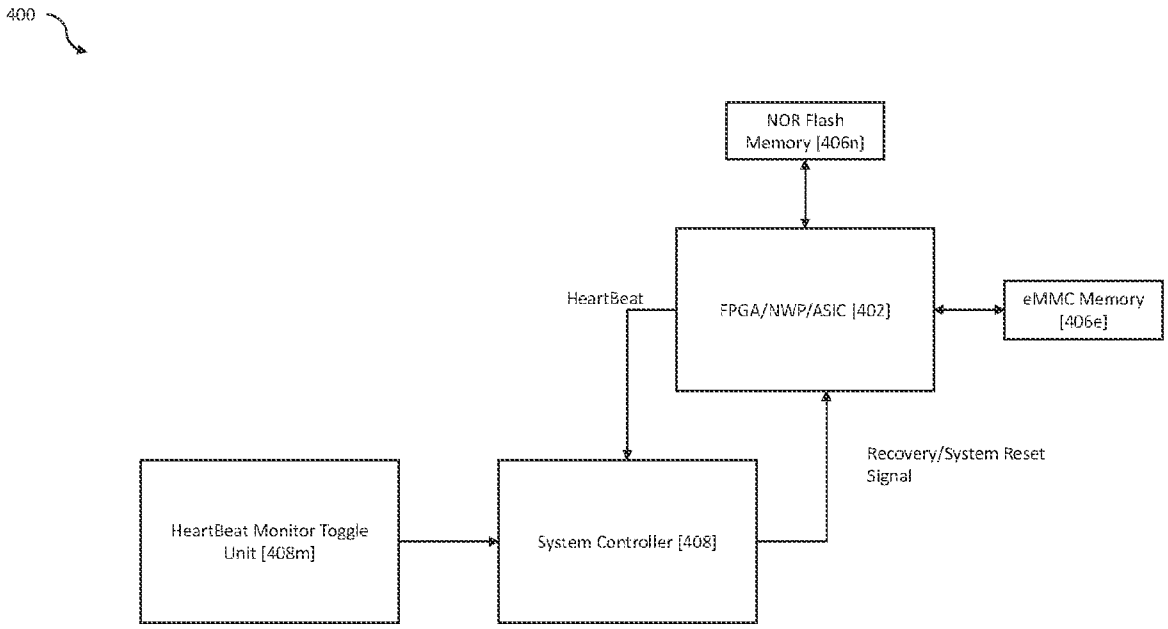

400
NOR Flash Memory [406n]
HeartBeat
FPGA/NWP/ASIC [402]
eMMC Memory [406e]
Recovery/System Reset Signal
HeartBeat Monitor Toggle Unit [408m]
System Controller [408]

FIG. 4A

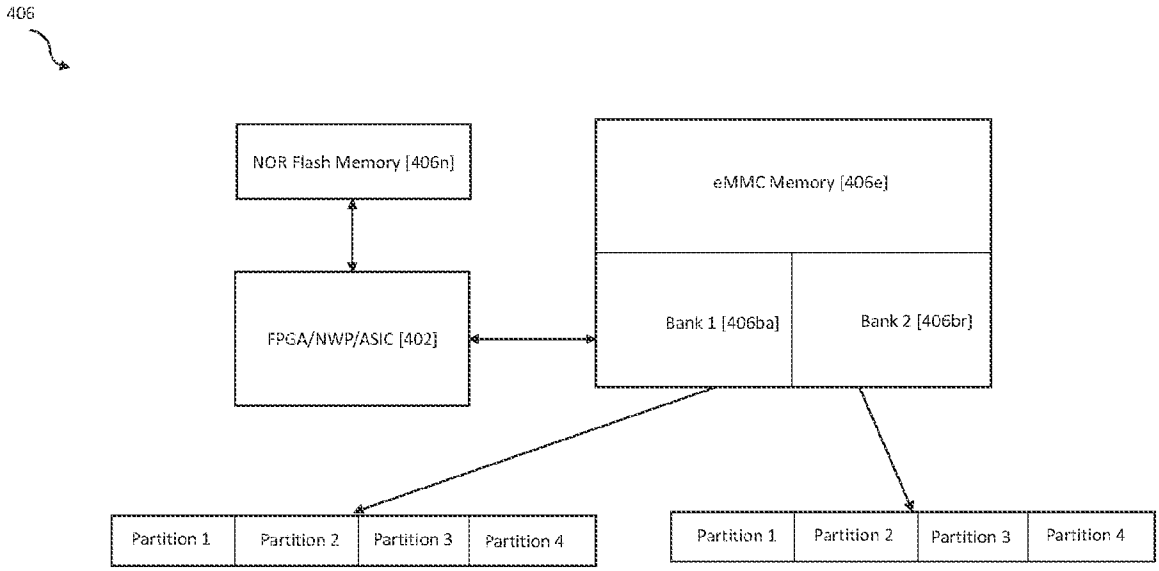

406
NOR Flash Memory [406n]
eMMC Memory [406e]
FPGA/NWP/ASIC [402]
Bank 1 [406ba]
Bank 2 [406br]
Partition 1
Partition 2
Partition 3
Partition 4
Partition 1
Partition 2
Partition 3
Partition 4

FIG. 4B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IN2024/051210

A. CLASSIFICATION OF SUBJECT MATTER
H04W24/04,H04W76/19,H04W88/08 Version=2024.01

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H04W

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database consulted during the international search (name of database and, where practicable, search terms used)

PatSeer, IPO Internal Database

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	KR20160078547A (INNOWIRELESS CO LTD) 05/07/2016 (05 July 2016) (English Translation Copy from Espacenet) whole document	1-11
Y	CN214851850U (DALIAN CITY GONGJIN TECH CO LTD) 23/11/2021 (23 Nov 2021) (English Translation Copy from Espacenet) whole document	1-11

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18-11-2024	18-11-2024
Name and mailing address of the ISA/ Indian Patent Office Plot No.32, Sector 14,Dwarka,New Delhi-110075 Facsimile No.	Authorized officer Vinay Kumar Gautam Telephone No. +91-1125300200