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(71) Applicant (for all designated States except US): **THOMSON LICENSING** [FR/FR]; 46, Quai A. Le Gallo, F-92100 Boulogne-Billancourt (FR).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **CHEN, Hou-Shin** [CN/US]; 26 Plains Gap Road, North Brunswick, New Jersey 08802 (US). **GAO, Wen** [CN/US]; 73 Warwick Road, West Windsor, New Jersey 08550 (US).

(74) Agents: **SHEDD, Robert, D.** et al.; c/o Thomson Licensing LLC, 2 Independence Way Suite 200, Princeton, New Jersey 08540 (US).

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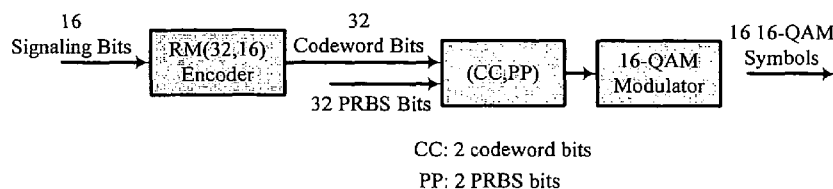


Figure 3

(57) Abstract: A frame header of Forward Error Correction (FEC) is provided, suitable for using in the DVB-C2 Standard. In the DVB-C2 Standard, Adaptive Coding and Modulation (ACM) or Variable Coding and Modulation (VCM) is applied to each FEC block to provide as much flexibility as possible. As a result, a frame header is attached in front of each FEC frame to inform the coding rate, modulation type and physical layer pipe identifier. Besides the signaling of physical layer related information, the FEC frame header has to provide a structure so that it can be easily and reliably detected in the receiver. Motivated by the need in DVB-C2 Standard, an efficient and reliable FEC header suitable for DVB-C2 Standard is provided in at least one implementation in this disclosure. In addition, the detection Method of the FEC header is described.



METHOD AND APPARATUS FOR TRANSMITTING AND RECEIVING FEC FRAME HEADERS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Application Serial No. 61/200667, filed December 2, 2008, which is incorporated by reference herein in its entirety.

TECHNICAL FIELD

The present principles relate to cable transmission systems and techniques. More particularly, it relates to an FEC header design for cable television transmissions.

BACKGROUND OF THE INVENTION

LDPC (Low Density Parity Check) codes are a class of Forward Error Correction (FEC) block codes, often used in transmission environments to protect audio and/or video data. These Forward Error Correction codes increase the possibility of receivers recovering from and correcting errors in a received multimedia stream, without the need to retransmit data that is received with errors. The FEC error control system requires the transmitter add redundant data to a data stream. The maximum fraction of errors that can be corrected by the FEC is determined by the way the error correction code is calculated. Examples of FEC are block codes, such as LDPC codes that work on fixed-sized blocks, packets, or symbols of a predetermined size, and convolutional codes that work on bit or symbol streams of arbitrary length. Many types of block error correction codes exist, such as Reed-Solomon or, as already mentioned, the LDPC (Low-Density Parity Check). Other types of error correction codes have been developed for specific use in transmission of digital video streams over IP networks, such as SMPTE 2022 (Society of Motion Picture and Television Engineers), which unlike other typical FEC schemes such as Reed-Solomon, relies on very simple algorithms, and is useful in environments where limited resources are available, such as a Set Top Box receiver for Digital Television.

The DVB-S2 LDPC codes family, which were originally designed for forward error control in satellite communications, have also been used by DVB-T2 (Second Generation DVB Standard for Terrestrial Channels), and are strongly recommended for DVB-C2 (Second Generation DVB Standard for Cable Channels). OFDM modulation will be adopted as well as the coding technique (BCH+LDPC) specified in DVB-T2 Standard. However, DVB-T2 Standard is designed for use in the terrestrial wireless channel while the DVB-C2 Standard is designed for use in the cable channel. The signal frame structure and preambles used in DVB-T2 may not be suitable to be reused in DVB-C2 Standard.

A frame header of Forward Error Correction (FEC) is designed for use in the DVB-C2 Standard. The FEC data block is composed of a Bose-Chaudhuri-Hocquenghem (BCH) outer code and a Low-Density-Parity-Check (LDPC) inner code. Two dimensional interleaving is also performed. Interleaving is a procedure for rearranging the order of a sequence to fulfill different objectives. For channels subject to selective fading over time and frequency domains, bit and/or symbol interleaving have been used in conjunction with channel coding to distribute the error bursts. A frame header is attached in front of each FEC frame to indicate the coding rate, modulation type and physical layer pipe identifier. Besides the signaling of physical layer related information, the FEC frame header has to provide a structure so that it can be easily and reliably detected in the receiver.

SUMMARY OF THE INVENTION

An efficient and reliable FEC frame header for digital cable television transmission is provided in at least one implementation in this specification. In addition, a method of detecting the FEC header is described. An exemplary implementation is shown, using the DVB-C2 standard as an example.

An efficient and reliable FEC frame header for DVB-C2 Standard is provided in at least one implementation in this specification. In the DVB-C2 Standard, Adaptive Coding and Modulation (ACM) or Variable Coding and Modulation (VCM) is applied to each FEC block to provide as much flexibility as possible. As a result, a frame header is attached in front of each FEC frame to indicate a receiver as to the coding rate, modulation type and physical layer pipe identifier. Besides signaling physical layer related information, it is desirable for the FEC frame header to provide a structure so that it can be easily and reliably detected in the receiver. In addition, a method of detecting the FEC header is described.

The number of symbols of FEC frame header in an exemplary implementation in this specification is 32 which is less than other methods having 45 symbols.

The FEC frame header according to the present principles uses Reed-Muller (32,16) Code (RM(32,16)) to protect signaling bits while the FEC frame header of prior methods use BCH (45,18) code. The RM(32,16) code can be decoded by majority-logic decoding which requires less complexity than previous decoding methods. Thus, the decoding complexity of the FEC frame header in an implementation according to the present principles is much less than decoding of a FEC frame header according to other known arrangements.

Additionally, the Reed-Muller code has a symmetric code structure during majority-logic decoding process. The detection of FEC frame header can be performed by taking advantage of this symmetric structure.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows the frame structure of the frequency-domain DVB-C2 signals.

Figure 2 shows Generation of 32-Symbol FEC Frame Header.

Figure 3 shows Generation of 16-Symbol FEC Frame Header.

Figure 4 shows the Generator Matrix of RM(32,16) code.

Figure 5 shows a conceptual framework for 32-Symbol FEC frame header detection.

Figure 6 shows a conceptual framework for 16-Symbol FEC frame header detection.

Figure 7 shows a method for encoding a header using the principles described herein.

Figure 8 shows an apparatus for encoding a header according to the principles herein.

Figure 9 shows a first method of decoding the encoded header information according to the principles described herein.

Figure 10 shows a first apparatus for decoding the encoded header information according to the principles described herein.

Figure 11 shows a second method decoding the encoded header information according to the principles described herein.

Figure 12 shows a second apparatus for decoding the encoded header information according to the principles described herein.

DETAILED DESCRIPTION OF THE INVENTION

The DVB-C2 Standard is the next generation digital cable transmission system being developed by the DVB Project. The DVB-C2 Standard uses aspects of the DVB-T2 terrestrial transmission standard as much as possible. As a result, OFDM modulation will be adopted as well as the coding technique (BCH+LDPC) specified in DVB-T2 Standard. However, it must be noted that DVB-T2 Standard is designed for use in the terrestrial wireless channel while the DVB-C2 Standard is designed for use in the cable channel. Cable channels differ from wireless channels because the cable channel is a high quality, high Signal-to-Noise Ratio (SNR) channel with only a few weak echoes and because the wireless spectrum assigned for TV broadcasting is generally defined by a

governmental agency, such as the FCC, while the spectrum of the cable networks can be used with somewhat fewer limitations. Consequently, the signal frame structure and preambles used in DVB-T2 may not be suitable to be used in DVB-C2 Standard. The principles described herein allow an FEC frame header to be detected under noisy channel conditions with minimal receiver complexity.

The data transmitted according to the DVB-C2 standard is contained in Data Slice Packets. Data Slice Packets are formed from one or two FEC Frame cells. These Data Slice Packets can either be Data Slice Type 1 or Data Slice Type 2. Data Slice Type 1 packets only transmit the FEC Frame data and use a pointer within the Level 1 Signaling Part 2 to detect their start. Data Slice Type 2 packets carry a 16-bit FEC Frame header that allows for synchronization to the Data Slice Packets without further information being transmitted. This header carries information regarding the modulation, coding parameters, PLP identifiers, and number of FEC Frames (one or two) following the header. Encoding of the header information must ensure that the header can be properly synchronized and decoded.

Simulation results have shown that use of RM(32,16) code with BPSK modulation can achieve error free results for FEC Header signaling at 10 dB SNR in additive white Gaussian noise (AWGN) channels. Majority decoding has very low complexity leading to simple decoders as well.

FEC Frame Structure

In the DVB-C2 Standard, in order to support ACM or VCM over each FEC frame, a FEC frame header is attached to each FEC frame. The FEC frame structure is shown in Figure 1. Each FEC-coded frame is Quadrature Amplitude Modulation (QAM) modulated with different order and coding rate. These two critical parameters are carried in the FEC frame header that precedes each FEC frame.

FEC Frame Header Structure

The FEC frame header contains 16 signaling bits as described below:

1. QAM Modulation Order – 3 bits (16, 64, 256, 1K, 4K)
2. FEC Block Length – 1 bit (16200, 64800)
3. FEC Coding Rate – 3 bits
4. Physical Layer Pipe (PLP) ID – 8 bits
5. Header Change Indicator or parity check bit– 1 bit: when the bit is Header Change Indicator, the value of “1” indicates the first 4 parts of the FEC header of next FEC frame will be modified while the value of “0” indicates no change. The receiver will know if the bit is the header change indicator or parity check bit based on layer-1 signaling.

The signaling bits are protected by RM code which can be decoded with a low-complexity majority-logic decoding method. The RM(32,16) code is selected and thus 16 message bits are coded into 32 codeword bits. A PRBS (Pseudo-Random Binary Sequence) of length 32 is embedded in the FEC frame header structure to enable frame header detection in the receiver. An example of the 32 PRBS bit is F8261D92 in hex notation. It is a section from a PRBS having a generator polynomial of $x^{11}+x^2+1$. Two frame header structures with different length are designed in at least one implementation in this specification. The frame header structure with shorter length is provided for use in a high SNR environment.

A. 32-Symbol FEC Frame Header

A conceptual framework for generating a 32-Symbol FEC frame header is shown in Figure 2. The 16 signaling bits are coded by RM(32,16) code. The resulting 32 codeword bits are modulated by in-phase BPSK or quadrature BPSK in a modulator using a PRBS. The in-phase BPSK is used if the corresponding PRBS bit is 1. Otherwise, the quadrature BPSK is used.

B. 16-Symbol FEC Frame Header

A conceptual framework for generating a 16-Symbol FEC frame header is shown in Figure 3. The 16 signaling bits are coded by RM(32,16) code. The resulting 32 codeword bits and 32 PRBS bits are 16-QAM modulated into 16 symbols by a 16-QAM modulator after every two codeword bits are paired with two PRBS bits. Each 16-QAM symbol is produced from two codeword bits in the two most significant bits and two PRBS bits in the two least significant bits. The two codeword bits determine the quadrant and the two PRBS bits determine the position in the quadrant. In another exemplary embodiment of a 16-QAM symbol, the two most significant bits carry the codeword bits and the two least significant bits carry the PRBS bits.

FEC Frame Header Detection Method

Based on the PRBS embedded in FEC frame header and the use of RM(32,16) code, the detection of the FEC frame header is performed by a two step method. The first step is the correlation of the transmitted PRBS and received bit-stream. Let $PN(n)$, $n = 0, 1, \dots, 31$ be the transmitted 32-bit PRBS. The correlation with a given index i is given by

$$R_{PN}(i) = \sum_{n=0}^{31} PN(n) \cdot Y(i+n) \quad (1)$$

where $Y(n)$ is the received binary stream for PRBS. Note that the correlation of two binary streams is computed by substituting 1 and 0 to 1 and -1 and then performing correlation. Also note that if the PRBS is the only feature used for FEC frame header detection, the estimated FEC frame header position is given by

$$i_o = \arg \max_i R_{PN}(i) \quad (2)$$

The second step is based on the RM(32,16) code structure. Although the RM(32,16) code is not a first order Reed-Muller code, its codeword does not have a symmetric structure. However, during the majority-logic decoding process, after the first layer

decoding, the modified codeword has a symmetry structure. This can be explained as follows: The codewords of RM(32,16) code are linear combinations of 16 rows of the generator matrix shown in Figure 4.

$$\mathbf{x} = (m_0, m_1, \dots, m_{15})\mathbf{G}. \quad (3)$$

The majority-logic decoding consists of 3 stages. The last 10 bits, $(m_6, m_7, \dots, m_{15})$, are decoded from the received code vector $\mathbf{r} = (r_0, r_1, \dots, r_{31})$ in the first stage. These 10 bits are removed from $\mathbf{r}$ to form a modified code vector. Assume $\mathbf{r}^{(1)} = (r_0^{(1)}, r_1^{(1)}, \dots, r_{31}^{(1)})$ is the modified received vector

$$\mathbf{r}^{(1)} = \mathbf{r} - (0, \dots, 0, m_6, m_7, \dots, m_{15})\mathbf{G}. \quad (4)$$

Let $\mathbf{x}^{(1)} = (x_0^{(1)}, x_1^{(1)}, \dots, x_{31}^{(1)})$ be its corresponding transmitted modified code vector. It can be seen that $\mathbf{x}^{(1)}$ is a linear combination of the first 6 rows of the generator matrix of RM(32,16) code as shown in Figure 4. It can be easily verified that $\mathbf{x}^{(1)}$ has a symmetric structure. The sub-code vectors $(x_0^{(1)}, x_1^{(1)}, \dots, x_{15}^{(1)})$ and $(x_{16}^{(1)}, x_{17}^{(1)}, \dots, x_{31}^{(1)})$ are either the same or flipped. This kind of symmetry happens in sub-code vectors $(x_0^{(1)}, x_1^{(1)}, \dots, x_7^{(1)})$ and $(x_8^{(1)}, x_9^{(1)}, \dots, x_{15}^{(1)})$, $(x_{16}^{(1)}, x_{17}^{(1)}, \dots, x_{23}^{(1)})$ and $(x_{24}^{(1)}, x_{25}^{(1)}, \dots, x_{31}^{(1)})$, $(x_0^{(1)}, x_1^{(1)}, x_2^{(1)}, x_3^{(1)})$ and $(x_4^{(1)}, x_5^{(1)}, x_6^{(1)}, x_7^{(1)})$, and so on. Let $\mathbf{r}^{(1)}(i) = (r_0^{(1)}(i), r_1^{(1)}(i), \dots, r_{31}^{(1)}(i))$ be the received modified code vector which has index i as the starting position of FEC frame header. The RM autocorrelation of the received modified code vector is given by

$$R_{\text{RM}}(i, k) = \sum_{m=0}^{2^k-1} \sum_{n=0}^{2^{4-k}-1} r_{m \cdot 2^{5-k}+n}^{(1)}(i) \cdot r_{m \cdot 2^{5-k}+2^{4-k}+n}^{(1)}(i) \quad (5)$$

where k from 0 to 4 is an index for 5 symmetric structures embedded in $\mathbf{x}^{(1)}$. In addition, define the RM symmetry measure as

$$T_{\text{RM}}(i) = \sum_{k=0}^4 |R_{\text{RM}}(i, k)|^2. \quad (6)$$

Note that the RM symmetry measure can be computed for $k = 0$ only to reduce complexity. The conceptual framework for detection of 32-Symbol FEC frame headers

is shown in Figure 5. The conceptual framework for detection of 16-symbol FEC frame headers is shown in Figure 6. The only difference is in demodulating the information bits. For the 32-Symbol FEC header, the bit stream for PRBS correlation is decoded by comparing the amplitudes of real part and imaginary part of the received signal. For the 16-Symbol FEC header, the bit stream is from the 2 LSB of 16-QAM demodulator. A 32-bit PRBS correlation is then performed. The further RM correlation measure is performed only for those index i for which $R_{RM}(i)$ is greater than a threshold. This threshold is adjustable in the receiver. The decision statistic of the frame header detection is given by

$$T = 5 \cdot |R_{PN}(i)|^2 + 4 \cdot T_{RM}(i) \quad (7)$$

Another variation for frame header detection is that the estimated frame header position is given by

$$i_o = \arg \max_i \left(5 \cdot |R_{PN}(i)|^2 + 4 \cdot T_{RM}(i) \right) \quad (8)$$

We thus provide one or more implementations having particular features and aspects. However, features and aspects of described implementations may also be adapted for other implementations. Although implementations described herein may be described in a particular context, such descriptions should in no way be taken as limiting the features and concepts to such implementations or contexts.

The present description illustrates the present principles as applied to the 16-bit header of DVB-C2 as an example. It will thus be appreciated that those skilled in the art will be able to devise various arrangements that, although not explicitly described or shown herein, embody the present principles and are included within its spirit and scope. The present principles are equally applicable to header information of different lengths with appropriate modification of the methods and apparatus of the present invention.

Figure 7 illustrates the method 700 for encoding the FEC header information under the present principles. FEC Encoding is performed in step 710, using for example, RM(32,16) coding. Modulation with a pseudo-random binary sequence is then performed in step 720.

Figure 8 illustrates an apparatus for encoding the FEC header information under the principles described herein. Header information is received at the input of encoder 810. After encoding, using for example RM(32,16) encoding, the output is sent to the input of modulator 820, where the FEC encoded header information is modulated with a pseudo-random binary sequence.

Figure 9 illustrates a first method 900 of decoding the encoded FEC header information. Header information is received in step 910. The real and imaginary parts of the received header information are compared and a logical one is output when the real part has magnitude greater than or equal to the imaginary magnitude, and a logical zero is output otherwise in step 920. This result is then correlated with a pseudo-random binary sequence in step 930 to produce a correlation result. The correlation result is compared to a threshold in step 940. If the correlation result of step 930 is greater than the threshold, demodulation and symmetry detection is performed in step 950, producing a symmetry measure. If the correlation result is not greater than the threshold, the process is reinitiated by receiving header information in step 910.

Figure 10 illustrates an apparatus 1000 for performing this first method of decoding the encoded FEC header information. Comparator 1010 compares the real and imaginary portions of the received header information and outputs the correct bits as detailed above. Correlator 1020 correlates the result with a pseudo-random binary sequence to produce a correlation result. The correlation result is input to demodulator 1030, which compares it to a threshold and, if greater than the threshold, demodulator 1030 demodulates the header information, followed by symmetry detection of the header information performed by block 1040, which outputs a symmetry measure.

Figure 11 illustrates a second method 1100 of decoding the encoded FEC header information. Header information is received in step 1110 and demodulated in step 1120. The demodulated symbol produces 4 bits for 16-QAM. The two least significant bits are correlated with a pseudo-random binary sequence in step 1130 to produce a correlation result. The correlation result is compared to a threshold in step 1140. If the correlation result is greater than the threshold, symmetry detection is performed on the two most significant bits of the demodulated symbol information in step 1150. If the correlation result is not greater than the threshold, the process is reinitiated by receiving header information in step 1110.

Figure 12 illustrates an apparatus to perform this second method of decoding the encoded FEC header information. Demodulator 1210 demodulates header symbols. Correlator 1220 correlates the two least significant bits with a pseudo-random binary sequence. Symmetry detector 1230 checks the correlation result against a threshold, and if the correlation result is greater than the threshold, symmetry detection is performed using, for example, majority decoding if a second order Reed-Muller code was used. The output of symmetry detector 1230 produces a symmetry measure.

The implementations described herein may be implemented in, for example, a method or process, an apparatus, or a software program. Even if only discussed in the context of a single form of implementation (for example, discussed only as a method), the implementation or features discussed may also be implemented in other forms (for example, an apparatus or program). An apparatus may be implemented in, for example, appropriate hardware, software, and firmware. The methods may be implemented in, for example, an apparatus such as, for example, a computer or other processing device. Additionally, the methods may be implemented by instructions being performed by a processing device or other apparatus, and such instructions may be stored on a computer readable medium such as, for example, a CD, or other computer

readable storage device, or an integrated circuit. Further, a computer readable medium may store the data values produced by an implementation.

As should be evident to one of skill in the art, implementations may also produce a signal formatted to carry information that may be, for example, stored or transmitted. The information may include, for example, instructions for performing a method, or data produced by one of the described implementations.

Additionally, many implementations may be implemented in one or more of an encoder, a pre-processor to an encoder, a decoder, or a post-processor to a decoder. The implementations described or contemplated may be used in a variety of different applications and products. Some examples of applications or products include set-top boxes, cell phones, personal digital assistants (PDAs), televisions, personal recording devices (for example, PVRs, computers running recording software, VHS recording devices), camcorders, streaming of data over the Internet or other communication links, and video-on-demand.

Further, other implementations are contemplated by this specification. For example, additional implementations may be created by combining, deleting, modifying, or supplementing various features of the disclosed implementations.

All examples and conditional language recited herein are intended for pedagogical purposes to aid the reader in understanding the present principles and the concepts contributed by the inventor(s) to furthering the art, and are to be construed as being without limitation to such specifically recited examples and conditions.

Other hardware, conventional and/or custom, may also be included. Similarly, any switches shown in the figures are conceptual only. Their function may be carried out through the operation of program logic, through dedicated logic, through the interaction of program control and dedicated logic, or even manually, the particular

technique being selectable by the implementer as more specifically understood from the context.

Reference in the specification to “one embodiment” or “an embodiment” of the present principles, as well as other variations thereof, means that a particular feature, structure, characteristic, and so forth described in connection with the embodiment is included in at least one embodiment of the present principles. Thus, the appearances of the phrase “in one embodiment” or “in an embodiment”, as well any other variations, appearing in various places throughout the specification are not necessarily all referring to the same embodiment.

CLAIMS:

1. A method of encoding FEC frame header information, the method comprising:

encoding header bits in the header information for data packets using Reed-Muller coding;

modulating the Reed-Muller coded header bits with a pseudo-random binary sequence.
2. The method of Claim 1, wherein the header information is used in a digital cable television environment.
3. The method of Claim 1, wherein said modulating step uses a pseudo-random binary sequence using 32 offset binary phase shift keying.
4. The method of Claim 1, wherein said modulating step uses a pseudo-random binary sequence using 16-QAM.
5. The method of Claim 1, wherein the Reed-Muller encoding step uses a second order Reed-Muller code.
6. An apparatus for encoding FEC frame header information, comprising:

an encoder for Reed-Muller encoding data packets in the header information; and

a modulator for modulating the Reed-Muller encoded data packets with a pseudo-random binary sequence.
7. The apparatus of Claim 6, wherein the encoder operates on header information in a digital cable television environment
8. The apparatus of Claim 6, wherein the Reed-Muller encoder uses a second order Reed-Muller code.

9. The apparatus of Claim 6, wherein the modulator uses 32 offset binary phase shift keying.
10. The apparatus of Claim 6, wherein the modulator uses 16-QAM.
11. A method of decoding header information, the method comprising:
 - receiving a bitstream from a digital cable television transmission;
 - comparing amplitudes of the real and imaginary parts of said received signal and producing a logic one bit when said real part is greater than or equal to said imaginary part and producing a logic zero bit when said real part is less than said imaginary part and producing a first value; and
 - correlating a transmitted pseudo-random binary sequence with said first value to produce a correlation result;
 - demodulating said digital cable television bitstream and a majority logic decoding process to produce a symmetry measure if said correlation result is greater than a threshold.
12. The method of Claim 11, wherein the correlating step uses a 32-bit pseudo-random binary sequence.

13. An apparatus for decoding header information, comprising:
 - a comparator for comparing real and imaginary parts of said header information for data packets in a digital cable television environment and producing a logic one bit when said real part is greater than or equal to said imaginary part and producing a logic zero bit when said real part is less than said imaginary part to produce a first value;
 - a correlator for correlating said first value with a pseudo-random binary sequence to produce a correlation result;
 - a demodulator for performing offset binary phase shift keying demodulation on said received header information if said correlation result is greater than a threshold;
 - and
 - a Reed-Muller symmetry detector for processing said demodulated received header information to produce a symmetry result.
14. The apparatus of Claim 13, wherein the correlator uses a 32-bit pseudo-random binary sequence.
15. A method of decoding header information, the method comprising:
 - receiving symbols from a digital cable television transmission;
 - demodulating said received symbols by using 16-QAM demodulation to produce a demodulation result;
 - correlating a transmitted pseudo-random binary sequence with the two least significant bits of said demodulation result to produce a correlation result;
 - decoding the two most significant bits of said demodulation result using a majority logic decoding process if said correlation result is greater than a threshold to produce a symmetry measure.

16. The method of Claim 15, wherein the correlating step uses a 32-bit pseudo-random binary sequence.
17. An apparatus for decoding header information, comprising:
 - a demodulator for demodulating received header information symbols using 16-QAM to produce a demodulation result bit stream;
 - a correlator for correlating a transmitted pseudo-random binary sequence with the two least significant bits of said demodulation result to produce a correlation result;
 - a symmetry detector for performing a majority logic decoding process on the two most significant bits of said demodulation result if said correlation result is greater than a threshold to produce a symmetry measure.
18. The apparatus of Claim 17, wherein the correlating step uses a 32 bit pseudo-random binary sequence.

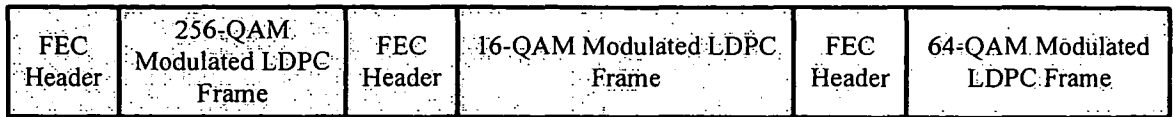


Figure 1

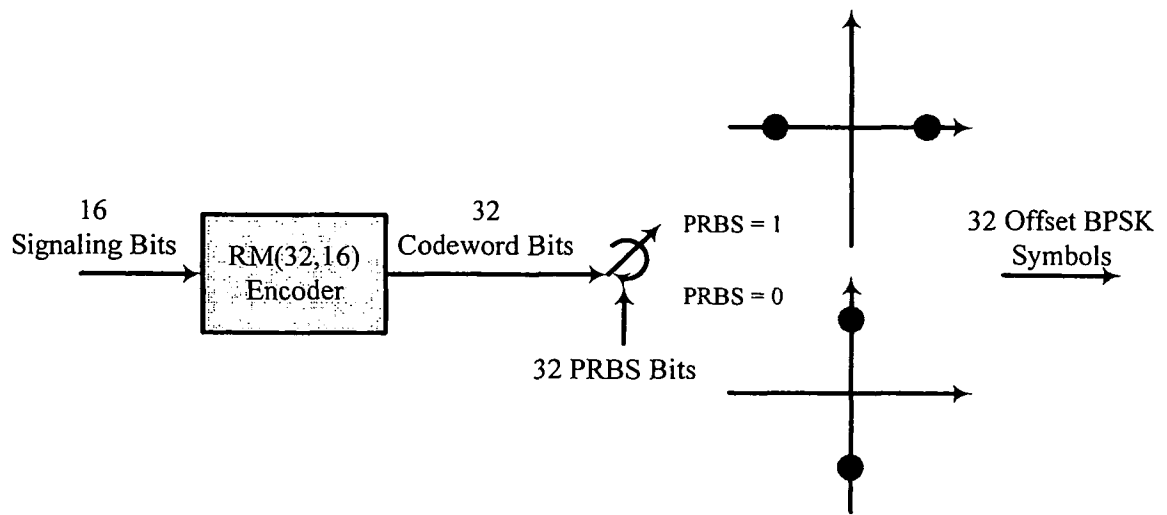


Figure 2

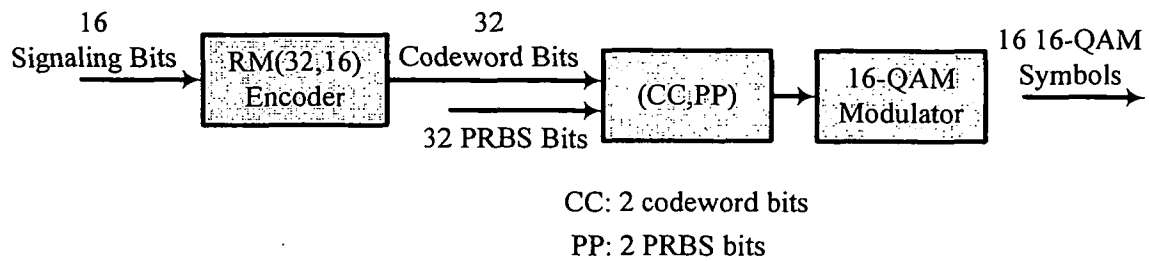


Figure 3

[illegible]

Figure 4

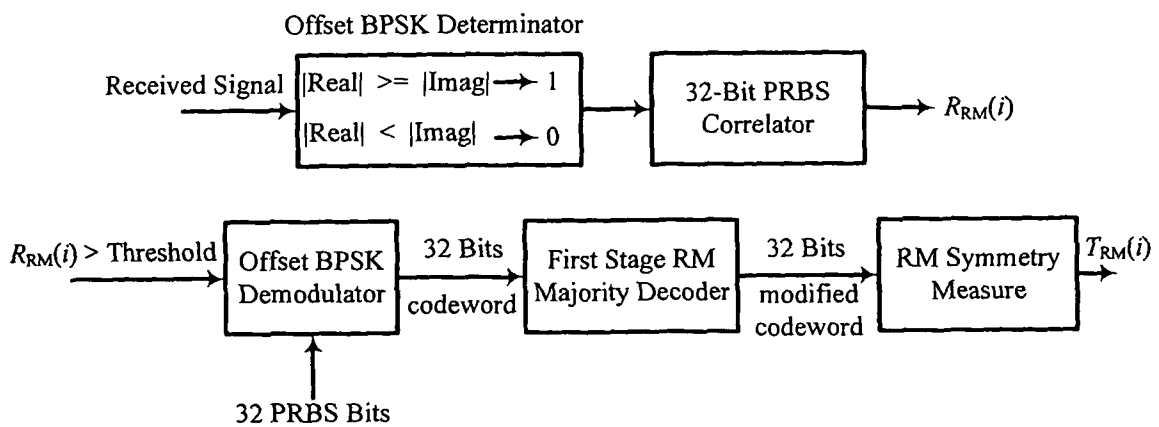


Figure 5

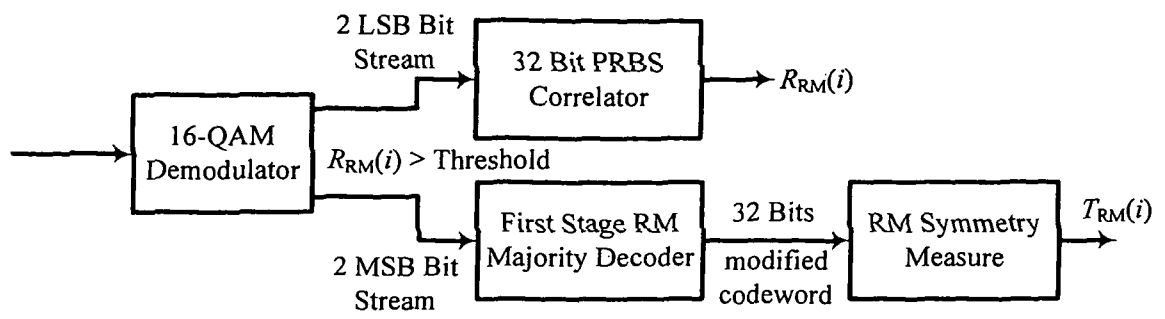


Figure 6

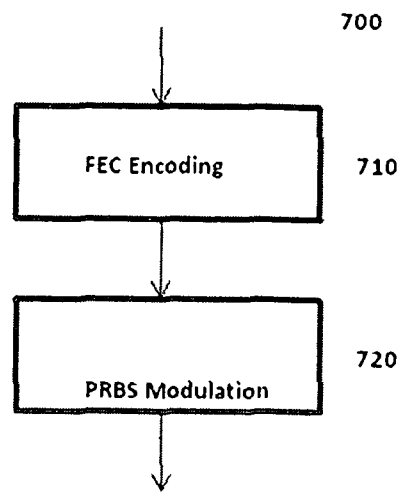


Figure 7

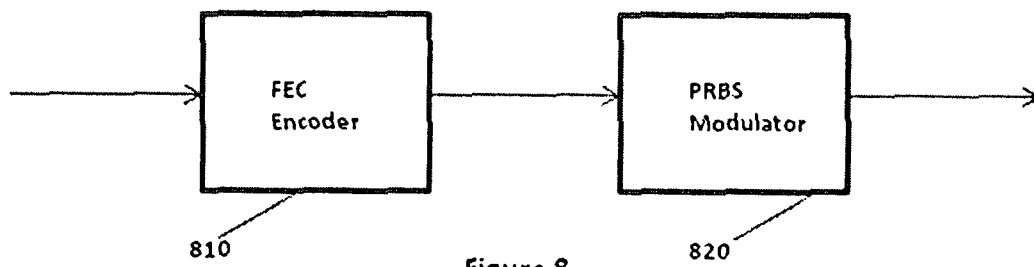


Figure 8

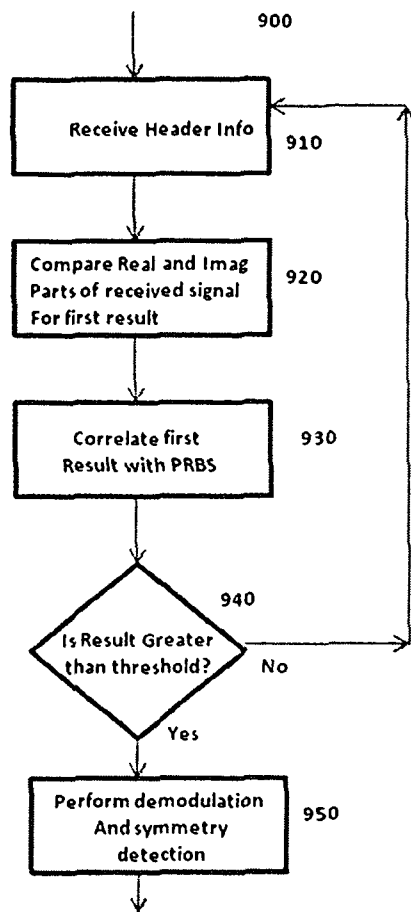


Figure 9

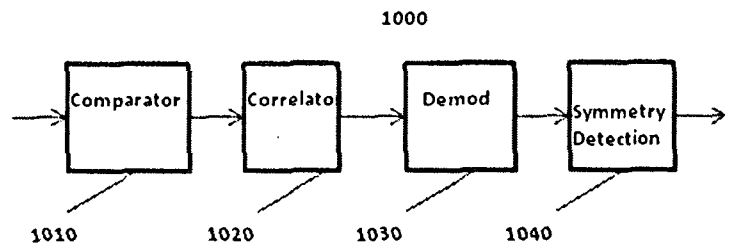


Figure 10

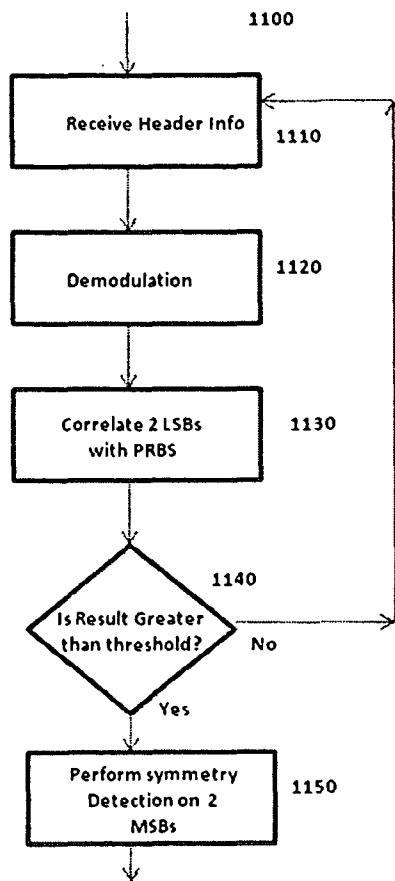


Figure 11

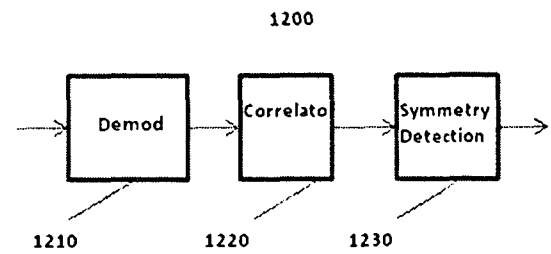


Figure 12