Section 29(1)
Regulation 3.1(2)

AUSTRALIA

PATENTS ACT 1990

N O T I C E O F E N T I T L E M E N T

We, SF2 CORPORATION of 140 Kifer Court, Sunnyvale, CA 94086, U.S.A. being the applicant in respect of Application No. 60,596/90, state the following:-

The person nominated for the grant of the patent:
has entitlement from the actual inventor(s) by virtue of the following:
The applicant is the assignee of the invention from the inventor.

The person nominated for the grant of the patent:
has entitlement from the applicant of the application listed in the declaration under Article 8 of the PCT by virtue of the following:
The applicant is the assignee of the invention from the inventor

The basic application(s) listed in the declaration made under Article 8 of the PCT
is/are the first application(s) made in a Convention country in respect of the invention

SF2 CORPORATION
By their Patent Attorneys
CULLEN & CO.

RONALD A. HALIDAY

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METHOD AND CIRCUIT FOR DECODING A MANCHESTER CODE SIGNAL

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(71) Applicant(s)
MICRO TECHNOLOGY, INC.

(72) Inventor(s)
HOKE STEPHENS JOHNSON

(74) Attorney or Agent
CULLEN & CO , GPO Box 1074, BRISBANE QLD 4001

(57) Claim

1. A method for extracting a data signal from a Manchester code signal, the Manchester code signal having low and high states, rising and falling transitions between the low and high states, and a clock period defining data cells, the method comprising the steps of:

detecting the transitions in the Manchester code signal;

for each detected transition, determining the state of the Manchester code signal at a point in the Manchester code signal between one-half and one clock period preceding the detected transition; and

generating an output signal having first and second states corresponding respectively to low and high states, the output signal being characterized with respect to each detected transition and correspondingly determined state of the Manchester code signal in that:

.../2

a. if a detected transition is a rising transition and the determined state of the Manchester code signal is a low state, the output signal changes from the second state to the first state;

b. if a detected transition is a rising transition and the determined state of the Manchester code signal is a high state, the output signal remains in its previous state;

c. if a detected transition is a falling transition and the determined state of the Manchester code signal is a low state, the output signal remains in its previous state; and

d. if a detected transition is a falling transition and the determined state of the Manchester code signal is a high state, the output signal changes from the first state ~~state~~ to the second state.

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(71) Applicant: ~~SF2 CORPORATION~~ [US/US]; ~~140 Kifer Court, Sunnyvale, CA 94086~~ (US).

(72) Inventor: JOHNSON, Hoke, Stephens, III ; 16191 Rose Avenue, Monte Sereno, CA 95030 (US).

(74) Agents: ROWLAND, Mark, D. et al.; Fish & Neave, 875 Third Avenue, New York, NY 10022 (US).

(71) MICRO TECHNOLOGY, INC.
5085 E. Hunter Avenue, Anaheim
California 92807, U.S.A.

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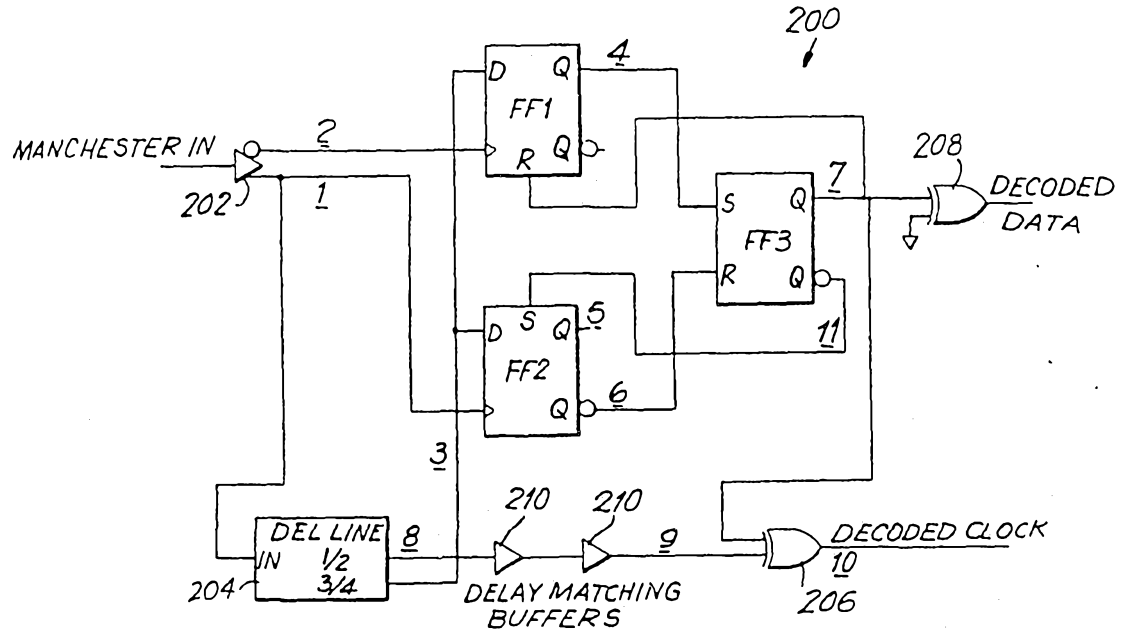
(54) Title: METHOD AND CIRCUIT FOR DECODING A MANCHESTER CODE SIGNAL



(57) Abstract

A circuit for decoding a high speed Manchester encoded digital communication signal is provided. The circuit includes a pair of latch circuits which are used to detect clock edges in the encoded signal for providing respectively set and reset pulses to a third latch circuit, an output of which comprises the decoded data of the Manchester code signal. Additional logic is provided to extract a clock signal from the Manchester code signal.

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METHOD AND CIRCUIT FOR DECODING A MANCHESTER CODE SIGNAL

Background of the Invention

The present invention relates to a circuit for extracting separate data and clock signals from a Manchester encoded digital communication signal.

Manchester encoding is commonly used in bit-serial digital communications, and numerous types of Manchester decoder circuits exist in the prior art. Many of these circuits are incapable of accurately decoding a Manchester signal at high speed, typically because signal propagation delays in the components of the circuits are either too long (i.e., the circuit is slow) or not sufficiently controllable. Such circuits include those having one-shot logic circuits and those implemented using TTL logic. Further, of the prior art Manchester decoder circuits that are capable of reliable operation at high speed, many are complicated and expensive. Such circuits include phase-locked loop circuits and fast-sampling state machines.

Summary Of The Invention

The present invention is a reliable method and circuit for decoding a Manchester encoded signal. The circuit includes a pair of latch circuits which are used to

detect transitions or edges in the encoded signal for providing respectively set and reset pulses to a third latch circuit, an output of which comprises the decoded data of the Manchester signal. The circuit also includes two delay elements, input and delay matching buffers, and one or more logic gates. Logical combination of the decoded data with a delayed encoded signal provides a decoded clock. The circuit can be implemented using fast ECL devices in a single integrated circuit. In a preferred embodiment, the latch circuit pair comprise flip-flop logic circuits matched on an integrated circuit to equalize signal propagation delays through the flip-flops.

Brief Description Of The Drawings

The above and other advantages of the present invention will be apparent upon consideration of the following detailed description, taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a signal diagram illustrating the method of the present invention.;

FIG. 2 is a schematic of an embodiment of the Manchester decoder circuit of the present invention; and

FIG. 3 is a timing diagram of the circuit of FIG. 2.

Detailed Description Of The Invention

Manchester encoding is a method of combining a serial data stream and a synchronized clock signal into a

single signal. It can be accomplished, for example, by combining a serial data stream of NRZ data with a synchronized 50% duty cycle clock signal in an exclusive-NOR logical operation. As a result of this operation, the data becomes encoded as a series of two-bit codes. A logical "1" is represented as a data bit cell in which the signal is at a high level for the first half of the data bit cell and at a low level for the second half. Thus a logical "1" is encoded as a two-bit code 1,0, each code bit cell being one-half the data bit cell. A logical "0" is represented as a data bit cell in which the signal is at a low level for the first half of the data bit cell and at a high level for the second half. Thus a logical "0" is encoded as a two-bit code 0,1.

By examining examples of typical Manchester encoded data streams, it can be seen that a transition in the original data from a logical "0" to a logical "1" causes the Manchester encoded data stream to contain a sequence of two code bits equal to 1. Likewise when the original data transitions from a logical "1" to a logical "0", the Manchester encoded data stream contains a sequence of two code bits equal to 0. At all other times, i.e., when the original data is a stream of consecutive logical "1"s or "0"s, the Manchester encoded data stream consists of alternating 1 and 0 code bits.

Referring to FIG. 1, an exemplary Manchester

encoded waveform 100 having clock periods 102 is shown. Each clock period 102 defines a data bit cell including two code bit cells (e.g., high state code bit cell 104 and low state code bit cell 106). Waveform 100 has falling edge transitions A,C,E,G,I,K,M and O and rising edge transitions B,D,F,H,J,L and N. Transitions A,B,C,E,F,H,J,L,M and O each occurs in the center of a clock period, and thus each conveys information: the falling edge transitions represent logical "1's", and the rising edge transitions represent logical "0's". Transitions D,G,I,K and N each occur at an edge of a clock period, and thus do not convey data. The preferred method of the present invention for extracting a data signal from a Manchester encoded waveform is described below with reference to the exemplary waveform of FIG. 1.

As a first step in the preferred method, each transition in the waveform is detected, although, as will be apparent, it is only necessary to detect the transitions occurring in the middles of clock periods 102. For each detected transition, the state (high or low) of the waveform 100 between one-half and one clock period preceding the detected transition is determined. Thus, for example, assuming transition B to have been detected, the state (low) of waveform 100 at point 101 is determined.

An output signal 103 is then generated having a first and a second state, preferably comprising a low state respectively to represent a logical "0" in the encoded data and a high

state to represent a logical "1", although an inverse relationship may also be used if desired to represent the original data. The output signal, the clock periods of which may be delayed with respect to the clock periods of waveform 100, is characterized by the following rules based on the direction of the detected transitions and the correspondingly determined state of waveform 100:

a. if a detected transition is a rising transition and the determined state of the waveform is a low state (e.g., the conditions shown by arrow 108), the output signal (which in the example is assumed to begin as a logical "1") changes from a high state to a low state;

b. if a detected transition is a rising transition and the determined state of the waveform is a high state (e.g., the conditions shown by arrow 110), the output signal remains in its previous state;

c. if a detected transition is a falling transition and the determined state of the waveform is a low state (e.g., the conditions shown by arrow 112), the output signal again remains in its previous state; and

d. if a detected transition is a falling transition and the determined state of the waveform is a high state (e.g., the conditions shown by arrow 114), the output signal changes from a low state to a high state.

As can be seen, transitions which occur at an edge of the clock period (e.g., 116 and 118) are governed by

rules (b) and (c) above, and thus produce no change in output signal 103.

An embodiment 200 of the Manchester decoder circuit of the present invention is shown in FIG. 2. For purposes of illustration, a timing diagram of the circuit 200 of FIG. 2 is shown in FIG. 3, with corresponding signal points indicated in each figure. Referring to FIGS. 2 and 3, a Manchester encoded signal 300 is coupled through buffer circuit 202 to the clocking input of flip-flop FF2 and to the input of delay element circuit 204. Buffer circuit 202 also inverts the encoded signal 300 and provides inverted signal 302 to the clocking input of flip-flop FF1.

Delay element circuit 204 generates delayed encoded signals 304 and 306. Signal 304 is delayed by 1/2 of a clock period of the original clock encoded in signal 300, and signal 306 is delayed by 3/4 of a clock period. The length of the delay depends on the speed at which data is transferred to circuit 200. For example, at a data transfer rate of 100 Megabits per second, delay element circuit 204 would be implemented to delay signal 304 by 5.0 nanoseconds(ns), and signal 306 by 7.5 ns. Delay element circuit 204 may be implemented using a fixed or programmable delay line circuit. Alternately, if it is desired that circuit 200 be implemented in a fully integrated circuit, delay element circuit 204 may be implemented as a high-speed clock circuit and a multiple-output shift register circuit

to generate the delayed signals 304 and 306.

Delayed encoded signal 306 is provided to the data input D of each flip-flop FF1, FF2. Flip-flops FF1 and FF2 are rising edge triggered flip-flop circuits. FF1 samples delayed encoded signal 306 when the inverted encoded signal 302 at its clocking input transitions from a low level to a high level (i.e., on a rising edge of inverted signal 302). Thus in effect FF1 is clocked once for each falling edge of encoded signal 300. FF2 samples delayed encoded signal 306 when the original encoded signal 300 at its clocking input transitions from a low level to a high level (i.e., on a rising edge of encoded signal 300). As described above, it is a property of a Manchester encoded signal that a transition occurs in the midpoint of every data cell due to the encoded clock signal. The encoded data is represented by the direction of that transistion. Thus, depending on the data represented in each data cell of the encoded signal, either FF1 or FF2 will be clocked by an edge or transition at the midpoint of each data cell. Although edges are also present at the boundaries of the data cells, these transitions do not cause the latched data output of either flip-flop FF1 or FF2 to change because the data at the input of the flip-flop will be the same as the data previously latched.

The data signal at the D input of FF1 (delayed signal 306) represents the original encoded signal 300

delayed by 3/4 of a data cell, which is equivalent to 1-1/2 code bit cells. If, when a rising edge transition in inverted signal 302 causes FF1 to sample the data at its D input, the sampled data is a 1, then it is known that original encoded signal 300 has been a 1 for two consecutive code bit cells and that the decoded data should change from a logical "0" to a logical "1". Flip-flop FF1 accordingly outputs a 1 on its Q output which is coupled to the set control input of an SR flip-flop FF3. This transition, shown for example by point 308 on signal 310, causes the Q output of FF3 to be set to a "1". The signal 312 at the Q output of flip-flop FF3 is coupled back to the reset control input of FF1 to cause signal 310 at the Q output of FF1 to return to 0 after FF3 has been successfully set. This prevents flip-flop FF1 from trying to set flip-flop FF3 at the same time flip-flop FF2, the operation of which is described below, may try to reset flip-flop FF3.

If, on the other hand, the data at the D input of flip-flop FF1 is a 0 when sampled, it is known that original encoded signal 300 has not been a 1 for two consecutive code bit cells, indicating that the encoded data has not changed from a logical "0" to a logical "1". Therefore flip-flop FF1 remains in the 0 state (i.e., the signal at Q output of FF1 remains 0) and FF3 is not set. This is the result, for example, whenever flip-flop FF1 is clocked by an edge at the boundary of a data cell.

Flip-flop FF2 operates in a similar manner to reset FF3 whenever the data at its D input (delayed signal 306) is a 0 when flip-flop FF2 is clocked by a rising edge in signal 300. As in the case of FF1, the data signal at the D input of FF2 (delayed signal 306) represents the original encoded signal 300 delayed by 3/4 of a data cell, which is equivalent to 1-1/2 code bit cells. If, when a rising edge transition in non-inverted signal 300 causes FF2 to sample the data at its D input, the sampled data is a 0, then it is known that original encoded signal 300 has been a 0 for two consecutive code bit cells and that the decoded data should change from a logical "1" to a logical "0". Flip-flop FF2 accordingly outputs a 1 on its inverted Q output which is coupled to the reset control input of SR flip-flop FF3. This transition, shown for example by point 314 on signal 316, causes the Q output of FF3 to be set to a "0". The signal at the inverted Q output of flip-flop FF3 is coupled back to the set control input of FF2 to cause signal 316 at the inverted Q output of FF2 to return to 0 after FF3 has been successfully reset. This coupling back prevents flip-flop FF2 from trying to reset flip-flop FF3 at the same time flip-flop FF1 may be trying to set flip-flop FF3.

If, on the other hand, the data at the D input of flip-flop FF2 is a 1 when sampled, it is known that original encoded signal 300 has not been a 0 for two consecutive code

bit cells, indicating that the encoded data has not changed from a logical "1" to a logical "0". Therefore flip-flop FF2 remains in the 1 state (i.e., the signal at inverted Q output of FF2 remains 0) and FF3 is not reset. This is always the result when flip-flop FF2 is clocked by an edge at a boundary of a data cell.

The Q output of flip-flop FF3 is coupled to an input of each of exclusive-OR logic gates 206 and 208. A second input of logic gate 206 is coupled to to the 1/2 clock period delay line of delay element circuit 204 by a plurality of delay matching buffer circuits 210. The Manchester encoded data signal delayed by 1/2 clock period (signal 304) is combined with the decoded data at the Q output of FF3 (signal 312) to recover the clock from the encoded signal.

There is a delay in the decoded data of signal 312 relative to the original data encoded in signal 300. This delay includes a 1/2 data cell delay which, in recovering the clock signal, is compensated for by the delay of 1/2 clock period in signal 304. There is additional delay in the decoded data due to signal propagation delays through flip-flops FF1/FF2 and FF3. Delay matching buffer circuits 210 compensate for this delay (see signal 317). Preferably, flip-flops FF1, FF2 and FF3, and delay matching buffers 210 are implemented in a single integrated circuit to minimize variations in the signal propagation delays of the different

component circuits that might be caused by variations in the semiconductor processes used to manufacture the circuits. ECL devices are preferred because of their speed, although other technologies also may be used. Delay matching buffers 210 can be implemented as desired to emulate the signal propagation delays of the flip-flops during operation. If the circuit is implemented using discrete components, delay matching buffers can be implemented using conventional fixed or programmable delay elements.

The clock signal at the output of exclusive-OR gate 206 (signal 318) is inverted with respect to original clock signal 320. This arrangement is useful for subsequent circuitry because the rising edge of the inverted clock occurs in the center of each data cell of the decoded data (signal 312), thus giving equal set up and hold times for clocking the decoded data into additional circuits. Because the decoded data signal 312 is coupled through exclusive-OR gate 206 to generate the recovered clock 318, the recovered clock will be delayed from the center of the data cells of the decoded data by the propagation delay of exclusive-OR gate 206. If it is desired that the propagation delay of exclusive-OR gate 206 be cancelled, the decoded data signal 312 can be coupled through an optional delay element, such as exclusive-OR gate 208 shown in FIG. 2, preferably in the same integrated circuit, to provide a data signal output having a matching delay.

Thus a novel circuit for decoding a Manchester encoded digital communication signal has been described. One skilled in the art will appreciate that the present invention can be practiced by other than the described embodiments. For example, flip-flops FF1 and FF2 can be replaced by falling edge triggered flip-flops if the clocking inputs provided to the two flip-flops are reversed. Further, each flip-flop can be replaced by other latch circuits having cross-coupled logic gates, and alternate circuitry may be used to condition the control signals provided to set and reset flip-flop FF3 to avoid conflict. The described embodiments are presented for purposes of illustration and not of limitation, and the present invention is limited only by the claims which follow.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:-

1. A method for extracting a data signal from a Manchester code signal, the Manchester code signal having low and high states, rising and falling transitions between the low and high states, and a clock period defining data cells, the method comprising the steps of:

detecting the transitions in the Manchester code signal;

for each detected transition, determining the state of the Manchester code signal at a point in the Manchester code signal between one-half and one clock period preceding the detected transition; and

generating an output signal having first and second states corresponding respectively to low and high states, the output signal being characterized with respect to each detected transition and correspondingly determined state of the Manchester code signal in that:

a. if a detected transition is a rising transition and the determined state of the Manchester code signal is a low state, the output signal changes from the second state to the first state;

b. if a detected transition is a rising transition and the determined state of the Manchester code signal is a high state, the output signal remains in its previous state;

c. if a detected transition is a falling transition and the determined state of the Manchester code signal is a

low state, the output signal remains in its previous state; and

d. if a detected transition is a falling transition and the determined state of the Manchester code signal is a high state, the output signal changes from the first state ~~state~~ to the second state.

2. The method of claim 1 further comprising a method for extracting a clock signal from the Manchester code signal, the clock signal extracting method comprising the steps of:

delaying the Manchester code signal; and

combining the generated output signal in an exclusive-OR logic operation with the delayed Manchester code signal.

3. An apparatus for extracting a data signal from a Manchester code signal, the Manchester code signal having low and high states, rising and falling transitions between the low and high states, and a clock period defining data cells, the apparatus comprising:

means for detecting the transitions in the Manchester code signal;

means for determining for each detected transition the state of the Manchester code signal at a point in the Manchester code signal between one-half and one clock period preceding the detected transition; and

means for generating an output signal having first and second states corresponding respectively to low and high states, the output signal being characterized with respect to each detected transition and correspondingly determined state of the Manchester code signal in that:

a. if a detected transition is a rising transition and the determined state of the Manchester code signal is a low state, the output signal changes from the second state to the first state;

b. if a detected transition is a rising transition and the determined state of the Manchester code signal is a high state, the output signal remains in its previous state;

c. if a detected transition is a falling transition and the determined state of the Manchester code signal is a low state, the output signal remains in its previous state; and

d. if a detected transition is a falling transition and the determined state of the Manchester code signal is a high state, the output signal changes from the first state to the second state.

4. The apparatus of claim 3 further comprising means for extracting a clock signal from the Manchester code signal, the clock signal extracting means comprising:

means for delaying the Manchester code signal; and

means for combining the generated output signal in an exclusive-OR logic operation with the delayed Manchester code signal.

5. An apparatus for decoding a Manchester code signal having data cells each defined by a pair of high state and low state code bit cells and a rising or falling state transition between the code bit cells, the apparatus comprising:

first and second latch means each having a data input, a clocking input, and a data output, for latching a data signal from the data input to the data output when a clocking edge is present at the clocking input;

means for delaying the Manchester code signal between one and two code bit cells and for supplying the delayed code signal to each of the data inputs of the first and second latch means;

means for clocking the first latch means by providing a clocking edge to the clocking input of the first latch means in accordance with each falling transition of the Manchester code signal;

means for clocking the second latch means by providing a clocking edge to the clocking input of the second latch means in accordance with each rising transition of the Manchester code signal;

means for generating a data output signal at a data output, the data output signal generating means having first and second output states corresponding respectively to low and high states and first and second control

inputs;

first circuit means coupled to the first latch means and the data output signal generating means for supplying a first control signal to the first control input of the data output signal generating means when the delayed Manchester code signal supplied to the data input of the first latch means is in a high state when latched by the first latch means, the first control signal causing the data output signal generating means to operate in a first output state; and

second circuit means coupled to the second latch means and the data output signal generating means for supplying a second control signal to the second control input of the data output signal generating means when the delayed Manchester code signal supplied to the data input of the second latch means is in a low state when latched by the second latch means, the second control signal causing the data output signal generating means to operate in a second output state,

whereby the data output signal generating means generates a data output signal representative of data encoded in the Manchester code signal.

6. The apparatus of claim 5, further comprising means for decoding a clock signal from the encoded data signal.

7. The apparatus of claim 5, wherein the first and second latch means respectively comprise first and second edge triggered flip-flop circuits.

8. The apparatus of claim 7, wherein:

the first and second flip-flop circuits each has a control input;

the data output signal generating means includes means for generating an inverted data output signal;

the first circuit means includes means for supplying one of the data output signal and the inverted data output signal to the control input of the first flip-flop circuit; and

the second circuit means includes means for supplying the other of the data output signal and the inverted data output signal to the control input of the second flip-flop circuit.

9. The apparatus of claim 5, wherein the delaying means delays the encoded data signal for 1-1/2 code bit cells.

10. The apparatus of claim 6, wherein the clock signal decoding means comprises:

second means for delaying the Manchester code signal by

at least one code bit cell; and

means for coupling the at least one code bit delayed code signal to one input of an exclusive-OR logic gate, another input of which is coupled to the data output of the data output signal generating means.

11. The apparatus of claim 7, wherein the first and second flip-flop circuits are components of a single integrated circuit.

12. A decoder circuit for generating at a data output an output signal representative of data encoded in a Manchester code signal having a clock period, the circuit comprising:

an input buffer circuit having a data input for receiving a Manchester code signal, an inverting data output and a non-inverting data output;

a delay element having an input coupled to the non-inverting data output of the input buffer circuit, and having an output, the delay element having a delay of three-quarters of a clock period;

a first flip-flop circuit having a data input coupled to the output of the delay element, a clocking input coupled to the inverting data output of the input buffer circuit, a non-inverting data output and a reset input;

a second flip-flop circuit having a data input coupled

to the output of the delay element, a clocking input coupled to the non-inverting data output of the input buffer circuit, an inverting data output and a set input; and

a third flip-flop circuit having a set input coupled to the non-inverting data output of the first flip-flop circuit, a non-inverting data output coupled to the reset input of the first flip-flop circuit and to the data output of the decoder circuit, a reset input coupled to the inverting data output of the second flip-flop circuit, and an inverting data output coupled to the set input of the second flip-flop circuit.

13. The decoder circuit of claim 12, further comprising means for generating at a clock output of the decoder circuit a clock signal representative of the clock encoded in the Manchester code signal, and for generating at the data output of the decoder circuit a synchronized data signal, the means comprising:

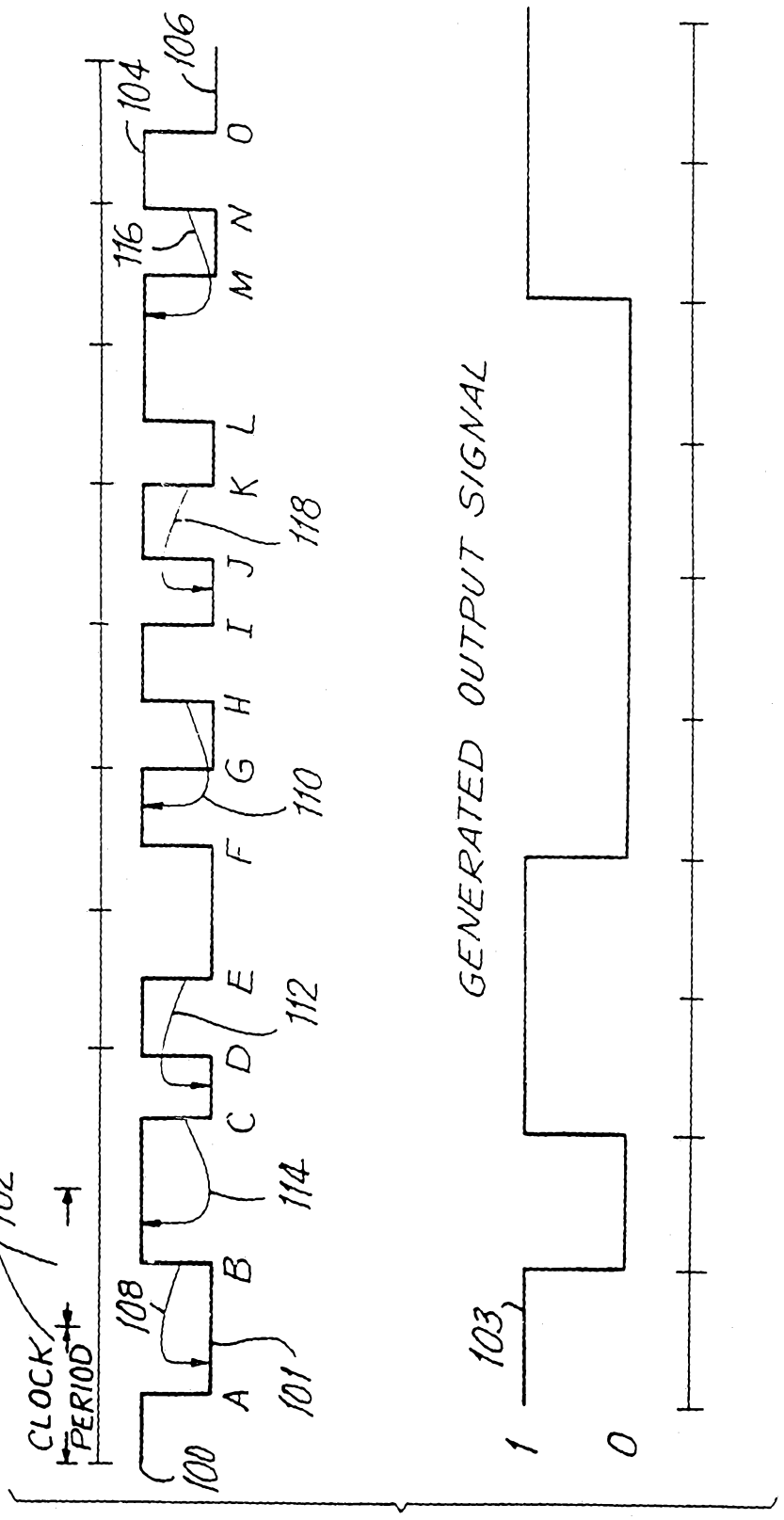
an exclusive-OR logic gate having a first data input coupled to the non-inverting data output of the third flip-flop circuit, a second data input and a data output coupled to the clock output of the decoder circuit;

a second delay element having an input coupled to the non-inverting data output of the input buffer circuit, a data output and a delay of one-half of a clock period;

at least one delay matching buffer circuit coupled in

series between the data output of the second delay element and the second data input of the exclusive-OR logic gate; and

a third delay element coupled between the non-inverting data output of the third flip-flop circuit and the data output of the decoder circuit.


MANCHESTER ENCODED WAVEFORM
CLOCK PERIOD
102
100
101
108
A
B
114
C
D
112
E
F
110
G
H
I
J
118
K
L
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M
N
104
106
O
GENERATED OUTPUT SIGNAL
103
1
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FIG. 1

60596/90

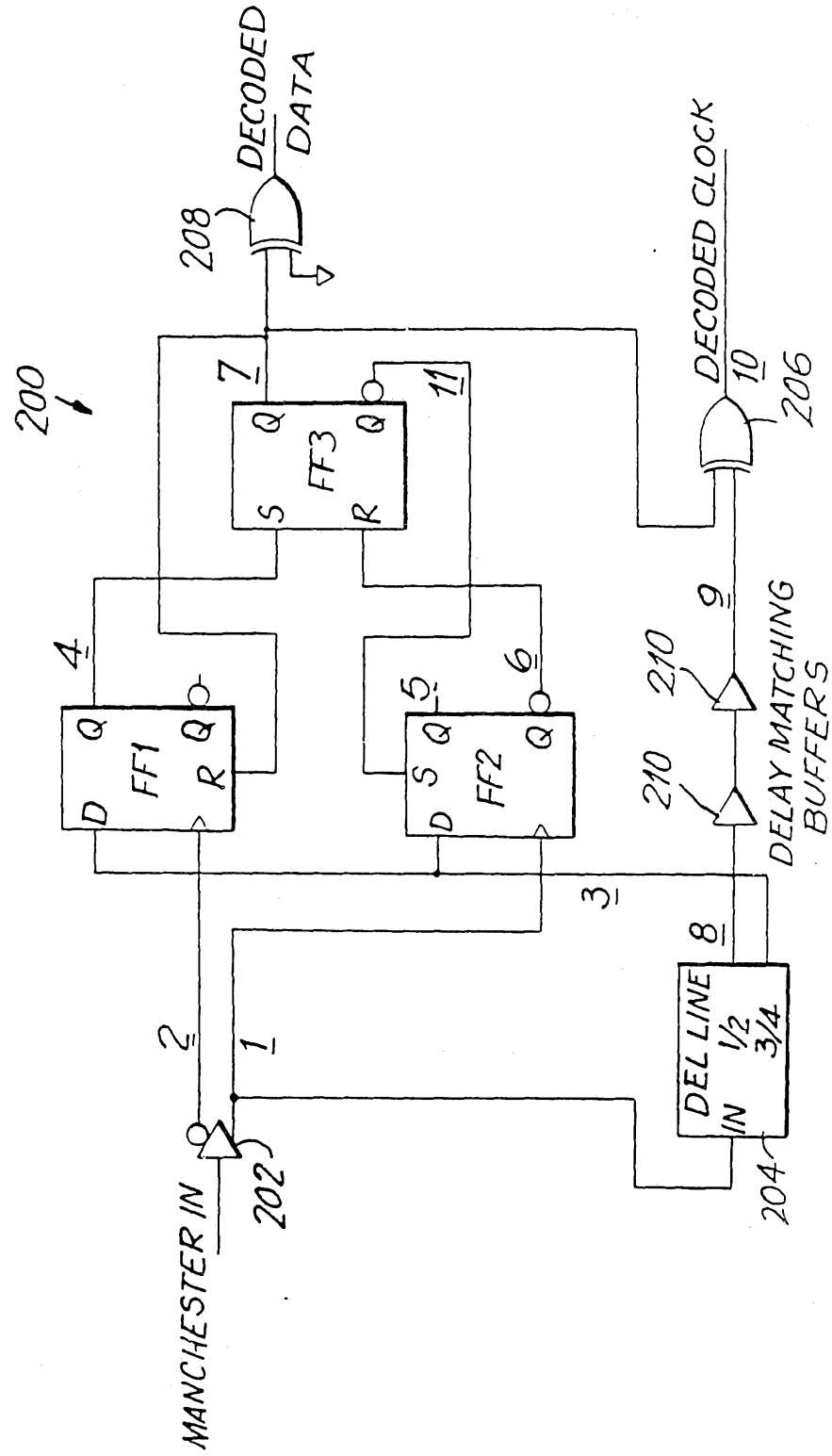
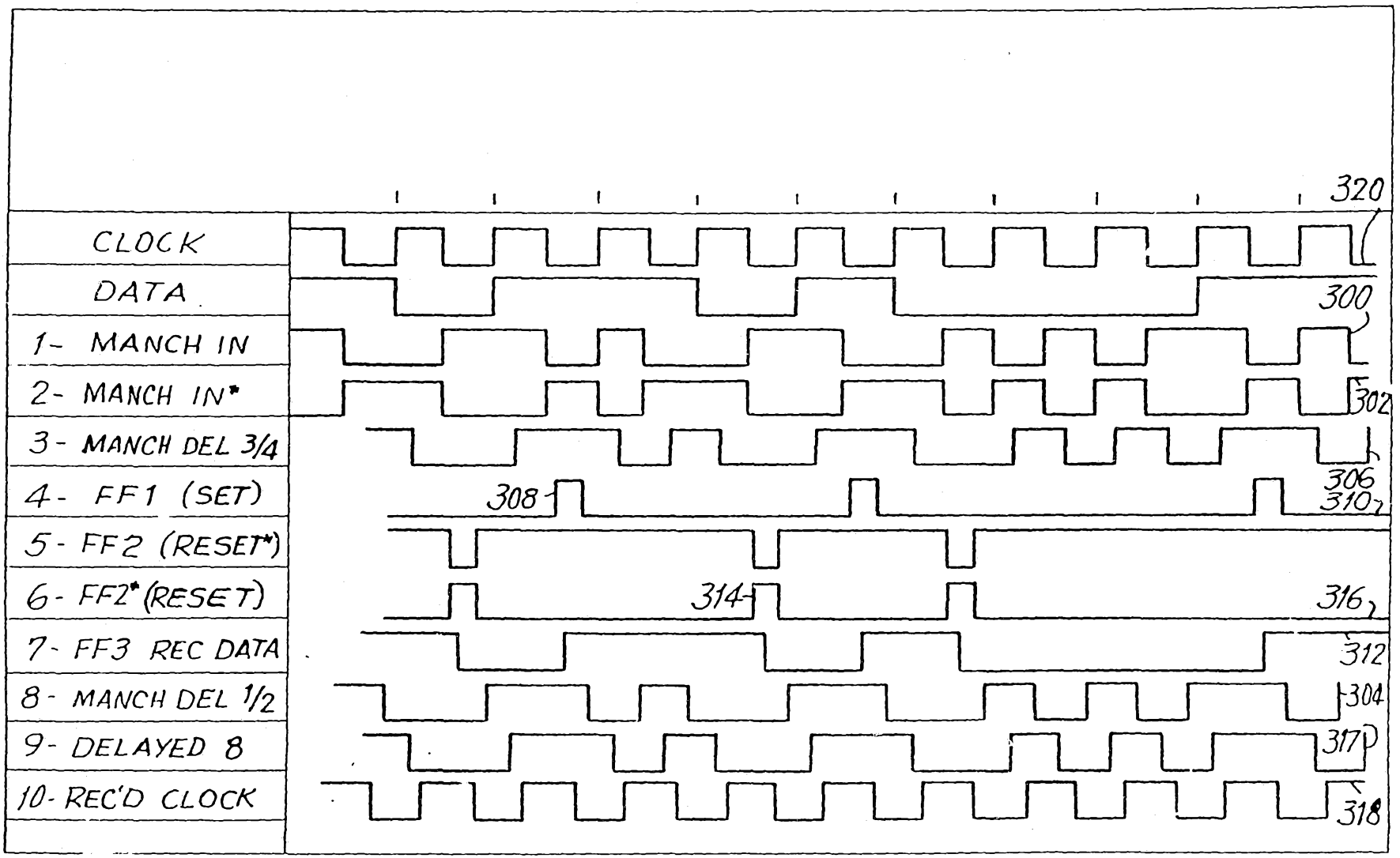


FIG. 2

FIG. 3



INTERNATIONAL SEARCH REPORT

International Application No PCT/US 90/03629

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 H03M5/12

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	H03M ; G11B ; H04L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category[10]	Citation of Document,[11] with indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
X	US,A,3659286 (C.R.PERKINS ET AL.) 25 April 1972 see column 2, line 30 - column 4, line 70; figures 1-2 ---	1, 3-4, 12-13
A	DE,A,2234203 (LICENTIA PATENT-VERWALTUNGS-GMBH) 31 January 1974 see page 8, line 25 - page 38, line 8; figures 1-5 ---	1-4, 12-13
A	EDN ELECTRICAL DESIGN NEWS. vol. 17, no. 18, 15 September 1972, NEWTON, MASSACHUSETT page 48 P.ALFKE: "EXCLUSIVE-OR GATES SIMPLIFY MODEM DESIGNS" see the whole document ---	1-5, 12-13

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[10] Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
22 OCTOBER 1990	16. 11. 90
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	CARTRYSSE A.

Form PCT/ISA/210 (second sheet) (January 1985)

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
A	INTERNATIONAL JOURNAL OF ELECTRONICS. vol. 49, no. 2, August 1980, LONDON GB pages 175 - 177; M.S.PRAKASH RAO ET AL.: "MANCHESTER DECODER USING SN-7474" ---	
A	US,A,3594738 (P.R.CALLENS) 20 July 1971 ---	
A	EP,A,0168770 (SIEMENS AG.) 22 January 1986 ---	
A	GB,A,2171277 (THE PLESSEY COMPANY PIC) 20 August 1986 ---	
A	EP,A,0194385 (INTERNATIONAL COMPUTERS LIMITED ICL HOUSE) 17 September 1986 ---	
A	PATENT ABSTRACTS OF JAPAN vol. 9, no. 23 (E-293)(1746) 30 January 1985, & JP-A-59 171242 (FUJITSU K.K.) 27 September 1984, see the whole document ---	

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO.

PCT/US 90/03629
SA 38927

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information. 22/10/90

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A-3659286	25-04-72	None	
DE-A-2234203	31-01-74	None	
US-A-3594738	20-07-71	DE-A- 1913357	09-10-69
		FR-A- 1584497	26-12-69
		GB-A- 1227517	07-04-71
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		US-A- 4663767	05-05-87
GB-A-2171277	20-08-86	None	
EP-A-0194385	17-09-86	AU-B- 582220	16-03-89
		AU-A- 5442186	11-09-86
		JP-A- 61208318	16-09-86
		US-A- 4688232	18-08-87