

[54] **FLEXIBLE COMPUTER ACCESSED
TELEMETRY**

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[58] **Field of Search** 340/172.5, 150; 178/50, 69.5;
179/15 BV

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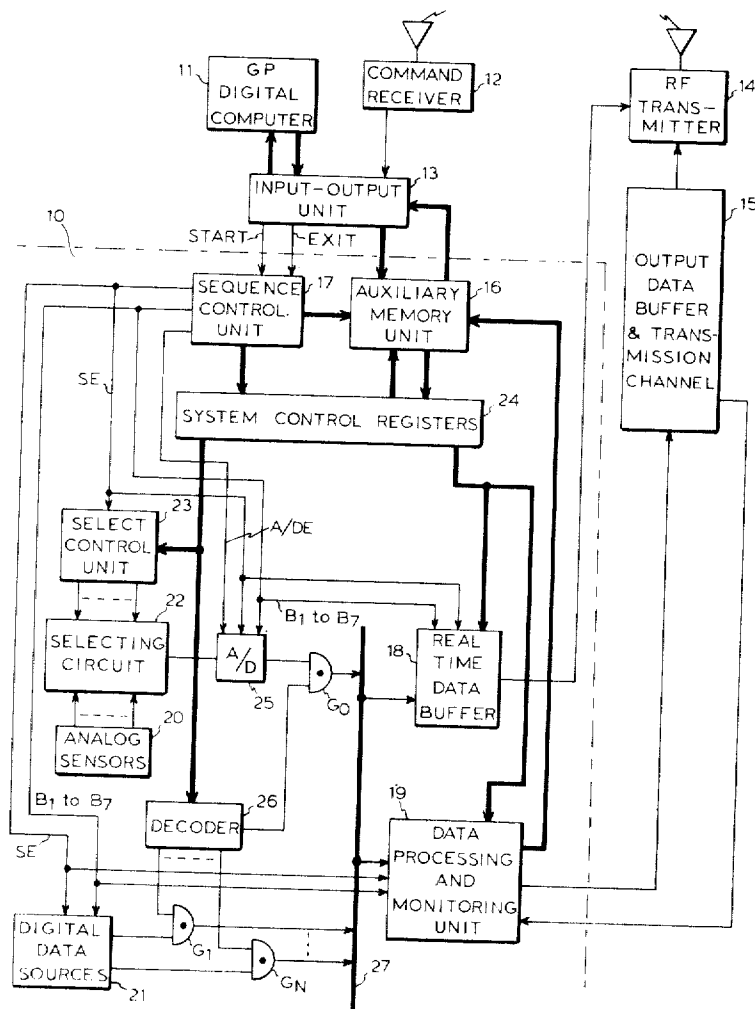
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[57]

ABSTRACT

Flexible, computer-accessed telemetry is provided by a sequence control unit, auxiliary memory and system control registers to permit sensors and digital data sources to be sampled in a programmed format with various groups of samples taken at different rates. Each programmed sample may be processed for transmission in a specified way by including an operation code with the programmed address code used to select the designated sensor or digital data source. Index registers and a scratch pad memory permit flexibility in programming sample sequencing formats. A particular format may be started, stopped and altered by ground station commands received through a receiver, or directly by a digital computer.

12 Claims, 6 Drawing Figures



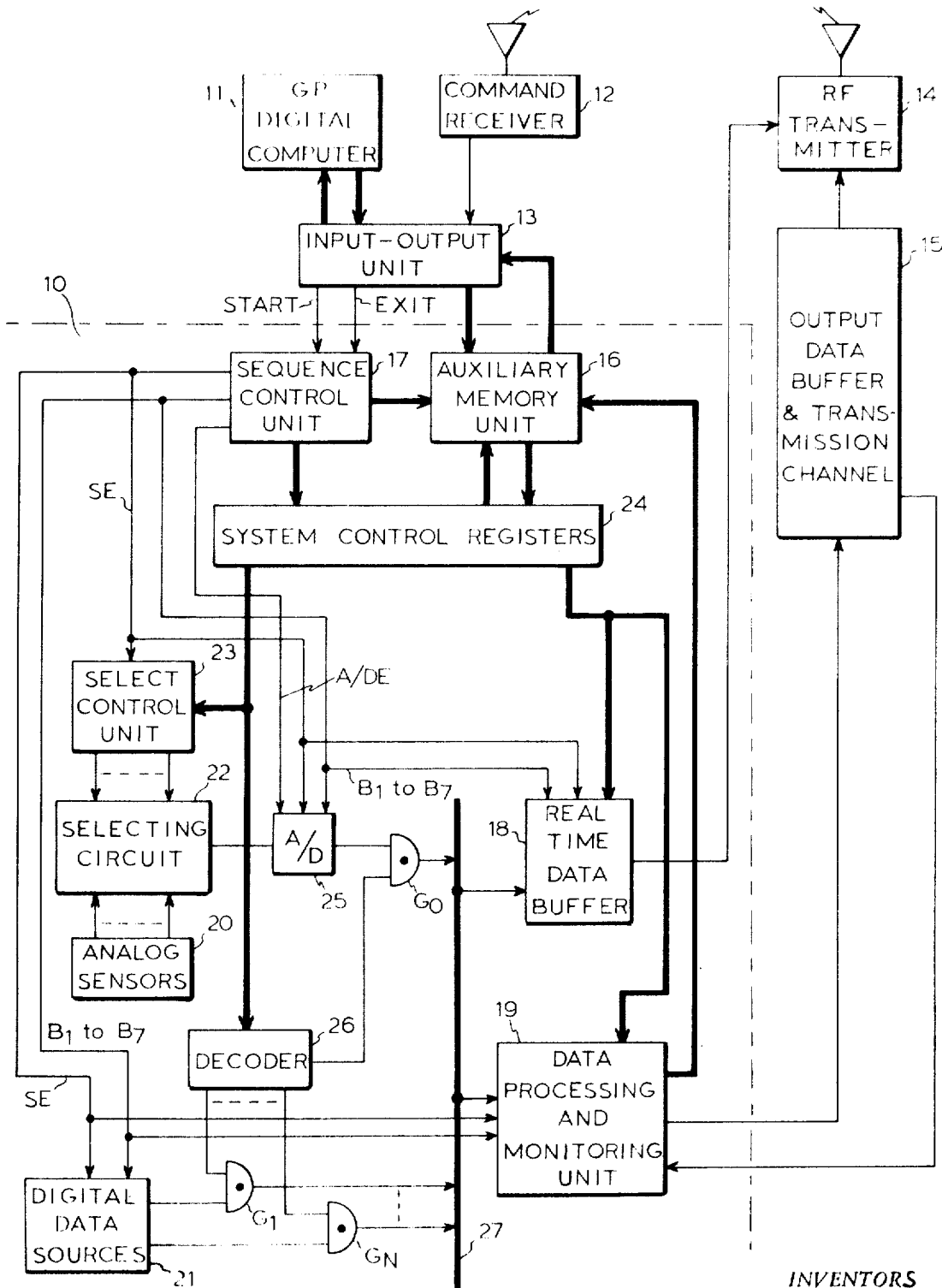


FIG. 1

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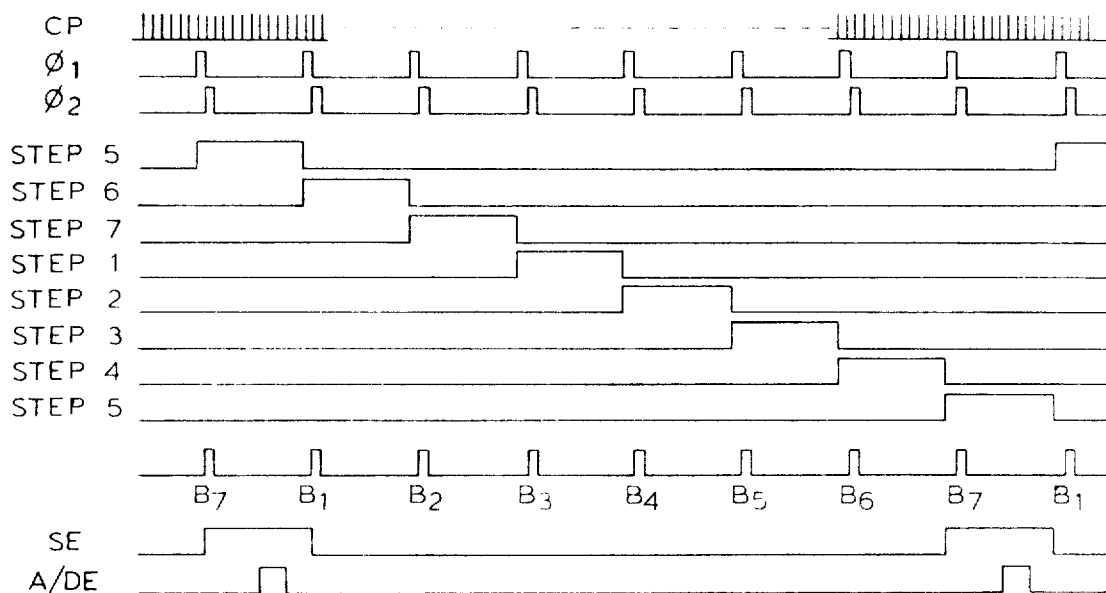


FIG. 2

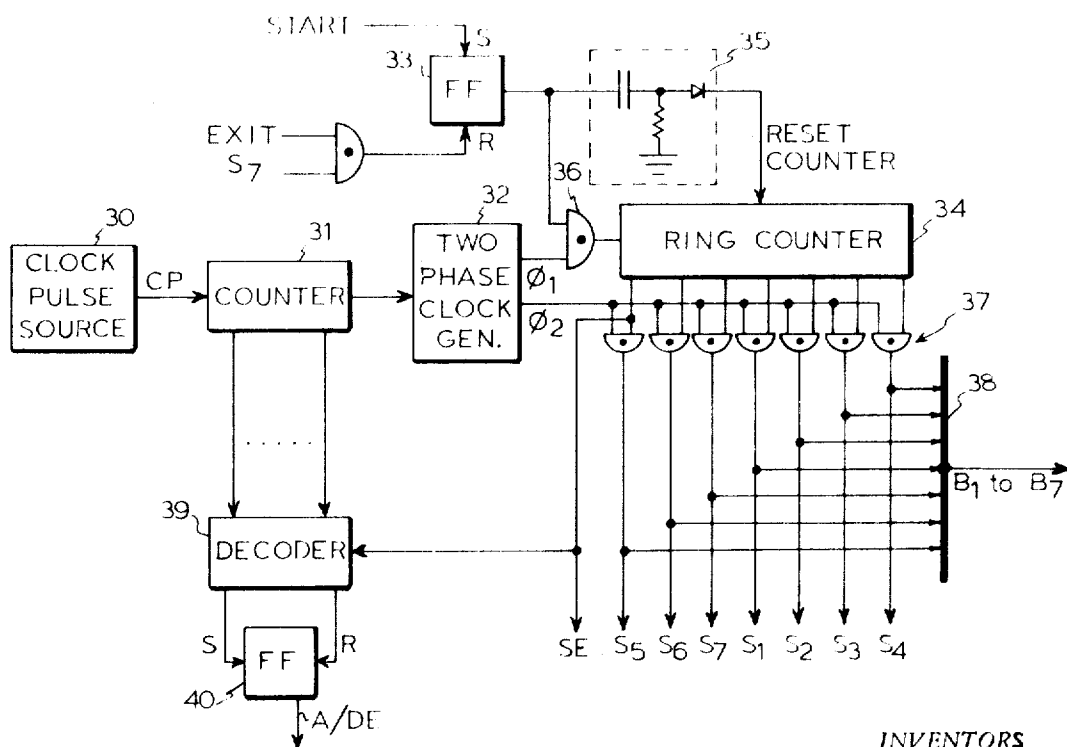
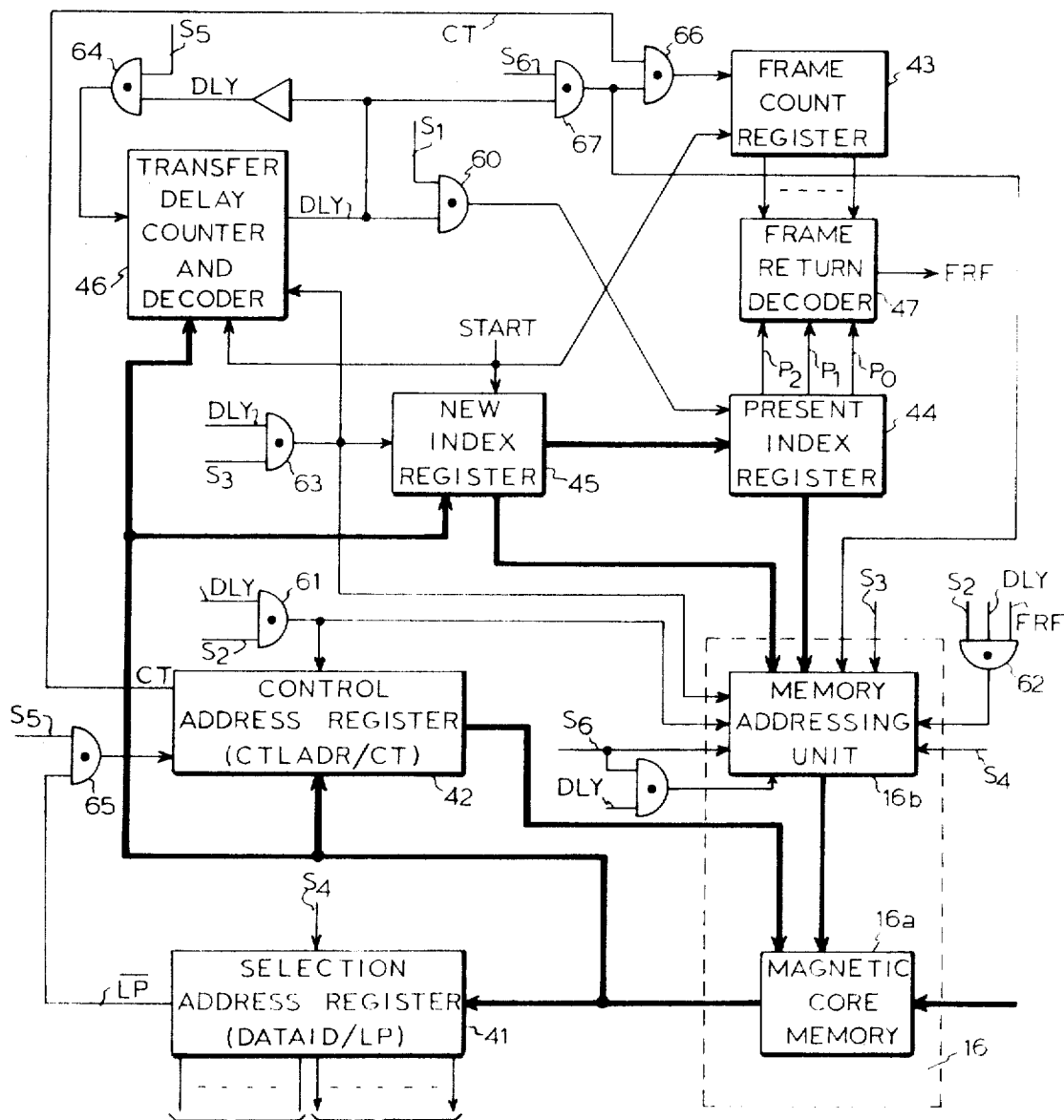


FIG. 3

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OP CODE ADDRESS CODE
BITS TO TO SELECTION
UNITS CONTROL UNIT 23
18 & 19 AND DECODER 26

FIG. 4

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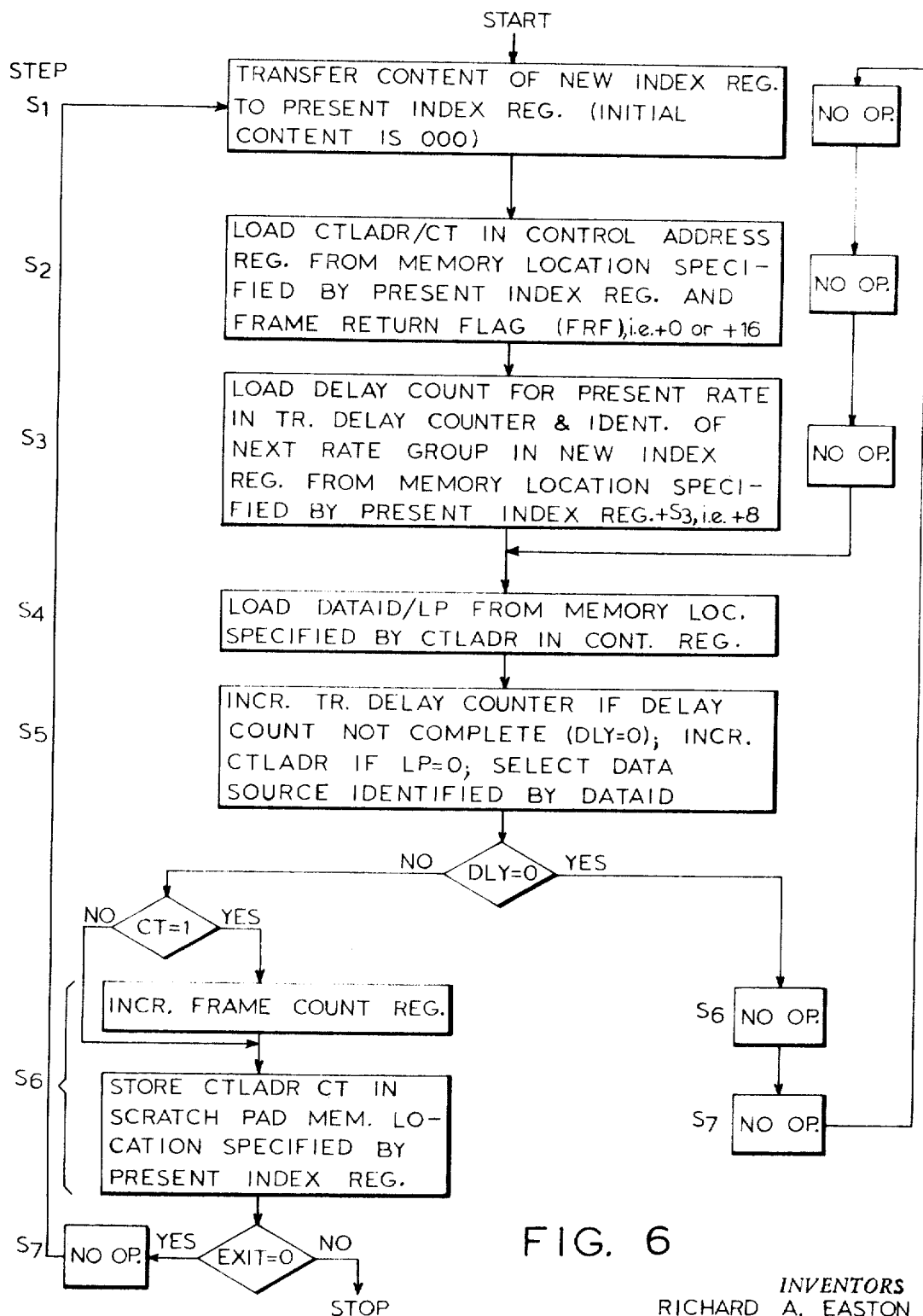


FIG. 6

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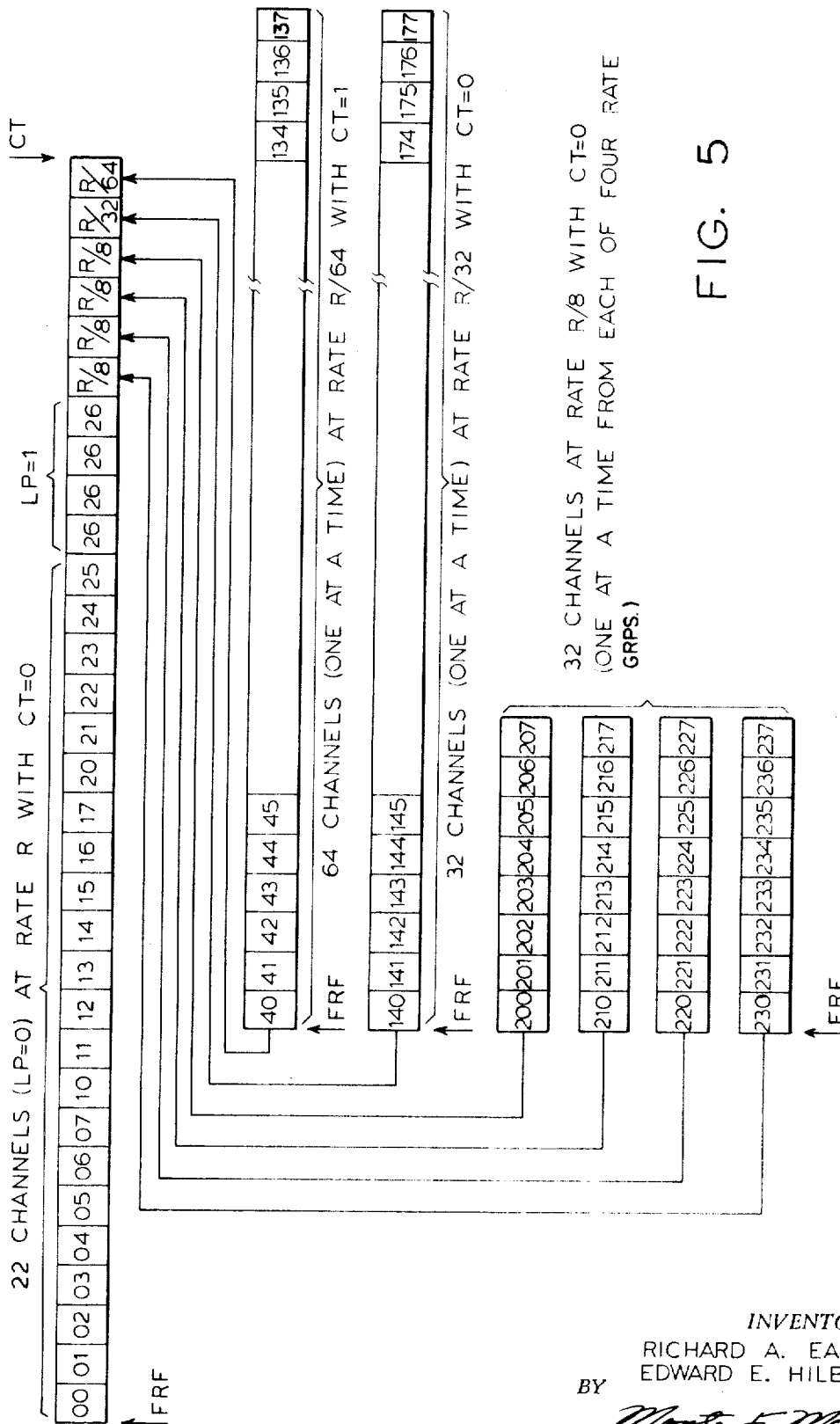


FIG. 5

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FLEXIBLE COMPUTER ACCESSED TELEMETRY

ORIGIN OF INVENTION

The invention described herein was made in the performance of work under a NASA contract and is subject to the provisions of Section 305 of the National Aeronautics and Space Act of 1958, Public Law 85,568 (72 Stat. 435; 42 USC 2457).

BACKGROUND OF THE INVENTION

This invention relates to data telemetry and more particularly to programmed telemetry which can be accessed by a computer to change the program for greater flexibility.

In the past data telemetry systems have been provided with a substantially fixed sampling sequence derived from a clock controlled commutator. In the extreme, the commutator has been comprised of stepping switches with one or more decks for sampling different groups of sensors or digital data sources at different rates. To change the sequence, a physical change was required in the clocks. In more recent systems using solid state commutators, the task of changing the sequence required changes in logic or selection networks. It would be desirable to provide a flexible telemetry system which can be readily changed by a computer under control of a stored program or by external commands. Such a system would have great advantage in many applications, particularly space exploration applications where changing conditions require different sequencing formats at different stages of the exploration mission, particularly for outer planet missions which will last anywhere from eight to twelve years.

SUMMARY OF THE INVENTION

In accordance with the present invention, a computer-accessed telemetry system is provided to control sampling of analog and digital data from a plurality of sources, each data source being identified by a unique code. The system comprises an auxiliary memory unit which stores the identification codes of sources to be sampled in groups according to the rate at which they are to be sampled, each group being stored in sequential locations of a separate block of memory. Three additional blocks of memory are reserved for sequence control, each block having a number of memory locations for a corresponding number N of distinct rates of R , $R/2^1$, $R/2^2$, ..., $R/2^n$, where R is the maximum rate at which any source may be sampled for a given sequencing format, and N is equal to $n+1$. One block of N locations is used to store a control word for each rate which specifies the memory location of the first source identification code to be sampled in the particular rate. Each time the control word is used to obtain a source identification code, a sequence control unit increments the control word and stores it in a memory location of another block (scratch pad) of N locations associated with the first by the rate of the group controlled by the word. The control word or each group includes a flag bit (CT) set equal to 1 for only the last group to be serviced in order. The third block of N memory locations is reserved for storing the number of samples to be included in each group. That provides controlled delay for the sequence control unit between groups. The control unit automatically cycles through programmed groups, taking the number of samples of each group in sequence (as specified by the number stored in an associated memory location of the third block of N locations) before storing the control word associated therewith in the associated scratch pad location. The control unit then obtains a new control word for the next group from the memory location associated with that next rate group.

The delay control number for the previous rate group, as read from a location in the third block of N locations, includes a field of binary digits uniquely identifying both the rate and the associated memory location in the first, second and third blocks of memory. That field is stored in a first register while the previous rate group is being serviced and then transferred to a second register for use while servicing the identified rate

group. Once a control word has been read, incremented and stored in the associated scratch pad memory location, it is retrieved from scratch pad memory for subsequent servicing of the rate group. A counter counts the CT flags included with the control words (which flags are also stored in scratch pad memory as part of the control words) to permit a determination of when the sequence control unit should go back to the first block of N memory locations to obtain the original control word for a given rate group, thus recycling within the rate group automatically. Each data source identification read from the auxiliary memory includes a flag LP which, when programmed as a bit 1, will inhibit the control word (for the group in which included) from being incremented, thus providing for multiple sampling in rapid succession. A computer may alter the program at any time by stopping the sequencing unit after any seven-step cycle in progress and altering the sequencing format in memory before starting the sequencing unit again.

The novel features that are considered characteristic of this invention are set forth with particularity in the appended claims. The invention will best be understood from the following description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a programmable telemetry system according to the present invention.

FIG. 2 is a timing diagram for a sequence control unit of the system of FIG. 1.

FIG. 3 is a schematic diagram of a timing circuit for producing the timing signals of FIG. 2.

FIG. 4 is a schematic diagram of the sequence control unit of FIG. 1 for control of processing a programmed sequencing format stored in an auxiliary memory unit through control registers in accordance with a preferred embodiment of the present invention.

FIG. 5 is an exemplary sample sequencing format to be processed in accordance with the present invention.

FIG. 6 is a flow chart for operation of the apparatus of FIG. 4.

DESCRIPTION OF PREFERRED EMBODIMENTS

FIG. 1 shows the general organization of a programmable access telemetry system 10 in a spacecraft having a general purpose (GP) digital computer 11 and a command receiver 12. An input-output (I/O) unit 13 is provided to enable the GP computer to receive commands from a ground station through the receiver 12 and to cause the system 10 to transmit spacecraft data, either on a real-time basis directly through a transmitter 14 or on a programmed basis through an output data buffer and transmission channel 15.

It should be noted that while a programmable access telemetry system has been shown in a spacecraft application, the present invention embodied therein is not limited to spacecraft applications. As noted herein-before, the present invention departs from the prior art technique of sampling data in a fixed sequence set by a clock-controlled commutator to sampling data in a sequence set by a program stored in an auxiliary memory unit 16 of the telemetry system. The memory unit is preferably a random access memory shared by the GP computer via the I/O unit 13 and a telemetry sequence control unit 17. Accordingly, the telemetry system and the command receiver are both essentially simply external or peripheral units coupled to the GP computer 11 in a conventional manner through the I/O unit.

I/O units for scientific applications are often designed for the particular application, as are the GP computers, particularly in spacecraft applications because of size, weight and power restrictions. However, standard or commercial computers and I/O units designed for scientific applications may be employed in other applications, such as marinecraft applications. For example, the SDS-930 computer with a data mul-

timeplexing system supplementing the standard I/O unit of the computer could be used, but the SDS-920 computer with standard input output buffers would be adequate for those applications which do not have high data rates. In most applications, the GP computer will interface with still other systems not shown.

The sequence control unit is started by a START command signal from the GP computer to initiate a programmed data sampling sequence stored in the memory unit as "index words" and "control words" which can be altered by the GP computer, to change the rate at which certain data is sampled, for example. The sampling sequence programmed is repeated until the digital computer stops the sequence control unit with an EXIT command. The ground station can also start, stop and alter the sampling sequence through commands entered into the computer via the command receiver 12 and I/O unit 13. For more direct ground control, the I/O unit can be provided with direct communication channels from the receiver to the sequence control unit and memory unit. However, for simplicity it is assumed that communication is through the GP computer in this exemplary embodiment.

Basically, the sequence control unit functions as a special purpose control computer using a nested DO loop procedure, i.e., using iterative subroutines to sample data at any desired frequency. Every sample ordered is called for by a stored program. Because that program can be arbitrarily altered at will, sampling can be said to be with random access. However, in order not to tie up the GP computer and/or the command receiver, the system 10 operates independently and the programmed sequence is changed by the GP computer 11 only as circumstances require, such as when data from a given sensor exceeds limits so as to require more frequent sampling of that sensor while remedial action is being taken, or when a command is received from a ground control station through the receiver 12.

This programming flexibility also makes it possible to sample and generate two or more simultaneous sequences at once so that one can be transmitted to ground in real time, while a different one is being processed, monitored and/or stored for later transmission via the channel 15. The data processing is selected for each particular data source and may include data and data compression according to any one of a plurality of known techniques. The latter may be used to alert the GP computer of a condition which requires more frequent sampling, remedial action or some other action under supervisory control of the GP computer. The real time data transmission is accomplished through a data buffer 18 which allows data samples at random times to be stored for transmission at regular times and may also allow for data compression using any one of a plurality of known techniques selected for the particular samples. Such a technique for buffering real time data is standard. The data processing and monitoring techniques contemplated for inclusion in unit 19 are also standard. What is new is provision for a readily alterable program with either real time data sampling and transmission, or data processing and monitoring of sampled data with delayed transmission of some or all data, or both simultaneously. The sequence control unit to be described more fully with reference to FIG. 4 makes this flexibility possible.

The data being sampled emanates from either analog sensors represented by a block 20 or other data sources such as scientific instruments which provide data already in digital form. The digital data sources are represented by a block 21. In either case, there are the two possible major paths for data in the system, one for real time data transmission via the buffer 18, and one for data processing and monitoring (with possible delayed transmission) via the unit 19.

The outputs of the analog sensors are applied to a selecting circuit 22, such as a selecting tree. A control unit 23 receives address codes from a unit of system control registers 24 to select a sensor for sampling and analog-to-digital conversion in an A/D converter 25 under timing control of the sequence control unit 17. The system control registers are loaded from

memory under timing control of the unit 17. A digital data source is similarly selected through a decoder 26 which enables a selected one of AND gates G_0 to G_n associated with the desired data source. When one of the gates G_1 to G_n is not being selected, the gate G_0 is thus selecting the A/D converter as the data source. That is readily accomplished by reserving for the analog sensors the lower half of the 2^n selecting codes possible with an n -bit code. The gate G_0 is then enabled only when the most significant bit is false, and one of the gates G_1 to G_n is enabled when the most significant bit is true. An OR gate 27 couples the outputs of the AND gates G_0 to G_n to the data buffer 18 and the data processing and monitoring unit 19. The selection of a data source is controlled by a field of binary digits in the selection being stored in one of the system control registers for the given sample.

The A/D converter is provided with an output register, such as a seven-bit register, in which the digital value of the analog signal is developed. For example, using the successive-approximations technique, the bits are set true in the register in sequence starting with the most significant bit position, and the output of the register is converted back into analog form for comparison with the sample stored in a sample-and-hold circuit. If the sample signal is exceeded, the last bit set is reset, and the process of conversion continues until all seven bits have been properly set in just eight clock periods. The clock periods are metered by clock pulses (CP) from a high frequency oscillator 30 shown in FIG. 3. Once eight clock pulses have been applied, following a sample pulse from the sequence control unit 17, further application of CP pulses to the output register is inhibited until the next sample pulse occurs. In the meantime seven shift control pulses B_1 to B_7 are applied to the output register for serial readout through the gate G_0 . Data from selected digital data sources are similarly read from output registers in the block 21 under control of the shift control pulses B_1 to B_7 from the sequence control unit 17.

FIG. 2 shows a timing diagram for these shift control pulses B_1 to B_7 from the sequence control unit. The selection of sensor, or data source, is made during STEP 5 of the sequence control unit by a select enable signal (SE). The conversion is then enabled by an A/D signal which is true for eight clock pulses. The leading edge of the next A/D pulse can be used to reset the output register for the next conversion cycle, but in practice that register is simply cleared as the seven-bit number is shifted out. For a digital data source, the signal SE is used to read into buffer registers within the block 21 data from all of the sources. The seven shift pulses B_1 to B_7 are then used to simultaneously read out the data words in series. The decoder 26 then selects only one data word. This organization is feasible because the bank of buffer registers necessary can be readily provided using integrated circuit technology. An alternative organization would be to provide only one buffer register and banks of selection gates to read out only one digital data source in parallel into that register in response to the signal SE. The shift pulses would then be employed to serially transfer the data word to the data buffer 18 and monitoring unit 19. These arrangements are suggested by way of example, and not limitation; still other equivalent arrangements within the scope of the invention will occur to those skilled in the art.

The sequence control unit includes a sequencing section shown in FIG. 3 for producing the timing signals shown in FIG. 2. System clock pulses from a source 30 are counted by a counter 31 (to divide the clock pulses by 32, for example). The lower rate pulses are then applied to a two-phase clock generator 32, thereby producing phase displaced clock pulses 0_1 and 0_2 at the lower rate. A START command signal from the GP computer sets a flip-flop 33 to enable a seven-stage ring counter 34 to be reset to an initial condition (state 1) in response to a pulse generated by a differentiating network, 35 and to enable the ring counter to be operated by 0_1 clock pulses via a gate 36. As successive stages of the counter are turned on in sequence, signals from the stages mark the seven steps of a sample sequencing cycle. Each step signal gates a 0_2 pulse through one of a bank of gates 37 to produce a sequence of pulses, S_1 to S_7 .

All of the signals S_1 to S_7 are combined through an OR gate 38 to produce a continuous train of shift pulses (B_1 to B_7). The STEP 5 signal, from which the pulse S_8 is derived, is employed as the select enable signal SE referred to hereinbefore. It is also employed to enable a decoder 39 connected to the counter 31 to set a flip-flop 40 at a predetermined count (for example 18) and to reset the flip-flop eight system clock pulses later. The output of the flip-flop is then employed as a control signal A/DE to enable the A/D converter 25. A sensor is thus selected, and a sample taken, during the first 18 periods of the system clock pulses. Conversion then takes place during the next 8 periods of the system clock pulses. Thereafter, bit pulses B_1 to B_7 read out the digital number.

If an analog sensor is not selected, the gate G_2 is not enabled, thus effectively shutting out the A/D converter. In practice, operation of the A/D converter would be inhibited when an analog sensor is not being selected to avoid unduly exercising the A/D converter.

The control lines and serial data transmission lines in the system thus far described are properly represented as single lines, except the selection lines from system control registers 24 to the sensor select control unit 23 and decoder 26; those lines are represented by heavy lines to be cables because they include separate lines for parallel transmission of a selection code, such as an eight-bit code for a system of 511 possible analog sensors and digital data sources to be selected. As each sensor or data source is selected in response to a selection code read from memory, the channel and mode of channel operation are selected by an operation code taken from a different field of the same word read from memory to obtain the selection code. Accordingly, cables are shown for parallel transfer of words to and from the system control registers, and to the buffer 18 and data processing unit 19. Cables are also shown for parallel transfer of data words to the memory unit for stage and/or transfer to the GP computer via the I/O unit 13 and from the GP computer to the memory unit via the same unit. In addition, cables are shown between the sequence control unit 17 and both the system control registers and the sequence control unit for transmission of the various control signals.

The sequence control unit 17 includes the timing networks of FIG. 3 and other control logic while the system control registers 24 include as a unit all registers and counters. Since the control unit and control registers interact extensively, both will be described in greater detail with reference to FIG. 4. To further facilitate understanding an exemplary embodiment of the present invention, the auxiliary memory unit 16 is shown in FIG. 4 divided into a magnetic core memory 16a and an addressing unit 16b which controls both storing and reading operations in a conventional random access core memory system. Thus it should be understood that with reference to the organization illustrated in FIG. 1, the memory unit 16 and the registers and counters of FIG. 4 are not a part of the sequence control unit; this division is arbitrary and for purposes of description only.

The memory access rate is 1.5 MHz, and can be used to program the sampling of data from one group of up to 256 locations or channels of sensors and digital data sources (normally 32) at a given rate R ; and additional groups of locations at lower rates $R/2, R/4, \dots, R/2^n$, where n is arbitrarily selected to be equal to seven for a total of eight different rate groups. If 256 is the total number of locations or channels to be selected, their addressed may be arranged in one of various different rate-group patterns (referred to hereinafter as formats) in memory. The number of different formats possible is virtually without limit since the total number of different accessible channels can be arranged in different combinations and permutations. For an exemplary implementation, assume the memory locations are allocated (in octal code) for this telemetry system as follows:

LOCATION	CONTENT	USE
000-007	CTLADR/CT	Scratch pad memory for

010-017	DELAY/NI
020-027	CTLADR/CT
030-377	DATAID/LP

control words
Number of samples in present group and group rate identification for next group
Control word memory
Data source identification memory for next group

Each of the locations reserved for the group rate identification include a field DELAY of six bits to specify the number of data (analog or digital) sources to be sampled in a given rate group, and a field NI of three bits to specify the least significant octal digit of a memory location from 010 to 017 for the next rate group. For example, if it is to be a rate group $R/8$, the field NI will store an octal 3, thereby specifying memory location 013 for the next rate group identification. Assuming the present rate group is 26 at the rate R , the DELAY field will store a number equal to 63-26. As each data source of the present rate group is sampled, that number is incremented so that when the count of 63 is reached, a signal DLY is generated to advance the programmed sequence control unit to the next rate group specified in memory location 013.

The DELAY field for all rate groups of a given format except the first group at rate R , will always be 63-1, so that only one source is sampled before another signal DLY again advances the sequence control unit. For the rate group $R/8$, one source is sampled every minor frame (a minor frame being a sequence which runs through all programmed rate groups one time), and for the first seven minor frames, the location in memory for the data source identification to be used in the next minor frame is stored in the scratch pad memory at location 003. Thus the octal number 3 is used to not only point to a memory location 013 to go from the last rate group to the present, but also to point to the memory location 003 as the place to store a control word address (CTLADR/CT) after it has been incremented in order to fetch the data source identification (DATAID/LP) for the next source to be samples in that rate group $R/8$ during the next minor frame.

Upon entering a new frame group, such as the rate group $R/8$ for the first time, and every eighth time thereafter, the required control word address (CTLADR/CT) is taken from a location in the sequence 020 to 027 associated with that rate group by the least significant octal digit, in this case location 023. Thereafter, for the intervening minor frames, the control word address is taken from the scratch pad memory location associated with that rate group, in this case location 003.

Each control word address carries a flag bit CT which is a binary 0 in all cases for all rate groups, except the last rate group, and a binary 1 for the last rate group. Assuming the last rate group is a group of 64 data sources or channels as shown in an exemplary format in FIG. 5, for a group rate of $R/64$, the control word address CTLADR/CT of the memory location (in the block from 030 to 377) selected for the data source identification of the first channel 40 is read from memory location 026, used to select the channel 40, incremented and stored in scratchpad memory location 006. For example, the CTLADR field may specify memory location 126 where the code 040 is to be found. Before being stored in scratch-pad memory, it is incremented to 127 so that during the next minor frame, the code 041 may be read from memory location 127.

It should be noted that the source identification codes need not be grouped in sequential order since the source selection system described with reference to FIG. 1 permits random selection. The next channel could just as well have been 319, or any other of 511 channels. The limit of 511 is due to only eight bits being available in the data source identification (DATAID/LP) to be read from memory. It should also be noted that in this exemplary embodiment, the memory is assumed to include only 232 memory locations from 030 to 377 in octal code. Therefore, all 511 channels cannot be included in a programmed sequencing format because one memory location is required to store each data source identification code

of each included. In other words, although an eight-bit code permits 256 possible source identifications, only 232 can actually be accommodated. If more must be accommodated it would be a simple matter of providing for more bits in the source identification bit.

One bit of the data source identification word is a flag which is normally programmed as a binary 0 if the channel specified is to be addressed only once during the current minor frame. If a channel is to be sampled a number of times during the minor cycle, the flag LP is set equal to 1. That is used to inhibit incrementing the control word (CTLADR/CT), thereby causing the same channel to be addressed until the DELAY number has been incremented to 63. This special feature is useful, for example, to make several readings in rapid succession for the purpose of computing an average reading without repeating the data identification word DATAID in memory at successive memory locations. In an exemplary format, it is only used for that purpose at the end of the first rate group. If it is used in any other rate group, the delay counter is stored with the number controlling the number of samples to be taken before entering a new number in the new index register. Thereafter an FRF signal will cause the next control word to be taken from the associated memory location in the block from 020 to 027 instead of from the associated scratch pad memory location in the block 000 to 007.

Each source identification word (DATAID/LP) is, as just noted, a nine-bit word if only programmed sequencing is to be provided in accordance with the present invention. In some applications, it is desirable to program specific data processing for each sample, such as for real-time data transmissions with a particular type of data compression or delayed data transmission with data processing and monitoring. The data processing may, for example, include comparison with the last sample to determine whether the change has exceeded a predetermined value. If so, the GP computer may be alerted (over a line not shown) or the ground station may be alerted by including with the data to be transmitted a predetermined code. Following that the new sample value will replace the old sample value in the memory with the source identification, i.e. as a field of the DATAID/LP word. To accomplish that, the DATAID/LP word must include an additional field for an operations code which will specify the data processing to be carried out by the buffer 18 and the data processing and monitoring unit 19. How the operations are carried out is not part of this invention which relates to a programmable telemetry system.

Another feature of the system illustrated in FIG. 1 is that the output data buffer and transmission channel may be monitored to determine when the buffer is getting too full. When that occurs, the unit 19 will receive a buffer-full signal, and generate a code or interrupt signal which will cause the GP computer to alter the sample sequencing format to a form that will alleviate the buffer-fullness problem. Another possibility would be for the output data buffer to transmit buffer-fullness data and for the unit 19 to carry out all of the monitoring tasks on buffer fullness. In either case, the important feature of the present invention, namely a programmable sequencing format can be used to advantage in preventing the loss of data due to overflow of the output data buffer.

This novel arrangement allows sampling rates to be optimized individually for each sensor. By changing the program stored in the memory, any sensor or digital data source can be added, deleted, or have its sampling rate changed without significant change in the sample rates of others. In addition, disposition of the data can be tailored and changed at will for each sensor or digital data source.

Before describing the exemplary format shown in FIG. 5 in greater detail, the organization and operation of the sequence control unit 17 and system control registers will be more fully described with reference to FIG. 4, and a flow chart shown in FIG. 6. For convenience all of the system control registers, namely two index registers, and two address registers are shown with the components of the sequence control unit as

one integral unit. In addition, the memory unit 16 is reproduced in FIG. 4 to facilitate understanding the operation of the sequence control unit. As noted hereinbefore, the division into functional blocks in FIG. 1 is arbitrary, and for purposes of description only.

From the foregoing it will be appreciated that a programmed sequencing format entails a number of minor frames making up a major frame. When the last of a group sampled at the lowest rate has been completed, the major frame is complete, and the next minor frame starts a new major frame. A START command signal initiates the first minor frame of a major frame, and the major frame is completed again and again, until an EXIT command resets the flip-flop 33 (FIG. 3).

The step signal generator shown in FIG. 3 cycles once for each sample or digital data source selected. The selection is made by an address register 41 which receives data identification word (DATAID/LP). The location in memory from which this register is loaded is determined by the control word (CTLADR/CT) in a control address register 42. Four additional registers are required to complete sequence control of minor and major frames. A frame count register 43 is provided to keep track of which minor frame is in progress, and a three-bit present index register 44 is provided to point to the location in memory from which the control address register will be loaded with a control word that determines the memory location from which the address register 41 is loaded for the next selection. A three-bit new index register 45 points to the memory location for the next control word to make the next selection after taking the allotted number of samples at the present rate, i.e. to provide transition in the minor frame between sequences at different rates. A transfer delay counter and decoder 46 is also provided in the manner to be described next.

There will be a number (1 to 63) of samples programmed for each rate. For the maximum rate R, the complement of that number is loaded into the transfer delay counter and decoder 46 from the memory location 010 uniquely associated with the rate R. The function of the transfer delay counter and decoder 46 is to determine how many samples will be taken at a given rate in a minor cycle. If X samples are to be taken, the number 63-X is stored, and the decoder portion simply determines when X samples have been taken by detecting when a count of 63 has been reached. Until then the detector output DLY is false, i.e. equal to 0. Thus, the transfer delay counter must be loaded from memory once for each rate contained in each minor frame. The three bits in the present index register along with the signal S₃, determines the location from which the transfer delay counter will be loaded. Thus the present index register will specify a location from 000 to 007 and the signal S₃ will effectively add 8 to change the address to one from 010 to 017.

The frame counter register 43 is incremented at the end of every minor frame. To accomplish that, the control word stored in the address register 42 includes a flag bit (CT) which is used to increment the frame count register, as noted hereinbefore. Accordingly, the flag bit in every control word in memory pointing to the address of a sample at the rate included last in a minor frame is set equal to 1, and in all other control words, equal to 0.

Once all of the samples programmed at a given rate in a minor frame have been sampled, there must be some way of returning to the control word which points to the memory location containing the address of first sample to be taken again during the next minor frame. A frame return decoder 47 accomplishes that by comparing the number in the frame count register with the contents of the present index register which not only points to the location in memory from which the control address register is to be loaded next but also is associated with the rate of the group to be sampled next. For example, since the samples at a given rate R/2ⁿ repeat themselves every 2ⁿ minor frames, and since the present index register is loaded with the number n for the current rate groups of samples, when the frame count register reaches the minor frame count

of 2ⁿ for that rate group, the frame return decoder 47 transmits a signal FRF. The control address register will then be loaded from the same memory location as it was during the first minor frame, i.e., from an initial condition location in the block 020 to 027. Which of the eight locations depends upon the content of the present index register which will be an octal digit from 0 to 7 for the respective memory locations from 020 to 027. An advantage of this arrangement is that the programmable access telemetry system will automatically recycle to an initial condition so that any transient which may cause an error sequencing through any given rate groups will not be carried forward indefinitely.

The control word in the address register 42 is incremented after each sample and then stored in a scratch pad memory in order that it point to the memory location of the data identification word (DATAID/LP) for the sensor or digital data source to be sampled in the same rate group. Incrementing is automatic unless the data identification word has a bit 1 in a flag position (LP) as noted hereinbefore. Therefore, is LP=1 for a given data source, the system will return to the same memory location in the block from 030 to 377 each time the corresponding control word is called out for the particular rate group until the frame return signal FRF occurs. That allows successive multiple sampling from a single source. Each time the memory 16 is addressed, a memory addressing unit 16b is controlled by the address from the appropriate register by sequence control signals S₂, S₃, S₄ and S₆, either directly or conditionally through gates.

It should be clearly understood that each channel of each minor frame requires one 7-step cycle of the waveforms shown in FIG. 2 and generated as described with reference to FIG. 3. Therefore an understanding of that cycle will aid in understanding the system of FIG. 4. To facilitate that, the flow chart shown in FIG. 6 will be described in conjunction with a further description of FIG. 4.

As noted hereinbefore a START command signal initiates the first cycle for the first minor frame. The cycle repeats automatically until an EXIT command is received. The START command resets the new index register 45, resets the frame count register 43 and sets the transfer delay counter and decoder to the count of 63. It also sets the flip-flop 33 (FIG. 3). The first step then transfers the contents of the new index register 45 (which is not octal 0) to the present index register 44 to point to the memory location for the control word to be used in addressing the first rate group of channels in sequence. The control for that is through a gate 60 enabled by the sequencing signal S₁. A signal DLY from the transfer delay counter and decoder 46 will be true at this time (because it has just been set to 63 to make it possible).

In step 2, the first control word is transferred from the memory location specified by the present index register (which is now octal 0) plus 16 (which is equal to 020). The frame return flag FRF from the decoder 47 (now equal to 1 because both registers 43 and 44 are at 0) signifies that an initial condition location is to be used and not a memory scratch pad location. Gate 61 provides timing control during this operation and gate 62 provides the "plus 16" control. In step 3, the transfer delay counter and new index register are loaded from a memory location 010 specified by the number in the present index register (which is still octal 0) and the timing signal S₃. That is done by applying the signal S₃ to the memory addressing unit to combine a binary 1 with the three binary 0's in the present index register to obtain the octal code 010. The new index is a field of three bits of a nine-bit word read from the memory location 010. The balance of the nine-bit word go to the delay counter. A gate 63 provides timing control for this operation. That completes preparation for the first cycle with "initial conditions" taken from memory locations 010 and 020. For subsequent cycles which start a new rate group, operation of the sequence control unit is much the same as will be presently understood.

In step 4, the selection address register 41 is loaded from memory with the address of the sensor or data source to be

sampled as specified by the control word in the register 42. To accomplish that, the timing signal S₄ is applied to that register and the memory addressing unit.

The first sample is taken during step 5. Preparations are also made during step 5 for sampling the next channel by incrementing the transfer delay counter if the count of 63 has not been reached, i.e. if DLY=0, and by incrementing the control address register 42 to point to the next memory location in sequence containing the address of the sensor or digital data source to be sampled next, but only if the flag LP of the data identification code (DATAID/LP) in the address register for the current channel is zero. Thus, as noted hereinbefore, by programming a flag LP=1 in a data identification code, the system can be caused to sample the same channel repeatedly until a frame return signal FRF occurs. This allows multiple sampling from a single memory location as shown in the format of FIG. 5, thus conserving memory locations used for the format. A timing signal S₅ applied to gates 64 and 65 will respond to the signal S₅ to control these operations while the signal S₅ controls the sampling process directly, as described hereinbefore with reference to FIG. 1. Thus, if LP is 0, the control word in the register 42 is incremented to fetch from memory the next data identification code of the first rate group, and if DLY=0 the counter 46 is incremented to keep track of the number of channels sampled in sequence.

As long as DLY remains equal to zero, no operation will take place in the sixth and seventh steps of the current sequence control cycle, and no operation will take place in the first three steps of the next cycle either. In the fourth step, the selection address register 41 is loaded from the memory location specified by the contents (control word) of the register 42. The fifth step is then executed as before, and the process is repeated until the programmed number of samples at the first rate R have been taken in sequence, at which time the signal DLY becomes true (DLY=1).

In the sixth step the control word (CTLADR/CT) is stored in the scratch pad memory location 000 associated with the first rate group R, as specified by the present index register which is still at 0. The frame count register 43 is not incremented at this time, nor during subsequent rate group cycles, until the last, because the control words for the first rate group and the subsequent rate groups prior to the last rate group are not provided with a flag (CT=1).

Referring to FIG. 5, frame count register would be incremented only when the control word for the last rate group (rate R/64) is loaded into the register 42. Initially that control word has the address for the memory location of the data identification code for channel 40, and the flag bit CT. Thereafter, that control word is incremented in step 5 and stored in the scratch pad memory location specified by the present index register during step 6. The step signal S₆ provides control for these operations through gates 66, 67 and 68. The gate 68 is enabled only when DLY is true, i.e. not equal to 0, which is when the desired number of samples have been processed out of the rate group in progress. Accordingly, that output controls the operation of storing CTLADR/CT in the scratch pad memory location specified by the present index register.

Each subsequent rate group is processed in the same manner. During step 1, the contents of the new index register (loaded during step 3 of the first cycle for the last rate group) are transferred to the present index register to be used to load the control word for the ensuing rate group in the register 42 during step 2, and the load the delay counter and new index register during step 3. The latter is loaded with the octal number of the next rate group. Thus during the first rate group, the new index register is stored with the octal code 3 for the next rate group R/8. In the exemplary format of FIG. 5, there are 32 channels to be sampled at the same rate R/8. That is accomplished by programming a count of four (specifically 63-4) to be loaded into the delay counter. In that manner, the next four channels 230, 220, 210 and 200 are sampled in sequence during the first minor frames.

During subsequent minor frames, successive subgroups of 4 are sampled until eight minor frames have been completed. That is detected by the frame return decoder, which, in response to the octal 3 code in the present index register, causes binary 0's in the three least significant bit positions of the frame count register to be detected. The frame count register is, of course, incremented by only the programmed flag CT in the control word of the last rate group R/64.

It should be noted that for the rate group R/8 of 32 channels, the data identification codes 230, 220 . . . 231, 221 . . . 239, 229 . . . 207 are stored in successive memory locations in the block from 030 to 377 in order for one control word (CTLADR/CT) to be used for all 32 channels. It should also be noted that although all possible rate groups need not be included in a minor frame, any one rate group can be included only once. Therefore, all channels to be sampled at the same rate must be grouped together using subgroups as just illustrated for 32 channels at the rate R/8.

Storing the control word from the register 42 in a memory location of the scratch pad memory specified by the rate group code in the present index register in step 6 will allow the next minor frame to proceed with the next channel of the same rate group in sequence during the next minor frame. No operation takes place during step 7. The period for that step is provided in the sequence control unit cycle to allow for the last bit of a seven bit number to be serially transferred into the real time data buffer 18 or the data processing and monitoring unit, whichever is specified by operation-code bits read into the register 41 as part of the data identification code. The operation-code bits are applied to the data buffer 18 and the monitoring unit 19 to control operation of those units for the data then being sampled. It should be noted that if additional time is required, such as for data processing, before another sample is taken in sequence, the sequence control unit cycle can be extended to include additional idle steps following step 7 before recycling to step 1.

If an EXIT command has not been received by step 7, i.e. EXIT=0 before step 1 of any cycle, the 7-step cycle will be repeated starting with step 1; otherwise, the operation of the sequence control unit is terminated until another START command is received at which time the system will automatically go to a fixed program sequence to load the memory from the GP computer.

The frame return decoder first decodes the rate group number in the present index ($P_2 P_1 P_0$) register as 0, 1 . . . 7 for the rate groups R, R/2 . . . R/128 to generate signals $X_0, X_1, \dots, X_7$, respectively, and then decodes the frame count register bits C_0 to C_6 to generate the FRF signal as follows:

$$FRF = DLY[X_0 + X_1 \bar{C}_0 + X_2 \bar{C}_0 \bar{C}_1 + X_3 \bar{C}_0 \bar{C}_1 \bar{C}_2 + X_4 \bar{C}_0 \bar{C}_1 \bar{C}_2 \bar{C}_3 \dots Q + X_7 \bar{C}_0 \bar{C}_1 \bar{C}_2 \bar{C}_3 \bar{C}_4 \bar{C}_5 \bar{C}_6]$$

In that manner, the operation specified in steps 2 will use either "initial condition" memory locations 020 to 027 for control words, or the scratch pad memory locations 000 to 007 according to the following logic equations:

$$INITIAL\ CONDITION = (S_2 DLY FRF) S_3 P_2 P_1 P_0 (S_2 DLY FRF) \bar{S}_3 P_2 P_1 P_0$$

Following that, in step 3, the delay counter and present index register are loaded from the respective memory locations specified by the control logic $(\bar{S}_2 DLY FRF) S_3 P_2 P_1 P_0$. Thus, finally on step 6, the contents of the control address register is stored in scratch pad memory at a location specified by the present index register and control logic $(\bar{S}_2 DLY FRF) \bar{S}_3 P_2 P_1 P_0$. The next rate group is then introduced and the delay counter 46 is loaded with an appropriate number which will cause DLY to be equal to 1 when it has been incremented the required number of times. All subsequent rate groups are similarly introduced until the last rate group is introduced. The control word for that last rate group includes a bit CT which causes the frame count register 43 to be incremented. As a transition is made from one rate group to another during each minor frame, the scratch pad location is used to store the control word for the next sample of the one rate group.

Although particular embodiments of the invention have been described and illustrated herein, it is recognized that modifications and variations may readily occur to those skilled in the art. For example, to permit indirect addressing of data source identification words in the memory locations 030 to 377, the LP flag may be expanded to include a second binary digit. The binary code 00 would permit the control word CTLADR in the register 42 to be incremented as before, and the binary code 01 would inhibit the control word from being incremented. The code 11 would then be used to both inhibit the control word from being incremented and to cause the content of the selection address register to be transferred to the control address register, and the code 11 would also inhibit selection of a data source, all during step 5. The stored word DATAID/LP having LP=11 is then not a data source identification but simply a word having a control word filed (CTLADR) to be substituted for the present on in the register 42. Thus, at the expense of just one sequencing unit cycle, the format can be programmed to jump from one memory location to any other memory location for the data source identification word of the next sample. This indirect addressing possibility can be used to facilitate altering an existing format in memory without rewriting or rearranging the entire format.

Another example of a useful modification is an expansion of the rate group identification code to four or more bits in order to have more than seven rate groups, each with one associated memory location from each of three blocks of memory as before. A variant would be to use additional bits to specify second groups of the same rates. For instance, assuming a four bit code, the three least significant bits can be used for seven distinct rate groups as before with a bit zero in the fourth bit position, and for seven alternate rate groups of the same rates as the seven distinct rate groups with a bit one in the fourth bit position. In that manner, a given rate group can be included in the format twice, each time for a different set of sensors and data sources.

Still other modifications and variations will occur to those skilled in the art. Consequently, it is intended that the claims be interpreted to cover such modifications and variations.

What is claimed is:

1. A programmable telemetry system comprising
 - a memory unit having a plurality of randomly accessible memory locations for storing digital signals representing control words for sampling predetermined sources of data at different rates in a desired format, digital signals representing identification codes of said data sources, and digital signals representing the number of data sources to be sampled in sequence at a given rate,
 - a first register coupled to said memory unit for receiving data identification code words in rate groups from predetermined memory locations, all groups except one consisting of a plurality of data sources to be sampled at a desired rate, $R/2^n$ where n is a positive integer, relative to said one group which is to be sampled cyclically at a rate R, each group being stored in a unique block of memory locations,
 - a second register coupled to said memory unit for receiving control words in a predetermined order, each control word specifying the memory location of the first data identification code word of a unique rate group,
 - a delay counter coupled to said memory unit for receiving digital signals representing a delay word in the form of a number specifying the number of data sources of a given rate group to be sampled in sequence during one minor frame cycle, where a minor frame is defined as the interval between samples of a given data source occurring once in the highest rate group, and for counting the number of successive samples taken from a given rate group, and
 - sequence control means for loading control words into said second register one at a time from a predetermined block of memory locations, for loading delay words into said counter, one delay word for each control word from a

predetermined group of memory locations, for loading data identification control words into said first register from memory locations specified by the control word in said second register, each time incrementing both said control word in said second register and said delay word in said delay counter, for storing each incremented control word within another predetermined block at a memory location uniquely associated with the rate group controlled by the incremented control word being stored when the number of samples specified by said delay word have been taken, and for loading a given control word into said second register from either said predetermined block of memory locations reserved for unincremented control words or from said block reserved for incremented control words depending upon whether all of the samples from the rate groups controlled have just been completed during the previous minor frame cycle.

2. The combination defined by claim 1 wherein each unincremented control word loaded into said second register includes a flag indicating whether or not the rate group controlled thereby is the last rate group of a minor frame cycle, and said flag is stored with each incremented control word in said memory location uniquely associated with the rate group, each rate group $R/2^n$ is identified by the number n representing the exponent of 2 by which the highest rate is divided to determine its group rate, and said sequence control unit includes

a third register,

means for loading into said third register said number n associated with the rate group being controlled by the control word in said second register,

frame counting means for counting in binary form the number of times said flag, loaded into said second register with a control word, indicates that the rate group controlled thereby is the last of a minor frame,

means responsive to said number n in said third register for generating a frame return flag when the n least significant binary digits are each equal to zero, and

means responsive to said frame return flag for causing the control word for a given group to be loaded from a memory location reserved for an unincremented control word for the group of the group rate associated with the number n , and for causing an unincremented control word for the group of the highest group rate R to always be loaded from a memory location reserved for an unincremented control word.

3. The combination defined by claim 2 wherein which of said predetermined group of memory locations for unincremented control words is, in each instance, selected from a group of n memory locations, where the addresses for the locations in the two groups is comprised in the least significant parts of the numbers 0 to n , such that memory locations 0 to n are reserved for the respective rate groups R , $R/2^1$, ..., $R/2^n$.

4. The combination defined by claim 3 wherein each delay word for a given rate group is read from a memory location in a unique block of n memory locations, each location of said block is identified by the number n in the least significant portion of its address, and the number n identifying the rate group to be sampled next is read from the same memory location as said delay word for the current rate group to be sampled, and at the same time, including

a fourth register into which said number n is read while said delay word is being entered into said delay counter, and means for transferring the content of said fourth register to said third register when said delay counter has counted a number of samples specified by said delay word.

5. The combination defined by claim 4 including

a source of system clock pulses,

a cyclic timing means connected to said source of clock pulses and responsive thereto for generating a cyclical sequence of step control signals, and

wherein said sequence control means responds to said step control signals to transfer the content of said fourth re-

gister to said third register during the first step, to load said second register from a memory location specified by the content of said third register and said frame return flag during the second step, to load said delay counter and said fourth register from a memory location specified by said third register during the third step, to load said first register from a memory location specified by said second register during the fourth step, to increment said delay counter if the delay count is not complete, to increment said second register and select the data source specified by said first register during said fifth step, and, if, during the sixth step the number of samples specified by said delay count has been taken, to increment said frame counting means if said flag loaded into said second register with a control word during the second step indicates that the rate group controlled thereby is the last of a minor frame, and to store the incremented control word in a memory location specified by said third register; otherwise, if the number of samples has not been taken, to recycle to the fourth step from the fifth step.

6. The combination defined by claim 5 wherein said sequence control means recycles to the fourth step from the fifth step through idle sixth, first, second and third steps in order to allow the same amount of time for processing each sample.

7. The combination defined by claim 6 wherein there is at least one additional idle step following each sixth step to allow sufficient time for processing of sampled data.

8. The combination defined by claim 7 wherein each data identification code includes a repeat flag code which, when set to a predetermined value, indicates that the sample specified be taken repeatedly during successive sequencing cycles until the number of samples specified by said delay word for a given rate group has been taken, and wherein the step of incrementing said second register is conditioned on said repeat flag code of a given data identification code not being set to said predetermined value.

9. The combination defined by claim 1 wherein each data identification code word includes a flag code which, when at a predetermined value, indicates the same data identification code word is to be used again, and said sequence control means includes means for inhibiting said control word in said second register from being incremented, whereby the same data identification code word is used for successive samples until the number of samples specified by said delay word has been taken.

10. A programmable telemetry system comprising

a memory unit having a plurality of randomly accessible memory locations for storing digital signals representing control words for sampling predetermined sources of data at different rates in a desired format, digital signals representing identification codes of said data sources, and digital signals representing the number of data sources to be sampled in sequence at a given rate,

a first register coupled to said memory unit for receiving data identification code words in rate groups from predetermined memory locations, all groups except one consisting of plurality of data sources to be sampled at a desired rate, $R/2^n$ where n is a positive integer, relative to said one group which is to be sampled cyclically at a rate R , each group being stored in a unique block of memory locations,

a second register coupled to said memory unit for receiving control words in a predetermined order, each control word specifying the memory location of the first data identification code word of a unique rate group, and

sequence control means for loading a control words into said second register from a predetermined block of memory locations, loading data identification control words into said first register from memory locations specified by the control word in said second register, each time incrementing said control word in said second register, storing each incremented control word within

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another predetermined block at a memory location uniquely associated with the rate group controlled by the incremented control word being stored and loading a given control word into said second register from either said predetermined block of memory locations reserved for unincremented control words or from said block reserved for incremented control words depending upon whether all of the samples from the rate groups have just been completed during the previous minor frame cycle, where a minor frame is defined as the interval between samples of a given data source occurring once in the highest rate group.

11. The combination defined in claim 10 wherein each unincremented control word loaded into said second register includes a flag indicating whether or not the rate group controlled thereby is the last rate group of a minor frame cycle, and said flag is stored with each incremented control word in said memory location uniquely associated with the rate group, each rate group $R/2^n$ is identified by the number n representing the exponent of 2 by which the highest rate is divided to determine its group rate, and said sequence control unit includes

a third register,
means for loading into said third register said number n associated with the rate group being controlled by the con-

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trol word in said second register,
frame counting means for counting in binary form the number of times said flag, loaded into said second register with a control word, indicates that the rate group controlled thereby is the last of a minor frame,
means responsive to said number n in said third register for generating a frame return flag when the n least significant binary digits are each equal to zero, and
means responsive to said frame return flag for causing the control word for a given group to be loaded from a memory location reserved for an unincremented control word for the group of the group rate associated with the number n , and for causing an unincremented control word for the group of the highest group rate R to always be loaded from a memory location reserved for an unincremented control word.

12. The combination defined in claim 11 wherein which of said predetermined group of memory locations for unincremented control words is, in each instance, selected from a group of n memory locations, where the addresses for the locations in the two groups is comprised in the least significant parts of the numbers 0 to n , such that memory locations 0 to n are reserved for the respective rate groups $R, R/2^1, \dots, R/2^n$.

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