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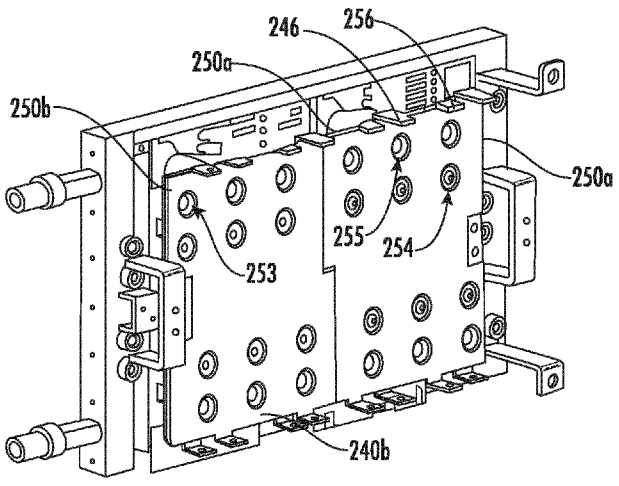


FIG. 5

(57) Abstract: A bus assembly includes a planar first bus, a second bus including a first planar bus section on the first bus and a second planar bus section connected to the first planar bus section and offset from the first planar bus section, and a third bus comprising a third planar bus section disposed between the first bus and the second planar bus section, and a fourth planar bus section connected to the third planar bus section, offset from third planar bus section, and disposed on the first planar bus section.

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[Continued on next page]

TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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LOW-IMPEDANCE BUS ASSEMBLIES AND APPARATUS INCLUDING THE SAME

BACKGROUND

[0001] The inventive subject matter relates to electrical power apparatus and methods and, more particularly, to bus assemblies for use with semiconductor switching devices.

[0002] Power electronics apparatus, such as power converters, solid-state circuit breakers and the like, may employ power transistors or other power semiconductor switching devices. Development of semiconductor technology has led to power semiconductor switching devices having dramatically increased voltage and switching frequency capabilities. For example, silicon carbide (SiC) transistors (e.g., SiC MOSFETs) have been developed capable of operating at frequencies that are multiples of operating frequencies of corresponding conventional silicon-based power devices (e.g., silicon IGBTs).

[0003] With the advent of such devices, impedance effects associated with conductive buses and other circuit components used with these devices have increased in significance. In particular, inductance and capacitance associated with such components may degrade system performance by introducing oscillation and other negative effects.

SUMMARY

[0004] Some embodiments of the inventive subject matter provide a bus assembly including a planar first bus, a second bus including a first planar bus section on the first bus and a second planar bus section connected to the first planar bus section and offset from the first planar bus section, and a third bus comprising a third planar bus section disposed between the first bus and the second planar bus section, and a fourth planar bus section connected to the third planar bus section, offset from third planar bus section, and disposed on the first planar bus section. In some embodiments, the second bus has a first slot between the first and second planar bus sections and an adjacent first connecting portion that connects the first and second planar bus sections and the third bus has a second slot between the third and fourth planar bus sections and an adjacent second connecting portion that connects the third and fourth planar bus sections. The first connecting portion may pass through the second slot and the second connecting portion may pass through the first slot. The first slot, the second slot, the first connecting portions and the second connecting portion may be aligned with a line bisecting the first bus.

[0005] In some embodiments, the first planar bus section and the second planar bus section may include respective conductive plates oriented in respective offset parallel planes, and the third planar bus section and the fourth planar bus section may include respective conductive plates oriented in respective offset parallel planes.

[0006] In further embodiments, the first bus may be configured to be disposed on a planar array of transistor packages and to electrically interconnect first terminals of the transistor packages and may have clearance holes that coincide with second terminals of the transistor packages. The first planar bus section may be configured to electrically interconnect the second terminals of a first group of the transistor packages and may have clearance holes that coincide with the first terminals of the first group of transistor packages. The second planar bus section may have clearance holes that coincide with first and second terminals of a second group of the transistor packages. The third planar bus section may have clearance holes that coincide with the first and second terminals of the first group of transistor packages. The fourth planar bus section may be configured to electrically interconnect the second terminals of the second group of transistor packages and may have clearance holes that coincide with the first terminals of the second group of transistor packages.

[0007] In further embodiments, the bus assembly may include connection tabs extending perpendicularly from edges of the first, second, third and fourth planar bus sections. First connection tabs extending from a first edge of the first planar bus assembly may be offset with respect to second connection tabs extending from a first edge of the fourth planar bus section aligned with the first edge of the first planar bus section. Third connection tabs extending from a first edge of the second planar bus section may be offset with respect to fourth connection tabs extending from a first edge of the third planar bus section aligned with the first edge of the second planar bus section.

[0008] Some embodiments provide an apparatus including a planar array of semiconductor device packages and a planar first bus disposed on the array of semiconductor device packages, electrically interconnecting first terminals of the semiconductor device packages, and having clearance holes that coincide with second terminals of the semiconductor device packages. The apparatus also includes a second bus comprising a first planar bus section on the first bus, electrically interconnecting the second terminals of a first group of the semiconductor device packages, and having clearance holes that coincide with the first terminals of the first group of

semiconductor device packages and a second planar bus section electrically connected to the first planar bus section, offset from the first planar bus section, and having clearance holes that coincide with first and second terminals of a second group of the semiconductor device packages. The apparatus further includes a third bus including a third planar bus section disposed between the first bus and the second planar bus section and having clearance holes that coincide with the first and second terminals of the first group of semiconductor device packages and a fourth planar bus section electrically connected to the third planar bus section, disposed on the first planar bus section, electrically interconnecting the second terminals of the second group of semiconductor device packages, and having clearance holes that coincide with the first terminals of the second group of semiconductor device packages.

[0009] In some embodiments, each of the semiconductor device packages may include three transistors, three first terminals and three second terminals. In some embodiments, each of the semiconductor device packages may include at least one insulated gate bipolar transistor (IGBT). The first terminals may include emitter terminals and the second terminals may include collector terminals.

[0010] The apparatus may further include a cooling plate on which the semiconductor device packages are mounted.

[0011] The apparatus may also include connection tabs extending perpendicularly from the first, second, third and fourth planar bus sections. At least one metal oxide varistor (MOV) may be disposed on the first, second and third buses and connected between ones of the connection tabs connected to the second terminals of the first group of semiconductor device packages and ones of the second terminals of the second group of semiconductor device packages.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIG. 1 is a schematic diagram of a power module according to some embodiments.

[0013] FIGs. 2- 7 are views of components of a power module according to some embodiments.

[0014] FIGs. 8-10 are views of a bus assembly for a power module according to some embodiments.

[0015] FIGs. 11-15 are isolated views of component bus bars of the bus assembly of FIGs. 8-10.

[0016] FIG. 16 is a perspective view illustrating MOV connections for the power module of FIGs. 2-7.

DETAILED DESCRIPTION

[0017] Specific exemplary embodiments of the inventive subject matter now will be described with reference to the accompanying drawings. This inventive subject matter may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the inventive subject matter to those skilled in the art. In the drawings, like numbers refer to like items. It will be understood that when an item is referred to as being "connected" or "coupled" to another item, it can be directly connected or coupled to the other item or intervening items may be present. As used herein the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0018] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the inventive subject matter. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless expressly stated otherwise. It will be further understood that the terms "includes," "comprises," "including" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, items, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, items, components, and/or groups thereof.

[0019] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this inventive subject matter belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the specification and the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0020] FIG. 1 is a circuit diagram for a power module according to some embodiments. The module includes two groups 110a, 110b of parallel-connected insulated gate bipolar transistors (IGBTs) connected in series. A group 120 of parallel-connected metal oxide varistors (MOVs)

are connected in parallel with the series-connected groups 110a, 110b of IGBTS. Side, perspective, and top views of such a module 200 are provided in FIGs. 6-9. FIGs. 2-5 show components of a bus assembly for such a module.

[0021] Referring to FIG. 2, the module includes multiple IGBT packages 220 mounted in a planar array on a cold plate 210. Each of the IGBT packages 220 includes three IGBTs and has three emitter terminals 222 and three collector terminals 224. As illustrated, the IGBT packages 220 are arranged such that the uppermost IGBT packages 220 have their emitter terminals 22 above their collector terminals 224 and the lowermost IGBT packages 220 have their emitter terminals 222 below their collector terminals 224. Referring to FIG. 3, an emitter bus bar 230 electrically connects the emitter terminals 222 of the IGBT packages 220 to one another, providing the connectivity indicated by the circled region of the schematic shown in FIG. 1. The emitter bus bar 230 is generally planar and has clearance holes 232 therein that expose the collector terminals 224 of the underlying IGBT packages 220.

[0022] Referring to FIG. 4, a first collector bus bar 240 overlies the emitter bus bar 230. The first collector bus bar 240 includes first and second planar portions 240a, 240b that are on different planes. A cleft or slot 242 partially separates the first and second portions 240a, 240b, which remain connected by a connecting step portion 243. The first portion 240a interconnects the collector terminals 224 of the rightmost two IGBT packages 220 and has clearance holes 241 therein that coincide with the underlying connections of the first bus bar 230 to the emitter terminals 222 of the IGBT packages 220. The second portion 240b of the first collector bus bar 240 has first clearance holes 244 that coincide with the collector terminals 224 of the leftmost two IGBT packages 220, and second clearance holes 245 that coincide with the connections of the emitter bus bar 230 to the emitter terminals 222 of the leftmost two IGBT packages 220. The first collector bus bar 240 further includes tab-like connection terminals 246 that extend perpendicularly from the first and second planar portions 240a, 240b and facilitate connection of the first collector bus bar 240 to MOVs, as described below with reference to FIGs. 6 and 7.

[0023] Referring to FIG. 5, a second collector bus bar 250 is interleaved with the first collector bus bar 240. The second collector bus bar 250 has a first portion 250a that overlaps the first portion 240a of the first collector bus bar 240 and a second portion 250b that is overlapped by the second portion 240b of the first collector bus bar 240. As illustrated, the second collector bus bar 250 is identical to the first collector bus bar 240 but is rotated 180 degrees with respect to

the first collector bus bar 240 such that the first and second collector bus bars 240, 250 may be interleaved. The first portion 250a of the second collector bus bar 250 has first clearance holes 254 that coincide with the collector terminal connections to the first portion 240a of the first collector bus bar 240, and second clearance holes 255 that coincide with the emitter terminal connections of the right-side IGBT packages 220 to the emitter bus bar 230. The second portion 250b of the second collector bus bar 250 interconnects the collector terminals 224 of left-side IGBT packages 220 and has clearance holes 253 that coincide with the connections of the emitter bus 230 to the emitter terminals 222 of the left-side IGBT packages 220. The second collector bus bar 250 further includes tab-like connection terminals 256 that extend perpendicularly from the first and second portions 250a, 250b and facilitate connection of MOVs to the second collector bus bar 250, as described below with reference to FIGs. 6 and 7.

[0024] FIGs. 6 and 7 provide side views of an assembled module 200, including the structures described above with reference to FIGs. 2-5, along with MOVs 260 attached to the terminals 246, 256 of the first and second collector bus bars 240, 250. FIG. 16 is a detailed perspective view of the MOV connections. As illustrated, the emitter bus bar 230 and the first and second collector bus bars 240, 250 may be coated with an insulating material to prevent shorting between the bus bars 230, 240, 250. In some embodiments, insulating material layers may be provided between the bus bars 230, 240, 250 to provide similar insulating effects.

[0025] It will be understood that FIGs. 1-8 illustrate a configuration that can be used for a bidirectional module, and that some embodiments may be implemented as a unidirectional embodiment wherein one of IGBT packages (e.g., IGBT package 110b) could be removed, with the MOVs being connected in parallel with the remaining IGBT package (e.g., IGBT package 110a). It will also be understood that other types of IGBT packages could be used.

[0026] FIGs. 8-10 are isolated views of the bus bar assembly, illustrating relationships among the emitter bus bar 230 and the collector bus bars 240, 250. FIGs. 11 and 12 are isolated views of the emitter bus bar 230, illustrating that the emitter bus bar 230 may be generally planar. FIGs. 13-15 are isolated views of the first collector bus bar 240, illustrating the cleft 242 and step portion 243 that facilitate interleaving with the second collector bus bar 250 as described above. It will be understood that the second collector bus bar 250 may be identical to the first collector bus bar 240.

[0027] The drawings and specification, there have been disclosed exemplary embodiments of the inventive subject matter. Although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the inventive subject matter being defined by the following claims.

THAT WHICH IS CLAIMED:

1. A bus assembly comprising:

a planar first bus;

a second bus comprising:

a first planar bus section on the first bus; and

a second planar bus section connected to the first planar bus section and offset from the first planar bus section;

a third bus comprising:

a third planar bus section disposed between the first bus and the second planar bus section; and

a fourth planar bus section connected to the third planar bus section, offset from third planar bus section, and disposed on the first planar bus section.

2. The bus assembly of claim 1, wherein the second bus has a first slot between the first and second planar bus sections and an adjacent first connecting portion that connects the first and second planar bus sections, wherein the third bus has a second slot between the third and fourth planar bus sections and an adjacent second connecting portion that connects the third and fourth planar bus sections, wherein the first connecting portion passes through the second slot and wherein the second connecting portion passes through the first slot.

3. The bus assembly of claim 2, wherein the first slot, the second slot, the first connecting portions and the second connecting portion are aligned with a line bisecting the first bus.

4. The bus assembly of claim 2, wherein the first planar bus section and the second planar bus section comprise respective conductive plates oriented in respective offset parallel planes, and wherein the third planar bus section and the fourth planar bus section comprise respective conductive plates oriented in respective offset parallel planes.

5. The bus assembly of claim 1:

wherein the first bus is configured to be disposed on a planar array of transistor packages and to electrically interconnect first terminals of the transistor packages and has clearance holes that coincide with second terminals of the transistor packages;

wherein the first planar bus section is configured to electrically interconnect the second terminals of a first group of the transistor packages and has clearance holes that coincide with the first terminals of the first group of transistor packages;

wherein the second planar bus section has clearance holes that coincide with first and second terminals of a second group of the transistor packages;

wherein the third planar bus section has clearance holes that coincide with the first and second terminals of the first group of transistor packages; and

wherein the fourth planar bus section is configured to electrically interconnect the second terminals of the second group of transistor packages and has clearance holes that coincide with the first terminals of the second group of transistor packages.

6. The bus assembly of claim 1, further comprising connection tabs extending perpendicularly from edges of the first, second, third and fourth planar bus sections.

7. The bus assembly of claim 6, wherein first connection tabs extending from a first edge of the first planar bus assembly are offset with respect to second connection tabs extending from a first edge of the fourth planar bus section aligned with the first edge of the first planar bus section and wherein third connection tabs extending from a first edge of the second planar bus section are offset with respect to fourth connection tabs extending from a first edge of the third planar bus section aligned with the first edge of the second planar bus section.

8. An apparatus comprising:

a planar array of semiconductor device packages;

a planar first bus disposed on the array of semiconductor device packages, electrically interconnecting first terminals of the semiconductor device packages, and having clearance holes that coincide with second terminals of the semiconductor device packages;

a second bus comprising:

a first planar bus section on the first bus, electrically interconnecting the second terminals of a first group of the semiconductor device packages, and having clearance holes that coincide with the first terminals of the first group of semiconductor device packages; and

a second planar bus section electrically connected to the first planar bus section, offset from the first planar bus section, and having clearance holes that coincide with first and second terminals of a second group of the semiconductor device packages; and

a third bus comprising:

a third planar bus section disposed between the first bus and the second planar bus section and having clearance holes that coincide with the first and second terminals of the first group of semiconductor device packages; and

a fourth planar bus section electrically connected to the third planar bus section, disposed on the first planar bus section, electrically interconnecting the second terminals of the second group of semiconductor device packages, and having clearance holes that coincide with the first terminals of the second group of semiconductor device packages.

9. The apparatus of claim 8, wherein the second bus has a first slot between the first and second planar bus sections and an adjacent first connecting portion that connects the first and second planar bus sections, wherein the third bus has a second slot between the third and fourth planar bus sections and an adjacent second connecting portion that connects the third and fourth planar bus sections, wherein the first connecting portion passes through the second slot and wherein the second connecting portion passes through the first slot.

10. The apparatus of claim 9, wherein the first slot, the second slot, the first connecting portions and the second connecting portion are aligned with a line bisecting the first bus.

11. The apparatus of claim 9, wherein the first planar bus section and the second planar bus section comprise respective conductive plates oriented in respective offset parallel planes, and wherein the third planar bus section and the fourth planar bus section comprise respective conductive plates oriented in respective offset parallel planes.

12. The apparatus of claim 8, wherein each of the semiconductor device packages comprises three transistors, three first terminals and three second terminals.

13. The apparatus of claim 8, wherein each of the semiconductor device packages comprises at least one insulated gate bipolar transistor (IGBT), wherein the first terminals comprise emitter terminals and wherein the second terminals comprise collector terminals.

14. The apparatus of claim 13, wherein each of the semiconductor device packages comprises three IGBTs, three emitter terminals, and three collector terminals.

15. The apparatus of claim 8, further comprising a cooling plate, and wherein the semiconductor device packages re mounted on the cooling plate.

16. The apparatus of claim 15, wherein first sides of the semiconductor device packages face the cooling plate and wherein second sides of the semiconductor device packages face the first bus.

17. The apparatus of claim 8, further comprising connection tabs extending perpendicularly from the first, second, third and fourth planar bus sections.

18. The apparatus of claim 17, further comprising at least one metal oxide varistor (MOV) disposed on the first, second and third buses and connected between ones of the connection tabs connected to the second terminals of the first group of semiconductor device packages and ones of the second terminals of the second group of semiconductor device packages.

19. The apparatus of claim 8, further comprising a plurality of metal oxide varistors (MOVs) disposed on the first, second and third buses and electrically connected between the second terminals of the first group of semiconductor device packages and the second terminals of the second group of semiconductor device packages.

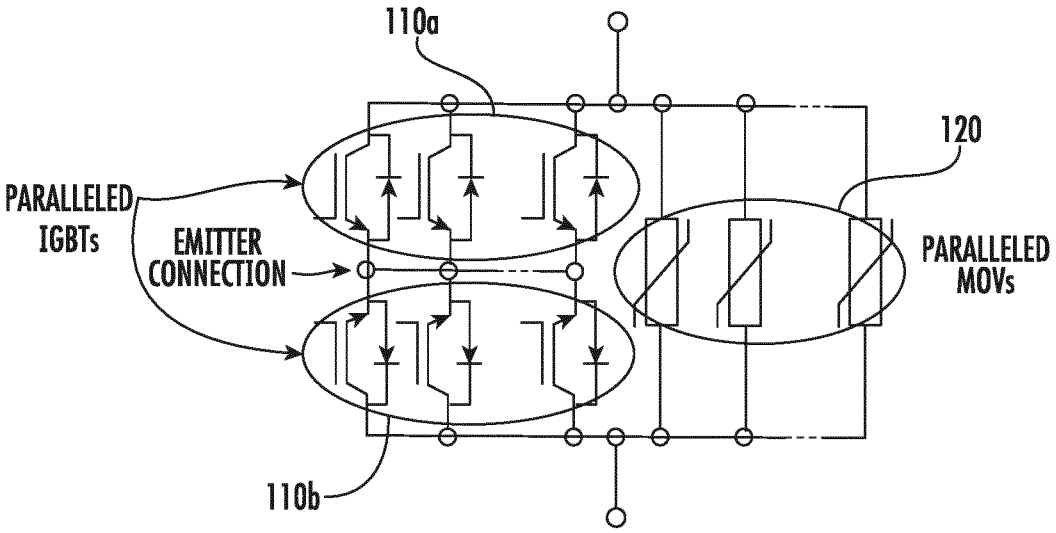

110a
120
PARALLELED
IGBTs
EMITTER
CONNECTION
PARALLELED
MOVs
110b

FIG. 1

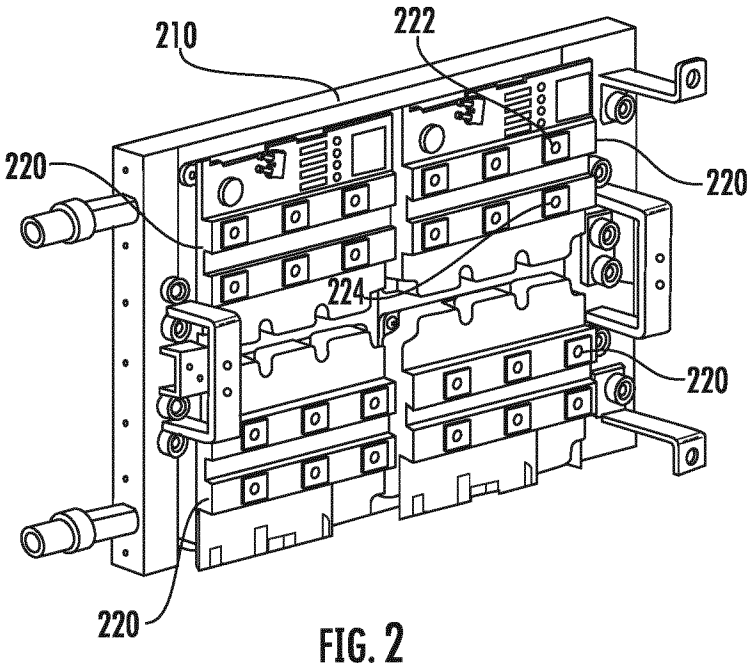


FIG. 2

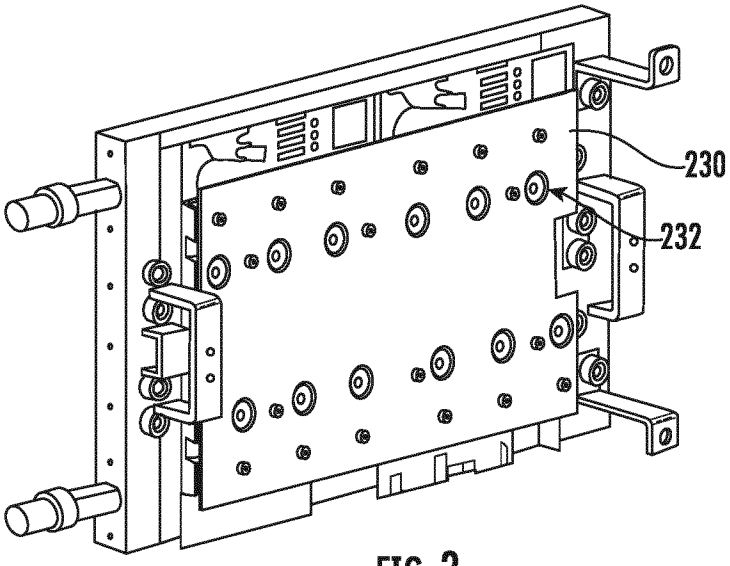


FIG. 3

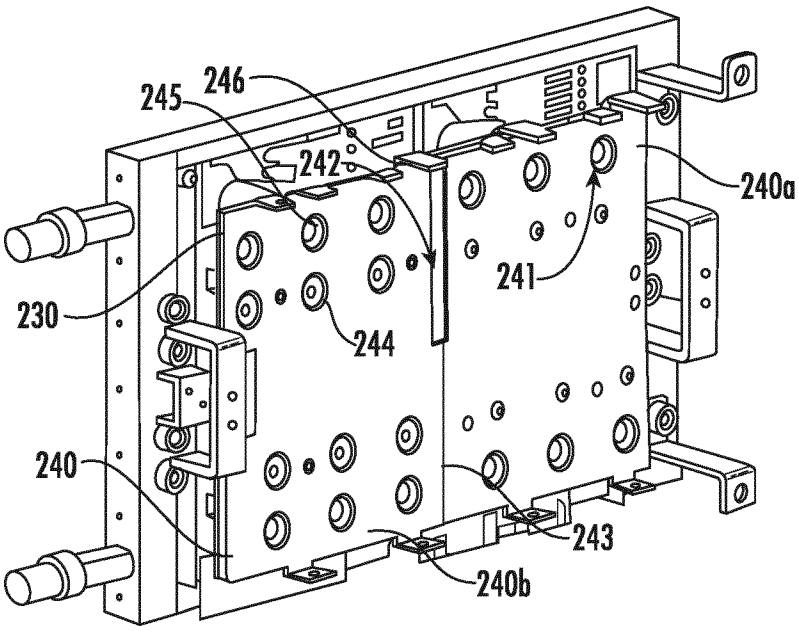

245
246
242
240a
241
230
244
240
243
240b

FIG. 4

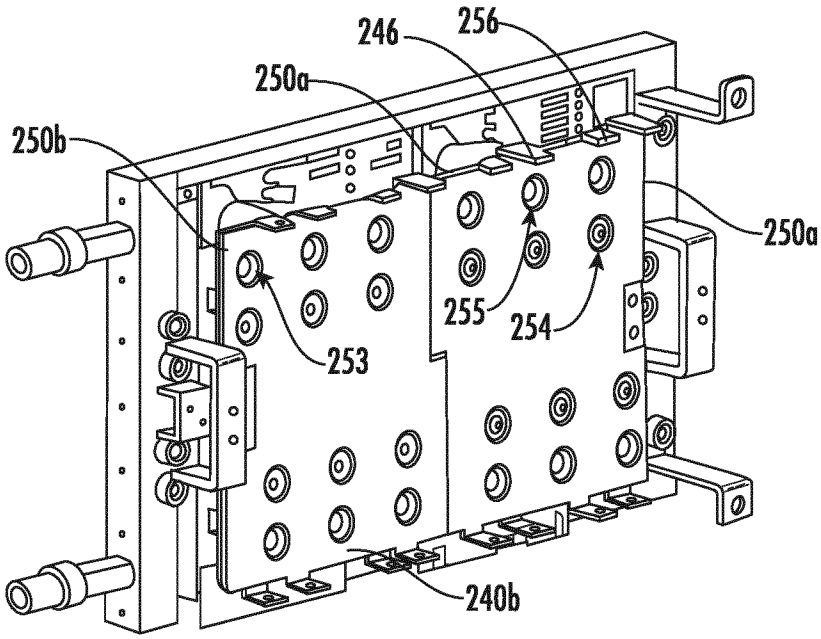

246
256
250a
250b
250a
255
254
253
240b

FIG. 5

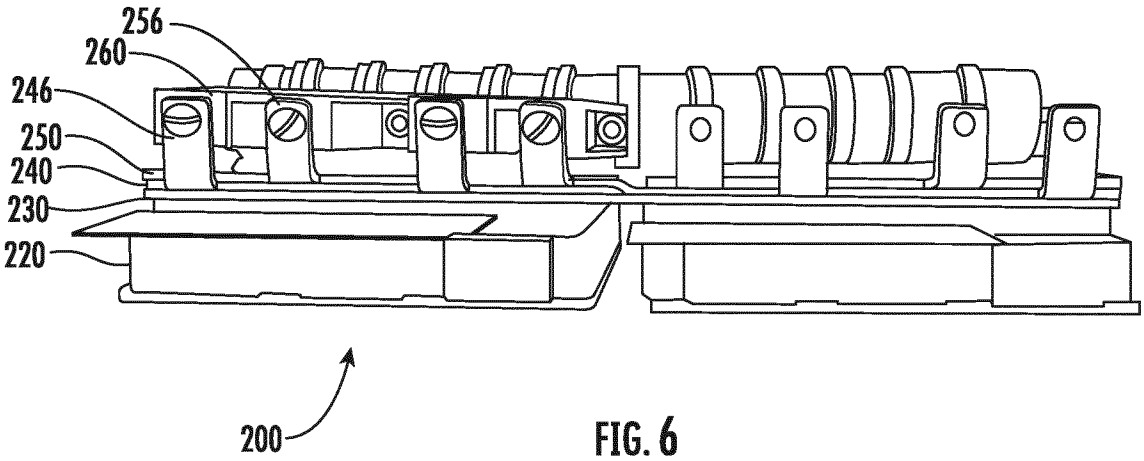


FIG. 6

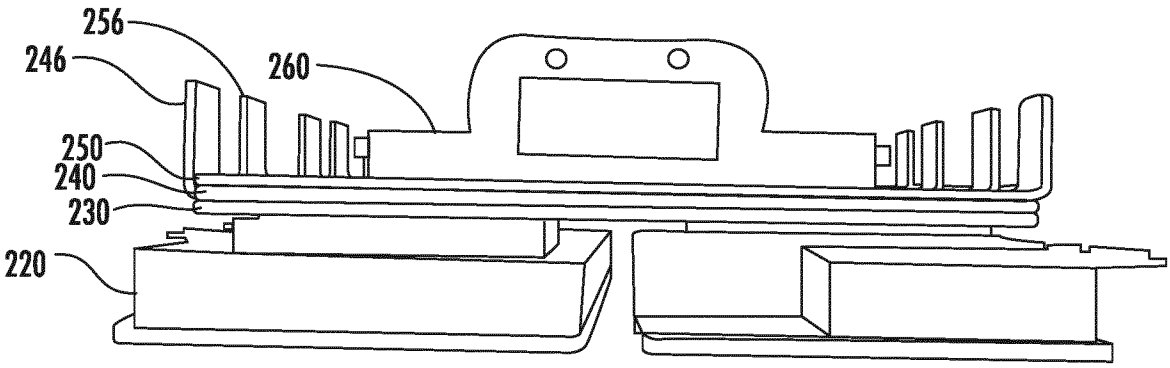


FIG. 7

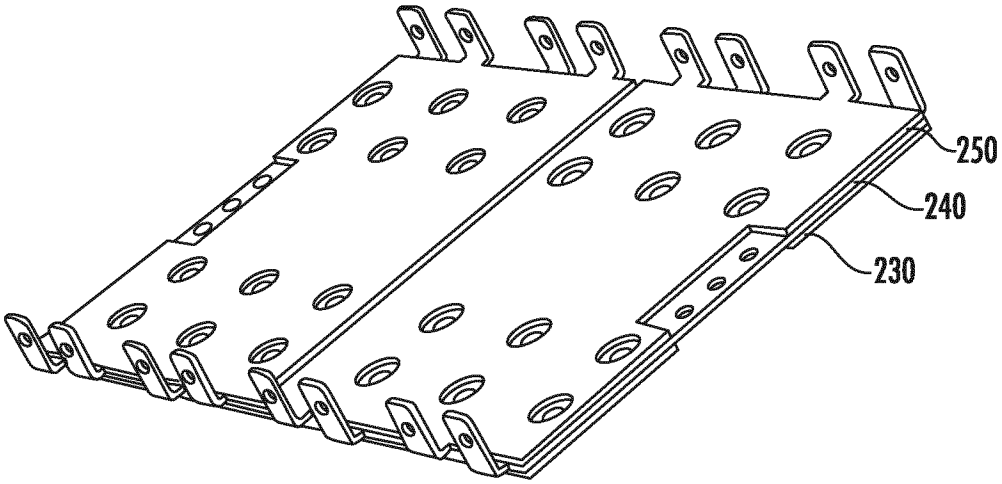


FIG. 8



FIG. 9

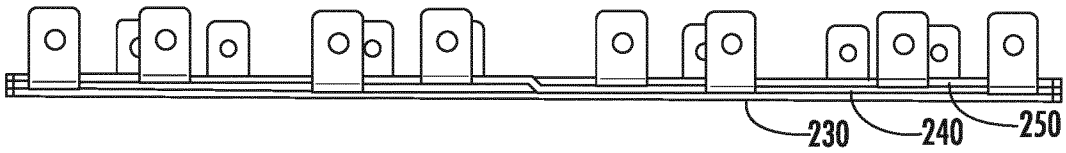


FIG. 10

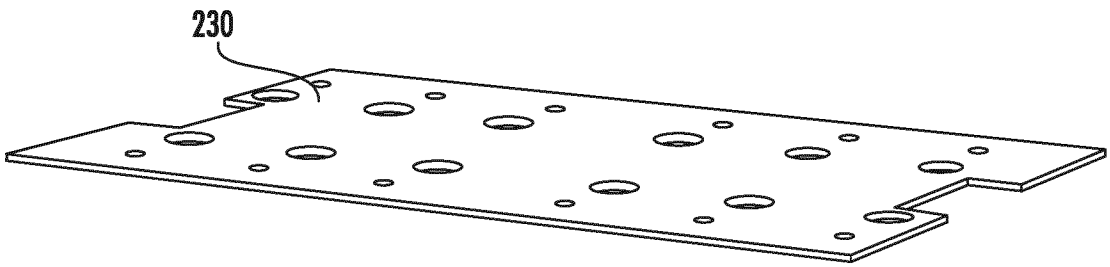


FIG. 11



FIG. 12

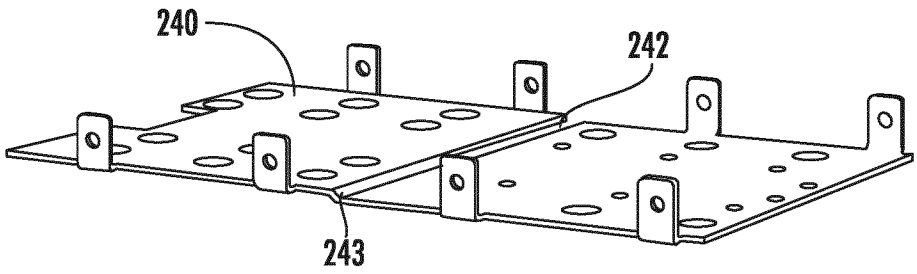


FIG. 13

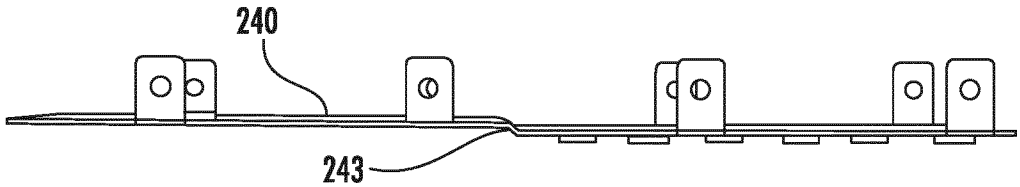


FIG. 14

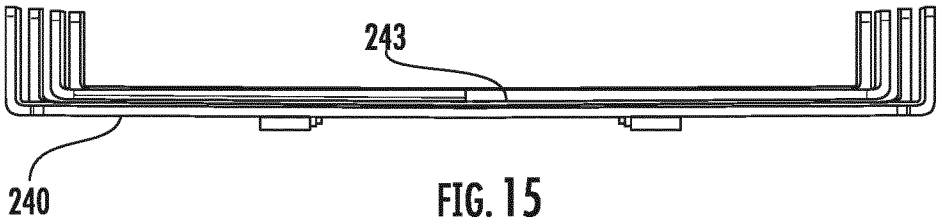


FIG. 15

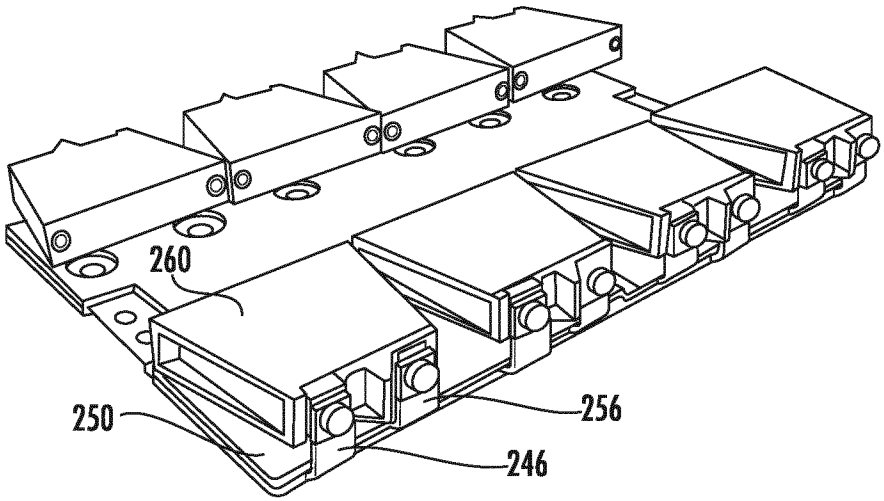


FIG. 16

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2020/025089

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L23/66 H01L23/64 H01L25/07 H02M7/00
ADD. H05K1/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L H05K H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2005 160248 A (FUJI ELECTRIC SYSTEMS CO LTD) 16 June 2005 (2005-06-16) paragraph [0033] - paragraph [0035]; figure 6	1,4,6,7
X	US 2019/006831 A1 (SHE XU [US] ET AL) 3 January 2019 (2019-01-03) paragraph [0037] - paragraph [0041]; figure 4	1-4
A	CN 204 349 816 U (SHENZHEN INVT ELECTRIC CO LTD) 20 May 2015 (2015-05-20) description relating to figures 3-5; figures 3-5	1-19

☐ Further documents are listed in the continuation of Box C.

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31 March 2020	08/04/2020

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2020/025089

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