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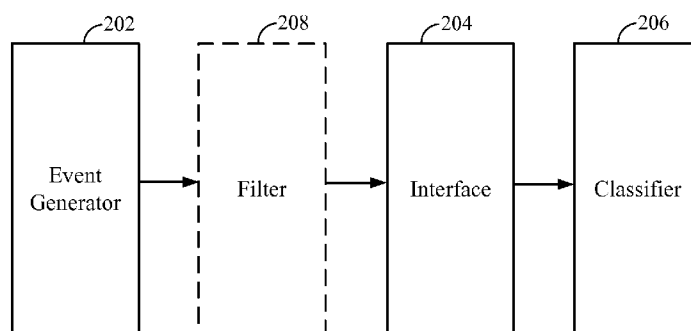
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(54) **Title:** INTERFACING AN EVENT BASED SYSTEM WITH A FRAME BASED PROCESSING SYSTEM



**FIG. 2**

(57) **Abstract:** A method of interfacing an event based processing system with a frame based processing system is presented. The method includes converting multiple events into a frame. The events may be generated from an event sensor. The method also in-  
cludes inputting the frame into the frame based processing system.

## **INTERFACING AN EVENT BASED SYSTEM WITH A FRAME BASED PROCESSING SYSTEM**

### **CROSS-REFERENCE TO RELATED APPLICATION**

**[0001]** This application claims the benefit under 35 U.S.C. § 119(e) to U.S. Provisional Patent Application No. 62/051,145, entitled “INTERFACING AN EVENT BASED SYSTEM WITH A FRAME BASED PROCESSING SYSTEM,” filed on September 16, 2014, the disclosure of which is expressly incorporated by reference herein in its entirety.

### **BACKGROUND**

#### **Field**

**[0002]** Certain aspects of the present disclosure generally relate to neural system engineering and, more particularly, to systems and methods for interfacing an event based system with a frame based processing system.

#### **Background**

**[0003]** An event-driven object detection system may use a sensor, such as a dynamic vision sensor (DVS), to detect moving objects, such as faces or cars. Furthermore, the event-driven object detection system may classify the detected objects in real time based on prior training. In some cases, it is desirable to interface an event based system with a frame based processing system to process the detected events.

### **SUMMARY**

**[0004]** In one aspect of the present disclosure, a method for interfacing an event based processing system with a frame based processing system is disclosed. The method includes converting multiple events into a frame. In one configuration, the events are generated from an event sensor. The method also includes inputting the frame into the frame based processing system.

**[0005]** Another aspect of the present disclosure is directed to an apparatus including means for converting multiple events into a frame. In one configuration, the events are generated from an event sensor. The apparatus also includes means for inputting the frame into the frame based processing system.

[0006] In another aspect of the present disclosure, a computer program product for interfacing an event based processing system with a frame based processing system is disclosed. The computer program product has a non-transitory computer-readable medium with non-transitory program code recorded thereon. The program code is executed by a processor and includes program code to convert multiple events into a frame. In one configuration, the events are generated from an event sensor. The program code also includes program code to input the frame into the frame based processing system.

[0007] Another aspect of the present disclosure is directed to an apparatus for interfacing an event based processing system with a frame based processing system having a memory and one or more processors coupled to the memory. The processor(s) is configured to convert multiple events into a frame. In one configuration, the events are generated from an event sensor. The processor(s) is also configured to input the frame into the frame based processing system.

[0008] Additional features and advantages of the disclosure will be described below. It should be appreciated by those skilled in the art that this disclosure may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present disclosure. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the teachings of the disclosure as set forth in the appended claims. The novel features, which are believed to be characteristic of the disclosure, both as to its organization and method of operation, together with further objects and advantages, will be better understood from the following description when considered in connection with the accompanying figures. It is to be expressly understood, however, that each of the figures is provided for the purpose of illustration and description only and is not intended as a definition of the limits of the present disclosure.

## **BRIEF DESCRIPTION OF THE DRAWINGS**

[0009] The features, nature, and advantages of the present disclosure will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters identify correspondingly throughout.

[0010] FIGURE 1 illustrates an example of components of an event-driven object-detection system in accordance with certain aspects of the present disclosure.

[0011] FIGURE 2 illustrates an example of an interface between an event based processing system and a frame based processing system.

[0012] FIGURE 3 is a flow diagram illustrating a method for interfacing an event based processing system with a frame based processing system in accordance with an aspect of the present disclosure.

[0013] FIGURE 4 is a block diagram illustrating different modules/means/components in an exemplary apparatus.

### DETAILED DESCRIPTION

[0014] The detailed description set forth below, in connection with the appended drawings, is intended as a description of various configurations and is not intended to represent the only configurations in which the concepts described herein may be practiced. The detailed description includes specific details for the purpose of providing a thorough understanding of the various concepts. However, it will be apparent to those skilled in the art that these concepts may be practiced without these specific details. In some instances, well-known structures and components are shown in block diagram form in order to avoid obscuring such concepts.

[0015] Based on the teachings, one skilled in the art should appreciate that the scope of the disclosure is intended to cover any aspect of the disclosure, whether implemented independently of or combined with any other aspect of the disclosure. For example, an apparatus may be implemented or a method may be practiced using any number of the aspects set forth. In addition, the scope of the disclosure is intended to cover such an apparatus or method practiced using other structure, functionality, or structure and functionality in addition to or other than the various aspects of the disclosure set forth. It should be understood that any aspect of the disclosure disclosed may be embodied by one or more elements of a claim.

[0016] The word “exemplary” is used herein to mean “serving as an example, instance, or illustration.” Any aspect described herein as “exemplary” is not necessarily to be construed as preferred or advantageous over other aspects.

[0017] Although particular aspects are described herein, many variations and permutations of these aspects fall within the scope of the disclosure. Although some benefits and advantages of the preferred aspects are mentioned, the scope of the disclosure is not intended to be limited to particular benefits, uses or objectives. Rather, aspects of the disclosure are intended to be broadly applicable to different technologies, system configurations, networks and protocols, some of which are illustrated by way of example in the figures and in the following description of the preferred aspects. The detailed description and drawings are merely illustrative of the disclosure rather than limiting, the scope of the disclosure being defined by the appended claims and equivalents thereof.

#### EVENT-DRIVEN OBJECT DETECTION SYSTEM

[0018] An event-driven object detection system may use a sensor, such as a dynamic vision sensor (DVS), to detect moving objects, such as faces or cars. Furthermore, the event-driven object detection system may classify the detected objects in real time based on prior training. The computations in the system may be triggered by sensor events. The event-driven object detection system may be referred to as the detection system.

[0019] According to aspects of the present disclosure, a detections system may process an image when an event is generated. That is, the detection system does not perform processing when events are not output from the sensor. Moreover, the processing load scales linearly with the sensor event rate.

[0020] The detection system 100 comprises various modules for processing data. As an example, as shown in FIGURE 1, the detection system may include a sensor 110, such as a dynamic vision sensor, an event-driven sort time spatial discrete Fourier transformer (DFT) 120, an event-driven feature extractor 130, and a classifier 140.

[0021] In one configuration, the sensor 110 is configured to detect events. Specifically, the events may be generated from a change in intensity of a detected pixel. For example, the sensor 110 may be a DVS128 sensor from iniLabs. The sensor array

may have a size of  $N \times N$  ( $N = 128$ ) of which each pixel is a level-crossing sampler of log-luminance in time. The temporal resolution of the pixel is on the order of ten micro seconds. The output of the sensor may be a polarized, coordinate-addressed event train  $\{(t_k; p_k; \mu_k; v_k)\}$ , where  $t_k$ 's and  $p_k$ 's are time stamps and polarities of events and  $(\mu_k; v_k)$  are the pixel coordinates of event  $t_k$ . Here  $t_k \in \mathbb{R}$ ,  $p_k \in \{-1, 1\}$  and  $\mu_k, v_k \in \{1, \dots, 128\}$ .

**[0022]** The pixel response functions may be defined as:

$$x_{\mu,v}(t) = \sum_k p_k \delta_{u,u_k} \delta_{v,v_k} \delta(t - t_k), \quad (1)$$

where  $(\mu, v) \in \{1, \dots, 128\}^2$  index pixels.  $\delta$  is the Kroenecker delta and  $\delta(\cdot)$  is the Dirac delta function. The matrix may also be written as:

$$X(t) = [x_{\mu,v}](t) \quad (2)$$

**[0023]** The event-driven spatial DFT (eSTsDFT) 120 receives an event train  $\{(t_k; p_k; \mu_k; v_k)\}$  as an input and outputs a real-time complex  $N \times N$  ( $N = 128$ ) matrix of spatial DFT:

$$\tilde{X}(t) = \int S_N X(T) S_N^T w(T - t) dT \quad (3)$$

**[0024]** Here

$$S_N = \left[ \frac{w_N^{mn}}{\sqrt{N}} \right] m, n = 0, \dots, N-1 = [s_N^0, \dots, s_N^n, \dots, s_N^{N-1}] = \frac{1}{\sqrt{N}} \begin{bmatrix} 1 & 1 & 1 & \dots & 1 \\ 1 & w_N & w_N^2 & \dots & w_N^{N-1} \\ 1 & w_N^2 & w_N^4 & \dots & w_N^{2(N-1)} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & w_N^{N-1} & w_N^{2(N-1)} & \dots & w_N^{(N-1)(N-1)} \end{bmatrix} \quad (4)$$

is the DFT matrix of  $N$ -th order, where  $w_N \triangleq e^{-\frac{2\pi i}{N}}$  is the  $N$ -th root of unity and

$$s_N^n \triangleq \frac{1}{\sqrt{N}} \begin{bmatrix} 1 \\ w_N^n \\ \vdots \\ w_N^{n(N-1)} \end{bmatrix} \text{ is the } (n+1)\text{-th column of } S_N.$$

**[0025]** Furthermore,  $w(-t) = \theta(t) \exp(-\omega_0 t)$  is an exponential short-time window function. The eSTsDFT 120 computes the value of  $\tilde{X}(t)$  at each sensor event  $\{t_k\}$ .

[0026] The event-drive feature extractor (eFE) 130 reduces the dimensionality of the output of the eSTsDFT 120 from  $N \times N \times 2$  ( $N = 128$ ) to  $L = 64$  (i.e., from 128 complex numbers to 64 real numbers). Specifically, the  $L$  features are binned instantaneous spectral power of  $\tilde{X}(t)$ ,  $y(t) = \varphi(\tilde{X} * (t)\tilde{X}(t))$  where  $*$  is the conjugate transpose and  $\varphi()$  is a log-linear transformation function, which is computed as follows.

[0027]  $\tilde{X} * \tilde{X}$  may be written as a  $128 \times 128$  dimensional vector  $x$  and the linear function  $\varphi()$ , may be expressed as a matrix multiplication followed by a logarithm  $y = \log(\Phi x)$ , where  $\Phi = \begin{bmatrix} \Phi_\rho \\ \Phi_\theta \end{bmatrix}$  is a binary matrix of size  $64 \times (128 \times 128)$ , which contains two components of size  $32 \times (128 \times 128)$ , corresponding to 32 radial and 32 angular power bins. These matrices are constant valued and computed priorly, i.e., hand-crafted features.

[0028] The event-driven feature extractor 130 computes the value of  $y(t)$  at the end of every sensor event packet that contains on the order of 100 to 200 events.

[0029] The classifier 140, such as an event-driven support vector classifier (eSVM), computes a time-varying class label function  $z(t)$  based on the real-time feature vector  $y(t)$  extracted by the eFE 130, i.e.,  $z(t) = \psi(y(t))$ , by virtue of a support vector machine with a Gaussian radial basis function (RBF) as kernels.

[0030] The classifier 140 computes the value of  $z(t)$  at the end of every sensor event packet that occurs at least  $\Delta t_{\min}$  since the last classification. As described below, TABLE 1 specifies mathematical description of the input/output objects to and from the modules/components of the system.

TABLE 1

Module	Input	Output	Output dimensions	Update schedule
DVS	Visual scene	$X(t, \{(t_k, p_k, \mu_k, \nu_k)\})$	$128 \times 128$ binary	
eSTsDFT	$X(t)$	$\tilde{X}(t, \omega_0)$	$128 \times 128$ complex	Every event
eFE	$\tilde{X}(t)$	$y(t, \Phi)$	$64 \times 1$ real	Every 100-200 events
eSVM	$y(t)$	$z(t)$	$1 \times 1$ categorical	Every 100-200 events separated by no less than 100 ms

[0031] TABLES 2 and 3 provide the constant and state variables used for the event-driven short-time spatial DFT. TABLE 4 is pseudo-code for a single iteration of the detection system during which an event packet of length  $K$  is processed from the DVS.

TABLE 2

Constant variable	Type	Dimension	Description
$\omega_0$	real	$1 \times 1$	Window function parameter (set to 10 Hz)
$S_{128}$	complex	$128 \times 128$	DFT matrix of order 128
$\Phi$	sparse binary	$64 \times (128 \times 128)$	Feature matrix
$\Delta t_{\min}$	real	$1 \times 1$	Minimum classification interval (set to 100 ms)

TABLE 3

State variable	Type	Dimension	Description
$\mathbf{t}$	real	$K \times 1$	Event packet time stamp vector
$\mathbf{p}$	$-1, 1$	$K \times 1$	Event packet polarity vector
$\mu$	$1, \dots, 128$	$K \times 1$	Event packet horizontal coordinate vector
$\nu$	$1, \dots, 128$	$K \times 1$	Event packet vertical coordinate vector
$\tilde{\mathbf{X}}$	complex	$128 \times 128$	Short-time spatial DFT matrix
$\mathbf{y}$	real	$64 \times 1$	Feature vector
$z$	categorical	$1 \times 1$	Class label
$t_{\text{current}}$	real	$1 \times 1$	Current event time
$t_{\text{last}}$	real	$1 \times 1$	Last event time
$t_{\text{classify}}$	real	$1 \times 1$	Last classification time

TABLE 4

	Pseudocode	Comment
1	fetch from DVS128 ( $\mathbf{t}, \mathbf{p}, \mu, \nu$ )	Event packet of length $K$
2	for $k$ from 1 to $K$ do	For each event
3	$t_{\text{current}} \leftarrow t_k$	Current event time
4	$\tilde{\mathbf{X}} \leftarrow \mu_k \left[ \mathbf{s} \mathbf{\Omega}^{-1} \mathbf{s} \mathbf{\Omega}^{-1T} \right] + e^{-\omega_0(t_{\text{current}} - t_{\text{last}})} \tilde{\mathbf{X}}$	Update $\tilde{\mathbf{X}}$
5	$t_{\text{last}} \leftarrow t_{\text{current}}$	Current event becomes last event
6	end for	
7	$\mathbf{y} \leftarrow \varphi(\tilde{\mathbf{X}}; \Phi)$	Feature extraction
8	if $t_{\text{current}} - t_{\text{classify}} > \Delta t_{\min}$ do	If long enough since last classification
9	$z \leftarrow \psi(\mathbf{y})$	Classification
10	end if	

## INTERFACING AN EVENT BASED SYSTEM WITH A FRAME BASED PROCESSING SYSTEM

[0032] As previously discussed, an event based processing system may use a sensor, such as a dynamic vision sensor (DVS), to detect moving objects, such as people or cars. For example, the sensor, such as the dynamic vision sensor, detects the change in luminance such that at least one event may be an indication that the luminance has changed at a particular location. Furthermore, the event-driven object detection system may classify the detected objects in real time based on prior training. Thus, the event



based processing system may output one or more detected events. In the present application, events may be referred to as pixel events.

**[0033]** Furthermore, a frame based processing system classifies objects detected in a frame, such as a picture. A frame may be processed by a frame based processing system, such as a Support Vector Machine (SVM) classifier. In a conventional system, the events output by the event based object detection system may not be processed by a frame based processing system. The frame based processing system may be referred to as a frame based classifier.

**[0034]** Still, in some cases, a frame based processing system may be specified for an event based object detection system. Because the desired input of the frame based processing system may not be compatible with the output of the event based object detection system, an interface may be specified to convert event based outputs to a frame input. The converting of the events may be performed in real time as events are received or when a specific number of events have been received. The event based object detection system may be referred to as the event based system or the event based processing system.

**[0035]** In one configuration, a timing interface is specified to generate a frame by aggregating events received over a predetermined time. Furthermore, the aggregated events are input into the frame based classifier from the interface. The specific time period may be dynamically modified based on desired results and/or processing load. In another configuration, an event number interface is specified to generate a frame by aggregating a specific number of events into a frame. The specific number of events may be dynamically modified based on desired results and/or processing load.

**[0036]** Furthermore, in one configuration, the interface is dynamically selected. That is, the interface may dynamically switch between aggregating events for a specific time period into the frame and aggregating a specific number of events into the frame, and vice versa. The switching may be initiated based on desired results and/or processing load.

**[0037]** It should be noted that aspects of the present disclosure are not limited to image processing and may also be applied to other sensors, such as audio sensors. For example, audio frequencies or other audio characteristics may be detected by an event

based object detection system and may be input to a frame based processing system or an equivalent type of processing system.

**[0038]** Additionally, or alternatively, in one configuration, a filter may be defined between the output of the event based object detection system and the input to the interface. The filter may be specified to filter (i.e., drop) specific events, such as events from specific areas that are not important, events from areas that produce an increased amount of noise, and/or events that satisfy other conditions. In one configuration, the downstream processing block determines that a number of events from a specific region have exceeded a threshold. Thus, the filtering of events to drop subsequent events from the specific region may be specified by the downstream processing block. The region may refer to a spatial area that produces events and/or a specific event generator, such as a specific vehicle that generates events.

**[0039]** It should be noted that the filter is not limited to filtering events that are visual and may also filter audio, temporal, or other events. For example, the filter may drop events occurring in a specific spectral frequency, such as an audio frequency, and/or the filter may drop events occurring at a specific time period. Additionally, events from a specific region or all events may be dropped when the processing load of the system exceeds a threshold and/or when another condition is satisfied.

**[0040]** For example, a specific area may have produced events that are greater than a threshold. Therefore, because the system has already received a specific number of events, the system may no longer desire to receive additional events from a specific region. Thus, the filter may be specified to filter events from specific regions. As another example, a downstream processing block, such as the frame based classifier, may desire to only classify events from one or more specific regions. Therefore, the filter may filter all or some events that are different from desired region(s).

**[0041]** FIGURE 2 illustrates an example of an interface according to an aspect of the present disclosure. As shown in FIGURE 2, an event may be generated at an event generator 202. The event generator may be a sensor, such as a camera, or other device that processes events. For example, the events may be events generated from pixels received at a camera. Furthermore, the events are input to the interface 204. As previously discussed, the interface may dynamically select between a timing interface

and an event number interface to generate a frame. Moreover, the generated frame is output to a classifier 206, such as frame based processing system. Additionally, as shown in FIGURE 2, an optional filter 208 may be defined between the event generator 202 and the interface 204. As previously discussed, the filter 208 may be used to filter all events or specific events.

**[0042]** FIGURE 3 illustrates a flow diagram 300 for interfacing an event based system with a frame based processing system in accordance with aspects of the present disclosure. As show in FIGURE 3, at block 302, the system converts multiple events into a frame. The events may be generated from an event sensor. Furthermore, at block 304, the system inputs the frame into the frame based processing system, such as a classifier.

**[0043]** FIGURE 4 is a diagram illustrating an example of a hardware implementation for an apparatus 400 employing a processing system 414 for interfacing an event based system with a frame based system. The processing system 414 may be implemented with a bus architecture, represented generally by the bus 424. The bus 424 may include any number of interconnecting buses and bridges depending on the specific application of the processing system 414 and the overall design constraints. The bus 424 links together various circuits including one or more processors and/or hardware modules, represented by the processor 422 the modules 402, 404, and the computer-readable medium 426. The bus 424 may also link various other circuits such as timing sources, peripherals, voltage regulators, and power management circuits, which are well known in the art, and therefore, will not be described any further.

**[0044]** The apparatus includes a processing system 414 coupled to a transceiver 430. The transceiver 430 is coupled to one or more antennas 420. The transceiver 430 enables communicating with various other apparatus over a transmission medium. The processing system 414 includes a processor 422 coupled to a computer-readable medium 426. The processor 422 is responsible for general processing, including the execution of software stored on the computer-readable medium 426. The software, when executed by the processor 422, causes the processing system 414 to perform the various functions described for any particular apparatus. The computer-readable medium 426 may also be used for storing data that is manipulated by the processor 422 when executing software.

**[0045]** The processing system 414 includes a converting module 402 for converting events, generated from an event sensor, into a frame. The processing system 414 also includes an inputting module 404 for inputting the frame into the frame based processing system. The modules may be software modules running in the processor 422, resident/stored in the computer-readable medium 426, one or more hardware modules coupled to the processor 422, or some combination thereof.

**[0046]** In one configuration, an interface 204 is configured for interfacing an event based processing system with a frame based processing system. The interface 204 may include means for converting and means for inputting. In one aspect, the converting means may be the converting module 402 configured to perform the functions recited by the converting means. The interface 204 is also configured to include a means for inputting. In one aspect, the inputting means may be the inputting module 404 configured to perform the functions recited by the inputting means. In another aspect, the aforementioned means may be any module or any apparatus configured to perform the functions recited by the aforementioned means.

**[0047]** The various operations of methods described above may be performed by any suitable means capable of performing the corresponding functions. The means may include various hardware and/or software component(s) and/or module(s), including, but not limited to, a circuit, an application specific integrated circuit (ASIC), or processor. Generally, where there are operations illustrated in the figures, those operations may have corresponding counterpart means-plus-function components with similar numbering.

**[0048]** As used herein, the term “determining” encompasses a wide variety of actions. For example, “determining” may include calculating, computing, processing, deriving, investigating, looking up (e.g., looking up in a table, a database or another data structure), ascertaining and the like. Additionally, “determining” may include receiving (e.g., receiving information), accessing (e.g., accessing data in a memory) and the like. Furthermore, “determining” may include resolving, selecting, choosing, establishing and the like.

**[0049]** As used herein, a phrase referring to “at least one of” a list of items refers to any combination of those items, including single members. As an example, “at least one of: a, b, or c” is intended to cover: a, b, c, a-b, a-c, b-c, and a-b-c.

**[0050]** The various illustrative logical blocks, modules and circuits described in connection with the present disclosure may be implemented or performed with a general purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array signal (FPGA) or other programmable logic device (PLD), discrete gate or transistor logic, discrete hardware components or any combination thereof designed to perform the functions described herein. A general-purpose processor may be a microprocessor, but in the alternative, the processor may be any commercially available processor, controller, microcontroller or state machine. A processor may also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

**[0051]** The steps of a method or algorithm described in connection with the present disclosure may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module may reside in any form of storage medium that is known in the art. Some examples of storage media that may be used include random access memory (RAM), read only memory (ROM), flash memory, erasable programmable read-only memory (EPROM), electrically erasable programmable read-only memory (EEPROM), registers, a hard disk, a removable disk, a CD-ROM and so forth. A software module may comprise a single instruction, or many instructions, and may be distributed over several different code segments, among different programs, and across multiple storage media. A storage medium may be coupled to a processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor.

**[0052]** The methods disclosed herein comprise one or more steps or actions for achieving the described method. The method steps and/or actions may be interchanged with one another without departing from the scope of the claims. In other words, unless a specific order of steps or actions is specified, the order and/or use of specific steps and/or actions may be modified without departing from the scope of the claims.

**[0053]** The functions described may be implemented in hardware, software, firmware, or any combination thereof. If implemented in hardware, an example hardware configuration may comprise a processing system in a device. The processing system may be implemented with a bus architecture. The bus may include any number of interconnecting buses and bridges depending on the specific application of the processing system and the overall design constraints. The bus may link together various circuits including a processor, machine-readable media, and a bus interface. The bus interface may be used to connect a network adapter, among other things, to the processing system via the bus. The network adapter may be used to implement signal processing functions. For certain aspects, a user interface (e.g., keypad, display, mouse, joystick, etc.) may also be connected to the bus. The bus may also link various other circuits such as timing sources, peripherals, voltage regulators, power management circuits, and the like, which are well known in the art, and therefore, will not be described any further.

**[0054]** The processor may be responsible for managing the bus and general processing, including the execution of software stored on the machine-readable media. The processor may be implemented with one or more general-purpose and/or special-purpose processors. Examples include microprocessors, microcontrollers, DSP processors, and other circuitry that can execute software. Software shall be construed broadly to mean instructions, data, or any combination thereof, whether referred to as software, firmware, middleware, microcode, hardware description language, or otherwise. Machine-readable media may include, by way of example, random access memory (RAM), flash memory, read only memory (ROM), programmable read-only memory (PROM), erasable programmable read-only memory (EPROM), electrically erasable programmable Read-only memory (EEPROM), registers, magnetic disks, optical disks, hard drives, or any other suitable storage medium, or any combination thereof. The machine-readable media may be embodied in a computer-program product. The computer-program product may comprise packaging materials.

**[0055]** In a hardware implementation, the machine-readable media may be part of the processing system separate from the processor. However, as those skilled in the art will readily appreciate, the machine-readable media, or any portion thereof, may be external to the processing system. By way of example, the machine-readable media

may include a transmission line, a carrier wave modulated by data, and/or a computer product separate from the device, all which may be accessed by the processor through the bus interface. Alternatively, or in addition, the machine-readable media, or any portion thereof, may be integrated into the processor, such as the case may be with cache and/or general register files. Although the various components discussed may be described as having a specific location, such as a local component, they may also be configured in various ways, such as certain components being configured as part of a distributed computing system.

**[0056]** The processing system may be configured as a general-purpose processing system with one or more microprocessors providing the processor functionality and external memory providing at least a portion of the machine-readable media, all linked together with other supporting circuitry through an external bus architecture. Alternatively, the processing system may comprise one or more neuromorphic processors for implementing the neuron models and models of neural systems described herein. As another alternative, the processing system may be implemented with an application specific integrated circuit (ASIC) with the processor, the bus interface, the user interface, supporting circuitry, and at least a portion of the machine-readable media integrated into a single chip, or with one or more field programmable gate arrays (FPGAs), programmable logic devices (PLDs), controllers, state machines, gated logic, discrete hardware components, or any other suitable circuitry, or any combination of circuits that can perform the various functionality described throughout this disclosure. Those skilled in the art will recognize how best to implement the described functionality for the processing system depending on the particular application and the overall design constraints imposed on the overall system.

**[0057]** The machine-readable media may comprise a number of software modules. The software modules include instructions that, when executed by the processor, cause the processing system to perform various functions. The software modules may include a transmission module and a receiving module. Each software module may reside in a single storage device or be distributed across multiple storage devices. By way of example, a software module may be loaded into RAM from a hard drive when a triggering event occurs. During execution of the software module, the processor may load some of the instructions into cache to increase access speed. One or more cache

lines may then be loaded into a general register file for execution by the processor. When referring to the functionality of a software module below, it will be understood that such functionality is implemented by the processor when executing instructions from that software module.

**[0058]** If implemented in software, the functions may be stored or transmitted over as one or more instructions or code on a computer-readable medium. Computer-readable media include both computer storage media and communication media including any medium that facilitates transfer of a computer program from one place to another. A storage medium may be any available medium that can be accessed by a computer. By way of example, and not limitation, such computer-readable media can comprise RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that can be used to carry or store desired program code in the form of instructions or data structures and that can be accessed by a computer. Also, any connection is properly termed a computer-readable medium. For example, if the software is transmitted from a website, server, or other remote source using a coaxial cable, fiber optic cable, twisted pair, digital subscriber line (DSL), or wireless technologies such as infrared (IR), radio, and microwave, then the coaxial cable, fiber optic cable, twisted pair, DSL, or wireless technologies such as infrared, radio, and microwave are included in the definition of medium. Disk and disc, as used herein, include compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk, and Blu-ray® disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Thus, in some aspects computer-readable media may comprise non-transitory computer-readable media (e.g., tangible media). In addition, for other aspects computer-readable media may comprise transitory computer-readable media (e.g., a signal). Combinations of the above should also be included within the scope of computer-readable media.

**[0059]** Thus, certain aspects may comprise a computer program product for performing the operations presented herein. For example, such a computer program product may comprise a computer-readable medium having instructions stored (and/or encoded) thereon, the instructions being executable by one or more processors to perform the operations described herein. For certain aspects, the computer program product may include packaging material.



**[0060]** Further, it should be appreciated that modules and/or other appropriate means for performing the methods and techniques described herein can be downloaded and/or otherwise obtained by a user terminal and/or base station as applicable. For example, such a device can be coupled to a server to facilitate the transfer of means for performing the methods described herein. Alternatively, various methods described herein can be provided via storage means (e.g., RAM, ROM, a physical storage medium such as a compact disc (CD) or floppy disk, etc.), such that a user terminal and/or base station can obtain the various methods upon coupling or providing the storage means to the device. Moreover, any other suitable technique for providing the methods and techniques described herein to a device can be utilized.

**[0061]** It is to be understood that the claims are not limited to the precise configuration and components illustrated above. Various modifications, changes and variations may be made in the arrangement, operation and details of the methods and apparatus described above without departing from the scope of the claims.

## CLAIMS

### WHAT IS CLAIMED IS:

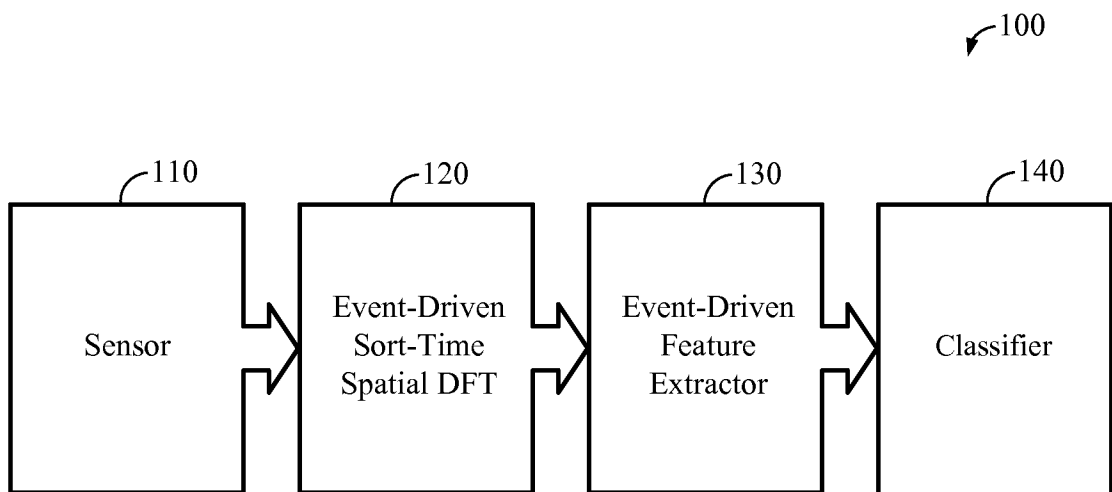
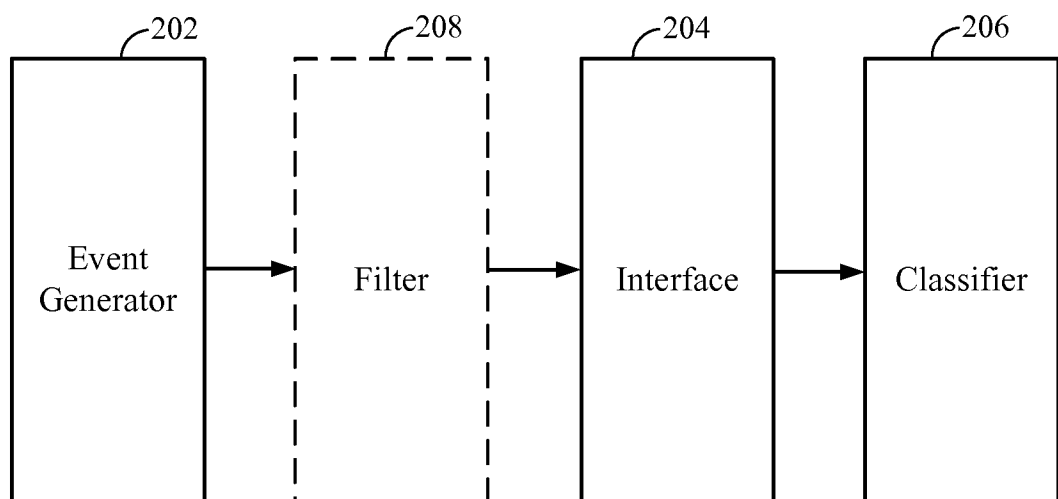
1. A method of interfacing an event based processing system with a frame based processing system, comprising:  
converting a plurality of events, generated from an event sensor, into a frame;  
and  
inputting the frame into the frame based processing system.
2. The method of claim 1, in which the plurality of events are aggregated for a specific time period into the frame.
3. The method of claim 2, in which the specific time period is dynamically modified based at least on desired results, processing load, or a combination thereof.
4. The method of claim 1, in which a specific number of events of the plurality of events are aggregated into the frame.
5. The method of claim 4, in which the specific number of events is dynamically modified based at least on desired results, processing load, or a combination thereof.
6. The method of claim 1, in which the converting comprises dynamically switching between aggregating events for a specific time period into the frame and aggregating a specific number of events into the frame.
7. The method of claim 1, further comprising filtering events based at least in part on a processing load, a number of events being greater than a threshold, or a combination thereof.
8. The method of claim 1, in which at least one event of the plurality of events is an indication from a vision sensor that a luminance has changed at a particular location.

9. An apparatus for interfacing an event based processing system with a frame based processing system, the apparatus comprising:  
a memory unit; and  
at least one processor coupled to the memory unit, the at least one processor being configured:  
to convert a plurality of events, generated from an event sensor, into a frame; and  
to input the frame into the frame based processing system.
10. The apparatus of claim 9, in which the plurality of events are aggregated for a specific time period into the frame.
11. The apparatus of claim 10, in which the specific time period is dynamically modified based at least on desired results, processing load, or a combination thereof.
12. The apparatus of claim 9, in which a specific number of events of the plurality of events are aggregated into the frame.
13. The apparatus of claim 12, in which the specific number of events is dynamically modified based at least on desired results, processing load, or a combination thereof.
14. The apparatus of claim 9, in which the at least one processor is further configured to convert by dynamically switching between aggregating events for a specific time period into the frame and aggregating a specific number of events into the frame.
15. The apparatus of claim 9, in which the at least one processor is further configured to filter events based at least in part on a processing load, a number of events being greater than a threshold, or a combination thereof.
16. The apparatus of claim 9, in which at least one event of the plurality of events is an indication from a vision sensor that a luminance has changed at a particular location.

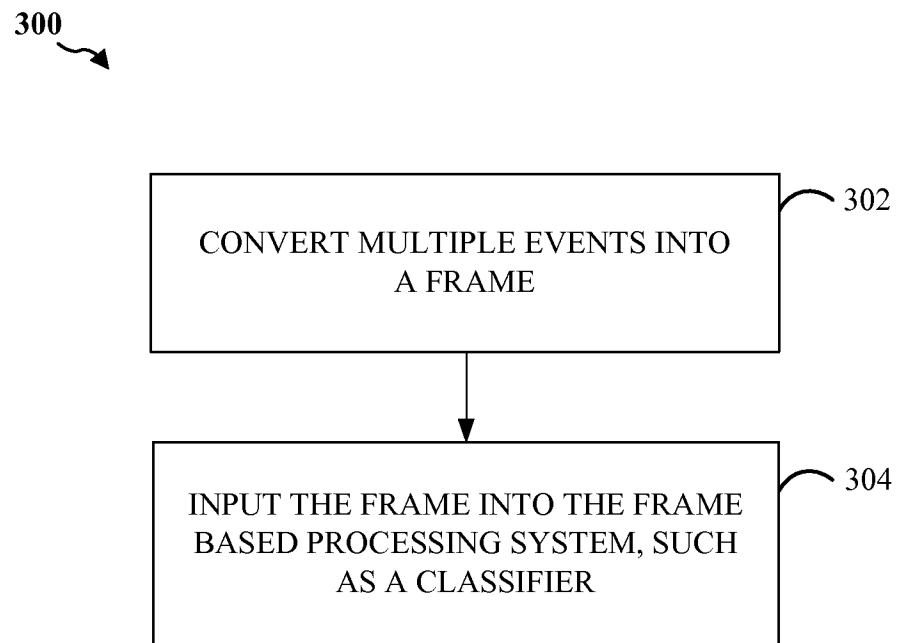
17. An apparatus for interfacing an event based processing system with a frame based processing system, the apparatus comprising:  
means for converting a plurality of events, generated from an event sensor, into a frame; and  
means for inputting the frame into the frame based processing system.
18. The apparatus of claim 17, in which the plurality of events are aggregated for a specific time period into the frame.
19. The apparatus of claim 18, in which the specific time period is dynamically modified based at least on desired results, processing load, or a combination thereof.
20. The apparatus of claim 17, in which a specific number of events of the plurality of events are aggregated into the frame.
21. The apparatus of claim 20, in which the specific number of events is dynamically modified based at least on desired results, processing load, or a combination thereof.
22. The apparatus of claim 17, in which the converting means dynamically switches between aggregating events for a specific time period into the frame and aggregating a specific number of events into the frame.
23. The apparatus of claim 17, further comprising means for filtering events based at least in part on a processing load, a number of events being greater than a threshold, or a combination thereof.
24. The apparatus of claim 17, in which at least one event of the plurality of events is an indication from a vision sensor that a luminance has changed at a particular location.

25. A computer program product for interfacing an event based processing system with a frame based processing system, the computer program product comprising:
- a non-transitory computer-readable medium having program code recorded thereon, the program code being executed by a processor and comprising:
    - program code to convert a plurality of events, generated from an event sensor, into a frame; and
    - program code to input the frame into the frame based processing system.

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**FIG. 1****FIG. 2**

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**FIG. 3**

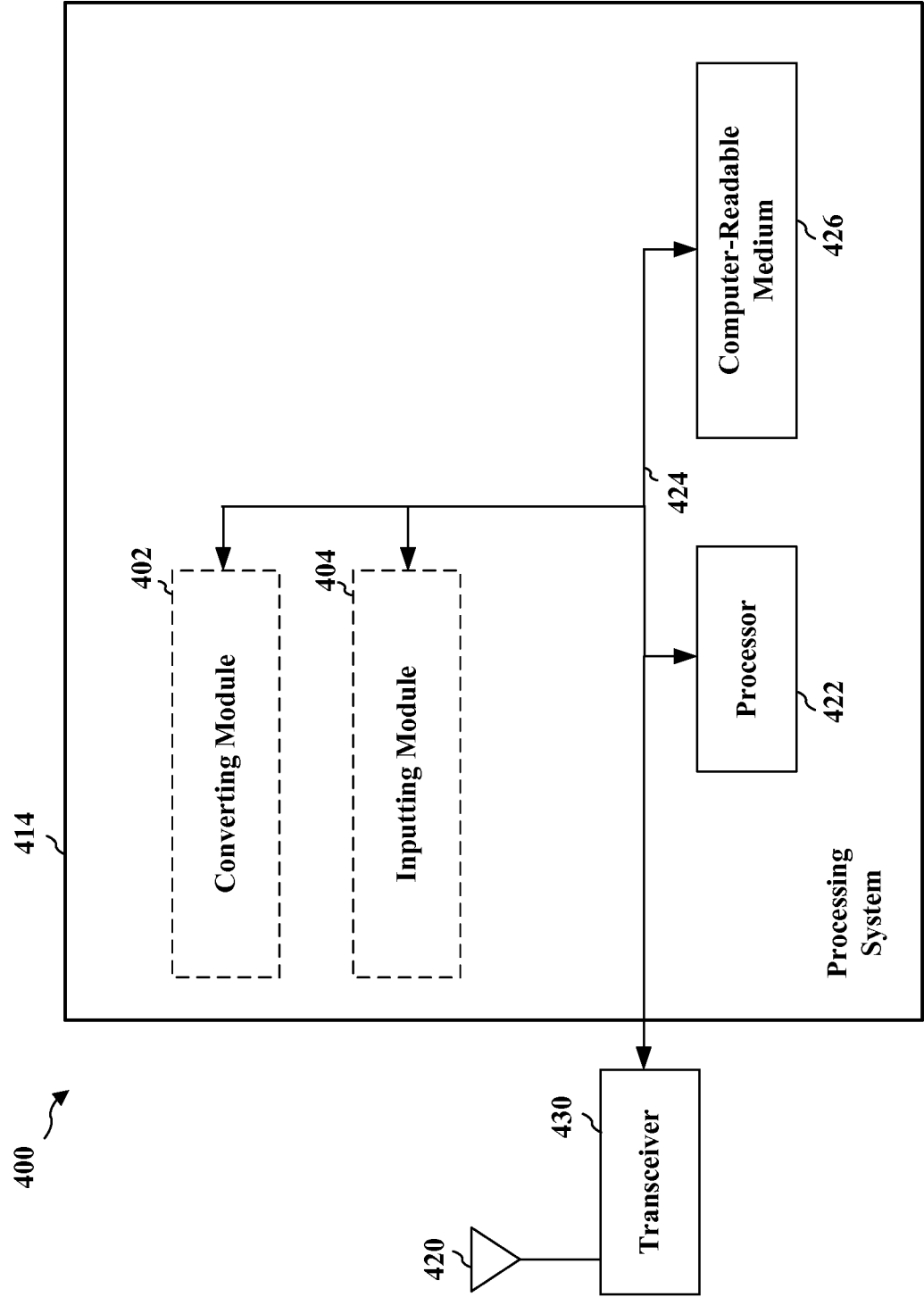


FIG. 4



## INTERNATIONAL SEARCH REPORT

International application No  
PCT/US2015/046066A. CLASSIFICATION OF SUBJECT MATTER  
INV. G06K9/20 G06K9/60  
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)  
G06K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	TEIXEIRA T ET AL: "Address-Event Imagers for Sensor Networks: Evaluation and Modeling", INFORMATION PROCESSING IN SENSOR NETWORKS, 2006. IPSN 2006. THE FIFTH INTERNATIONAL CONFERENCE ON NASHVILLE, TN, USA 19-21 APRIL 2006, PISCATAWAY, NJ, USA, IEEE, 19 April 2006 (2006-04-19), pages 458-466, XP010931928, DOI: 10.1145/1127777.1127847 ISBN: 978-1-59593-334-8 2. Address Event Architecture 4. Image Acquisition and communication figures 5,6 5.1 AER Conversion 5.2 Building an AER Emulator ----- -/--	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

## \* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&amp;" document member of the same patent family

Date of the actual completion of the international search

6 November 2015

Date of mailing of the international search report

18/11/2015

Name and mailing address of the ISA/

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Authorized officer

Meier, Ueli

## INTERNATIONAL SEARCH REPORT

International application No

PCT/US2015/046066

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
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X	----- PATRICK LICHTSTEINER ET AL: "A 128128 120 dB 15 s Latency Asynchronous Temporal Contrast Vision Sensor", IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE SERVICE CENTER, PISCATAWAY, NJ, USA, vol. 43, no. 2, 1 February 2008 (2008-02-01), pages 566-576, XP011200748, ISSN: 0018-9200, DOI: 10.1109/JSSC.2007.914337 figure 11	1-25
X	----- EP 2 574 511 A1 (HONDA RES INST EUROPE GMBH [DE]) 3 April 2013 (2013-04-03)	1,8,9, 16,17, 24,25
A	paragraph [0028]	2-7, 10-15, 18-23
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A	3.1 Silicon Retina Stereo Sensor	2-7, 10-15, 18-23
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# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2015/046066

Patent document cited in search report	Publication date	Patent family member(s)	Publication date	
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			JP 2013079937 A	02-05-2013
			US 2013085642 A1	04-04-2013
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