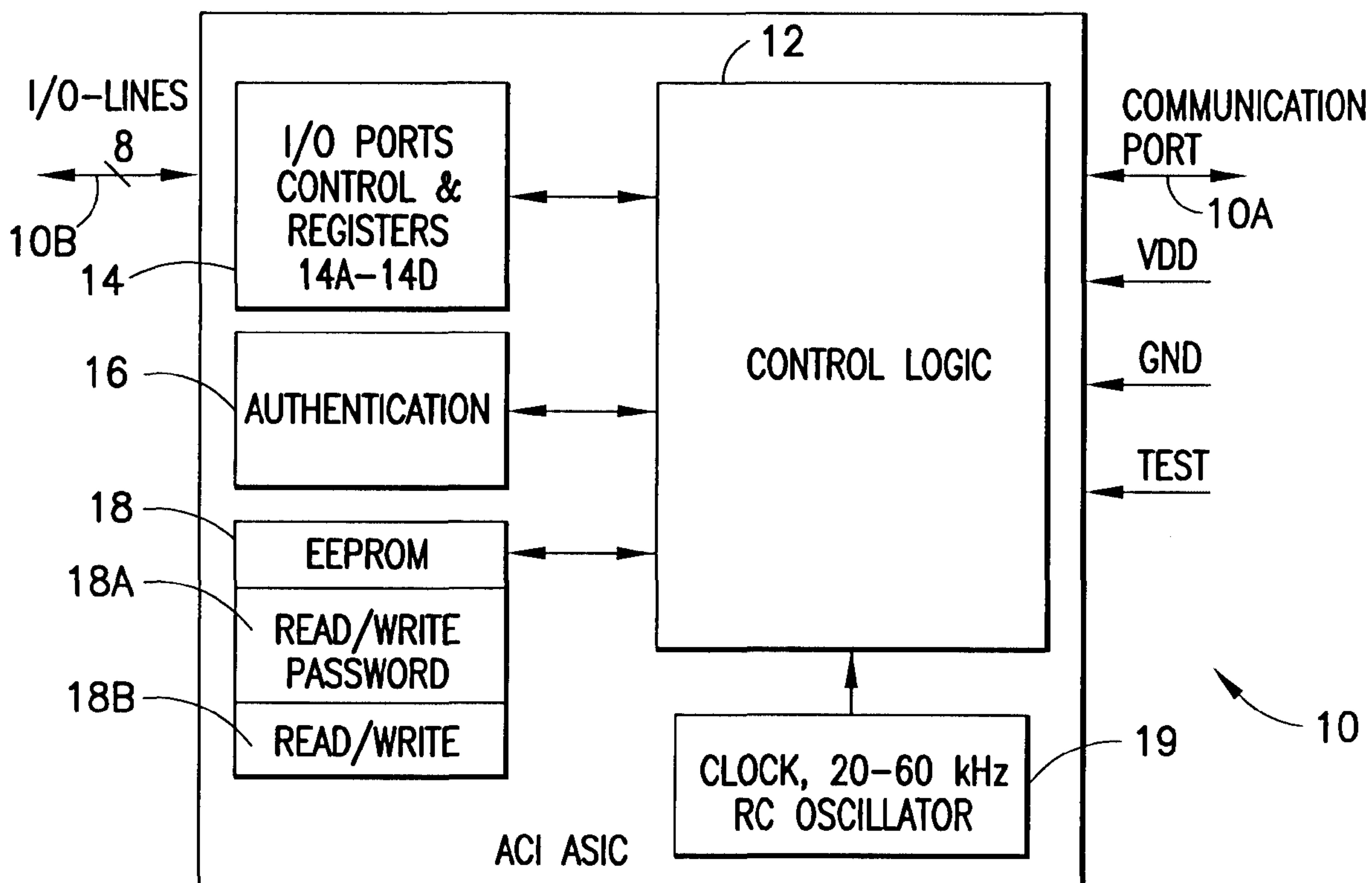




(86) Date de dépôt PCT/PCT Filing Date: 2003/02/13
(87) Date publication PCT/PCT Publication Date: 2003/09/18
(85) Entrée phase nationale/National Entry: 2004/08/20
(86) N° demande PCT/PCT Application No.: IB 2003/000548
(87) N° publication PCT/PCT Publication No.: 2003/077504
(30) Priorités/Priorities: 2002/03/08 (60/362,908) US;
2002/09/16 (10/245,053) US

(51) Cl.Int.⁷/Int.Cl.⁷ H04L 25/00
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(54) Titre : INTERFACE DE COMMANDE ACCESSOIRE
(54) Title: ACCESSORY CONTROL INTERFACE



(57) Abrégé/Abstract:

Disclosed is an interface (10, 40) between a master device (30) and a slave device (20). The interface includes a bit serial bidirectional signal line (10A) for conveying commands and associated data from the master device to the slave device, and for conveying a reset signal, an interrupt signal, and a learning sequence signal for specifying a duration of a bit time for data transferred from the slave device to the master device. The bit serial bidirectional signal line further indicates an accessory device connected/disconnected state to the master device.



(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
18 September 2003 (18.09.2003)

PCT

(10) International Publication Number
WO 03/077504 A3

(51) International Patent Classification⁷: **H04L 25/00**

(21) International Application Number: PCT/IB03/00548

(22) International Filing Date: 13 February 2003 (13.02.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:

60/362,908 8 March 2002 (08.03.2002) US
10/245,053 16 September 2002 (16.09.2002) US

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(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

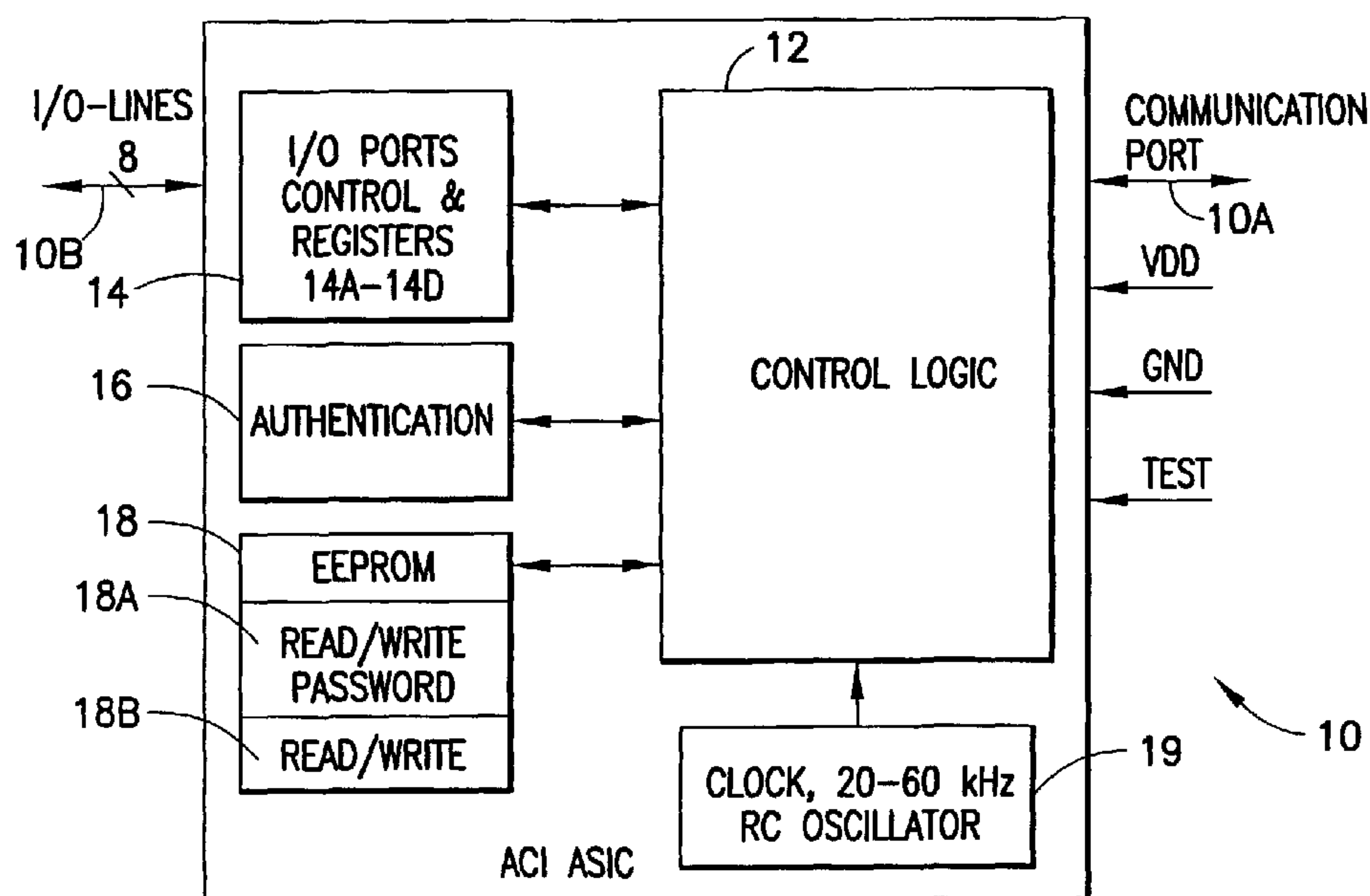
Published:

— with international search report

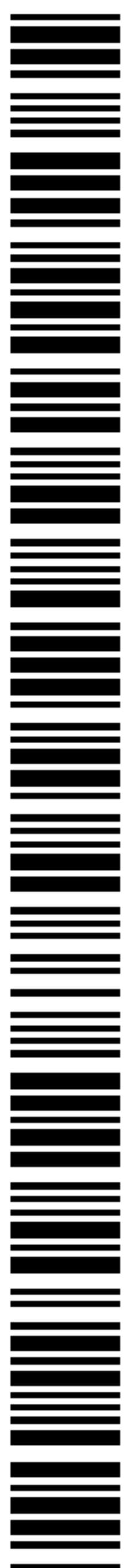
(88) Date of publication of the international search report:
18 December 2003

[Continued on next page]

(54) Title: ACCESSORY CONTROL INTERFACE



(57) Abstract: Disclosed is an interface (10, 40) between a master device (30) and a slave device (20). The interface includes a bit serial bidirectional signal line (10A) for conveying commands and associated data from the master device to the slave device, and for conveying a reset signal, an interrupt signal, and a learning sequence signal for specifying a duration of a bit time for data transferred from the slave device to the master device. The bit serial bidirectional signal line further indicates an accessory device connected/disconnected state to the master device.



WO 03/077504 A3

WO 03/077504 A3



For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

ACCESSORY CONTROL INTERFACE

TECHNICAL FIELD:

These teachings relate generally to electronic devices, such as mobile terminals,
5 including cellular telephones and personal communicators, and to accessory units for
mobile terminals, and more specifically to mobile terminal/accessory interface hardware
and software.

BACKGROUND:

10 Modern mobile terminals, such as cellular telephones and personal communicators, are
typically designed with an interface for connecting with external accessory devices.
These accessory devices extend the functionality of the mobile terminal and/or provide
other useful functions. Examples of accessories include battery chargers, headsets and
"hands free" adapters (enabling the mobile terminal to be used without being held in the
15 user's hand).

As can be appreciated, as the complexity of mobile terminals and their accessories have
increased the required mobile terminal/accessory interface has increased in complexity
as well. For example, the interface is typically required to accommodate the transfer of
20 data between the mobile terminal and the accessory.

It is desirable that the mobile terminal/accessory interface be physically and electrically
robust, be capable of handling low error rate data transfers, and yet still be low cost and
of minimal complexity. Another important consideration is the power consumption of
25 the mobile terminal/accessory interface. As in all battery powered devices, the
minimization of power consumption is an important goal.

When using conventional accessory interfaces it has been problematic for the mobile
terminal to detect certain specified accessories. Problems have also been observed using
30 analog to digital converter (ADC)-based accessory detection schemes. Furthermore, with
the ADC-based detection scheme there are only a limited number of accessories that can
be identified (limited at least by the precision of the analog voltage that is produced to
represent a given accessory, and by the conversion accuracy of the ADC in the mobile
terminal).

Prior to this invention, all of the foregoing various and somewhat conflicting needs and goals have not been realized in circuitry that provides a mobile terminal/accessory interface, and the foregoing problems have not received a satisfactory resolution.

- 5 While described above in the context of mobile terminals, it should be appreciated that the same or similar problems can exist in other types of equipment.

SUMMARY OF THE PREFERRED EMBODIMENTS

The foregoing and other problems are overcome, and other advantages are realized, in
10 accordance with the presently preferred embodiments of these teachings.

An Accessory Control Interface (ACI) encompasses an interface protocol and an accessory application specific integrated circuit (ASIC) that together provide an ability to identify, authenticate and control the operation of accessories used with a mobile
15 terminal. In the preferred embodiment the ACI ASIC is installed within the accessory, and communicates through an input/output port and associated connector with circuitry in the mobile terminal.

Through the use of the ACI ASIC the mobile terminal is enabled to recognize when an
20 accessory is inserted or removed. Preferably a mobile terminal interrupt signal line is activated by the ACI ASIC for interrupting the data processor of the mobile terminal. For example, when the mobile terminal is placed within a hands free (HF) stand the mobile terminal is automatically switched to the HF mode. When the mobile terminal is removed from the HF stand the mobile terminal is automatically switched out of the HF
25 mode and back to the normal mode of operation. The ACI ASIC enables the interface to identify different accessory types by parameters stored as digital data within a memory of the ACI ASIC, and transferred to the mobile terminal using a serial data bus.

An important feature of this invention is the power savings that are realized, since after
30 insertion detection is accomplished (the mobile terminal and accessory are physically and electrically coupled together) subsequent communications can be performed at a rate set by the low speed (e.g., 32kHz) mobile terminal sleep clock. The sleep clock is one used to periodically interrupt the mobile terminal to exit a low power, idle mode of operation.

This technique provides considerable savings in mobile terminal (and accessory) power consumption.

Another important feature is that the ACI ASIC includes or is coupled to a simple and inexpensive local oscillator that is implemented as an RC oscillator, as opposed to a crystal oscillator. This is made possible by the tolerance of the interface to the potentially wide frequency range (e.g., 20kHz to 60kHz, nominally about 27kHz) and inaccuracy of the accessory RC oscillator (+50%). The RC oscillator can be integrated into the ACI ASIC, thereby realizing considerable cost and circuit area savings, as well as improving the reliability and testability of the accessory and accessory interface.

A further advantage made possible by the use of this invention is the ability to design and offer new accessories, even for those mobile terminals that are already in the field. This is possible because the accessory is enabled to inform the mobile terminal of its relevant features due to the presence of a non-volatile memory within the ACI ASIC, where the memory stores feature data that is readable from the mobile terminal through the interface.

As will be shown below, this invention provides an interface between a master device and a slave device. The interface includes a bit serial bidirectional signal line for conveying commands and associated data from the master device to the slave device, and for conveying a reset signal, an interrupt signal, and a learning sequence signal for specifying a duration of a bit time for data transferred from the slave device to the master device. The bit serial bidirectional signal line further indicates an accessory device connected/disconnected state to the master device.

In the preferred embodiment the master device is or includes a mobile terminal. The mobile terminal samples the data transferred from the slave device to the master device in synchronism with its sleep clock. The interface includes, in the accessory device, an Accessory Control Interface chip and an on-chip RC oscillator providing a clock signal to the Accessory Control Interface chip. The bit time is a multiple of the clock signal, and the mobile terminal adapts the sampling of the data transferred from the slave device in accordance with the specified duration of the bit time.

The Accessory Control Interface chip further includes an on-chip non-volatile memory for storing at least accessory related feature data that is readable by the mobile terminal in response to a memory read command sent from the mobile terminal to the Accessory Control Interface chip over the bit serial bidirectional signal line.

5

The Accessory Control Interface chip further includes an on-chip challenge/response authentication function that is challenged in response to an authentication challenge command and associated challenge data sent from the mobile terminal to the Accessory Control Interface chip over the bit serial bidirectional signal line. Authentication result data is subsequently sent by the Accessory Control Interface chip to the mobile terminal over the bit serial bidirectional signal line in response to an authentication result command sent from the mobile terminal to the Accessory Control Interface chip.

10

While described herein in the context of a master device, or a mobile terminal, such as a mobile voice terminal such as a cellular telephone, this invention applies as well to personal digital assistants (PDAs) and other handheld or otherwise portable devices that are intended to be interfaced to external equipment, devices and/or accessories. As such, hereafter the term "mobile terminal", and also the term "master device", should be interpreted so as to include a wide variety of equipment types, both portable and non-portable, that include, but that are not limited to, cellular telephones, personal communicators, personal organizers, personal digital assistants (PDAs), email terminals, personal computers, laptop computers, notebook computers, workstations, home electronic devices, including game consoles as well as television monitors, and other devices that can be interfaced to external equipment, devices and/or accessories.

20

25

BRIEF DESCRIPTION OF THE DRAWINGS

30 The foregoing and other aspects of these teachings are made more evident in the following Detailed Description of the Preferred Embodiments, when read in conjunction with the attached Drawing Figures, wherein:

Fig. 1 is a block diagram of an embodiment of the Accessory Control Interface (ACI) ASIC that is constructed in accordance with this invention;

Fig. 2 is a block diagram showing the ACI ASIC of Fig. 1 installed within an exemplary accessory (a headset having speakers and a microphone), and the coupling between the ACI ASIC and a mobile terminal that includes a baseband ASIC;

Fig. 3 are waveform diagrams that illustrate the format of a single logical 1 bit and logical 0 bit (Fig. 3A), the format of a transmission of a byte (8-bits) in bit serial format (Fig. 3B), the format of two data bursts (active mode) separated by a mobile terminal sleep mode period (Fig. 3C), a Reset pulse (Fig. 3D), a Learning Sequence (Fig. 3E), and an Interrupt (Fig. 3F);

Fig. 4 illustrates an exemplary waveform that would appear on the bit serial data line shown in Fig. 2 from the time the accessory is inserted or attached to the mobile terminal to the time that it is removed or detached from the mobile terminal;

Fig. 5 illustrates a basic command data sequence, and the format of the initial command byte of the sequence; and

Fig. 6 is a waveform diagram that also illustrates an interrupt comparator used with a pull-up resistor that is switchably connected to the bit serial data line.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 illustrates a block diagram of one (non-limiting) embodiment of the Accessory Control Interface (ACI) ASIC 10 that is constructed in accordance with this invention. The ACI ASIC 10 includes a control logic block 12, an I/O port control registers and data registers block (I/O block) 14, an authentication block 16, a non-volatile memory 18 (e.g., 32 bytes) having a read/write (R/W) with password memory portion 18A and a normal R/W portion 18B. The memory could be a EEPROM or other type of suitable memory device or devices. A clock, preferably implemented as a low cost, on-chip resistor/capacitor (RC) oscillator 19 (frequency range about 20kHz to about 60kHz) is

also provided. The output of the RC oscillator 19 feeds the control logic block 12, and thus forms the master timing signal for the operation of the ACI ASIC 10, as well as controlling the timing of bit serial data that passes over the communications port 10A (preferably one signal line that operates in an asynchronous bit-serial format, as described in further detail below. A plurality of programmable I/O lines 10B (e.g., four or eight, depending on the embodiment) are also provided for controlling circuitry within the accessory that the ACI ASIC 10 is installed within (when programmed as outputs), or for reading back status and other signals (when programmed as inputs).

10 The authentication block 16 executes an authentication algorithm, preferably a challenge response type of algorithm, and can be used to verify that a given accessory is an authentic accessory, and not one provided from unauthorized third parties.

Reference can be had, for example, to commonly assigned U.S. Patent No.: 5,991,407 for a description of one type of authentication challenge/response system used in a radiotelephone network. Other or similar types of authentication challenge/response systems could be implemented as well with authentication block 16.

Referring now also to Fig. 2, the ACI ASIC 10 is shown installed within an accessory 20, in this non-limiting example a headset accessory that includes left and right audio transducers (miniature speakers) 22 and 24, respectively, and a microphone 26. Connection is made to the accessory via an accessory connector 40, where one half of the connector 40 is installed in the mobile terminal 30 and the other half, the mating half, is installed in or connected to the accessory 20. A multi-wire cable 42 can be used to carry the required analog and digital signal lines between the mobile terminal 30 and the accessory 20. All of these signal lines are interfaced to suitable circuitry in the mobile terminal 30, shown for convenience as a baseband ASIC 32. The details of the circuitry that drives the audio transducers 22, 24, and that receives the audio signal from the microphone 26, are not germane to an understanding of this invention.

30

Of greater interest to the teachings of this invention is the interface to the bit serial, bidirectional data signal line 10A. Included in this interface is a resistance R coupled between signal line 10A and circuit ground, and a suitable pull-up resistance (R_{PU})

installed in the mobile terminal 10. By example, R may be a 56k ohm resistor and R_{PU} may be in the range of about 100k to about 120k ohms. R and R_{PU} together form a resistor voltage divider network. When connected as shown, the presence of the resistance R affects the level of the signal line 10A, thereby enabling detection of the presence of the accessory 20 by the mobile terminal 30. Disconnection of the accessory is also detectable. Referring as well to Fig. 4, insertion of the accessory containing the ACI ASIC 10 and associated circuitry (point A) places R_{PU} in series with R, thereby pulling the data signal line 10A down from a level V1 to a lower level V2 and crossing a detection threshold V_{THRESH} (e.g., $V_{THRESH} = 0.74V_{CC}$).

10

Referring now as well to Fig. 6, at points B, C, F and G the data signal line 10A is pulled up with a strong pull-up resistor (R_{strong} , e.g., 4.7 k) by the master device. This mode can be referred to as "data line reserved". In this mode the mobile terminal 30 and the ACI ASIC 10 can communicate by pulling the data signal line 10A low. At points D and H the data signal line is released and assumes the level of V2 (resulting from the action of resistor divider R_{PU} and R. At point I the accessory 20 is detached, and R_{PU} operates to pull up the level of data signal line 10A to V1 (e.g., to V_{CC}).

Fig. 6 also shows an interrupt comparator 32A and a Switch used for selectively coupling and decoupling R_{strong} to the data signal line 10A. The comparator 32A operates to compare the voltage appearing on the data signal line to the V_{THRESH} voltage.

As shown in Fig. 3A, a single bit time T can be in the range of about 500 microseconds to about 1500 microseconds, depending on the frequency of the RC oscillator 19. More particularly, in a presently preferred, but non-limiting embodiment of this invention the control logic 12 operates with 30 clock cycles from the RC oscillator 19 to form the bit time. Assuming the lower frequency of 20kHz, one clock cycle is 50 microseconds, and one bit time T is 30×50 microseconds or 1500 microseconds. Assuming the higher frequency of 60kHz, one clock cycle is 16.6 microseconds, and one bit time T is 30×16.6 microseconds or 498 microseconds.

Each bit time is controlled by the control logic block 12 to begin as a positive transition and to end sometime after making a negative transition. When the negative transition is

made defines whether the bit is a logic one (a late negative transition) or a logic zero (an early negative transition.) As seen in Fig. 3B, which illustrates a byte frame, by sampling the waveform at $T/2$ it is possible to detect whether a logic one or a logic zero bit is being transmitted, as the negative transition is arranged to occur either before or after $T/2$.

5

Other signal transition periods preferably signal other events. For example, and as is shown in Fig. 3D, holding the signal line 10A low for a period T_{reset} (points B and E in Fig. 4) signals a warm (non-power on) reset state.

- 10 The data signal line 10A is also controlled to signal a Learning Sequence, as is illustrated in Fig. 3E. The Learning Sequence specifies the duration of T for an ensuing data transmission. Data transmission always begins by sending a logic one, which specifies the bit time T . This sequence is sent after a reset and at the beginning of a response from the ACI ASIC 10 (point B in Fig. 4). A low Start pulse period (S) starts each byte
- 15 transmission for synchronization, and is greater than some minimum period (e.g., 50 microseconds). The start of the byte pulse is always generated by the sender of the byte.

- The data signal line 10A is also controlled to generate an Interrupt from the ACI ASIC 10, as shown in Fig. 3F. Assume that the data signal line free state is a logic zero, the
- 20 ACI ASIC 10 then generates a pull-up pulse of duration T_{int} if the following conditions are fulfilled: an interrupt option bit has been set in one of the control registers 14; the data signal line 10A has been free for period T_{inten} (for example, for 200 internal clock cycles generated by the RC oscillator 19); and the state of the ASIC pin has been loaded into one of the data registers 14.

25

- Fig. 5 illustrates a basic command data sequence, and the format of the initial command byte of the sequence. The number of data bytes following the command byte are a function of the command. In the command byte format the first six bits specify an address to read/write in the memory 18, when the state of the Command Selection bit is
- 30 in a first state (the Read/Write bit specifies read or write), while the first six bits specify a command, when the state of the Command Selection bit is in the other state. Exemplary commands include, but need not be limited to: Authentication Challenge, Authentication Response, Read/Write an Interrupt Option I/O register 14A, Read/Write a Data Direction

I/O register 14B, Read/Write a Port I/O register 14C and Read a Latched I/O Port register 14D. The Authentication Challenge command (write) is followed by six data bytes (a 48-bit challenge word is presently preferred to input to the Authentication block 16), while the Authentication Response command is followed by three data bytes (a 24-bit response word is presently preferred to output from the Authentication block 16). The R/W I/O register commands are all followed by a single byte, as these registers are, in the current embodiment, one byte in width. For a write to I/O register operation the data byte is sourced from the mobile terminal 30. For a read access of an I/O register 14 the mobile terminal 30 sends the appropriate command byte on the data signal line 10A for specifying the I/O register to be read from, and the ACI ASIC 10 responds on the data signal line 10A with the data byte read from the specified I/O register location. The returned data byte is prefaced with the Learning Sequence (see Fig. 3E) that specifies the bit time T. Note as well that for a read of the EEPROM 18 the first byte returned from the ACI ASIC 10 is prefaced with the Learning Sequence, and the specified bit time T applies to the bits of the first returned data byte and any other returned bytes for that read operation. The same Learning Sequence operation is used for the first returned byte of the Authentication Response command, and the bit timing applies as well to the following two bytes of the three byte Authentication Response return. In this way the control logic block 12 is enabled to inform the data bit reading logic of the mobile terminal 10 of the duration of the bit time T for the impending data transfer, and the data bit reading logic is enabled to adjust the T/2 timing of its sampling of the data signal line 10A accordingly, thereby ensuring accurate reading of the transferred bits.

When an input mode is programmed for a given I/O pin 10B the pin state can be read from the I/O data register 14C. An internal pull-up resistor is preferably supplied for the I/O pins. If the interrupt enable bit is set from the Interrupt Option register 14A, and a state change in the I/O input pin occurs, the ACI ASIC 10 generates the Interrupt pulse to the data signal line 10A (see Fig. 3F). If a delay enable bit is set in the Interrupt Option register 14A, and the change of state occurs on the I/O pin, the ACI ASIC 10 instead latches the I/O pin input states to the Latched I/O Port register 14D after a delay (preferably about 20 milliseconds), and then generates the Interrupt pulse to the data signal line 10A. This mode of operation is useful, as an example, for debouncing accessory 20 switch contact closures.

Note in Fig. 3C that between two data transfer active modes is a mobile terminal sleep mode. Each active period can include a Command byte (read or write) and at least one data byte. The bit timing in the ACI ASIC 10 is preferably 30 clock cycles of the RC oscillator 19, which is possible to be read using the timing of the sleep clock (e.g., 32kHz) of the mobile terminal 30. At the beginning of communication the mobile terminal 30 sends a Reset pulse (Fig. 3D) to the ACI ASIC 10 on the data signal line 10A, and the ACI ASIC 10 responds with the one bit Learning Sequence (Fig. 3E), enabling the mobile terminal 30 to adapt its bit receive timing (based on the 32 kHz sleep clock). In view of this adaptive bit serial timing arrangement between the mobile terminal 30 and the ACI ASIC 10 it can be appreciated that tight timing tolerances are not required between the mobile terminal 30 and the number of possible accessories 20 that it may operate with.

Reference with regard to radiotelephone operation with a sleep clock can be had to the following exemplary commonly-assigned U.S. Patents: 5,870,683; 5,758,278; 5,752,201; and 5,471,655, incorporated by reference herein insofar as there is no conflict with the teachings of this invention.

The memory 18 preferably stores data descriptive of the features of the accessory 20. As an example, and assuming the headset accessory, there may be a one row display having 15 characters and four user-controlled switches or buttons, such as Answer/Call, Volume Up and Volume Down. Other stored parameters can include audio parameters such as echo cancellation on/off, gains and equalizations. All of this information can be communicated between the accessory 20 and the mobile terminal 30, enabling the mobile terminal 30 to configure and operate with a wide range of accessories, including accessories that are released for sale after the mobile terminal 30 is placed into service.

The use of the single bit serial data line 10A is also an advantage that accrues from the use of this invention, as this one signal line can be used for transferring data bidirectionally between the mobile terminal 30 and the accessory 20 containing the ACI ASIC 10, as well as for accessory insertion and removal detection, as well as for the adaptation of bit timing, reset and interrupt signalling.

While described in the context of the accessory 20 and ACI ASIC 10 being connected to the mobile terminal 30, it should be realized that the ACI ASIC 10 could be interfaced with other types of devices, such as a portable computer device, or a pager, or a PDA, or a home electronics device (including a game console), or any type of device that can
5 be used with an attachable accessory device. In any of these embodiments the controlling device may be simply referred to as a master device, and the ACI ASIC 10 and the associated accessory as a slave device.

The teachings of this invention are also not intended to be limited in scope by, as
10 examples, any of the specific frequencies, time periods, numbers of bits, numbers of bytes, types of commands, numbers of signal lines or registers and so forth that were discussed above. The ACI device is also not constrained to being implemented as an ASIC, as any suitable type of single chip or multiple chip integrated circuit embodiment can be used. In addition, the various blocks can be implemented in a number of suitable
15 ways. For example, the control logic 12 could be implemented as combinatorial logic circuits, or as a state machine, or as a suitably programmed microprocessor core. The oscillator 19 could be implemented using discrete resistor and capacitor components, or it could be implemented using a crystal or a resonator or any suitable frequency signal generator.

20

Thus, while the foregoing discussion is has been made in the context of presently preferred embodiments of this invention, these presently preferred embodiments are not intended to be read as limiting the scope or the practice of this invention to only these
25 embodiments.

CLAIMS

What is claimed is:

1. An interface between a master device and a slave device, said interface comprising a bit serial bidirectional signal line for conveying commands and associated data from said master device to said slave device, said bit serial bidirectional signal line further conveying other signals, said other signals comprising a reset signal, an interrupt signal, and a learning sequence signal for specifying a duration of a bit time for data transferred from said slave device to said master device.
2. An interface as in claim 1, where said master device is comprised of a personal digital assistant.
3. An interface as in claim 1, where said master device is comprised of a mobile terminal.
4. An interface as in claim 3, where said mobile terminal samples the data transferred from said slave device to said master device at a rate established by a mobile terminal sleep clock.
5. An interface as in claim 1, where said interface comprises, in said slave device, an Accessory Control Interface chip and an oscillator providing a clock signal to said Accessory Control Interface chip, where the bit time is a multiple of the clock signal, and where said master device adapts the sampling of the data transferred from said slave device in accordance with the specified duration of the bit time.
6. An interface as in claim 1, where said interface comprises, in said slave device, an Accessory Control Interface chip and a non-volatile memory for storing slave device related feature data that is readable by said master device over said bit serial bidirectional signal line in response to a memory read command sent from said master device to said Accessory Control Interface chip over said bit serial bidirectional signal line.
7. An interface as in claim 1, where said interface comprises, in said slave device, an

Accessory Control Interface chip and a challenge/response authentication function that is challenged in response to an authentication challenge command and associated challenge data sent from said master device to said Accessory Control Interface chip over said bit serial bidirectional signal line, and where authentication result data is sent by said Accessory Control Interface chip to said master device over said bit serial bidirectional signal line in response to an authentication result command sent from said master device to said Accessory Control Interface chip over said bit serial bidirectional signal line.

8. An interface as in claim 1, where said bit serial bidirectional signal line further conveys a slave device connected/disconnected state to said master device.

9. An interface circuit for coupling a slave device to a master device, said interface circuit supporting a bit serial bidirectional signal line that conveys commands and associated data from said master device to said slave device, said bit serial bidirectional signal line further conveying other signals, said other signals comprising a reset signal, an interrupt signal, and a learning sequence signal for specifying a duration of a bit time for data transferred from said slave device to said master device.

10. An interface circuit as in claim 9, where said interface circuit is disposed within said slave device and comprises an oscillator for generating a clock signal, where the bit time is a multiple of the clock signal period, and where said master device samples said bit serial bidirectional signal line in accordance with the specified duration of the bit time.

11. An interface circuit as in claim 9, where said interface circuit is disposed within said slave device and comprises a non-volatile memory for storing slave device related feature data that is readable by said master device over said bit serial bidirectional signal line in response to a read command sent from said master device to said interface circuit over said bit serial bidirectional signal line.

12. An interface circuit as in claim 9, where said interface circuit is disposed within said slave device and comprises a challenge/response authentication function that is challenged in response to an authentication challenge command and associated challenge data received from said master device over said bit serial bidirectional signal line, and

where authentication result data is sent to said master device over said bit serial bidirectional signal line in response to receiving an authentication result command from said master device over said bit serial bidirectional signal line.

13. An interface circuit as in claim 9, where said bit serial bidirectional signal line further conveys a slave device connected/disconnected state to said master device.

14. An interface circuit as in claim 9, where said master device is comprised of a mobile terminal.

15. An interface circuit as in claim 14, where said mobile terminal samples said bit serial bidirectional signal line at a rate established by a mobile terminal sleep clock.

16. An interface circuit as in claim 9, where said master device is comprised of a personal digital assistant.

17. An interface circuit for coupling a slave device to a master device, said interface circuit being disposed in said slave device and supporting a bit serial bidirectional signal line that conveys commands and associated data from said master device to said slave device, said bit serial bidirectional signal line further conveying other signals, said other signals comprising a reset signal.

18. An interface circuit as in claim 17, where said other signals further comprise an interrupt signal and a learning sequence signal for specifying a duration of a bit time for data transferred from said slave device to said master device.

19. An interface circuit for coupling a slave device to a master device, said interface circuit being disposed in said slave device and supporting a bit serial bidirectional signal line that conveys commands and associated data from said master device to said slave device, said bit serial bidirectional signal line further conveying other signals, said other signals comprising an interrupt signal.

20. An interface circuit as in claim 19, where said other signals further comprise a reset

signal and a learning sequence signal for specifying a duration of a bit time for data transferred from said slave device to said master device.

21. An interface circuit for coupling a slave device to a master device, said interface circuit being disposed in said slave device and supporting a bit serial bidirectional signal line that conveys commands and associated data from said master device to said slave device, said bit serial bidirectional signal line further conveying other signals, said other signals comprising a learning sequence signal for specifying a duration of a bit time for data transferred from said slave device to said master device.

22. An interface circuit as in claim 21, where said interface circuit comprises an oscillator for generating a clock signal, where the duration of the bit time is a multiple of the clock signal period, and where said master device samples said bit serial bidirectional signal line in accordance with the specified duration of the bit time.

23. An interface circuit as in claim 22, where a logic zero and a logic one are distinguished by a presence or absence of a transition occurring on said bit serial bidirectional signal line by a predetermined point in the specified duration of the bit time.

24. An interface circuit as in claim 23, where the specified duration of the bit time is given by T , and where the predetermined point is about $T/2$.

25. An interface circuit as in claim 21, where said interface circuit comprises at least one register that is readable by said master device over said bit serial bidirectional signal line.

26. An interface circuit as in claim 21, where said interface circuit comprises at least one register that is writable by said master device over said bit serial bidirectional signal line.

27. An interface circuit as in claim 21, where said interface circuit comprises at least one memory device location that is readable by said master device over said bit serial bidirectional signal line.

28. An interface circuit as in claim 21, where said interface circuit comprises at least one

memory device location that is writable by said master device over said bit serial bidirectional signal line.

29. An interface circuit as in claim 21, where said interface circuit comprises an authentication block that is addressable by commands sent by said master device over said bit serial bidirectional signal line, and that responds to at least one command with response data sent to said master device over said bit serial bidirectional signal line.

30. An interface circuit as in claim 21, where said other signals further comprise a reset signal and an interrupt signal.

31. A method for communicating between a master device and a slave device, comprising:

coupling the slave device to the master device through an interface, the interface comprising a bit serial bidirectional signal line;

sending a reset signal from the master device to the slave device over the bit serial bidirectional signal line;

sending a learning sequence signal to the master device over the bit serial bidirectional signal line for specifying a duration of a bit time for data transferred between the master device and the slave device; and

communicating at least one of data and commands between the master device and the slave device over the bit serial bidirectional signal line.

32. A method as in claim 31, where communicating comprises the master device sampling the bit serial bidirectional signal line in accordance with the specified duration of the bit time.

33. A method as in claim 32, where a logic zero and a logic one are distinguished by a presence or absence of a transition occurring on the bit serial bidirectional signal line by

a predetermined point in the specified duration of the bit time.

34. A method as in claim 33, where the specified duration of the bit time is given by T , and where the predetermined point is about $T/2$.

1/5

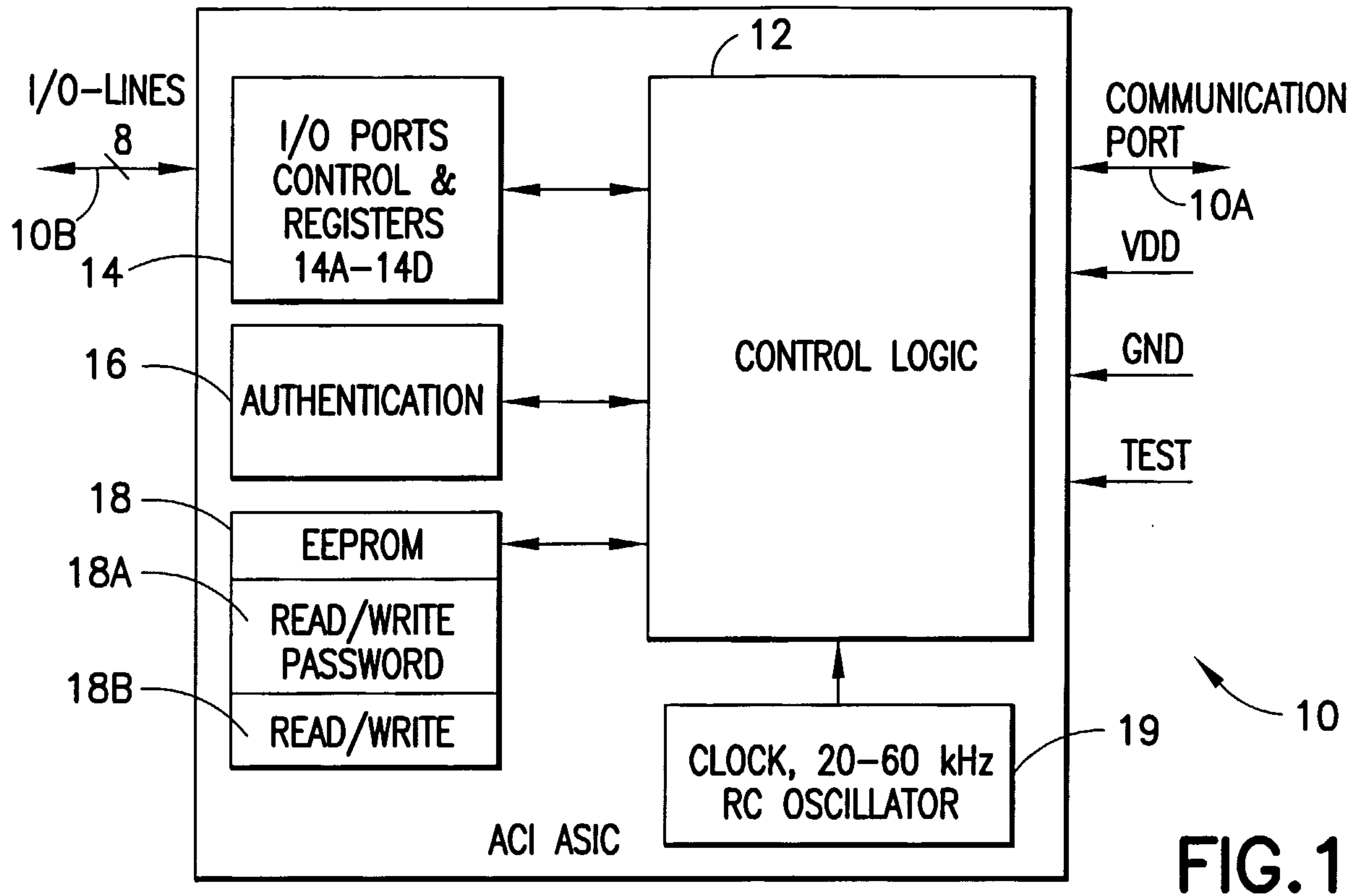


FIG. 1

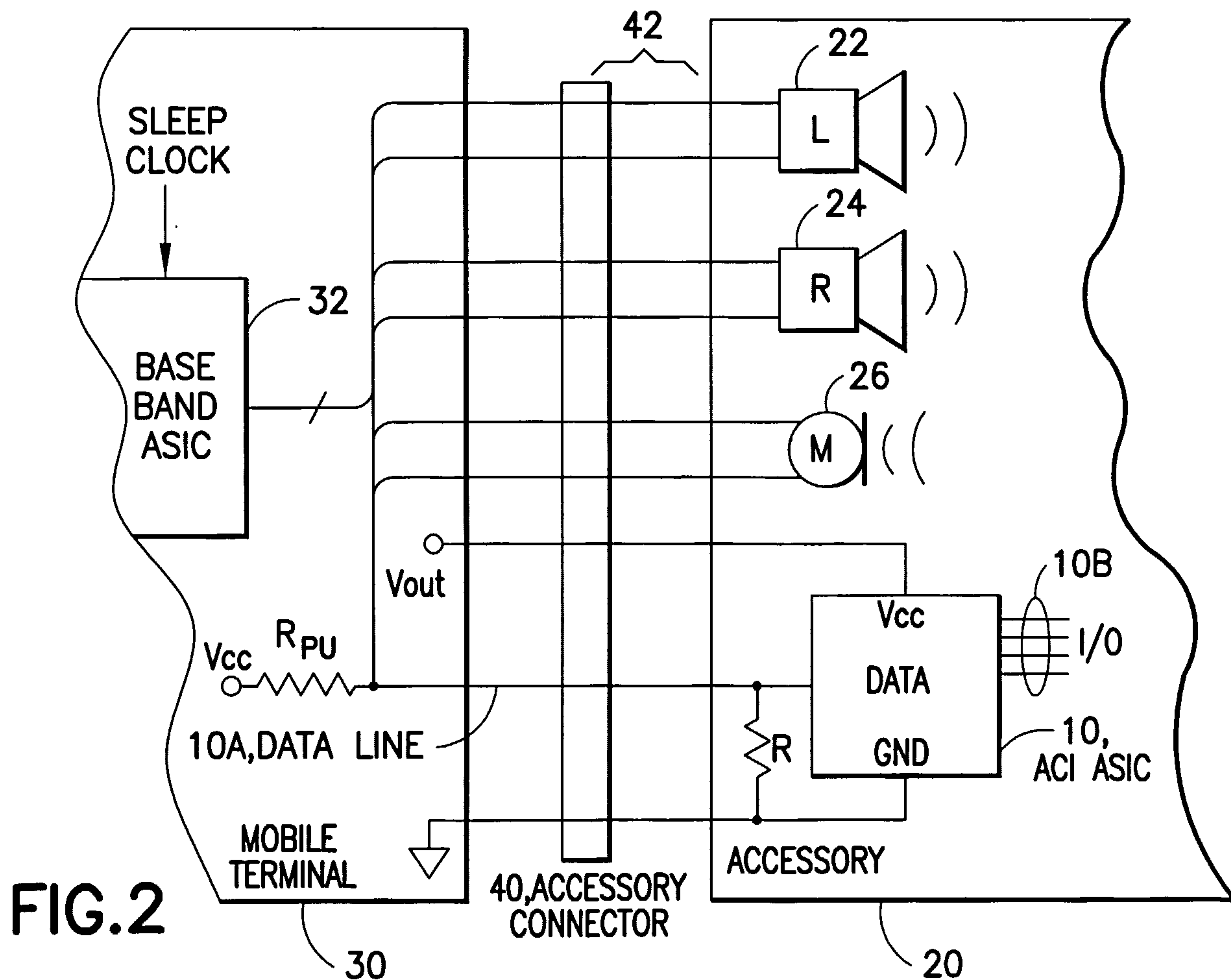
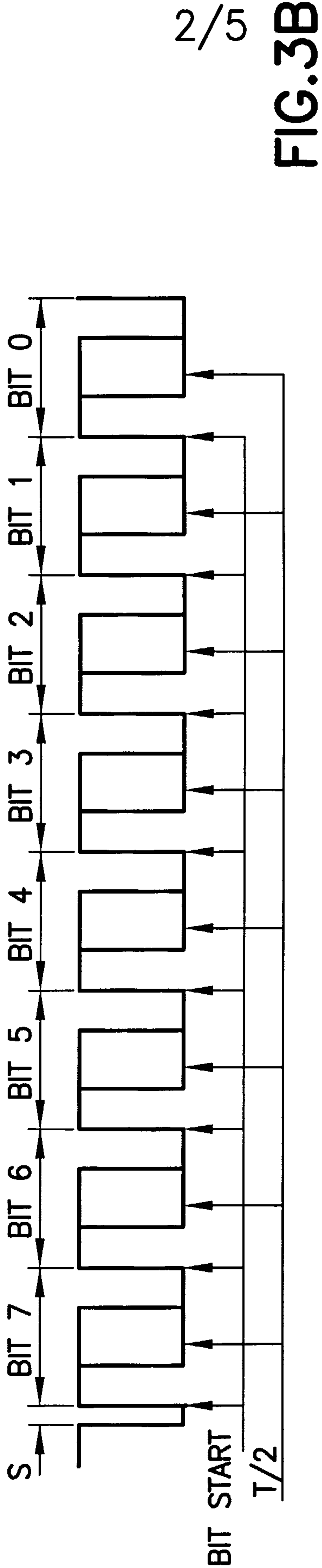
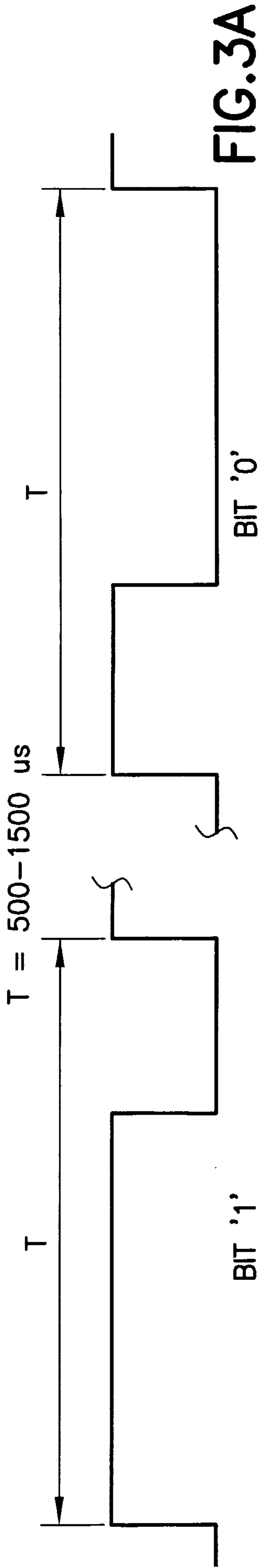
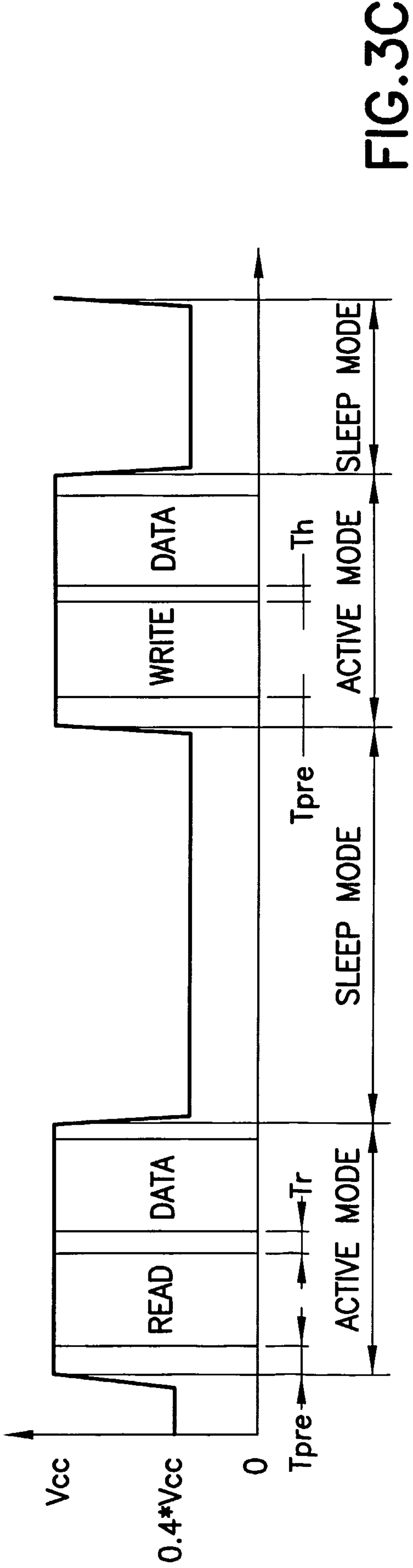


FIG. 2



2/5



3/5

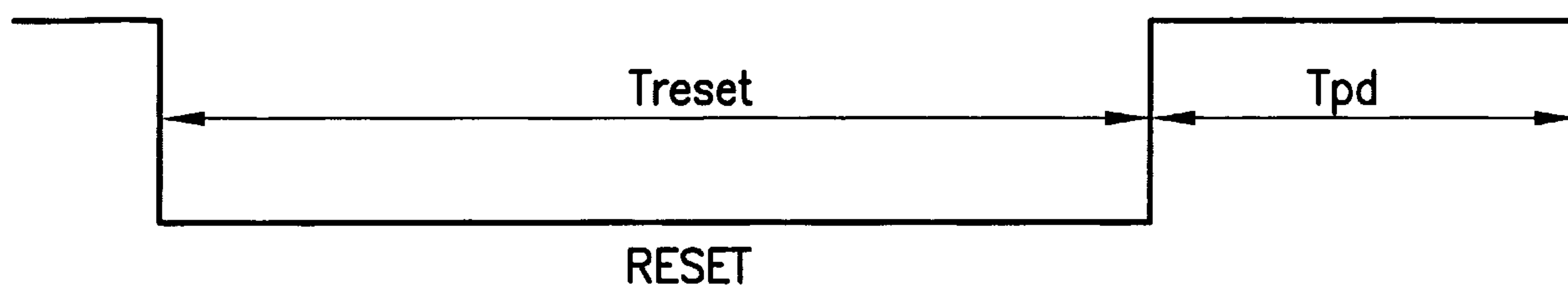


FIG.3D

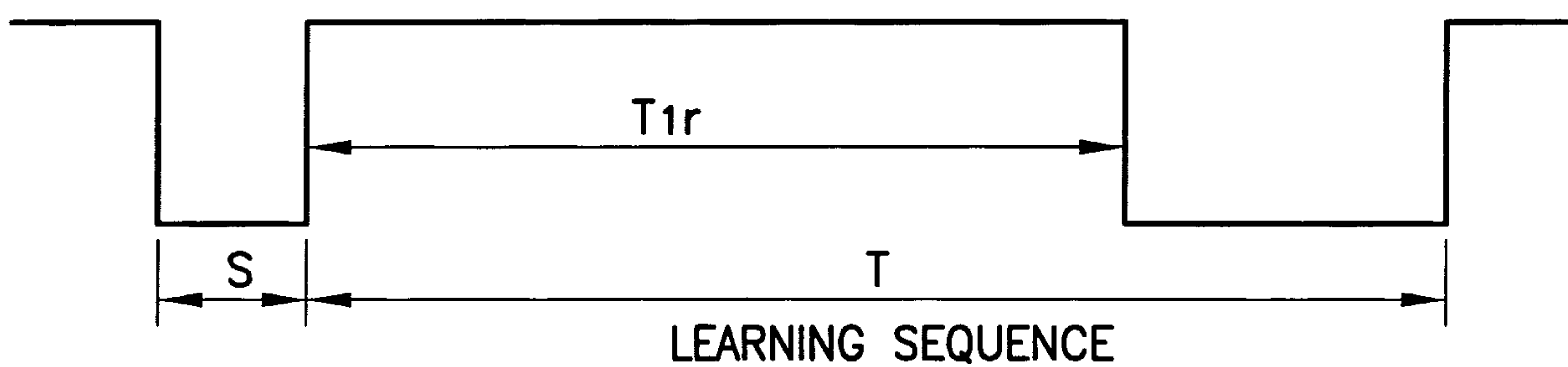


FIG.3E

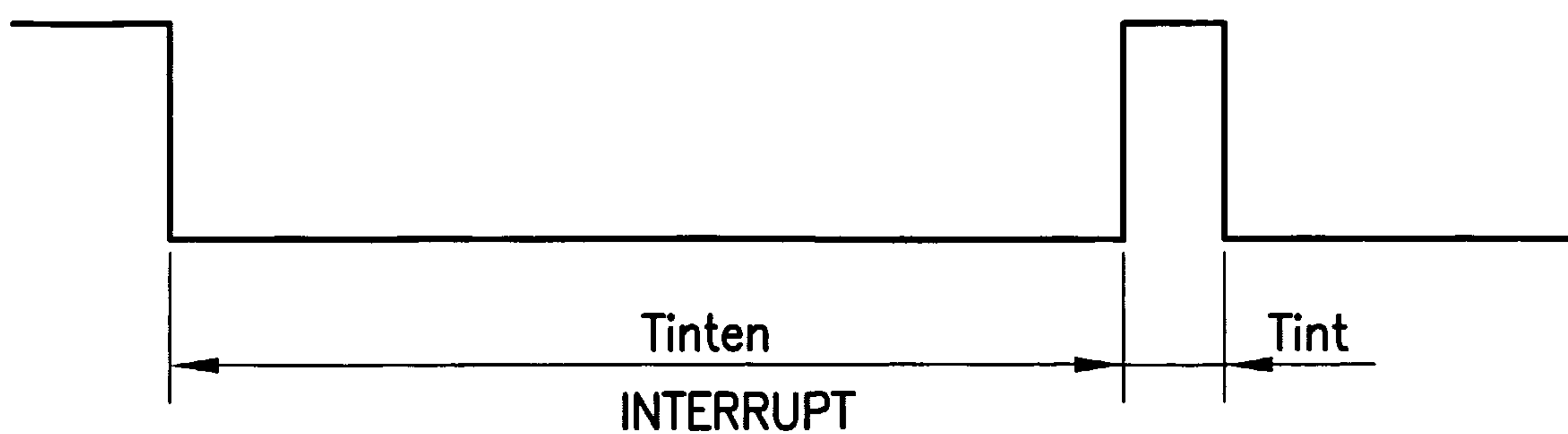


FIG.3F

FIG.4

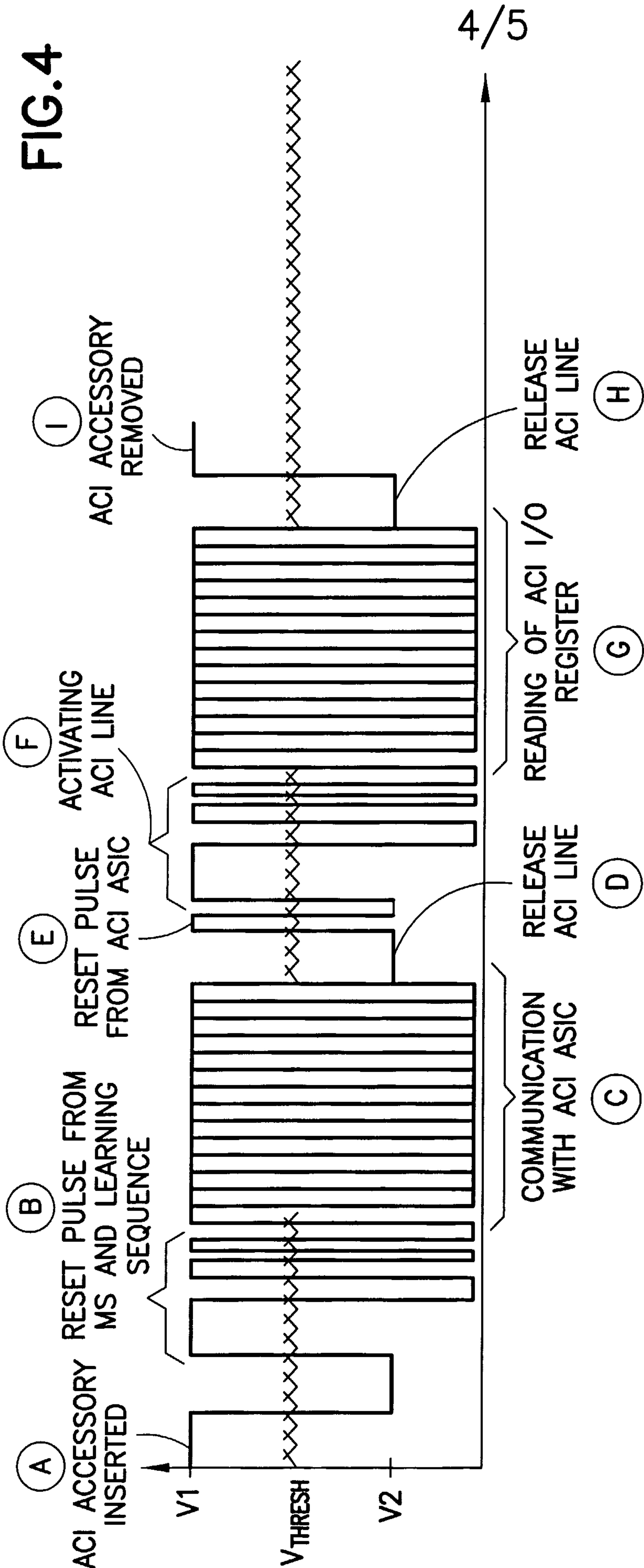
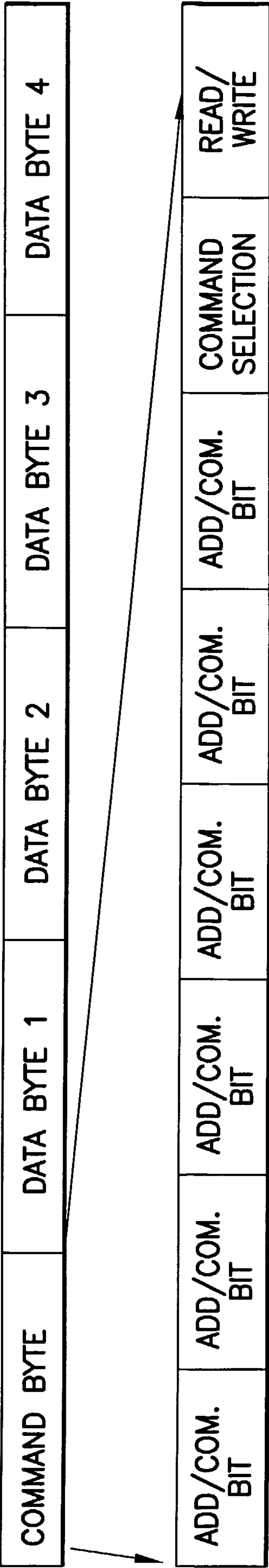


FIG.5



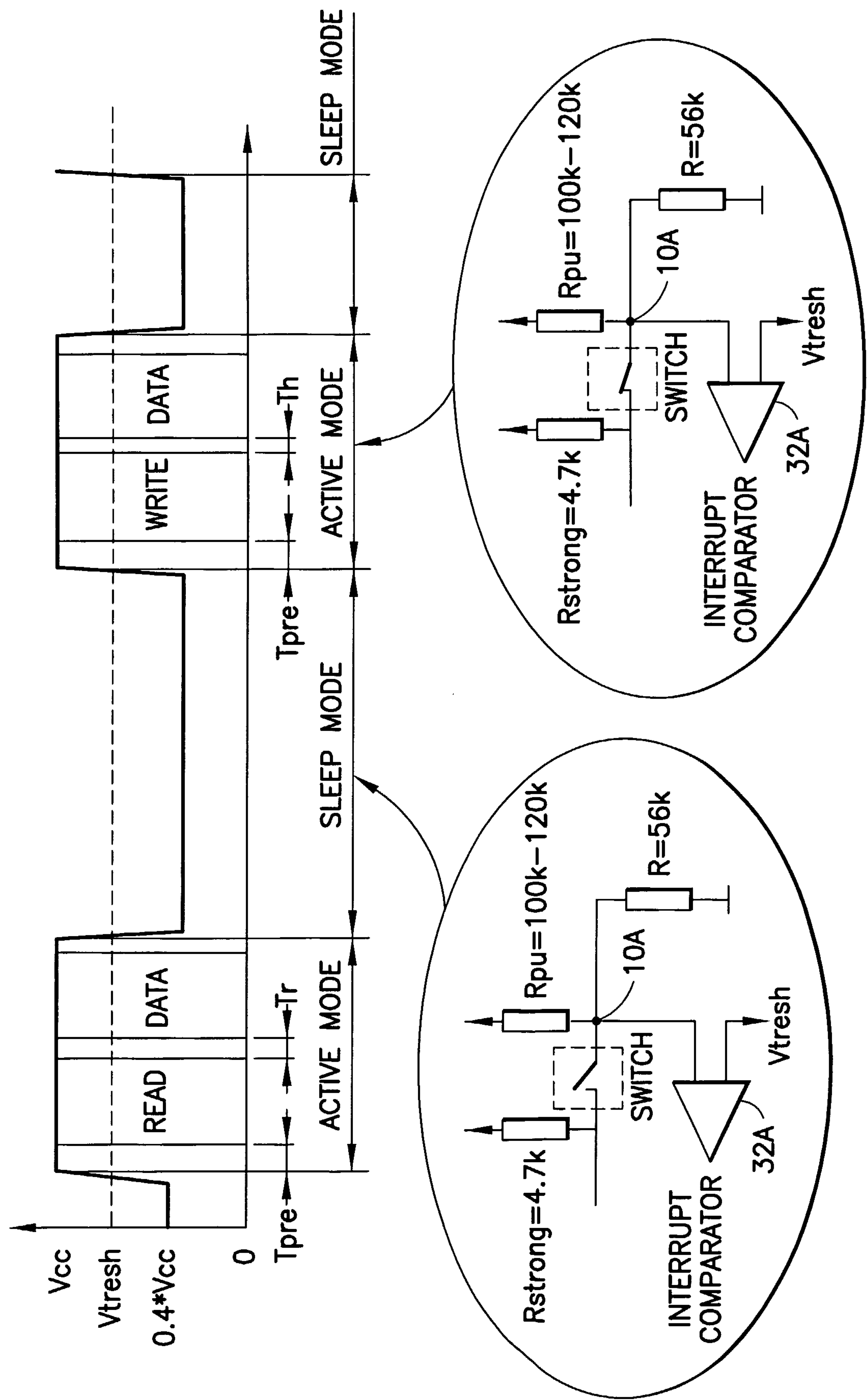


FIG. 6

