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(54) Title: VERTICAL FIELD-EFFECT TRANSISTOR DEVICE HAVING A BYPASS DIODE

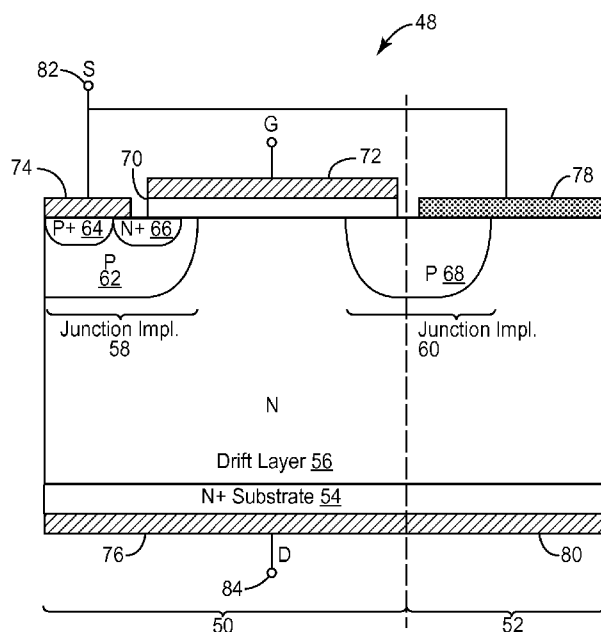


FIG. 7

(57) Abstract: A semiconductor device (48) includes a vertical field-effect transistor device (50) and a bypass diode (52) such as a Schottky bypass diode. The transistor includes a gate contact (72), a source contact (74), and a drain contact (76). The gate contact and the source contact are separated from the drain contact by at least a drift layer (56). The bypass diode is coupled between the source contact and the drain contact and monolithically integrated adjacent to the transistor such that a voltage placed between the source contact and the drain contact is distributed throughout the drift layer by the bypass diode in such a way that a voltage across each one of a plurality of P-N junctions formed between the source contact and the drain contact by junction implants (58, 60, 112, 114) within the transistor is prevented from exceeding a barrier voltage of the respective P-N junction.



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VERTICAL FIELD-EFFECT TRANSISTOR DEVICE HAVING A BYPASS DIODEField of the Disclosure

5 **[0001]** The present disclosure relates to power transistors including a bypass diode.

Background

10 **[0002]** Power transistor devices are often used to transport large currents and support high voltages. One example of a power transistor device is the power metal-oxide-semiconductor field-effect transistor (MOSFET). A power MOSFET has a vertical structure, wherein a source contact and a gate contact are located on a first surface of the MOSFET device that is separated from a drain contact by a drift layer formed on a substrate. Vertical MOSFETs are sometimes referred to
15 as vertical diffused MOSFETs (VDMOS) or double-diffused MOSFETs (DMOSFETs). Due to their vertical structure, the voltage rating of a power MOSFET is a function of the doping level and thickness of the drift layer. Accordingly, high voltage power MOSFETs may be achieved with a relatively small footprint.

20 **[0003]** Figure 1 shows a conventional power MOSFET device 10. The conventional power MOSFET device 10 includes an N-doped substrate 12, an N-doped drift layer 14 formed over the substrate 12, one or more junction implants 16 in the surface of the drift layer 14 opposite the substrate 12, and an N-doped junction gate field-effect transistor (JFET) region 18 between each one of the
25 junction implants 16. Each one of the junction implants 16 is formed by an ion implantation process, and includes a P-doped deep well region 20, a P-doped base region 22, and an N-doped source region 24. Each deep well region 20 extends from a corner of the drift layer 14 opposite the substrate 12 downwards towards the substrate 12 and inwards towards the center of the drift layer 14.
30 The deep well region 20 may be formed uniformly or include one or more protruding regions. Each base region 22 is formed in a shallow portion on the

surface of the drift layer 14 opposite the substrate 12 within the boundaries of the deep well region 20. Each source region 24 is formed adjacent to the base region 22 in a shallow portion on the surface of the drift layer 14 opposite the substrate 12 within the boundaries of the deep well region 20. The JFET region 18 defines a channel width between each one of the junction implants 16.

[0004] A gate oxide layer 26 is positioned on the surface of the drift layer 14 opposite the substrate 12, and extends laterally between a portion of the surface of each source region 24, such that the gate oxide layer 26 partially overlaps and runs between the surface of each source region 24 in the junction implants 16. A

gate contact 28 is positioned on top of the gate oxide layer 26. Two source contacts 30 are each positioned on the surface of the drift layer 14 opposite the substrate 12 such that each one of the source contacts 30 partially overlaps both the source region 24 and the deep well region 20 of one of the junction implants 16, respectively, and does not contact the gate oxide layer 26 or the gate contact 28. A drain contact 32 is located on the surface of the substrate 12 opposite the drift layer 14.

[0005] In operation, when a biasing voltage below the threshold voltage of the device is applied to the gate contact 28, and the P-N junction formed between each deep well region 20 and the drift layer 14 is reverse biased, the

conventional power MOSFET device 10 is placed in an OFF state. In the OFF state of the conventional power MOSFET device 10, any voltage between the source and the drain contact is supported by the drift layer 14. Due to the vertical structure of the conventional power MOSFET device 10, large voltages may be placed between the source contacts 30 and the drain contact 32 without damaging the device.

[0006] Figure 2 shows a three-dimensional representation of the conventional power MOSFET device 10 shown in Figure 1. As shown in Figure 2, the conventional power MOSFET device 10 is rectangular, essentially extending the two-dimensional representation shown in Figure 1 into the page. As will be appreciated by those of ordinary skill in the art, the conventional power MOSFET device 10 may be tiled into or out of the page to form a conventional power

MOSFET “stripe” including a plurality of conventional power MOSFET devices 10 connected in series. Further, additional power MOSFET devices may be laterally tiled with the conventional power MOSFET device 10, as shown in Figure 3.

Figure 3 shows three conventional power MOSFET devices 10, each integrated

5 directly adjacent to one another and connected in series. As will be appreciated by those of ordinary skill in the art, each one of the conventional power MOSFET devices 10 may be tiled into or out of the page to form a plurality of conventional power MOSFET “stripes.” Arranging the conventional power MOSFET devices 10 in “stripes” allows a large number of conventional power MOSFET devices 10 to be integrated into a small area of semiconductor die, thereby saving space in a device in which the conventional power MOSFET devices 10 are integrated.

[0007] Figure 4A shows operation of the conventional power MOSFET device 10 when the device is in an ON state (first quadrant) of operation. When a positive voltage is applied to the drain contact 32 relative to the source contacts 15 30 and the gate voltage increases over the threshold voltage of the device, an inversion layer channel 34 is formed at the surface of the drift layer 14 underneath the gate contact 28, thereby placing the conventional power MOSFET device 10 in an ON state of operation. In the ON state of operation of the conventional power MOSFET device 10, current (shown by the shaded 20 region in Figure 4) is allowed to flow from the drain contact 32 to the source contacts 30 of the device. An electric field presented by junctions formed between the deep well region 20, the base region 22, and the drift layer 14 constricts current flow in the JFET region 18 into a JFET channel 36. At a certain spreading distance from the inversion layer channel 34 when the electric field 25 presented by the junction implants 16 is diminished, the flow of current is distributed laterally, or spread out in the drift layer 14.

[0008] Figure 4B shows operation of the conventional power MOSFET device 10 when the device is operating in the third quadrant. When a voltage below the threshold voltage of the device is applied to the gate contact 28 of the 30 conventional power MOSFET device 10 and a positive voltage is applied to the source contacts 30 relative to the drain contact 32 of the device, current will flow

from the source contacts through each respective base region 22 and deep well region 20 and into the drift layer 14.

[0009] As current flows from the deep well region 20 into the drift layer 14 of the conventional power MOSFET device 10 while the device is operating in the third quadrant, stacking faults may occur. Stacking faults occur as a result of basal plane dislocations (BPDs) present in the drift layer 14 due to imperfections in the semiconductor materials and/or manufacturing defects. As current runs through one or more BPDs in the drift layer 14, the crystalline structure of the semiconductor material may be altered, thereby creating one or more stacking faults. The stacking faults may substantially degrade the performance of the conventional power MOSFET device 10. For example, the stacking faults may cause the resistance of one or more areas in the drift layer 14 of the conventional power MOSFET device 10 to increase substantially.

[0010] One possible way to prevent stacking faults in the conventional power MOSFET device 10 is with more stringent manufacturing or testing of each conventional power MOSFET device 10 to reduce or eliminate BPDs. However, such manufacturing or testing procedures are often impractical or impossible, due to cost or difficulty.

[0011] An additional way to prevent stacking faults in the conventional power MOSFET device 10 is by placing an external bypass diode between the source contacts 30 and the drain contact 32 of the conventional power MOSFET device 10. Figure 5 shows the conventional power MOSFET device 10 connected to an external bypass diode 40. As will be appreciated by those of ordinary skill in the art, the external bypass diode 40 may be chosen to be a Schottky diode, because of the low barrier voltage afforded by such a device. The external bypass diode 40 includes an anode 42, a cathode 44, and a drift layer 46. The anode 42 of the external bypass diode 40 is coupled to the source contacts 30 of the conventional power MOSFET device 10. The cathode 44 of the external bypass diode 40 is coupled to the drain contact 32 of the conventional power MOSFET device 10. The anode 42 and the cathode 44 are separated from one another by the drift layer 46.

[0012] When a bias voltage below the threshold voltage of the conventional power MOSFET device 10 is applied to the gate contact 28 of the device, and the junction between each deep well region 20 and the drift layer 14 is reverse biased, the conventional power MOSFET device 10 is placed in an OFF state and the external bypass diode 40 is placed in a reverse bias mode of operation. In the reverse bias mode of operation of the external bypass diode 40, current does not flow through the device.

[0013] Figure 6A shows operation of the conventional power MOSFET device 10 including the external bypass diode 40 when the conventional power

MOSFET device 10 is operating in on ON state (first quadrant) of operation.

When a positive voltage is applied to the drain contact 32 relative to the source contacts 30 and the gate voltage increases over the threshold voltage of the device, the conventional power MOSFET is placed in an ON state (first quadrant) of operation, and the external bypass diode 40 is placed in a reverse bias mode of operation. In the ON state (first quadrant) of operation of the conventional power MOSFET device 10, current is allowed to flow between the drain contact 32 and the source contacts 30 of the device. As a result of the respective electric fields presented by the deep well regions 20, the current is constricted into a JFET channel. At a certain vertical distance when the electric fields presented by the deep well regions 20 become less pronounced, the current laterally spreads to fill the drift layer 14. Because the external bypass diode 40 is reverse biased, current does not flow from through the device.

[0014] Figure 6B shows operation of the conventional power MOSFET device 10 including the external bypass diode 40 when the conventional power

MOSFET device 10 is operating in the third quadrant. When a voltage below the threshold voltage of the conventional power MOSFET device 10 is applied to the gate contact 28 and a positive voltage is applied to the source contacts 30, the conventional power MOSFET device 10 begins to operate in the third quadrant, while the external bypass diode 40 is placed in a forward bias mode of operation.

In the forward bias mode of operation of the external bypass diode 40, current (shown by the shaded region in Figure 6) flows from the anode 42 into the drift

layer 46, where it is delivered to the cathode 44 of the external bypass diode 40. Although the external bypass diode 40 creates a low impedance path for current flow between the source contacts 30 and the drain contact 32, a small amount of current may still flow through each one of the deep well regions 20 and into the drift layer 14 of the conventional power MOSFET device 10. This may be due at least in part to the inductance associated with the connections between the external bypass diode 40 and the conventional power MOSFET device 10 and the packaging of the external bypass diode 40.

[0015] By creating a high-speed, low-impedance path for current flow around the drift layer 14 of the conventional power MOSFET device 10, the overall current through the drift layer 14 can be substantially reduced. However, even a small amount of current flow in the drift layer 14 while the conventional power MOSFET device 10 is operating in the third quadrant may generate stacking faults over a long enough period of time, thereby significantly degrading the performance of the device. Although the area of the external bypass diode 40 can be increased in an attempt to prevent current flow through the P-N junctions in the conventional power MOSFET device 10 altogether, the area required by the external bypass diode 40 for such a solution is impractical for most applications.

[0016] Accordingly, there is a need for a power MOSFET device including a bypass diode that effectively prevents current flow through the drift layer of the power MOSFET device, while minimizing the total area of the device.

Summary

[0017] The present disclosure relates to a semiconductor device including a vertical field-effect transistor (FET) device and a bypass diode for preventing current flow through one or more P-N junctions formed within the vertical FET device. According to one embodiment, the semiconductor device includes the vertical FET device and the bypass diode. The vertical FET device includes a gate contact, a source contact, and a drain contact. The gate contact and the source contact are separated from the drain contact by at least a drift layer. The

bypass diode is coupled between the source contact and the drain contact and monolithically integrated adjacent to the vertical FET device such that a voltage placed between the source contact and the drain contact is distributed throughout the drift layer by the bypass diode in such a way that a voltage across each P-N junction formed between the source contact and the drain contact within the vertical FET device is prevented from exceeding the barrier voltage of the respective P-N junction. By integrating the bypass diode in such a way, current flow through each P-N junction formed between the source contact and the drain contact of the vertical FET device is effectively diverted through the bypass diode, thereby preventing the formation of stacking faults and improving the longevity and performance of the vertical FET device.

[0018] According to one embodiment, the bypass diode is a Schottky diode formed by placing a Schottky metal in contact with the drift layer.

[0019] According to an additional embodiment, the distance between the bypass diode and the furthest edge of a P-N junction formed between the source contact and the drain contact of the vertical FET device does not exceed 15 microns.

[0020] Those skilled in the art will appreciate the scope of the disclosure and realize additional aspects thereof after reading the following detailed description in association with the accompanying drawings.

Brief Description of the Drawings

[0021] The accompanying drawings incorporated in and forming a part of this specification illustrate several aspects of the disclosure, and together with the description serve to explain the principles of the disclosure.

[0022] Figure 1 shows a schematic representation of a conventional power metal-oxide-semiconductor field-effect transistor (MOSFET) device.

[0023] Figure 2 shows a three-dimensional representation of the conventional power MOSFET device shown in Figure 1.

[0024] Figure 3 shows a plurality of conventional power MOSFET devices integrated adjacent to one another in order to form a plurality of MOSFET “stripes.”

[0025] Figure 4A shows details of the operation of the conventional power MOSFET device shown in Figure 1 when the device is in an ON state (first quadrant) of operation.

[0026] Figure 4B shows details of the operation of the conventional power MOSFET device shown in Figure 1 when the device is operating in the third quadrant.

[0027] Figure 5 shows a schematic representation of the conventional power MOSFET device shown in Figure 1 attached to an external bypass diode.

[0028] Figure 6A shows details of the operation of the conventional power MOSFET device and attached external bypass diode when the device is in an ON state (first quadrant) of operation.

[0029] Figure 6B shows details of the operation of the conventional power MOSFET device and attached external bypass diode when the device is operating in the third quadrant.

[0030] Figure 7 shows a schematic representation of a vertical field-effect transistor (FET) device and bypass diode according to one embodiment of the present disclosure.

[0031] Figure 8 shows details of the vertical FET device shown in Figure 5 according to one embodiment of the present disclosure.

[0032] Figure 9A shows details of the operation of the vertical FET device shown in Figure 5 according to one embodiment of the present disclosure.

[0033] Figure 9B shows details of the operation of the vertical FET device shown in Figure 5 according to one embodiment of the present disclosure.

[0034] Figure 10 is a graph illustrating the voltage and current (V-I) characteristics of the vertical FET device shown in Figure 5 according to one embodiment of the present disclosure.

[0035] Figure 11 shows a schematic representation of the vertical FET device and bypass diode according to an additional embodiment of the present disclosure.

[0036] Figure 12 shows a three-dimensional representation of the vertical FET device and bypass diode according to one embodiment of the present disclosure.

[0037] Figure 13 shows a three-dimensional representation of the vertical FET device and bypass diode according to an additional embodiment of the present disclosure.

[0038] Figures 14A and 14B show a three-dimensional representation of the vertical FET device and bypass diodes according to an additional embodiment of the present disclosure.

[0039] Figures 15A-15E illustrate a process for manufacturing the vertical FET device and bypass diodes shown in Figures 14A and 14B.

[0040] Figure 16 is a diagram showing the process for manufacturing the vertical FET device and bypass diodes shown in Figures 15A-15E.

Detailed Description

[0041] The embodiments set forth below represent the necessary information to enable those skilled in the art to practice the disclosure and illustrate the best mode of practicing the disclosure. Upon reading the following description in light of the accompanying drawings, those skilled in the art will understand the concepts of the disclosure and will recognize applications of these concepts not particularly addressed herein. It should be understood that these concepts and applications fall within the scope of the disclosure and the accompanying claims.

[0042] It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the present disclosure. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0043] Relative terms such as "below" or "above" or "upper" or "lower" or "horizontal" or "vertical" may be used herein to describe a relationship of one element, layer, or region to another element, layer, or region as illustrated in the Figures. It will be understood that these terms and those discussed above are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures.

[0044] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the disclosure. As used herein, the singular forms "a," "an," and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises," "comprising," "includes," and/or "including" when used herein specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0045] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure belongs. It will be further understood that terms used herein should be interpreted as having a meaning that is consistent with their meaning in the context of this specification and the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0046] Turning now to Figure 7, a semiconductor device 48 is shown including a vertical field-effect transistor (FET) device 50 and a monolithically integrated bypass diode 52 according to one embodiment of the present disclosure. The vertical FET device 50 may be a metal-oxide-semiconductor field-effect transistor (MOSFET) half-cell including a substrate 54, a drift layer 56 formed over the substrate 54, a first junction implant 58 in the surface of the drift layer 56 opposite the substrate 54, and a second junction implant 60 laterally separated from the first junction implant 58 in the surface of the drift layer 56 opposite the substrate 54. The first junction implant 58 may be formed by an ion implantation

process, and includes a first deep well region 62, a first base region 64, and a first source region 66. The first deep well region 62 extends from a corner of the drift layer 56 opposite the substrate 54 downwards towards the substrate 54 and inwards towards the center of the drift layer 56. The first deep well region 62 may be formed uniformly or include one or more protruding regions. The first base region 64 is formed in a shallow portion on the surface of the drift layer 56 opposite the substrate within the boundaries of the first deep well region 62. The first source region 66 is formed adjacent to the first base region 64 in a shallow portion on the surface of the drift layer 56 opposite the substrate 54 within the boundaries of the first deep well region 62. The second junction implant 60 includes a second deep well region 68, which is laterally separated from the first deep well region 62 of the first junction implant 58 in the surface of the drift layer 56 opposite the substrate 54.

[0047] A gate oxide layer 70 is positioned on the surface of the drift layer 56 opposite the substrate 54, and extends laterally between a portion of the surface of the first source region 66 and a portion of the second deep well region 68, such that the gate oxide layer 70 partially overlaps and runs between the surface of the first source region 66 of the first junction implant 58 and the second deep well region 68 of the second junction implant 60. A gate contact 72 is positioned on top of the gate oxide layer 70. A source contact 74 is positioned on the surface of the drift layer 56 opposite the substrate 54, and extends laterally to overlap a portion of the first base region 64 and the first source region 66 of the first junction implant 58. A drain contact 76 is located on the surface of the substrate 54 opposite the drift layer 56.

[0048] The bypass diode 52 is formed adjacent to the vertical FET device 50 on the same semiconductor die. According to one embodiment, the bypass diode 52 is a Schottky diode including the substrate 54, the drift layer 56, at least a portion of the second deep well region 68, an anode 78, and a cathode 80. The anode 78 is located on the surface of the drift layer 56 opposite the substrate 54, such that the anode 78 partially overlaps a portion of the drift layer 56 and the second deep well region 68, without contacting the gate oxide layer 70 or the

gate contact 72 of the vertical FET device 50. The cathode 80 is joined with the drain contact 76 of the vertical FET device 50 on the surface of the substrate 54 opposite the drift layer 56. The anode 78 and the source contact 74 of the vertical FET device 50 may be electrically coupled to an input node 82. The cathode 80 and the drain contact 76 of the vertical FET device 50 may be coupled to an output node 84.

[0049] According to one embodiment, the bypass diode 52 is formed adjacent to the vertical FET device 50 such that the bypass diode 52 is between no more than about 5-15 microns from the furthest edge of the P-N junction formed

between the first deep well region 62 and the drift layer 56. As will be discussed in further detail below, by placing the bypass diode 52 in such close proximity to the P-N junction formed between the first deep well region 62 and the drift layer 56, the potential across this junction can be kept below the barrier voltage of the junction. That is, the P-N junction formed between the first deep well region 62 and the drift layer 56 can be prevented from entering a forward bias mode of operation. If the P-N junction formed between the first deep well region 62 and the drift layer 56 does not enter a forward bias mode of operation, current does not flow through the junction. Accordingly, stacking faults are not formed in the drift layer 56, thereby improving the performance and longevity of the device.

Further, placing the bypass diode 52 in this manner allows the area of the bypass diode 52 to be kept quite low when compared with conventional solutions, on the order of 1.0-10.0 microns², while still preventing the flow of current through the P-N junction formed between the first deep well region 62 and the drift layer 56.

[0050] The vertical FET device 50 may be, for example, a silicon carbide (SiC) device. Those of ordinary skill in the art will appreciate that the concepts of the present disclosure may be applied to any materials system. The substrate 54 may be about 50.0-500.0 microns thick. The drift layer 56 may be about 3.5-250.0 microns thick, depending upon the voltage rating of the vertical FET device 50. The first deep well region 62 and the second deep well region 68 may be about 1.0-2.0 microns thick. Further, the semiconductor device 48 may include any number of additional layers without departing from the principles of the

present disclosure. For example, the vertical FET device 50 may include a junction field-effect transistor (JFET) region between the first junction implant 58 and the second junction implant 60.

[0051] According to one embodiment, the substrate 54 is an N-doped layer with a doping concentration about $1 \times 10^{18} \text{ cm}^{-3}$ to $1 \times 10^{20} \text{ cm}^{-3}$. The drift layer 56 may be an N-doped layer with a doping concentration about $3 \times 10^{14} \text{ cm}^{-3}$ to $1.5 \times 10^{16} \text{ cm}^{-3}$. The first deep well region 62 and the second deep well region 68 may be heavily P-doped regions with a doping concentration about $5 \times 10^{17} \text{ cm}^{-3}$ to $1 \times 10^{20} \text{ cm}^{-3}$. The first base region 64 may be a P-doped region with a doping concentration about $5 \times 10^{16} \text{ cm}^{-3}$ to $1 \times 10^{19} \text{ cm}^{-3}$. The first source region 66 may be an N-doped region with a doping concentration about $1 \times 10^{19} \text{ cm}^{-3}$ to $1 \times 10^{21} \text{ cm}^{-3}$. The N-doping agent may be nitrogen, phosphorous, or any other suitable element or combination thereof, as will be appreciated by those of ordinary skill in the art. The P-doping agent may be aluminum, boron, or any other suitable element or combination thereof, as will be appreciated by those of ordinary skill in the art.

[0052] The gate contact 72, the source contact 74, the drain contact 76, and the cathode 80 may be comprised of multiple layers. For example, each one of the contacts may include a first layer of nickel or nickel-aluminum, a second layer of titanium over the first layer, a third layer of titanium-nickel over the second layer, and a fourth layer of aluminum over the third layer. The anode 78 may comprise titanium, tantalum, or any other suitable low-barrier Schottky metal. Those of ordinary skill in the art will appreciate that the gate contact 72, the source contact 74, the drain contact 76, the anode 78, and the cathode 80 may comprise any suitable material without departing from the principles of the present disclosure.

[0053] As will be appreciated by those of ordinary skill in the art, in certain applications the bypass diode 52 may be connected in opposite polarity, wherein the anode 78 is coupled to the drain contact 76 of the vertical FET device 50 and the cathode 80 is coupled to the source contact 74 of the vertical FET device 50.

This may occur, for example, when the vertical FET device 50 is a P-MOSFET device.

[0054] Figure 8 shows the semiconductor device 48 including a simplified circuit diagram representing electrical components within each of the vertical FET device 50 and the bypass diode 52. As shown in Figure 6, the vertical FET device 50 includes a P-N junction 86 formed by the junction between the first deep well region 62 and the drift layer 56, a Schottky diode 88 formed by the junction between the anode 78 of the bypass diode 52 and the drift layer 56, a first vertical drift resistor 90 representative of the vertical resistance of the drift layer 56 below the first deep well region 62, a lateral drift resistor 92 representative of the lateral resistance of the drift layer 56 between the bypass diode 52 and the furthest edge of the junction between the first deep well region 62 and the drift layer 56, and a second vertical drift resistor 94 representing the vertical resistance of the drift layer 56 in the bypass diode 52. As discussed above, the purpose of the bypass diode 52 is to prevent the P-N junction 86 from entering a forward bias mode of operation so that the vertical FET device 50 does not conduct current through the P-N junction 86. This is accomplished by maintaining the potential of the portion of the drift layer 56 below the first deep well region 62 at a level such that the barrier voltage of the P-N junction 86 is not exceeded.

[0055] As will be appreciated by those of ordinary skill in the art, the resistance of the lateral drift resistor 92 is dictated at least in part by the lateral distance between the bypass diode 52 and the furthest edge of the junction between the first deep well region 62 and the drift layer 56. Further, the resistance of the first vertical drift resistor 90 is dictated at least in part by the vertical distance between the bottom of the first deep well region 62 and the drain contact 76. Finally, the resistance of the second vertical drift resistor 94 is dictated at least in part by the vertical distance between the anode 78 and the cathode 80 of the bypass diode 52. The bypass diode 52 is placed such that the potential generated across the first vertical drift resistor 90 ensures that the P-N junction 86 does not enter a forward bias mode of operation. This is

accomplished by ensuring that the voltage difference between the potential presented at the source contact 74 and the potential across the vertical drift resistor is less than the barrier voltage of the P-N junction 86.

[0056] As will be appreciated by those of ordinary skill in the art, the first

5 vertical drift resistor 90 and the lateral drift resistor 92 form a voltage divider. As described above, the dimensions of the drift layer 56 will dictate the resistance of each one of the first vertical drift resistor 90 and the lateral drift resistor 92. By keeping the lateral distance between the bypass diode 52 and the furthest edge of the junction between the first deep well region 62 and the drift layer 56 low, the
10 majority of the voltage placed across the bypass diode 52 can be distributed across the first vertical drift resistor 90, thereby fixing the potential below the junction such that the P-N junction 86 does not enter a forward bias mode of operation. In one exemplary embodiment, the lateral distance between the bypass diode 52 and the furthest edge of the junction between the first deep well
15 region and the drift layer 56 is between about 5-15 microns.

[0057] Figure 9A shows operation of the semiconductor device 48 when the vertical FET device 50 is in an ON state (first quadrant) of operation and the bypass diode 52 is in a reverse bias state of operation. When a positive voltage is applied to the drain contact 76 of the vertical FET device 50 relative to the
20 source contact 74 and the gate voltage increases above the threshold voltage, the vertical FET device 50 is placed in an ON state (first quadrant) of operation. Further, the bypass diode 52 is placed in a reverse bias state of operation.

Accordingly, current is allowed to flow from the drain contact 76 to the source contact 74 of the device. An electric field presented by the junctions formed
25 between the first deep well region 62 and the drift layer 56 and the second deep well region and the drift layer 56, respectively, constrict current flow into a channel. At a certain vertical distance from the first deep well region 62 and the second deep well region 68 when the electric fields are diminished, current begins to laterally spread to fill the drift layer 56. Because the bypass diode 52 is
30 reverse biased, current does not flow through the device.

[0058] Figure 9B shows operation of the semiconductor device 48 when the vertical FET device 50 is operating in the third quadrant and the bypass diode 52 is in a forward bias state of operation. When a bias voltage below the threshold voltage of the vertical FET device 50 is applied to the gate contact 72, and a positive voltage is applied to the source contact 74 of the semiconductor device 48 relative to the drain contact 76, current begins to flow from the anode 78 of the bypass diode 52 through the drift layer 56 to the cathode 80 of the bypass diode 52 and the drain contact 76 of the vertical FET device 50. As shown in Figure 9, as the current flows from the anode 78 of the bypass diode 52 into the drift layer 56, it is constricted into a channel by the electric field presented by the second deep well region 68. At a certain vertical distance from the second deep well region 68 when the electric field is diminished, current begins to laterally spread to fill the drift layer 56. The spreading current creates a potential voltage between each point in the drift layer 56 and the drain contact 76. As discussed above, the bypass diode 52 is placed such that the difference between the potential just below the P-N junction formed between the first deep well region 62 and the drift layer 56 and the potential presented at the source contact 74 is less than the barrier voltage of the P-N junction. Accordingly, the P-N junction formed between the first deep well region 62 and the drift layer 56 does not enter a forward bias mode of operation, thereby preventing current flow through the P-N junction. By preventing current flow through the P-N junction formed between the first deep well region 62 and the drift layer 56, stacking faults are prevented from being formed in the drift layer 56. Accordingly, the longevity and performance of the semiconductor device 48 is improved.

[0059] Figure 10 shows a graph 96 illustrating voltage-to-current characteristics of the bypass diode 52 and the P-N junction formed between the first deep well region 62 and the drift layer 56 in the vertical FET device 50. In Figure 10, a first curve 98 represents the voltage-to-current relationship of the bypass diode 52. Further, a second curve 100 represents the voltage-to-current relationship of the P-N junction formed between the first deep well region 62 and the drift layer 56. At a barrier voltage 102 of the bypass diode 52, the bypass

diode 52 will begin conducting current in a linear fashion. Further, at a barrier voltage 104 of the P-N junction formed between the first deep well region 62 and the drift layer 56, the P-N junction will also begin conducting current. The concepts disclosed herein are directed towards ensuring that the bypass diode 52, and not the P-N junction formed between the first deep well region 62 and the drift layer 56, conducts all of the current flowing between the source contact 74 and the drain contact 76 of the semiconductor device 48 when the vertical FET device 50 is operating in the third quadrant, such that the bypass diode 52 conducts all of the current up to at least three times the rated current of the vertical FET device 50.

[0060] Figure 11 shows an alternative embodiment of the semiconductor device 48, wherein the vertical FET device 50 is a full-cell MOSFET, and the semiconductor device 48 includes two bypass diodes 52. As shown in Figure 11, the semiconductor device 48 according to this embodiment is substantially similar to that shown in Figures 7-9, but further includes a second base region 106, a second source region 108, and an additional bypass diode 52. The second base region 106 is formed in a shallow portion on the surface of the drift layer 56 opposite the substrate 54 within the boundaries of the second deep well region 68. The second source region 108 is formed adjacent to the second base region 106 in a shallow portion on the surface of the drift layer 56 opposite the substrate 54 within the boundaries of the second deep well region 68. The bypass diodes 52 are Schottky diodes formed adjacent to both the first junction implant 58 and the second junction implant 60, respectively. By including two bypass diodes 52, the distance between each one of the P-N junctions formed between the first deep well region 62 and the drift layer 56 and the second deep well region 68 and the drift layer 56 and the closest one of the bypass diodes 52 may be further reduced when compared with the embodiment shown in Figures 7-9. Accordingly, the size of each one of the bypass diodes 52 may also be reduced while maintaining similar performance characteristics of the semiconductor device 48.

[0061] The semiconductor device 48 shown in Figure 11 will function in a substantially similar manner to that shown in Figures 7-9. When the vertical FET device 50 is in an OFF state of operation, current will not flow from the input node 82 to the output node 84 of the device. However, when the device is operating in the third quadrant, current will flow through the bypass diodes 52 and into the drift layer 56, such that a potential below each one of the P-N junctions formed between the source contact 74 and the drain contact 76 prevents the respective P-N junctions from entering a forward bias mode of operation. Accordingly, stacking faults are not formed in the drift layer 56 of the vertical FET device 50, and the performance and longevity of the device is improved.

[0062] Although only two different structures are shown for the vertical FET device 50 in Figures 7-9 and 11, those of ordinary skill in the art will appreciate that the principles of the present disclosure may be applied to any vertical FET device structure without departing from the principles of the present disclosure.

[0063] Figures 12-14 illustrate a variety of exemplary layouts for integrating the bypass diode 52 together with the vertical FET device 50 in the semiconductor device 48. Figure 12 shows a three-dimensional diagram of the semiconductor device 48 according to one embodiment of the present disclosure. As shown in Figure 12, the vertical FET device 50 is a full-cell MOSFET, which is substantially similar to that shown in Figure 11. The bypass diode 52 is integrated adjacent to the vertical FET device 50. The bypass diode 52 includes the anode 78 on the surface of the drift layer 56 opposite the substrate 54, which partially overlaps a portion of the second deep well region 68, the second base region 106, and the second source region 108. Notably, the layout of the components of the semiconductor device 48 shown in Figure 12 remain substantially the same as it extends into the page. Although the described layout will effectively prevent stacking faults from forming in the vertical FET device 50 as described above, the placement of the bypass diode 52 is inefficient, as it consumes a large amount of real estate in the semiconductor device 48 and results in the replacement of MOSFET channel area of the vertical FET device 50 with Schottky metal for the anode 78 of the bypass diode 52. Accordingly, a

smaller number of the semiconductor devices 48 can be tiled onto a single semiconductor die, thereby reducing the performance and increasing the costs associated with producing such a die.

[0064] Figure 13 shows a three-dimensional diagram of the semiconductor

device 48 according to an additional embodiment of the present disclosure.

Figure 13 is substantially similar to Figure 12, except that the first base region 64 and the second base region 106 have been moved into the third dimension, such that the first base region 64 and the second base region 106 are located some distance from a front face 110 of the semiconductor device 48. By moving the

first base region 64 and the second base region 106 into the third dimension, the overall cell pitch of the semiconductor device 48 can be reduced without impacting the performance of the device. Accordingly, more semiconductor devices can be integrated onto a single die, thereby improving the performance and costs associated with producing such a die. Even though the layout shown in Figure 13 is more efficient than that shown in Figure 12, the bypass diode 52 is still inefficiently placed, as it consumes a large amount of real estate in the semiconductor device 48 and results in the replacement of MOSFET channel area of the vertical FET device 50 with Schottky metal for the anode 78 of the bypass diode 52, as discussed above.

[0065] Figures 14A and 14B show a three-dimensional diagram of the semiconductor device 48 according to an additional embodiment of the present disclosure. As shown in Figures 14A and 14B, the vertical FET device 50 is a full-cell MOSFET, and the semiconductor device 48 includes two bypass diodes 52. Additionally, the first base region 64, the second base region 106, and the anodes 78 for each one of the bypass diodes 52 have been moved into the third dimension, such that the first base region 64, the second base region 106, and the anodes 78 for each one of the bypass diodes 52 are located some distance away from the front face 110 of the semiconductor device 48, such that each one of the bypass diodes 52 occupies only a portion of the depth of the semiconductor device 48.

[0066] Further, the first deep well region 62, the second deep well region 68, the first source region 66, and the second source region 108 are segmented in the third dimension in order to create a space for the anodes 78 of the bypass diodes 52 to directly contact the drift layer 56 at some distance away from the front face 110 of the semiconductor device 48 in order to form the bypass diodes 52. Accordingly, the first junction implant 58 and the second junction implant 60 are effectively further broken into a third junction implant 112 and a fourth junction implant 114, respectively, such that each one of the junction implants 112, 114 is located in a corner of the surface of the drift layer 56 opposite the substrate 54, extending downward toward the substrate 54 and inward towards the center of the surface of the drift layer 56 opposite the substrate 54. The third junction implant 112 includes a third deep well region 116, a third source region 118, and the first base region 64. The fourth junction implant 114 includes a fourth deep well region 120, a fourth source region 122, and the second base region 106.

[0067] Arranging the semiconductor device 48 as described above allows the bypass diodes 52 to be implemented without sacrificing MOSFET channel area in the vertical FET device 50. Further, the described arrangement allows the maximum distance between the furthest edge of each P-N junction between the source contact 74 and the drain contact 76 of the vertical FET device 50 and each bypass diode 52 to depend on the depth of the first source region 66 and the deep well region 68, rather than the total cell pitch. Accordingly, a larger number of the semiconductor devices 48 may be tiled onto a single semiconductor die, thereby increasing the performance and decreasing the cost associated with such a die.

[0068] Figures 15A-15E and Figure 16 illustrate a process for manufacturing the semiconductor device 48 shown in Figures 14A and 14B according to one embodiment of the present disclosure. First, the drift layer 56 is epitaxially grown on a surface of the substrate 54 (step 200 and Figure 15A). Next, the first deep well region 62, the second deep well region 68, the third deep well region 116, and the fourth deep well region 120 are implanted in the surface of the drift layer

56 opposite the substrate 54 (step 202 and Figure 15B). In order to achieve the depth required for the first deep well region 62, the second deep well region 68, the third deep well region 116, and the fourth deep well region 120, a two-step ion implantation process may be used, wherein boron is used to obtain the

5 necessary depth, while aluminum is used to obtain desirable conduction characteristics of the respective deep well regions. The first base region 64 and the second base region 106 are then implanted (step 204 and Figure 15C).

Next, the first source region 66, the second source region 108, the third source region 118, and the fourth source region 122 are implanted (step 206 and Figure

10 15D). The first deep well region 62, the second deep well region 68, the third deep well region 116, the fourth deep well region 120, the first base region 64, the second base region 106, the first source region 66, the second source region 108, the third source region 118, and the fourth source region 122 may be

15 implanted via an ion implantation process. Those of ordinary skill will appreciate that the aforementioned regions may be created by any suitable process without departing from the principles of the present disclosure.

[0069] Next, the gate oxide layer 70 is applied to the surface of the drift layer 56 opposite the substrate 54 (step 208 and Figure 15E). The gate oxide layer 70 is then etched and the ohmic contacts (the gate contact 72, the source contacts

20 74, and the drain contact 76) and the anodes 78 are attached to the semiconductor device 48 (step 210 and Figure 15E). An over-mold layer may be provided over the surface of the drift layer 56 opposite the substrate 54 in order to protect the contacts of the semiconductor device 48.

[0070] Those skilled in the art will recognize improvements and modifications to the embodiments of the present disclosure. All such improvements and modifications are considered within the scope of the concepts disclosed herein and the claims that follow.

Claims

What is claimed is:

1. A semiconductor device comprising:

- a vertical FET device including a gate contact, a source contact, and a drain contact, wherein the gate contact and the source contact are separated from the drain contact by at least a drift layer; and
- a bypass diode coupled between the source contact and the drain contact and monolithically integrated adjacent to the vertical FET device such that a voltage placed between the source contact and the drain contact is distributed through the drift layer by the bypass diode in such a way that a voltage across each one of a plurality of P-N junctions formed between the source contact and the drain contact in the vertical FET device is prevented from exceeding a barrier voltage of the respective P-N junction.

2. The semiconductor device of claim 1 wherein the bypass diode is a Schottky diode.

3. The semiconductor device of claim 1 wherein each one of the plurality of P-N junctions formed between the source contact and the drain contact of the vertical FET device is between about 5-15 microns from the bypass diode.

4. The semiconductor device of claim 1 wherein preventing each one of the plurality of P-N junctions from exceeding the barrier voltage of the respective P-N junction prevents the formation of stacking faults in the drift layer of the vertical FET device.

5. The semiconductor device of claim 1 wherein the vertical FET device is a metal-oxide-semiconductor field-effect transistor (MOSFET) half-cell.

6. The semiconductor device of claim 5 wherein the vertical FET device further comprises a substrate between the drain contact and the drift layer.

7. The semiconductor device of claim 6 wherein the vertical FET device further comprises:

- a first junction implant on a surface of the drift layer opposite the substrate; and
- a second junction implant laterally separated from the first junction implant on the surface of the drift layer opposite the substrate.

8. The semiconductor device of claim 7 wherein:

- the first junction implant comprises a first deep well region, a first base region inside the first deep well region, and a first source region adjacent to the first base region inside the first deep well region; and
- the second junction implant comprises a second deep well region.

9. The semiconductor device of claim 8 wherein the bypass diode comprises:

- an anode on the surface of the drift layer opposite the substrate, such that the anode partially overlaps a portion of the drift layer and the second deep well junction; and
- a cathode on a surface of the substrate opposite the drift layer.

10. The semiconductor device of claim 9 wherein the anode is coupled to the source contact via an input node, and the cathode is coupled to the drain contact via an output node.

11. The semiconductor device of claim 8 wherein:

- the source contact is located on the surface of the drift layer opposite the substrate, such that the source contact partially overlaps a portion of the first base region and the first source region; and

- the gate contact is located on top of a gate oxide layer, which is located on the surface of the drift layer opposite the substrate, such that the gate oxide layer partially overlaps and runs between a surface of the first source region and the second deep well region.

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12. A semiconductor device comprising:

- a vertical FET device including a gate contact, a pair of source contacts, and a drain contact, wherein the gate contact and the pair of source contacts are separated from the drain contact by at least a drift layer; and
- at least two bypass diodes coupled between the pair of source contacts and the drain contact and monolithically integrated adjacent to the vertical FET device such that a voltage placed between the pair of source contacts and the drain contact is distributed through the drift layer by the at least two bypass diodes in such a way that a voltage across each one of a plurality of P-N junctions formed between the pair of source contacts and the drain contact in the vertical FET device is prevented from exceeding a barrier voltage of the respective P-N junction.

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13. The semiconductor device of claim 12 wherein each one of the at least two bypass diodes is a Schottky diode.

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14. The semiconductor device of claim 12 wherein each one of the plurality of P-N junctions formed between the pair of source contacts and the drain contact of the vertical FET device is between about 5-15 microns from the furthest of the at least two bypass diodes.

30

15. The semiconductor device of claim 12 wherein preventing each one of the plurality of P-N junctions between the pair of source contacts and the drain contact of the vertical FET device from exceeding the barrier voltage of the respective P-N junction prevents the formation of stacking faults in the drift layer of the vertical FET device.

16. The semiconductor device of claim 12 wherein the vertical FET device is a metal-oxide-semiconductor field-effect transistor (MOSFET) full-cell.

17. The semiconductor device of claim 16 wherein the vertical FET device
5 further comprises a substrate between the drain contact and the drift layer.

18. The semiconductor device of claim 17 wherein the vertical FET device further comprises:

- 10 • a first junction implant on a surface of the drift layer opposite the substrate; and
- a second junction implant laterally separated from the first junction implant on the surface of the drift layer opposite the substrate.

19. The semiconductor device of claim 18 wherein the first junction implant
15 and the second junction implant each comprise a deep well region, a base region inside the deep well region, and a source region adjacent to the base region inside the deep well region.

20. The semiconductor device of claim 19 wherein each one of the at least
20 two bypass diodes is monolithically integrated adjacent to the first junction implant and the second junction implant, respectively, and each one of the at least two bypass diodes comprises:

- 25 • an anode on the surface of the drift layer opposite the substrate, such that the anode partially overlaps a portion of the drift layer and the second deep well junction; and
- a cathode on a surface of the substrate opposite the drift layer.

21. The semiconductor device of claim 20 wherein the anode is coupled to the pair of source contacts via an input node, and the cathode is coupled to the drain
30 contact via an output node.

22. The semiconductor device of claim 19 wherein:

- each of the pair of source contacts is located on the surface of the drift layer opposite the substrate, such that each of the pair of source contacts partially overlaps a portion of the respective base region and the
5 respective source region; and
- the gate contact is located on top of a gate oxide layer, which is located on the surface of the drift layer opposite the substrate, such that the gate oxide layer partially overlaps and runs between each one of the source regions.

23. A method for manufacturing a semiconductor device comprising:

- providing a substrate;
- growing a drift layer on a surface of the substrate;
- implanting a first junction implant and a second junction implant on the
15 surface of the drift layer opposite the substrate, such that the first junction implant is laterally separated from the second junction implant;
- providing a gate contact and a source contact on the surface of the drift layer opposite the substrate;
- providing a drain contact on the surface of the substrate opposite the drift
20 layer; and
- providing at least one Schottky metal contact on the surface of the drift layer opposite the substrate, the Schottky metal contact being coupled to the source contact in order to form a bypass diode between the source contact and the drain contact.

24. The method of claim 23 wherein the bypass diode is a Schottky diode.

25. The method of claim 23 wherein each one of a plurality of P-N junctions formed between the source contact and the drain contact of the vertical FET
30 device is between about 5-15 microns from the bypass diode.

26. The method of claim 23 wherein the Schottky metal contact is placed on the surface of the drift layer such that a voltage placed between the source contact and the drain contact is distributed through the drift layer by the bypass diode in such a way that a voltage across each one of the plurality of P-N

5 junctions formed between the source contact and the drain contact in the vertical FET device is prevented from exceeding a barrier voltage of the respective P-N junction.

27. The method of claim 26 wherein preventing each one of the plurality of P-
10 N junctions from exceeding the barrier voltage of the respective P-N junction prevents the formation of stacking faults in the drift layer of the vertical FET device.

28. The method of claim 23 wherein:

- 15
- the first junction implant comprises a first deep well region, a first base region inside the first deep well region, and a first source region adjacent to the first base region inside the first deep well region; and
 - the second junction implant comprises a second deep well region.

20 29. The method of claim 28 wherein the Schottky metal contact partially overlaps a portion of the drift layer and the second deep well region.

30. The method of claim 29 wherein:

- 25
- the source contact is located on the surface of the drift layer opposite the substrate, such that the source contact partially overlaps a portion of the first base region and the first source region; and
 - the gate contact is located on top of a gate oxide layer, which is located on the surface of the drift layer opposite the substrate, such that the gate oxide layer partially overlaps and runs between a surface of the first
30 source region and the second deep well region.

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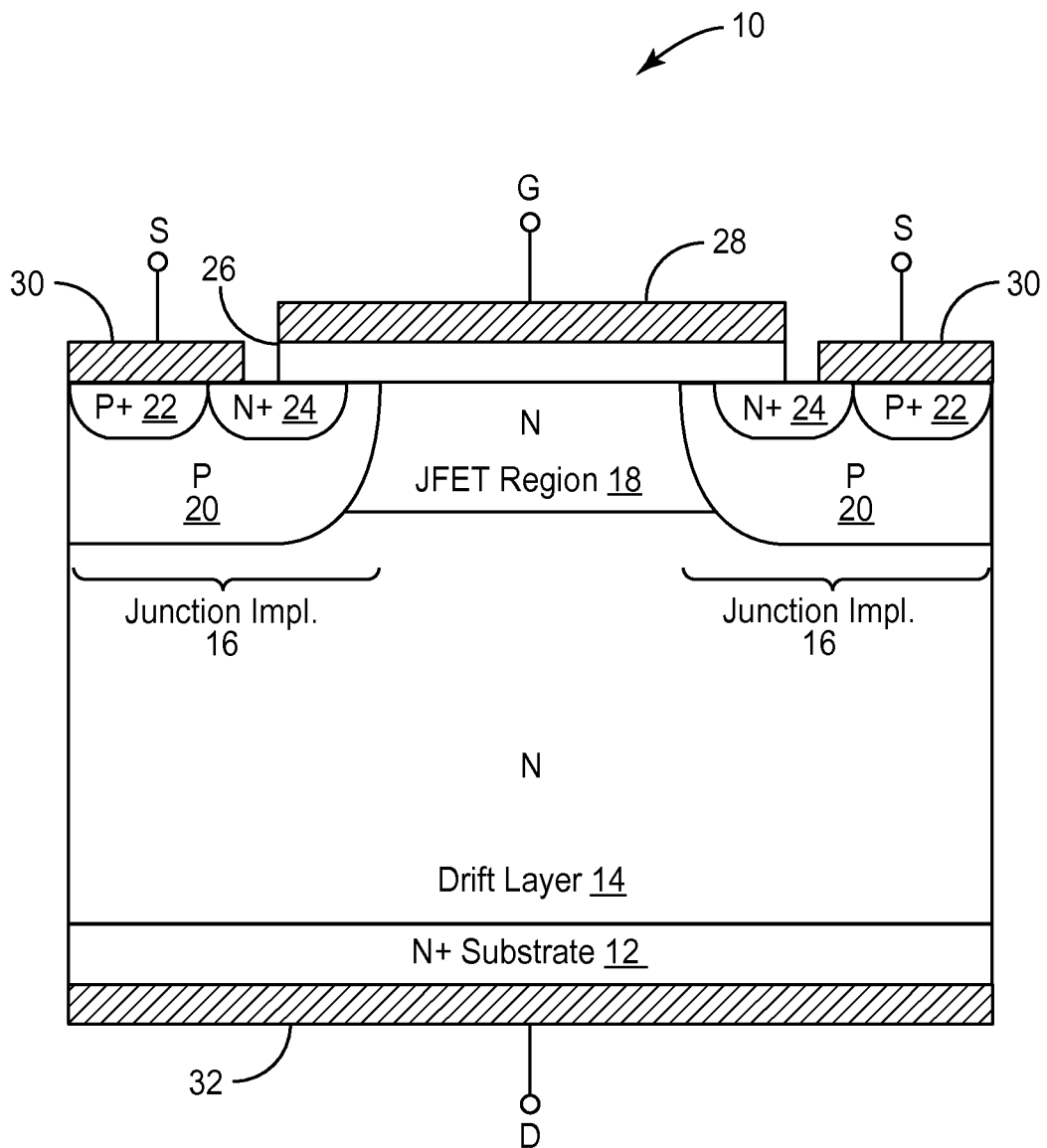


FIG. 1
(RELATED ART)

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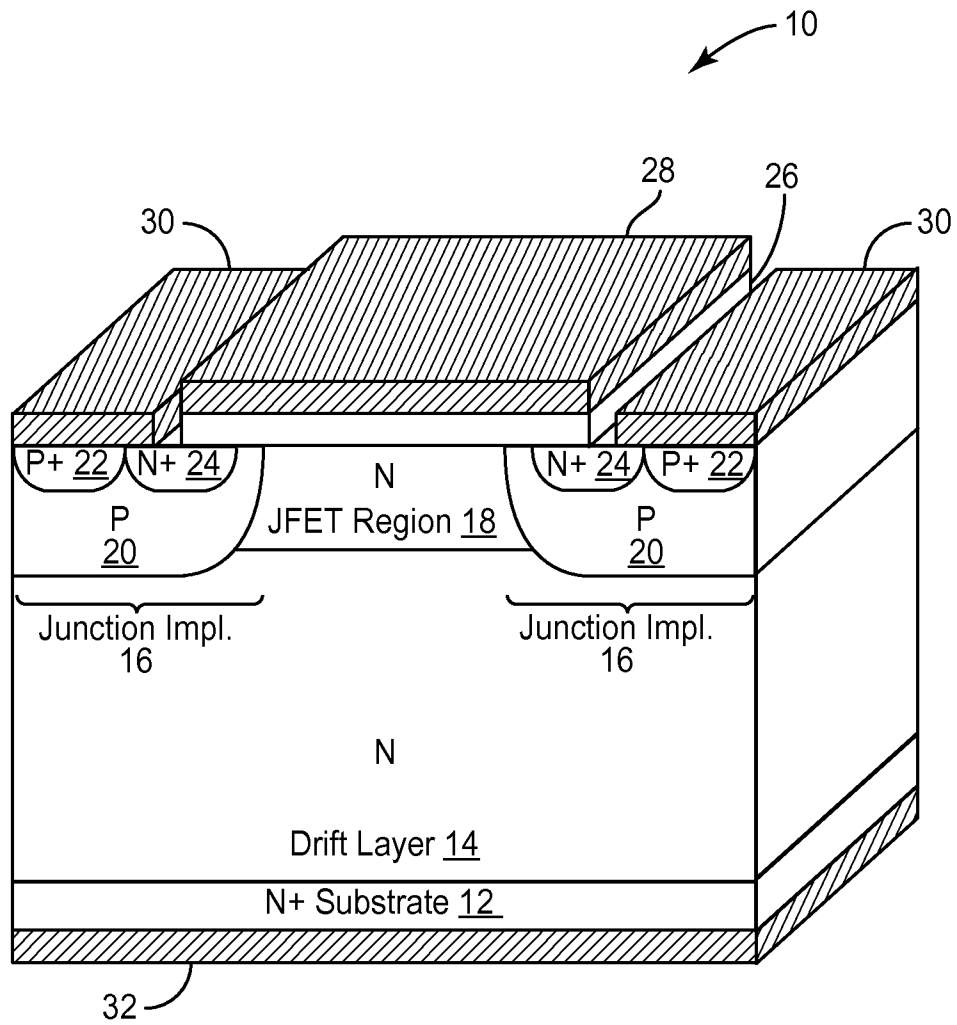


FIG. 2
(RELATED ART)

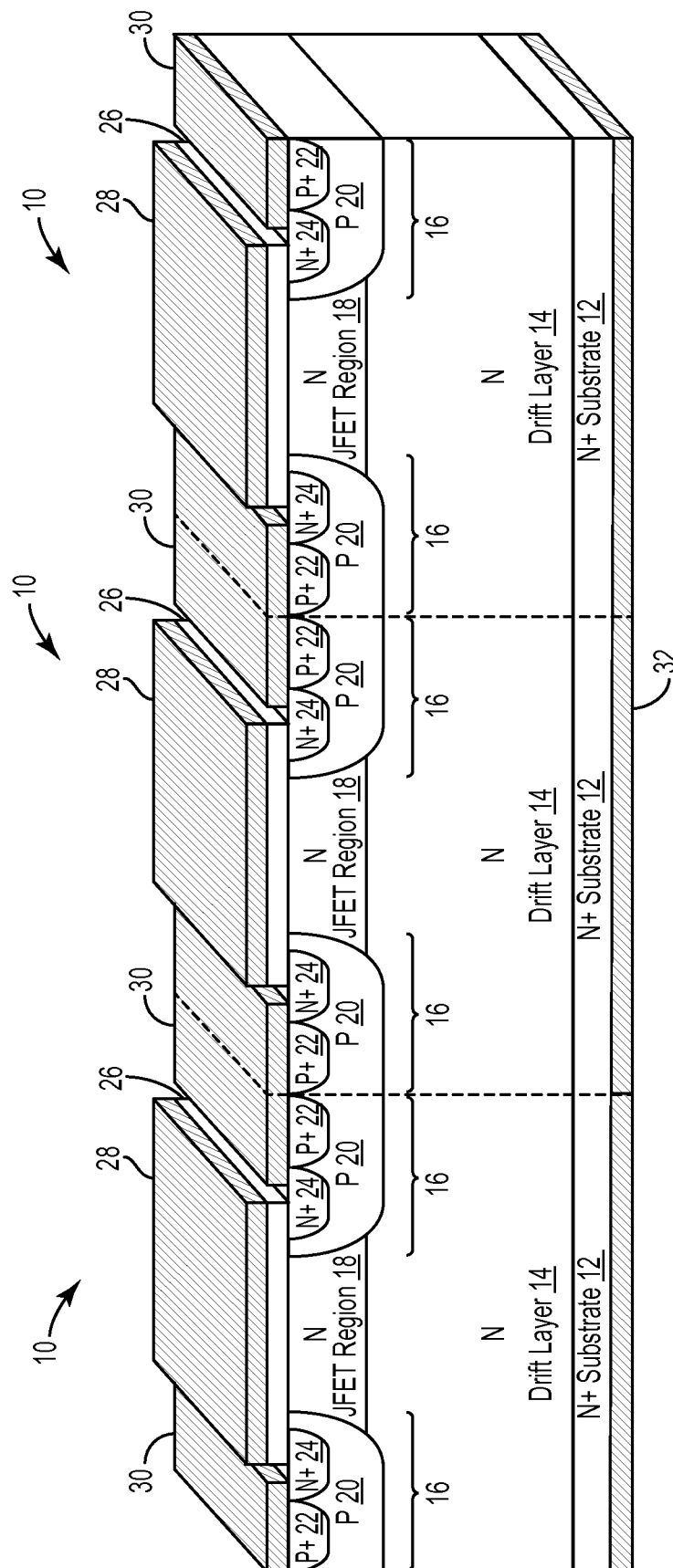


FIG. 3
(RELATED ART)

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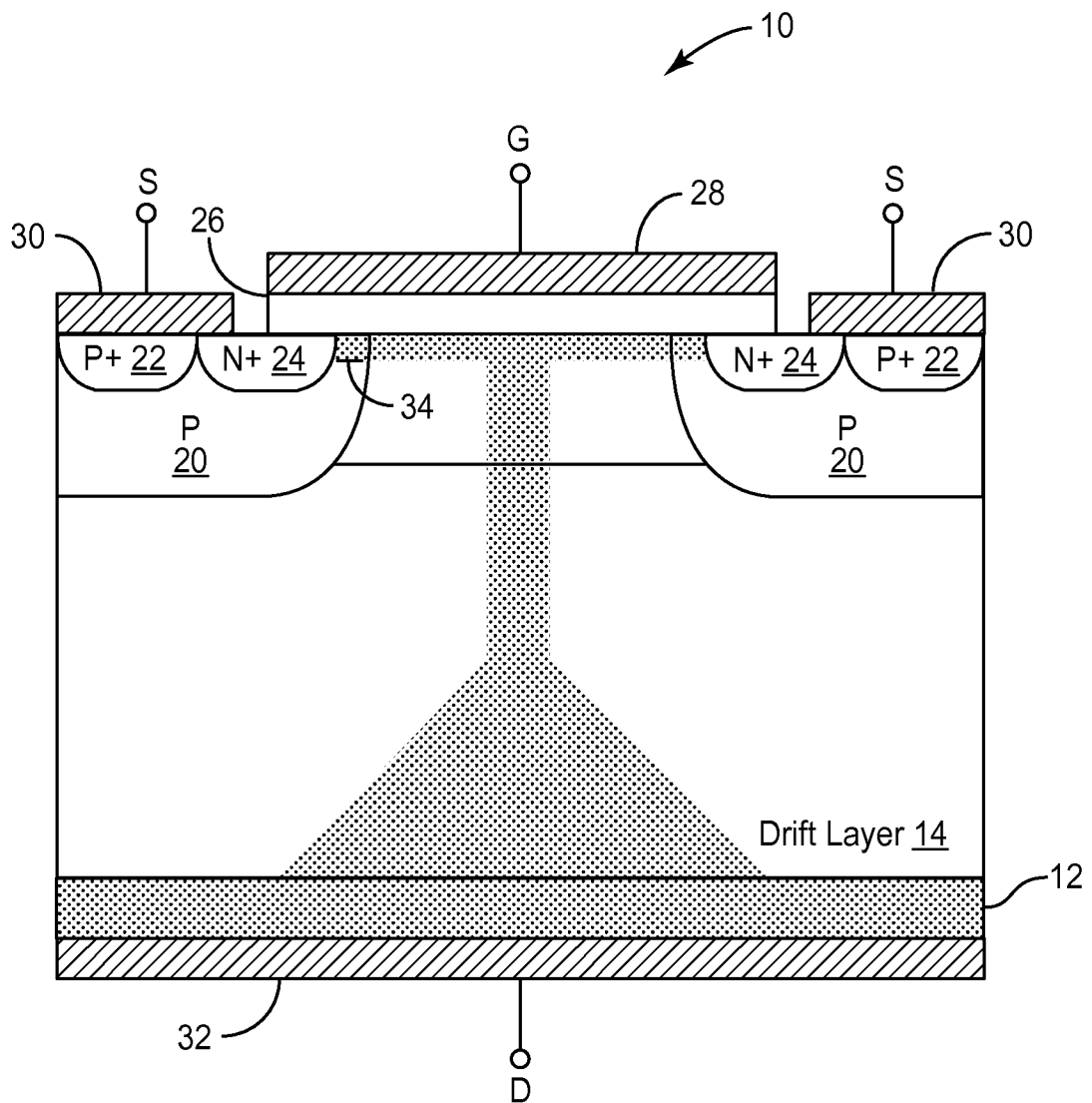


FIG. 4A
(RELATED ART)

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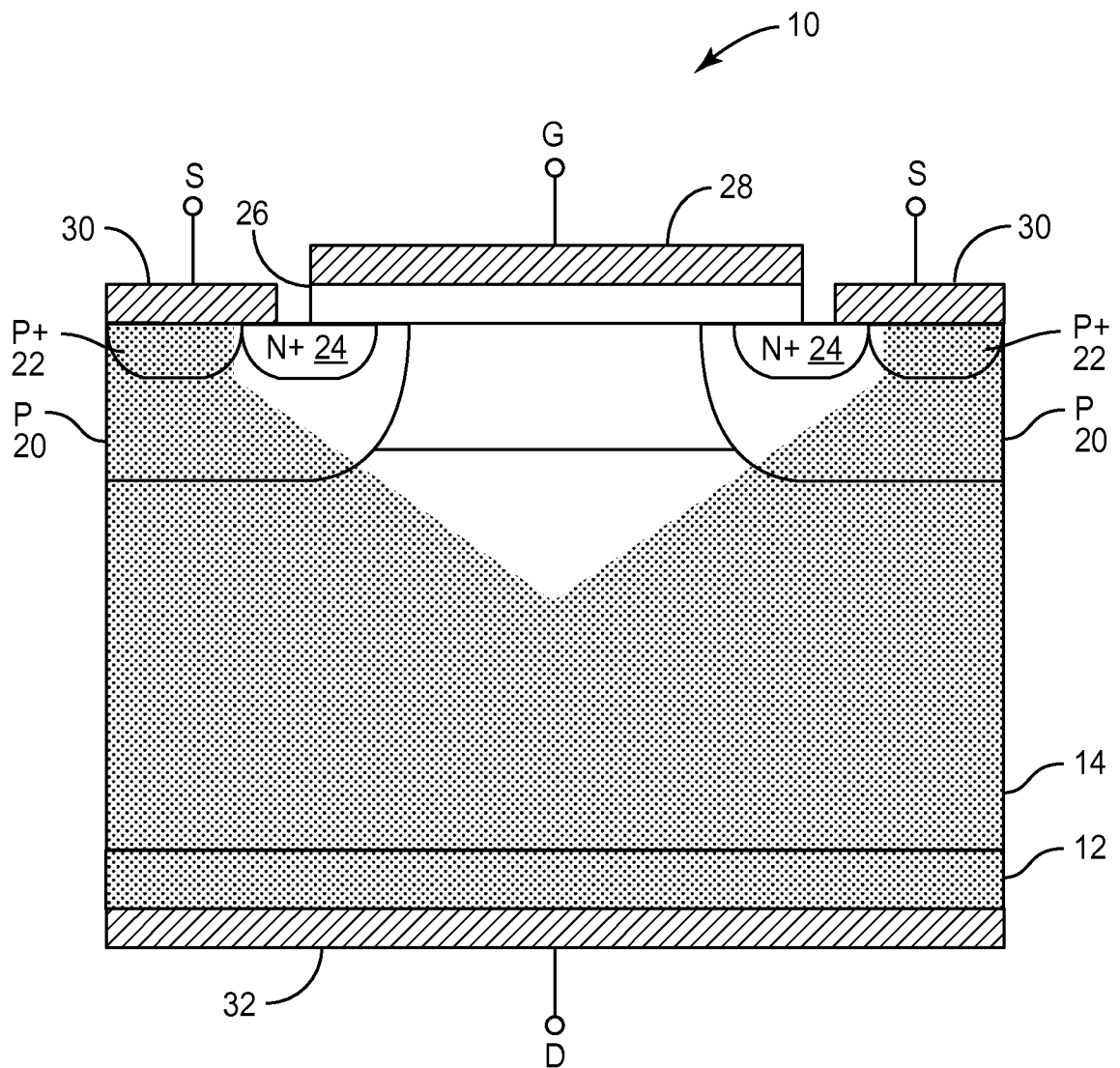


FIG. 4B
(RELATED ART)

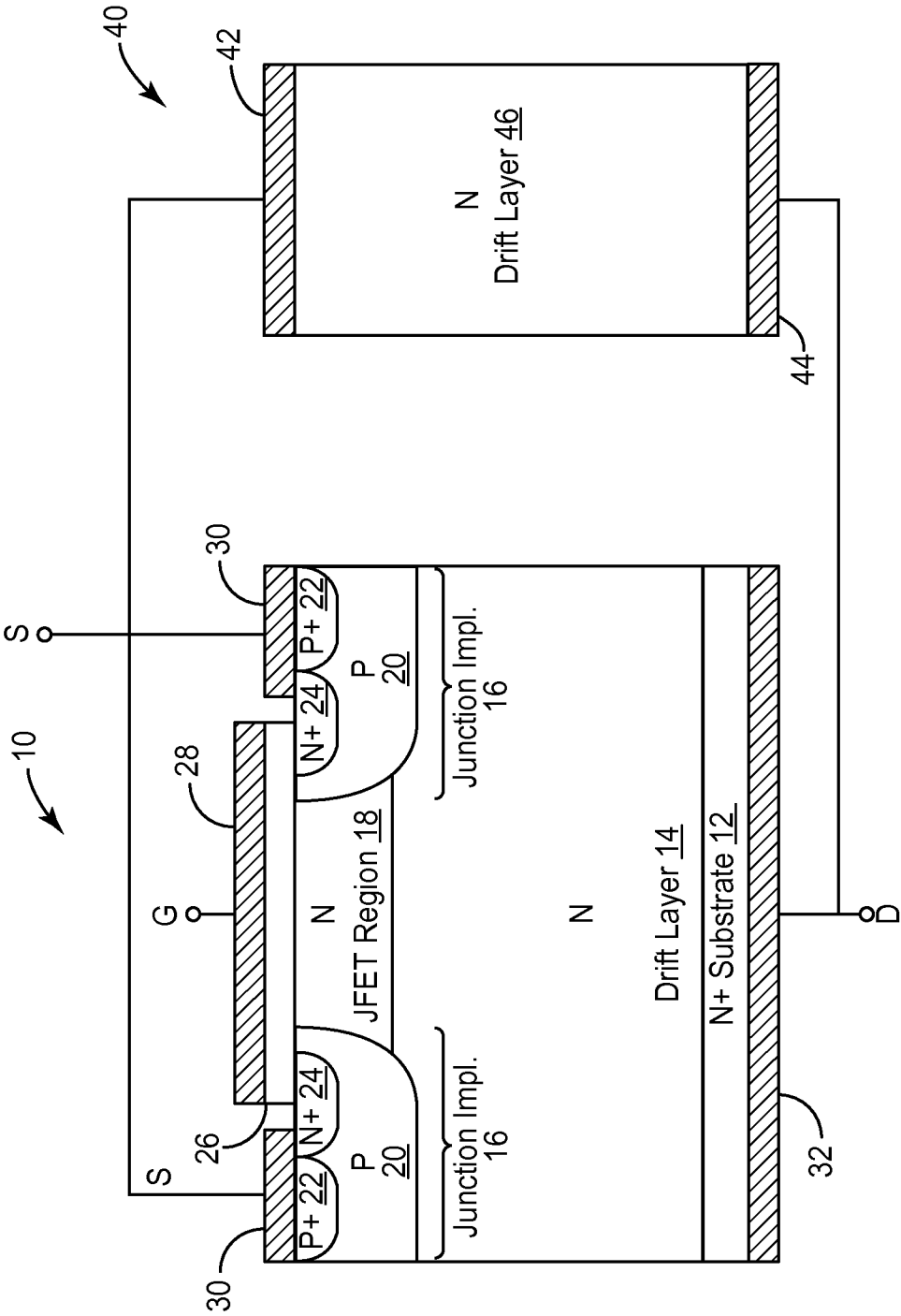


FIG. 5
(RELATED ART)

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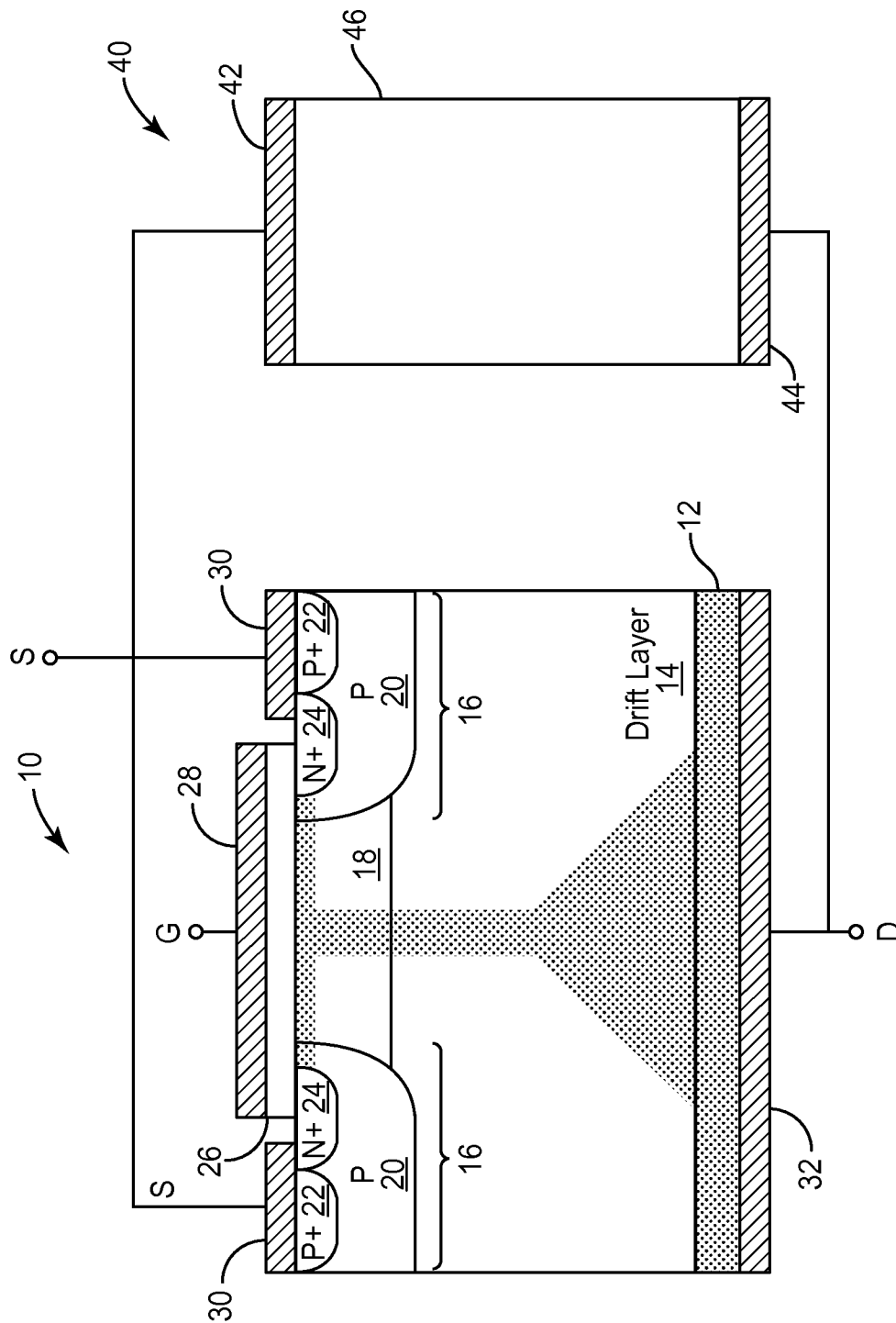


FIG. 6A
(RELATED ART)

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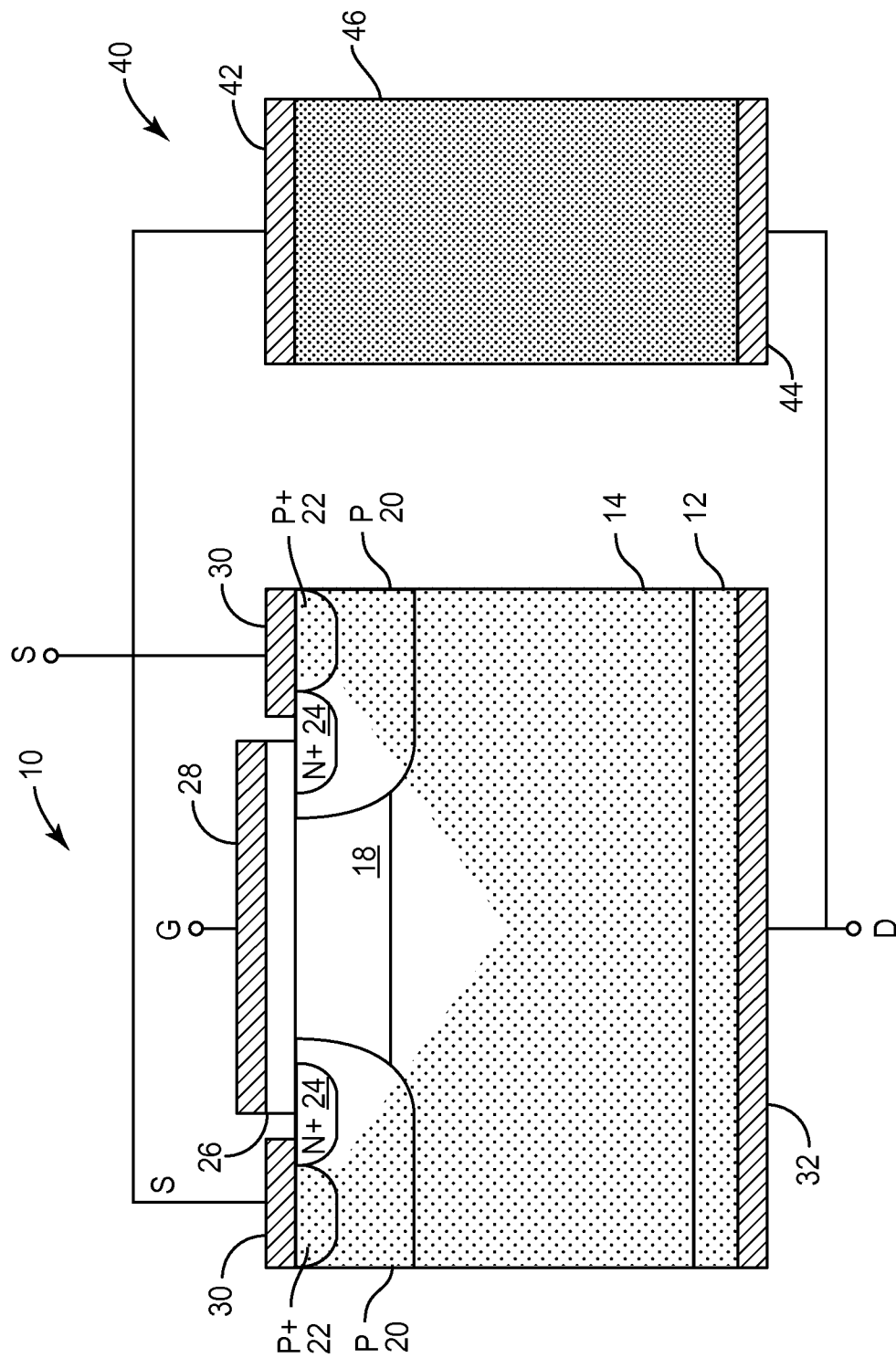
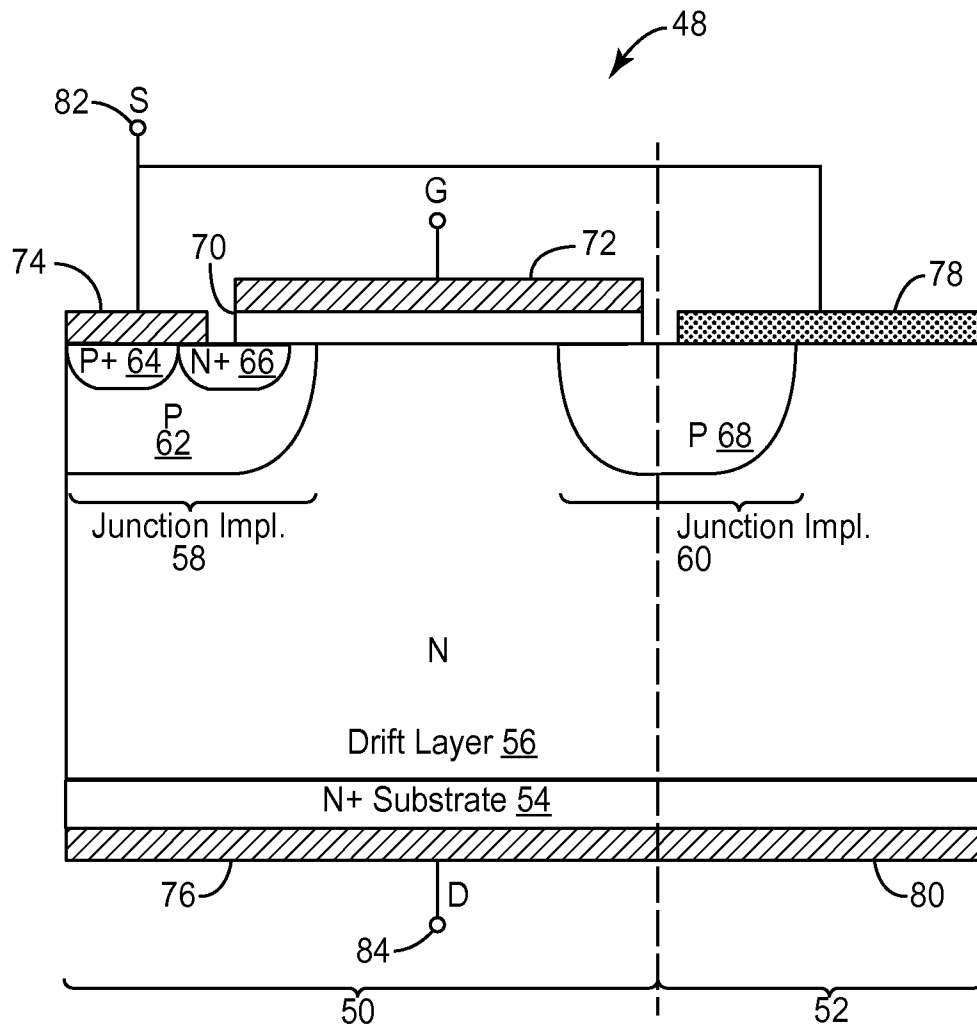


FIG. 6B
(RELATED ART)

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**FIG. 7**

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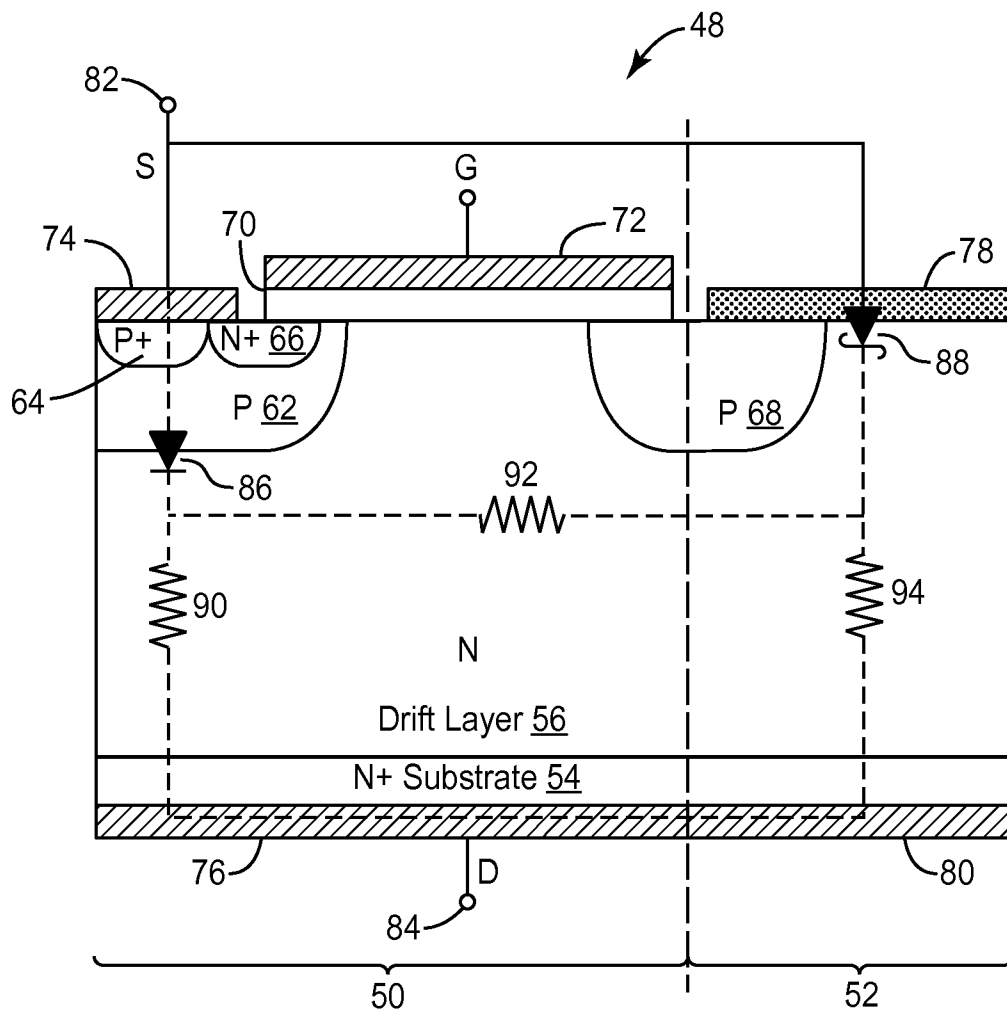


FIG. 8

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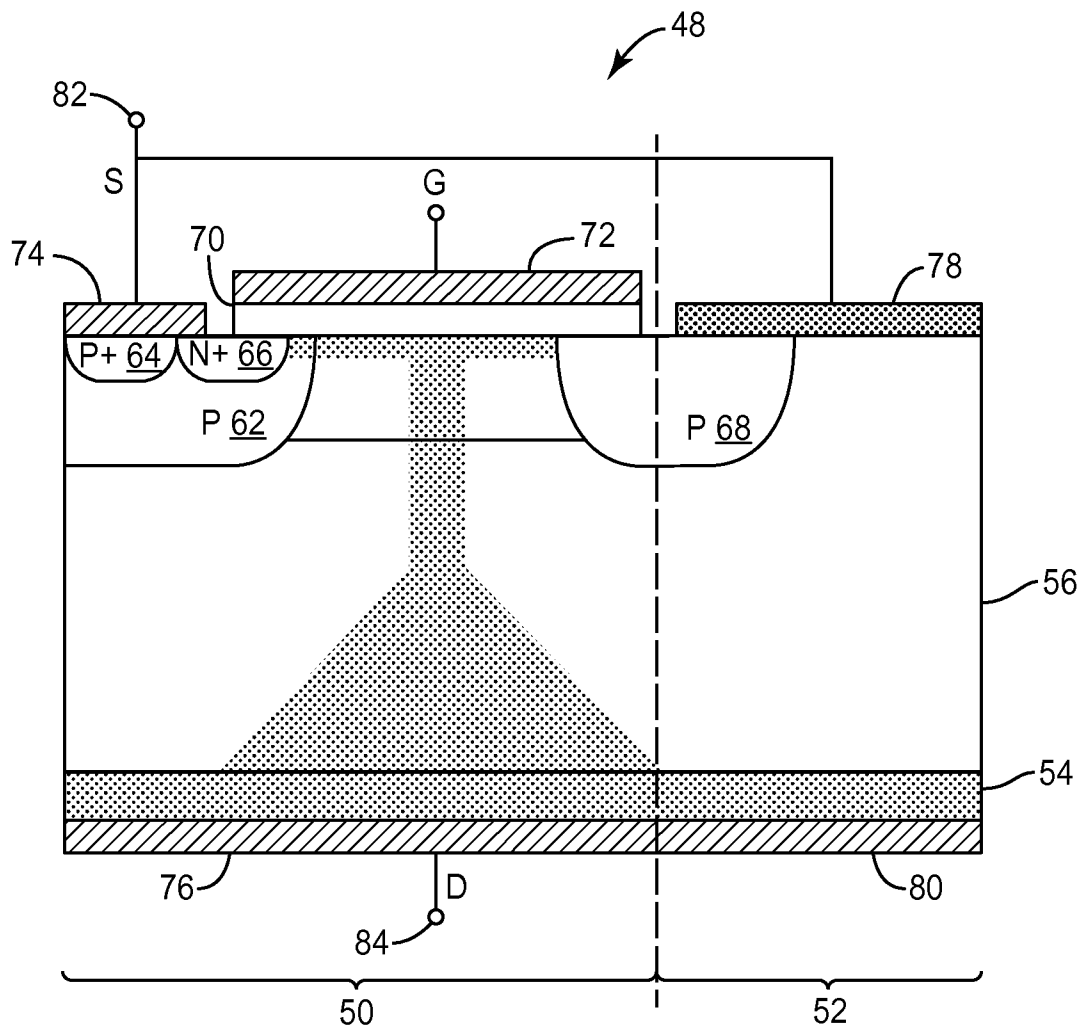


FIG. 9A

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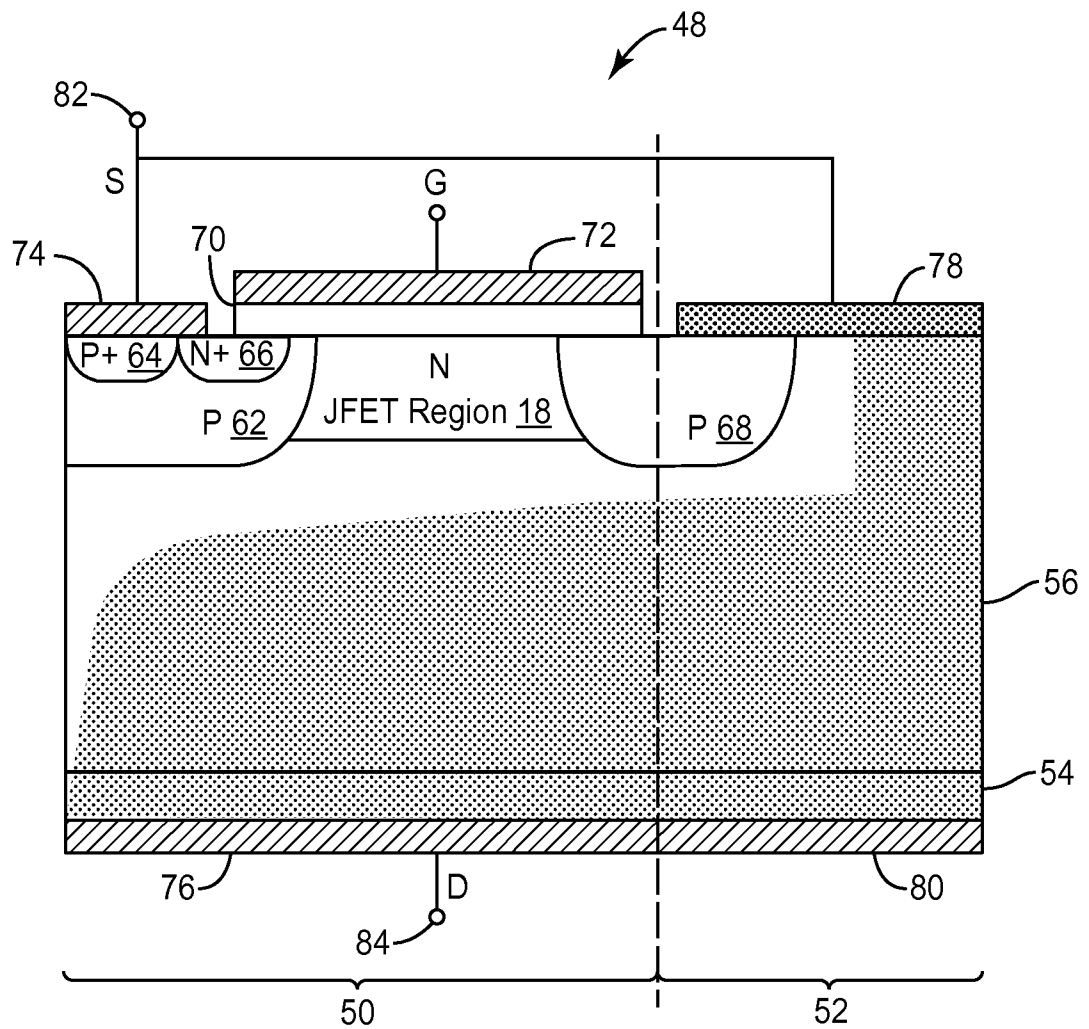


FIG. 9B

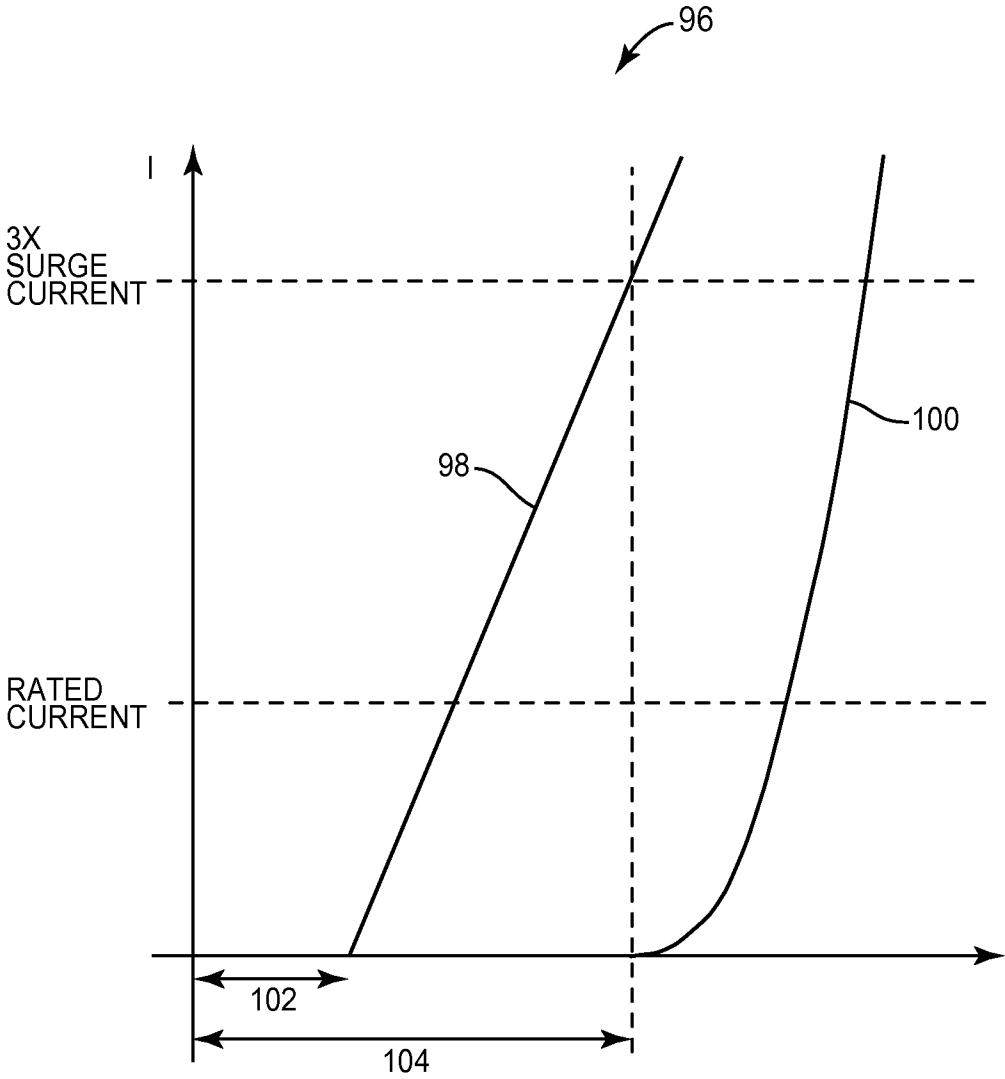


FIG. 10

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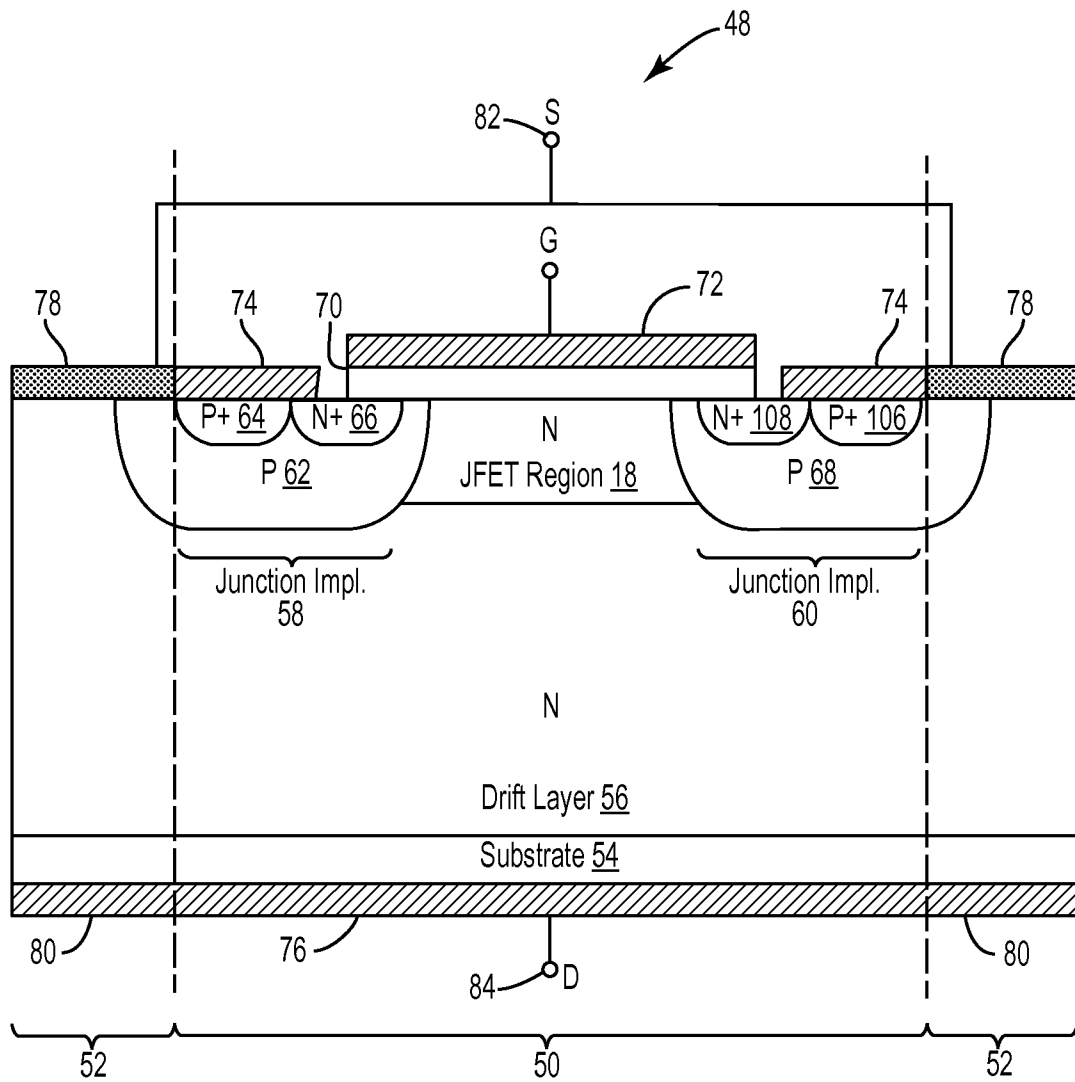


FIG. 11

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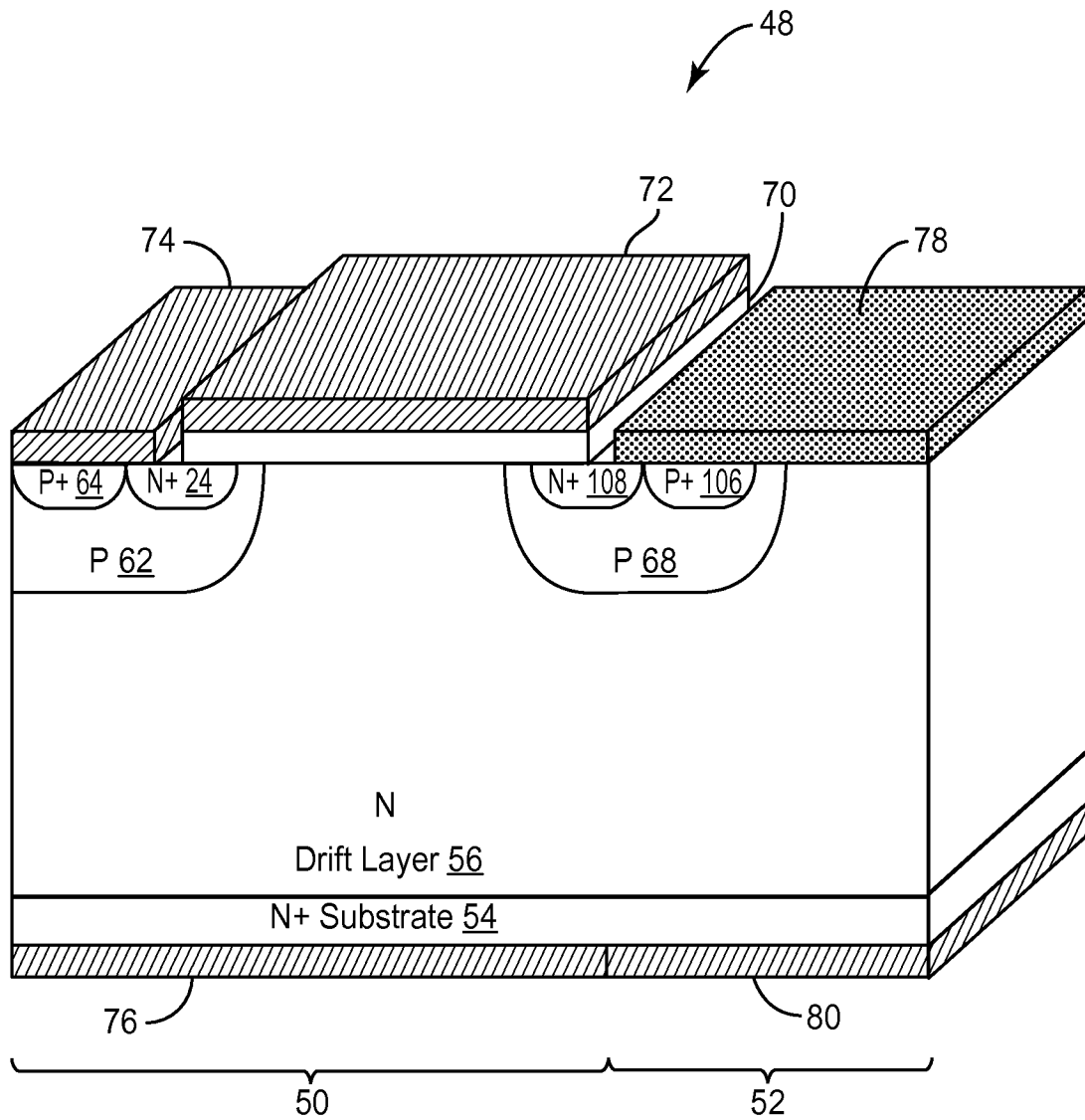
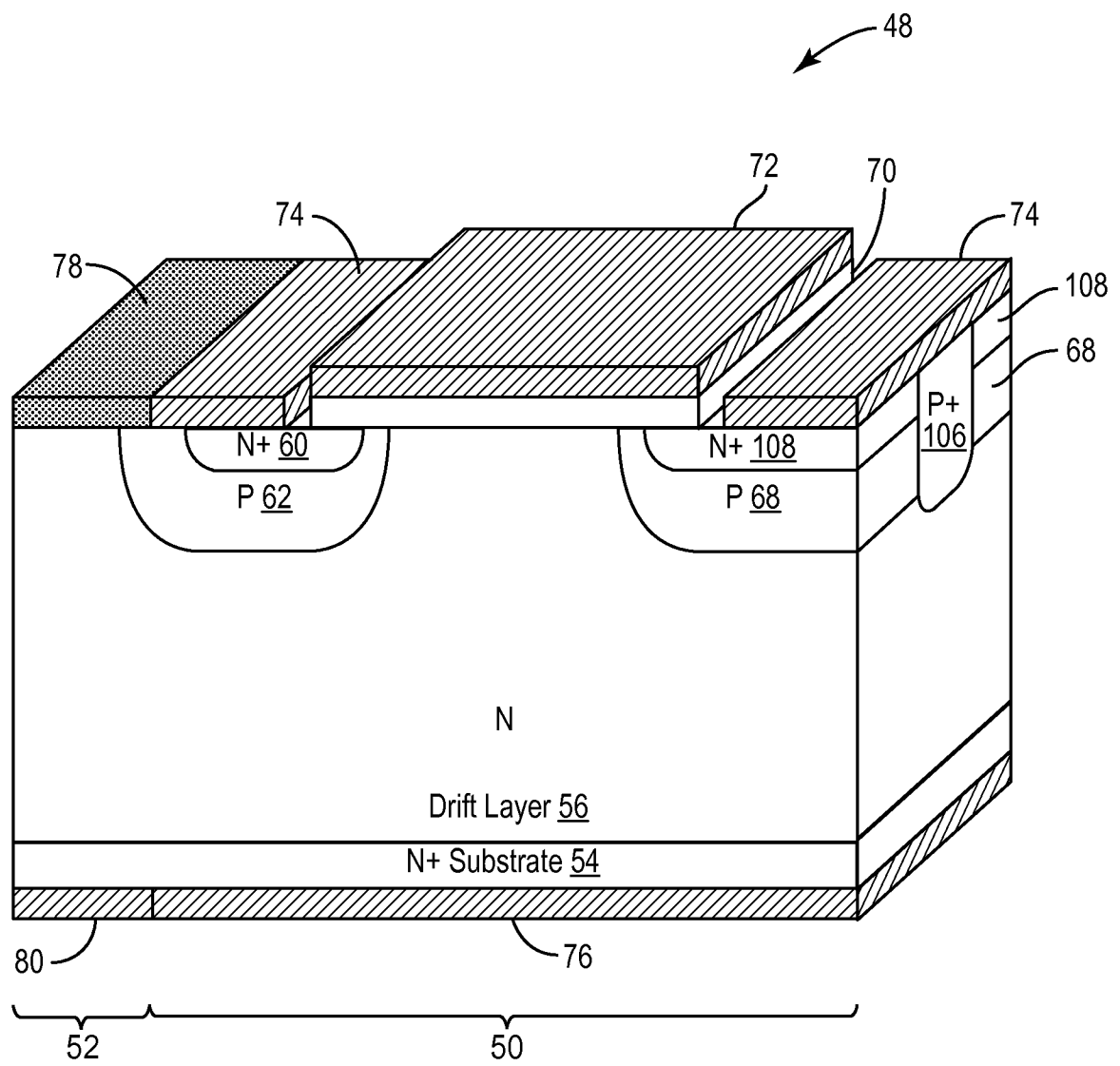


FIG. 12

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**FIG. 13**

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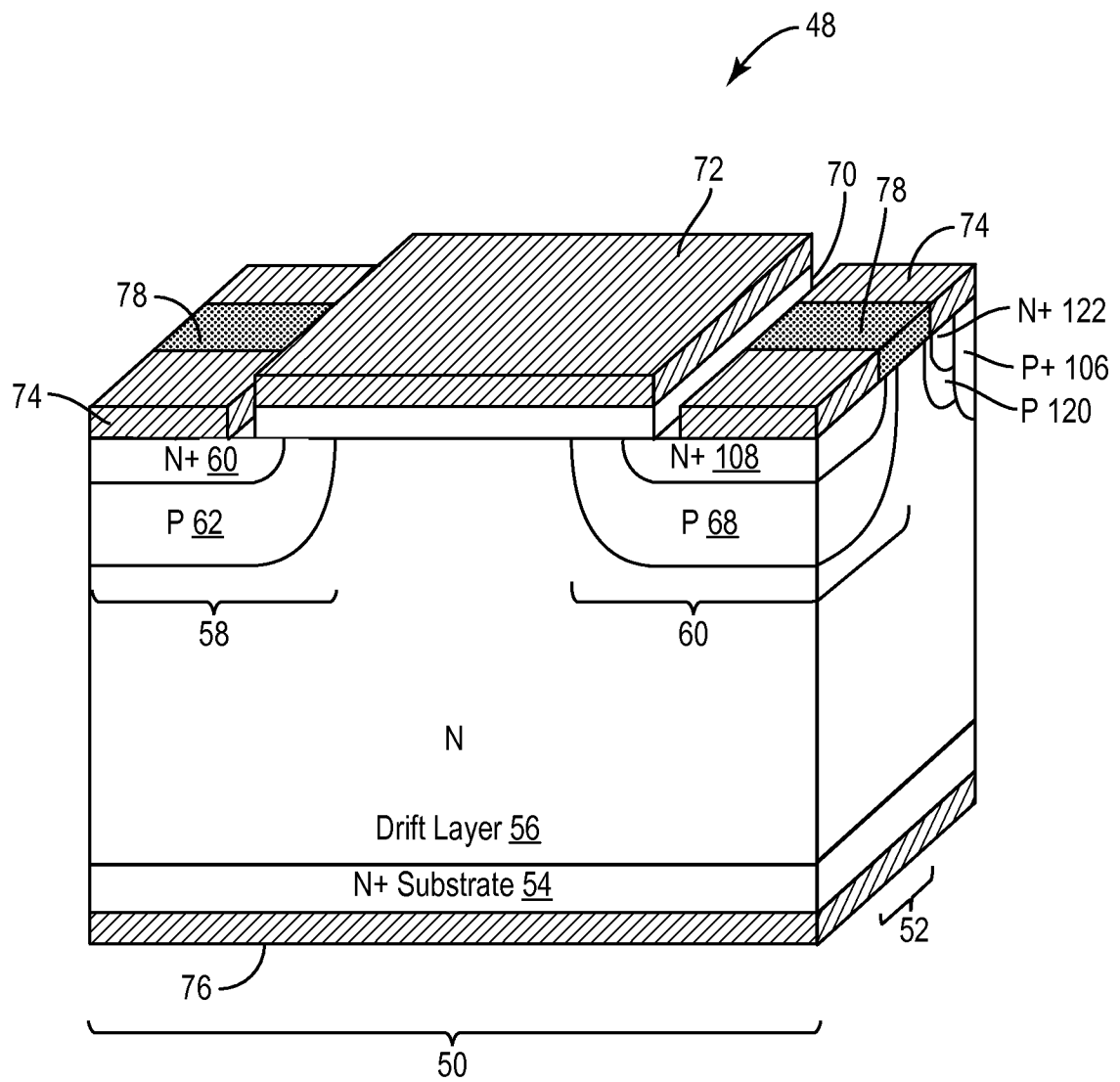
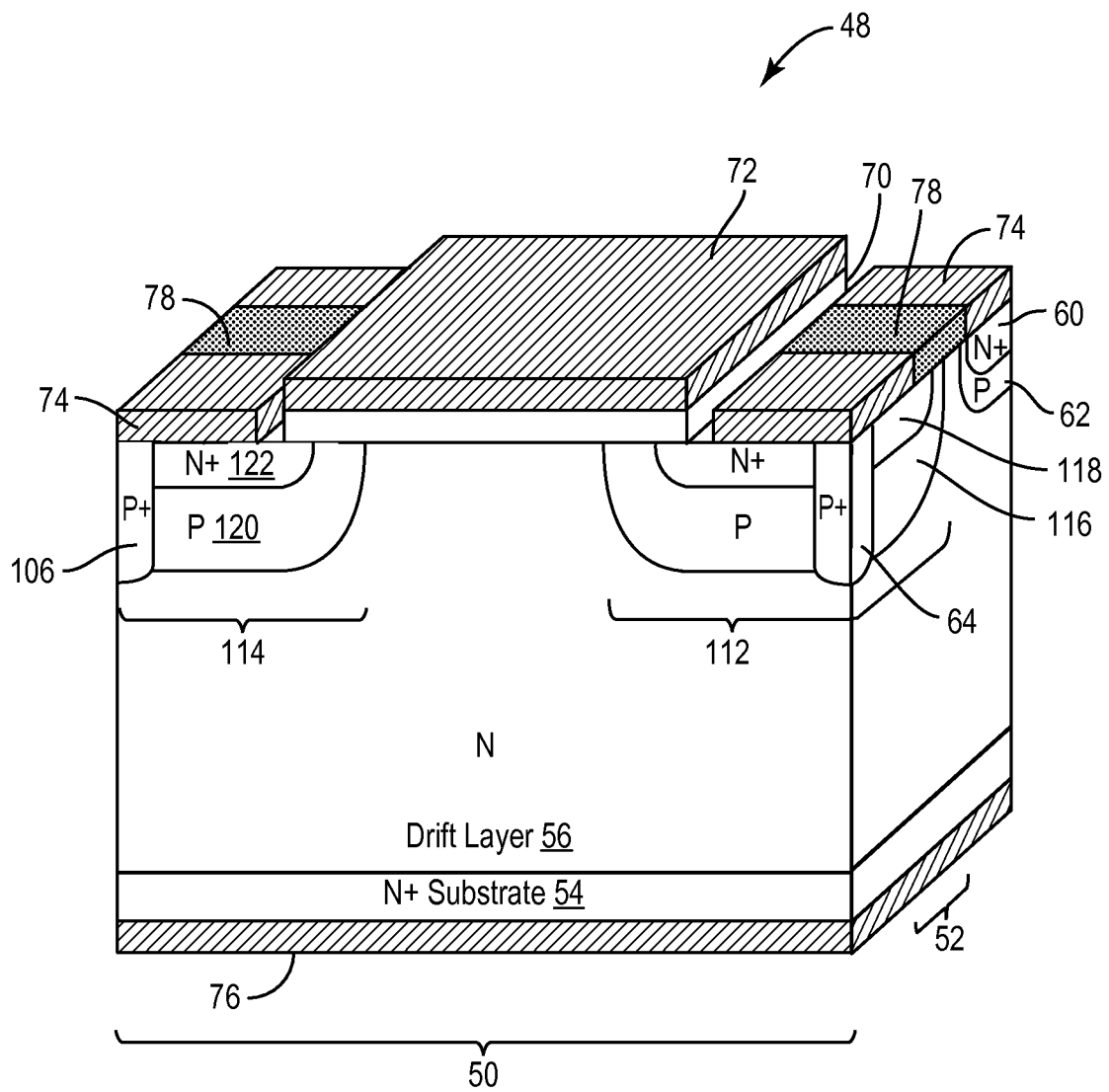


FIG. 14A

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**FIG. 14B**

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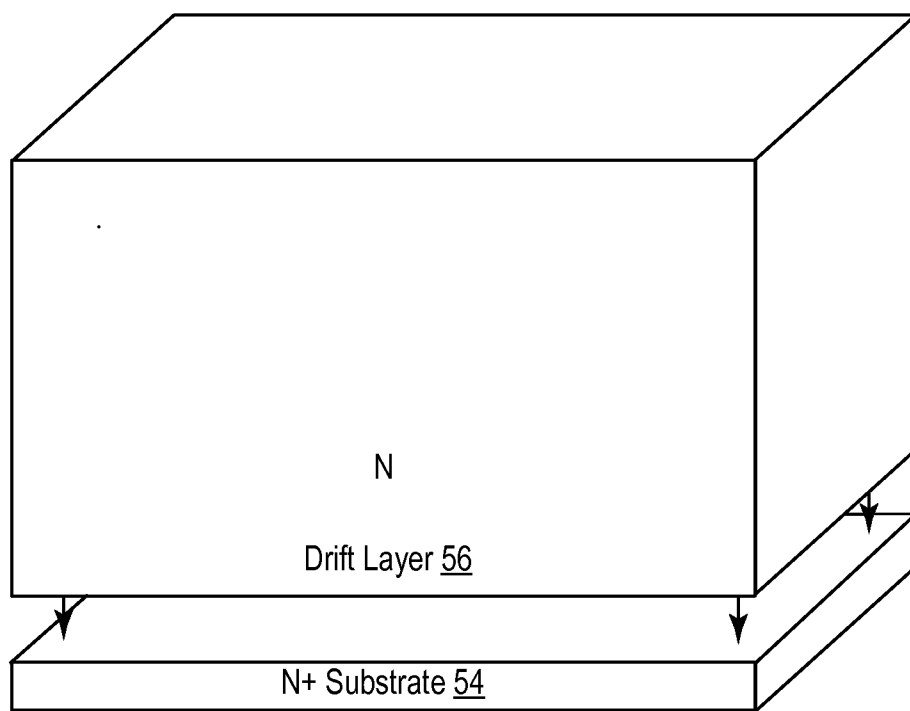


FIG. 15A

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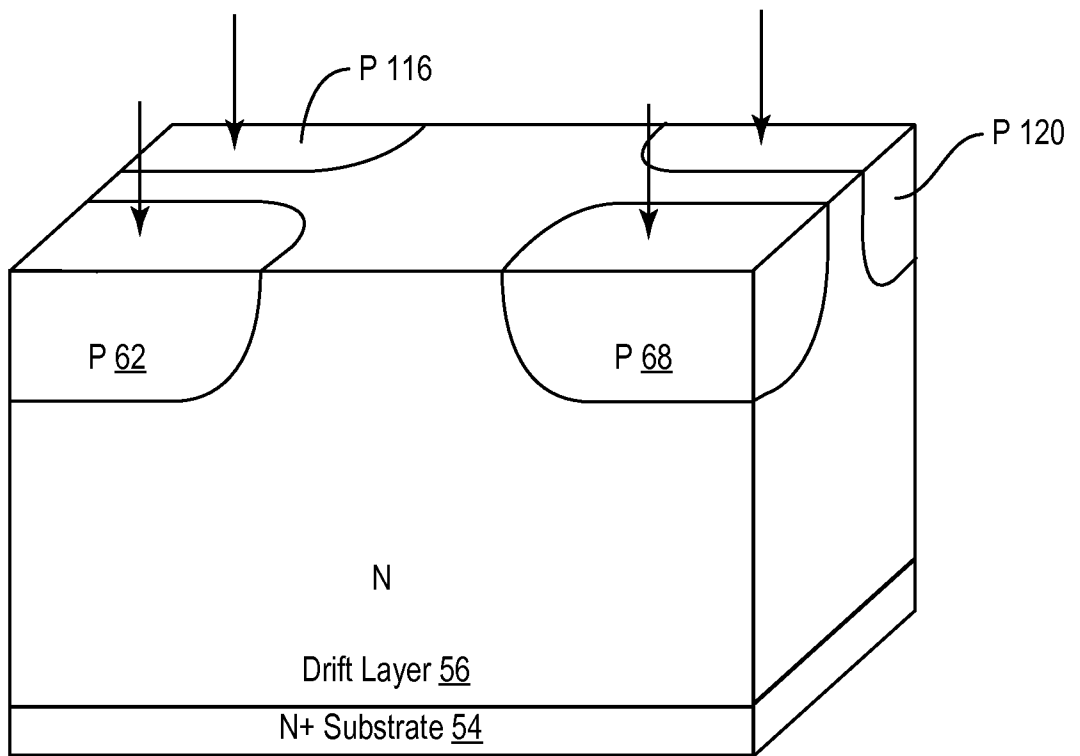


FIG. 15B

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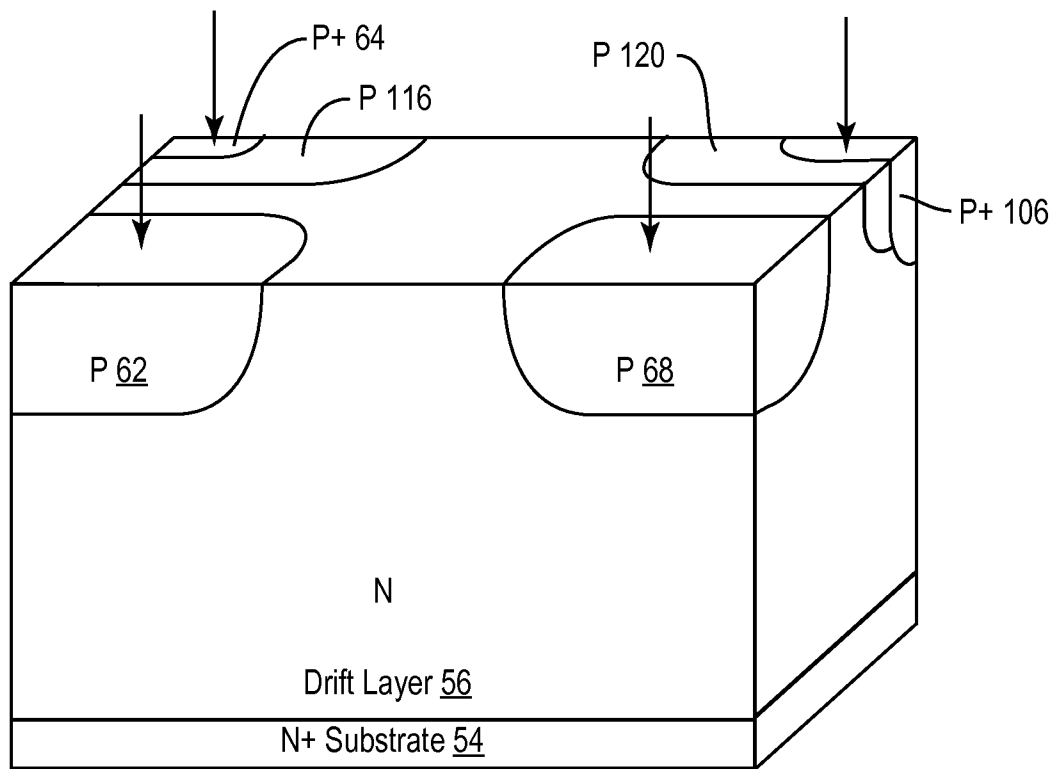


FIG. 15C

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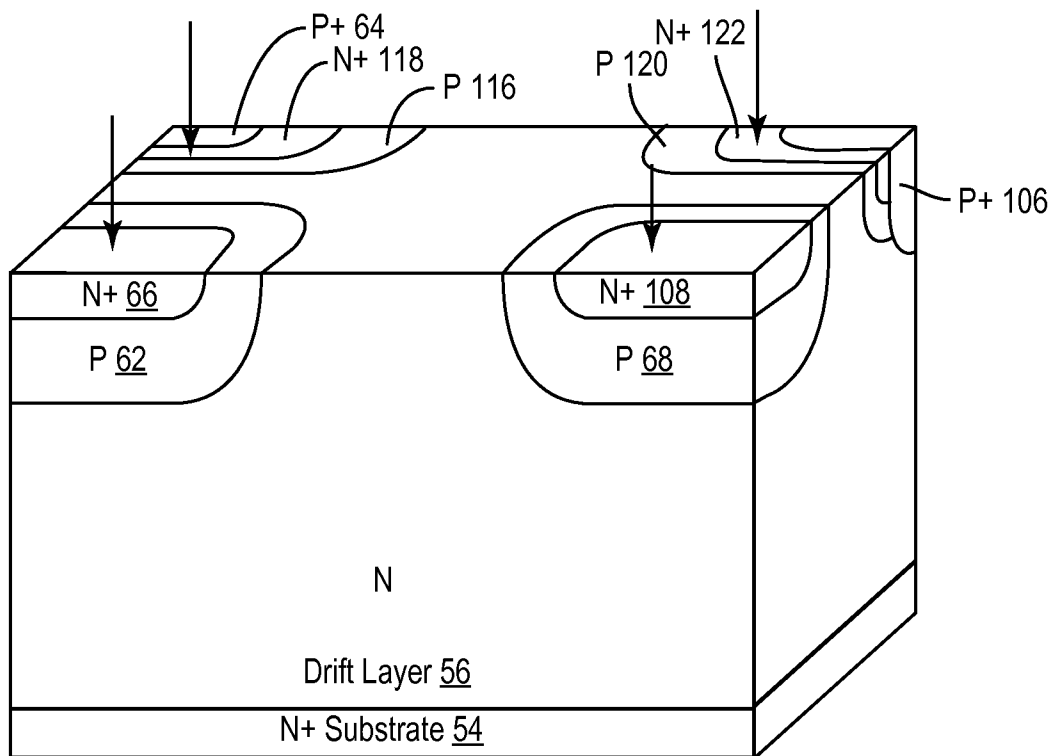


FIG. 15D

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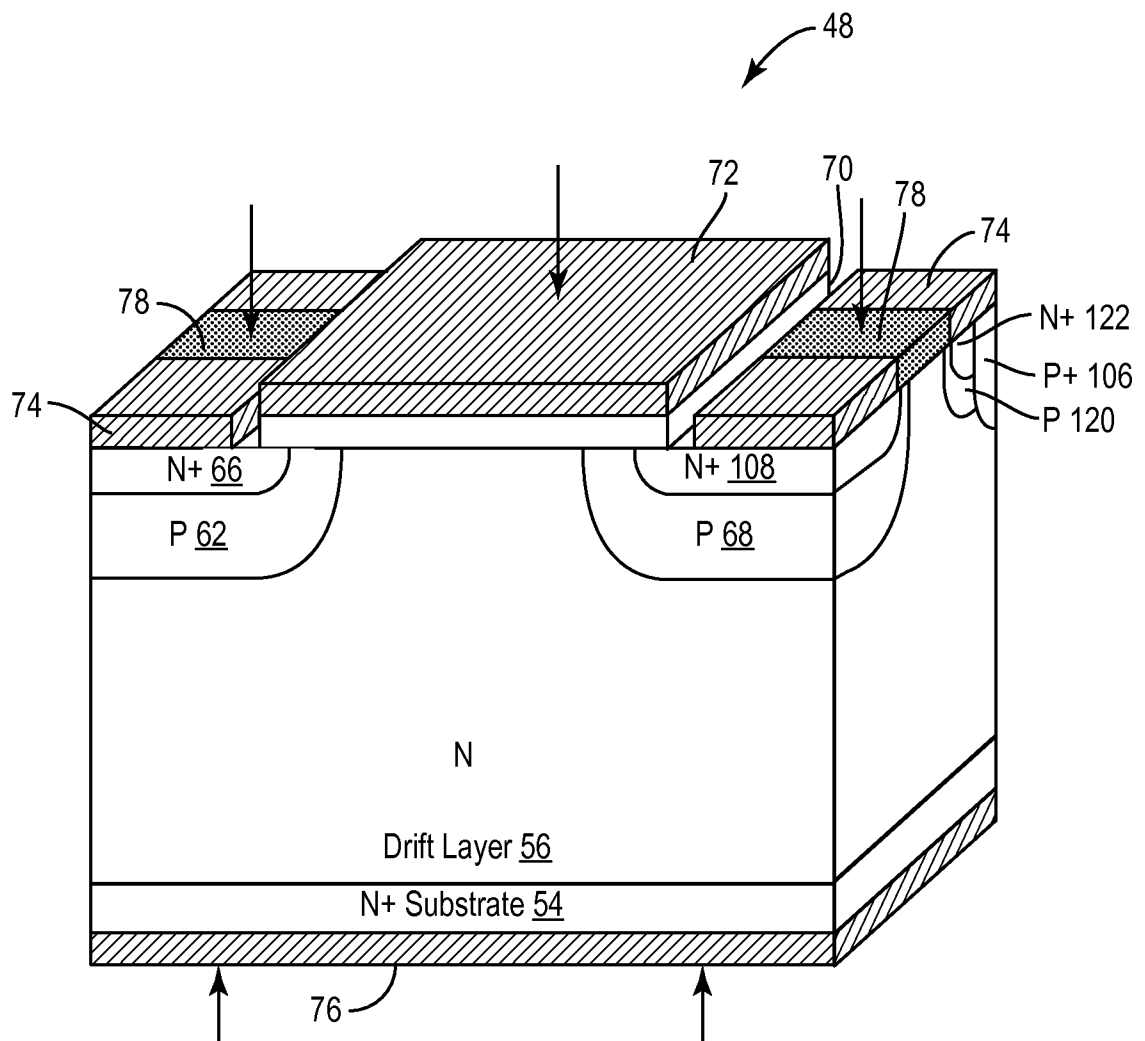
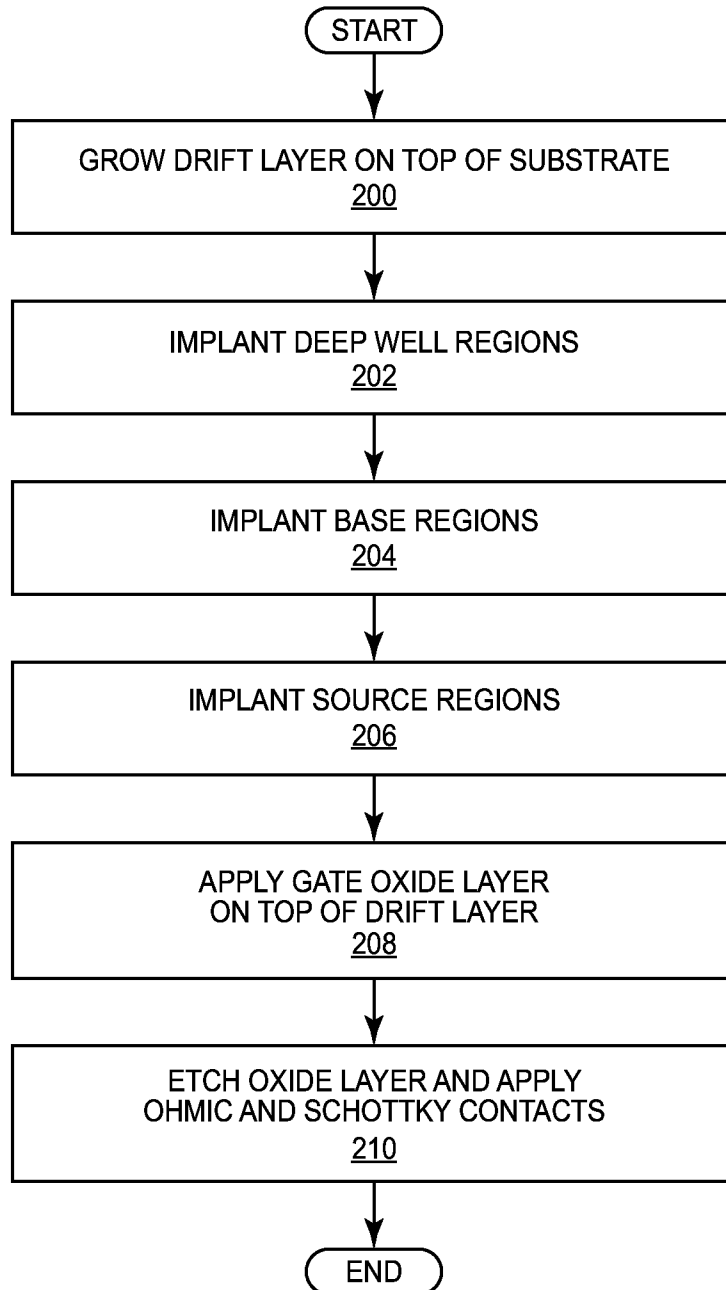


FIG. 15E

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**FIG. 16**

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/056093

A. CLASSIFICATION OF SUBJECT MATTER INV. H01L29/78 H01L21/336 ADD. H01L29/06 H01L29/08 H01L29/10 H01L29/16 H01L29/47		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H01L		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-Internal		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP S61 49474 A (MATSUSHITA ELECTRONICS CORP) 11 March 1986 (1986-03-11) abstract; figures 3,4 -----	1-30
X	EP 0 867 943 A1 (SGS THOMSON MICROELECTRONICS) 30 September 1998 (1998-09-30) column 5, line 28 - column 8, line 3; figures 4-16 column 8, line 11 - column 11, line 11; figures 17,18 -----	1-30
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents : "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 5 February 2015	Date of mailing of the international search report 18/02/2015	
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Morvan, Denis	

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2014/056093

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
JP S6149474	A	11-03-1986	NONE	

EP 0867943	A1	30-09-1998	EP 0867943 A1	30-09-1998
			JP H10284731 A	23-10-1998
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