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Declarations under Rule 4.17:

— *as to the identity of the inventor (Rule 4.17(i))*

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

Published:

— *with international search report (Art. 21(3))*

WO 2010/126490 A1

(54) Title: PERFORMING MULTIPLICATION USING AN ANALOG-TO-DIGITAL CONVERTER

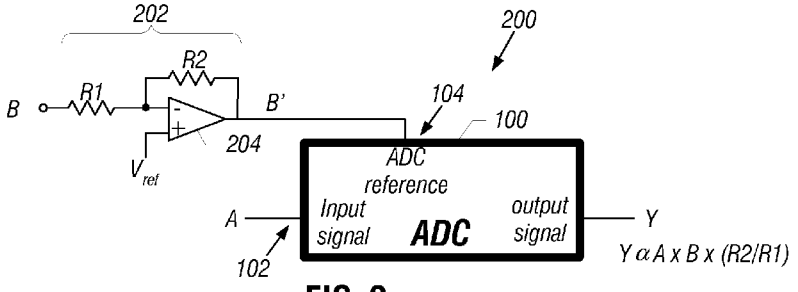

FIG. 2

(57) Abstract: A multiplier circuit to multiply a first signal with a second signal includes an analog-to-digital converter that has a first input and a second input. The first input is to receive the first signal. The multiplier circuit also has an inverting circuit having an input to receive the second signal, and an output connected to the second input of the analog-to-digital converter. An output value produced by a combination of the analog-to-digital converter and the inverting circuit is approximately a multiplication of the first signal and the second signal.

Performing Multiplication Using An Analog-To-Digital Converter

Background

[0001] In electronic devices, such as computer systems or other types of electronic devices, some operations involve multiplication of signals. Typically, such multiplication is performed using a microcontroller or other type of processor. However, under certain scenarios, using a processor to perform multiplications in electronic devices may not be efficient.

Brief Description Of The Drawings

[0002] Some embodiments of the invention are described with respect to the following figures:

Fig. 1 is a schematic diagram of an exemplary analog-to-digital (ADC) circuit;

Figs. 2-3 are schematic diagrams of circuitry according to some embodiments for performing multiplication of signals;

Fig. 4 is a block diagram of components in an electronic device that uses a multiplier circuit according to an embodiment;

Fig. 5 is a flow diagram of a process of multiplying signals according to an embodiment; and

Fig. 6 is a schematic diagram of circuitry according to another embodiment for performing multiplication of signals.

Detailed Description

[0003] In accordance with some embodiments, instead of using a processor (*e.g.,* a microcontroller, microprocessor, etc.) to perform multiplication of signals within an electronic device (*e.g.,* a computer, personal digital assistant, mobile telephone, storage system, communications switch, etc.), a multiplier circuit that includes an analog-to-digital converter (ADC) is used instead for enhanced efficiency. The multiplier circuit, used to multiply at least a first signal with a second signal, includes the ADC and an inverting circuit. The ADC has a first input to receive the first signal and a second input to receive an output of

the inverting circuit. The inverting circuit has an input to receive the second signal that is to be multiplied with the first signal. An output value produced by combination of the ADC and the inverting circuit is approximately a multiplication of the first signal and the second signal.

[0004] An ADC is a circuit to convert an analog signal to a digital signal. An "inverting circuit" refers to a circuit whose output decreases in a signal level (*e.g.,* voltage amplitude level) in response to an increase in signal level at the input of the inverting circuit, and vice versa.

[0005] Using the multiplier circuit according to some embodiments to perform multiplication operations instead of a processor in an electronic device, more efficient usage of the processor can be achieved, since processor cycles do not have to be consumed to perform the multiplication operations. Moreover, the electronic device may have a power savings mode, in which the processor of the electronic device may be placed into a lower power state where the processor may not be available to perform most or all of the operations of the processor. In a conventional electronic device in which a processor is used to perform multiplications, if a multiplication has to be performed, then the processor that is in a lower power state may have to be awakened (or turned "on") to allow the processor to perform the desired multiplication. This would result in increased and wasteful power consumption in the electronic device since the processor is being awakened just to perform the multiplication. If multiplication operations are regularly performed, then the processor would have to be regularly awakened to perform such multiplication operations.

[0006] Fig. 1 illustrates an exemplary ADC 100. The ADC 100 has a first input (signal input) 102 and a second input (reference voltage input) 104, where the signal input 102 is for connection to an analog input signal that is represented as A_{signal}. The reference voltage input 104 of the ADC 100 is for connection to a reference voltage, referred to as $V_{ADC\_reference}$. The output of the ADC 100 is a digital signal Y that includes a number of bits (represented as $Y_{00000000}$, $Y_{00000001}$, . . ., $Y_{11111110}$, $Y_{11111111}$). In the example of Fig. 1, the ADC 100 provides a 16-bit output signal Y. In different implementations, the output signal Y can include different numbers of output bits.

[0007] The ADC 100 basically takes a ratio of the analog input signal A_{signal} to the reference voltage $V_{ADC\_reference}$ ($A_{signal}/V_{ADC\_reference}$) to produce the digital output signal (Y).

In other words, the digital output signal (Y) is proportional to the ratio of A_{signal} to $V_{ADC\_reference}$, or $Y \propto \frac{A}{V_{ADC\_reference}}$. According to this relationship, the digital output signal Y is proportional to the analog input signal A_{signal}, which means that the digital output signal Y proportionately increases or decreases with the analog input signal A_{signal}.

[0008] On the other hand, the digital output signal Y has an inverse proportional relationship to the reference voltage $V_{ADC\_reference}$. An increase in the amplitude of $V_{ADC\_reference}$ (assuming A_{signal} stays constant) results in a decrease in the output value (Y), while a decrease in the amplitude of $V_{ADC\_reference}$ results in an increase in the output value (Y).

[0009] In the example shown in Fig. 1, the ADC 100 includes a series of resistors 106, and a number of comparators 108 to produce respective output bits of Y. The series of resistors 106 are connected between $V_{ADC\_reference}$ and a ground reference. The series of resistors effectively form voltage dividers such that different nodes along the series of resistors 106 are at different voltages.

[0010] The input analog signal A_{signal} is connected to the inverting (-) inputs of the comparators 108, while respective nodes of the series of resistors 106 are connected to corresponding non-inverting (+) inputs of the comparators 108. The comparators 108 output respective output bits based on a comparison of A_{signal} to the respective voltage level received at the non-inverting input of the comparator 108. It is noted that other components of the ADC 100 are not shown—the components depicted are provided to illustrate the relationship between A_{signal} and $V_{ADC\_reference}$.

[0011] In view of the fact that the ADC 100 effectively takes a ratio of the first input (102) to the second input (104), this characteristic can be used to form a multiplier circuit that uses the ADC 100. Such a multiplier circuit for multiplying input signals A and B is depicted as multiplier circuit 200 in Fig. 2, which includes the ADC 100 and an inverting circuit 202.

[0012] The inverting circuit 202 receives input signal B and applies an inverting operation on the signal to produce signal B'. The signal B' output from the inverting circuit

202 is then provided to the reference voltage input 104 of the ADC 100. The ADC 100 takes a ratio of A to B', which effectively is a multiplication of A and B.

[0013] In the embodiment of Fig. 2, the inverting circuit 202 includes an operational amplifier 204 and resistors R1 and R2. The resistor R2 is connected between the inverting (-) input of the operational amplifier 204 and the output of the operational amplifier 204, while the resistor R1 is connected between the inverting input of the operational amplifier 204 and input signal B. The non-inverting (+) input of the operational amplifier 204 is connected to an independent reference voltage V_{ref}, where V_{ref} is a generally fixed voltage level. The output (B') of the operational amplifier 204 is connected to the voltage reference input 104 of the ADC 100.

[0014] The gain of the operational amplifier 204 shown in Fig. 2 is -1, such that there is an inverse relationship between the input of the operational amplifier 204 and its output. In one example implementation, the relationship between B' and B is as follows: $B' = 2 \text{ x } V_{ref} - B$. An increase in B will cause a decrease in B', and vice versa.

[0015] The ADC 100 in Fig. 2 receives signal A at its analog signal input 102. Since the output Y of the ADC 100 has the relationship $Y \propto \frac{A}{V_{ADC\_reference}}$, as explained above in connection with Fig. 1, the relationship between Y and A, B is expressed as follows: $Y \propto \frac{A}{2 \text{ x } V_{ref} - B}$. According to this relationship, a change in the value of input signal A causes a proportional change in the output value Y. Moreover, the output value Y changes in proportion to $\frac{1}{1 - \Delta B / V_{ref}}$, where ΔB represents a change in the input signal B. In one example, a 1% increase in A results in a 1% increase in the output Y, while a 1% increase in B results in a $\frac{1}{1 - 0.01} = 1.010101\%$ decrease in the output Y.

[0016] The multiplier circuit 200 of Fig. 2 provides a relatively good approximation of the multiplication of input signals A and B for small variations in the value of B. The output

value Y is expressed as follows: $Y \propto A \times B \times \frac{R2}{R1}$. If R2 is selected to be equal to R1, then Y is basically an approximation of the scaled multiplication of just A and B.

[0017] The output value Y is considered an "approximation" of the multiplication of A and B because of the errors introduced due to possible variations of B. For small variations in B from a nominal value of B, the output value Y is a relatively accurate representation of the multiplication of A and B. However, for larger variations of B, an error is introduced such that the multiplication is less accurate (but still possibly usable for certain applications).

[0018] The table below illustrates the relationship of variations in B (ΔB)) to errors in the output value Y, according to one example (the table is provided for purposes of example, since relationships between ΔB and the error in Y are implementation-specific and can differ for different implementations):

ΔB	**Y error**
0.1%	0.0001%
1%	0.01%
2%	0.04%
5%	0.251%
10%	1.01%
20%	4.167%
50%	33.33%

[0019] If B varies by 0.1%, then the output Y has an error of approximately 0.0001%. If B varies by 1%, then the output Y has an error of approximately 0.01%. If B varies by 5%, then the output Y has an error of approximately 0.251%. If B varies by 10%, then the output Y has an error of approximately 1.01%. According to the example above, it can be seen that even with a 20% variation in B, the output error is still under 5%, which may be acceptable for certain applications.

[0020] Fig. 3 shows an alternative embodiment of a multiplier circuit 300 for multiplying input signals A and B. The multiplier circuit 300 includes the ADC 100 and an inverting circuit 302 that includes a linear regulator 304 and resistors R1, R2, and R3. The linear regulator 302 has an input to receive an input voltage (*e.g.,* 5V) and an output to provide an output voltage (represented as B') that is connected to the ADC reference voltage

input 104. The input signal B is provided through the resistor R3 to an adjustment input (ADJ) of the linear regulator 302. The resistors R1 and R2 are connected between B' and a ground reference, and the intermediate node between R1 and R2 is connected to a node of R3 and the ADJ input of the linear regulator 302.

[0021] The linear regulator 302 is a voltage regulator that operates in a linear region. The output voltage provided by the linear regulator 302 is fixed at a particular voltage based on the voltage level at the ADJ input of the linear regulator 304. Changes in voltage level at the ADJ input will cause a change to the output voltage level from the linear regulator 302.

[0022] In the arrangements shown in Fig. 3, an increase in the value of B causes a decrease in the value of B', and vice versa. Thus, this arrangement is considered to provide an inverting operation between B and B'.

[0023] The output value Y produced by the ADC 100 that is an approximate multiplication of A and B is scaled by a fixed scaling factor (FACTOR). In other words, the output (Y) of the multiplier circuit 300 is equal to A x B x FACTOR, where the value of FACTOR is dependent upon the values of R1, R2, and R3.

[0024] In an alternative implementation, an ADC may not include a reference voltage input 104 as is present in the ADC 100 of Fig. 2 or 3. For example, an ADC 100A that is part of a multiplier circuit 300A depicted in Fig. 6 includes a power supply input 104A (labeled "VCC" in Fig. 6) but does not include the reference voltage input 104 of Fig. 2 or 3. A power supply voltage is provided to the power supply input 104A of the ADC 100A to power the ADC 100A. In the embodiment shown in Fig. 6, the power supply voltage is provided by the inverting circuit 302 that includes the linear regulator 304 (described in connection with Fig. 3).

[0025] In this embodiment, the ADC reference voltage ($V_{ADC\ reference}$) is generated internally in the ADC 100A. The ADC reference voltage ($V_{ADC\ reference}$) is produced by a circuit 600 that is tied to the VCC input 104A. In some implementations, the circuit 600 can be a conductive line that connects $V_{ADC\ reference}$ to VCC. In another implementation, the circuit 600 may be a voltage divider circuit.

[0026] Since the internal ADC reference voltage ($V_{ADC\ reference}$) is proportional to VCC, the output Y of the ADC 100A is approximately a multiplication of A and B (and FACTOR), similar to the multiplier circuit 300 of Fig. 3.

[0027] The multiplier circuit shown in Fig. 2, 3 or 6 can be used in the context of power monitoring. In one example, as shown in Fig. 4, an electronic device 400 (*e.g.,* computer, personal digital assistant, mobile telephone, storage system, communications switch, etc.) includes the multiplier circuit 200 or 300, which receives input signals A and B. The input signal B can represent an input voltage, such as a power supply voltage used to power components of the electronic device, that is relatively stable (B has a relatively small range of variation such that the multiplier circuit 200, 300, or 300A can provide relatively accurate multiplications of A and B). The input signal A can be a representation of an electrical current, such as a current that is received from the power supply voltage used to power components of the electronic device, such as a power adapter (not shown) of the electronic device 400 or from another power source of the electronic device 400. The input signal A can have wide variations due to varying power consumption of the electronic device 400 (*e.g.*, the electronic device 400 transitioning between very active states and idle states, the electronic device 400 transitioning between different power states, etc.).

[0028] The multiplier circuit 200, 300, or 300A multiplies A and B to produce Y, which represents power (note that voltage multiplied by electrical current is equal to power). The output value Y (a digital value) is received by a controller 402, which includes a register 404 to store the output value Y. Multiple instances of the output value Y can be collected at different time points during a particular time interval. This allows the controller 402 to collect indications of power consumption over time in the particular time interval. The controller 402 can efficiently store such indications of power consumption, which can be later retrieved, such as by a power management system 406.

[0029] The power management system 406 is able to read the indications of power consumption collected in the register 404 to determine power consumption of the electronic device 400 over time. The power management system 406 can take actions based on what the power management system 406 observes in the register 404.

[0030] Although the power management system 406 is shown as being separate from the controller 402, note that the power management system 406 can be part of the controller 402 in an alternative embodiment.

[0031] Fig. 5 is a general flow diagram of a process performed in the electronic device 400 of Fig. 4. Input signals A, B are received (at 502) by the multiplier circuit 200 or 300. The multiplier circuit 200 or 300 is used (at 504) to multiply A and B. The output value of the multiplier circuit 200 or 300 is collected (at 506) in the register 404 of the controller 402. The register 404 can collect multiple output values over time to collect information about power consumption over time. Next, the power management system 406 retrieves (at 508) the output values from the register 404 to take an appropriate power management action in response to the detected power conditions. The power management action can include shutting off components, placing components into an inactive state or low power state, reporting power draw to the user, and so forth.

[0032] Although Figs. 4 and 5 show an embodiment in which power consumption calculated by the multiplier circuit 200, 300, or 300A is used by a power management system 406, it is noted that in difference implementations, the power consumption calculated by the multiplier circuit 200, 300, or 300A can be used for other purposes.

[0033] In the foregoing description, numerous details are set forth to provide an understanding of the present invention. However, it will be understood by those skilled in the art that the present invention may be practiced without these details. While the invention has been disclosed with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover such modifications and variations as fall within the true spirit and scope of the invention.

What is claimed is:

1. A multiplier circuit to multiply a first signal with a second signal, comprising:

an analog-to-digital converter having a first input and a second input, wherein the first input is to receive the first signal; and

an inverting circuit having an input to receive the second signal, and an output connected to the second input of the analog-to-digital converter,

wherein an output value produced by a combination of the analog-to-digital converter and the inverting circuit is approximately a multiplication of the first signal and the second signal.

2. The multiplier circuit of claim 1, wherein the inverting circuit includes an operational amplifier and resistors.

3. The multiplier circuit of claim 2, wherein the operational amplifier has an inverting input for connection to the second signal through a first of the resistors, wherein the operational amplifier has an output connected to the second input of the analog-to-digital converter, and wherein a second of the resistors is connected between the inverting input and output of the operational amplifier.

4. The multiplier circuit of claim 3, wherein the operational amplifier further has a non-inverting input for connection to a reference voltage.

5. The multiplier circuit of claim 3 or 4, wherein the first resistor has a resistance R1, the second resistor has a resistance R2, the first signal is represented as A, the second signal is represented as B, and wherein the output value is proportional to $A \times B \times \frac{R2}{R1}$.

6. The multiplier circuit of claim 1, wherein the inverting circuit includes a linear regulator having a voltage input for connection to a power supply voltage, and a voltage output connected to the second input of the analog-to-digital converter, and wherein the linear regulator has an adjustment input for connection to the second signal.

7. The multiplier circuit of claim 6, wherein an increase in a voltage of the second signal causes a reduction in a voltage of the output of the linear regulator.

8. The multiplier circuit of any of the preceding claims, wherein the second input is one of a voltage reference input and a power supply voltage input of the analog-to-digital converter.

9. A system comprising:

a controller; and

the multiplier circuit of any of the preceding claims, wherein the first signal is representative of an electrical current, and the second signal is a voltage, and wherein the controller is to receive the output value that is an indication of power.

10. The system of claim 9, wherein the controller is to accumulate multiple instances of the output value of the multiplier circuit at multiple time points in a given time interval.

11. The system of claim 9 or 10, further comprising:

a power management system to retrieve the output value from the controller, and in response to the output value, to effect a power management action.

12. The system of any of claims 9-11, wherein the voltage is a power supply voltage.

13. A method of multiplying a first signal with a second signal, comprising:

receiving the first signal at a signal input of an analog-to-digital converter, wherein the analog-to-digital converter further has a second input;

receiving the second signal at an input of an inverting circuit, wherein an output of the inverting circuit is connected to the second input of the analog-to-digital converter; and

providing an output from the analog-to-digital converter in response to the first signal and the output of the inverting circuit, wherein the output of the analog-to-digital converter is a digital value representing an approximate multiplication of the first signal and the second signal.

14. The method of claim 13, wherein receiving the second signal at the input of the inverting circuit comprises receiving the second signal at the inverting circuit that includes one of an operational amplifier and a linear regulator.

15. The method of claim 13 or 14, wherein the first signal represents an electrical current, and the second signal is a voltage, the method further comprising:

receiving the output of the analog-to-digital converter, wherein the output represents power.

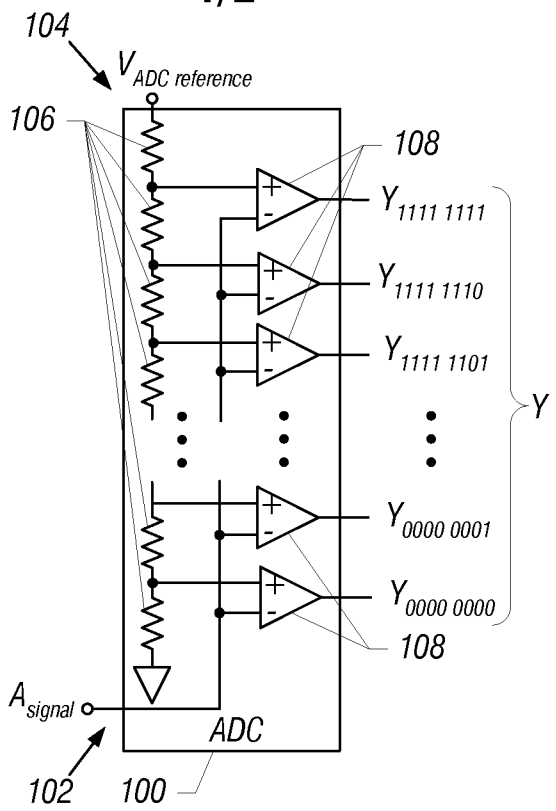

FIG. 1

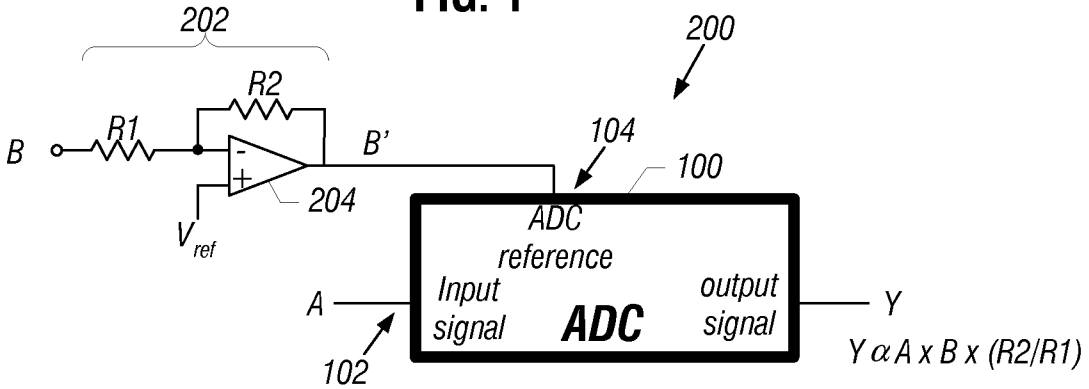

FIG. 2

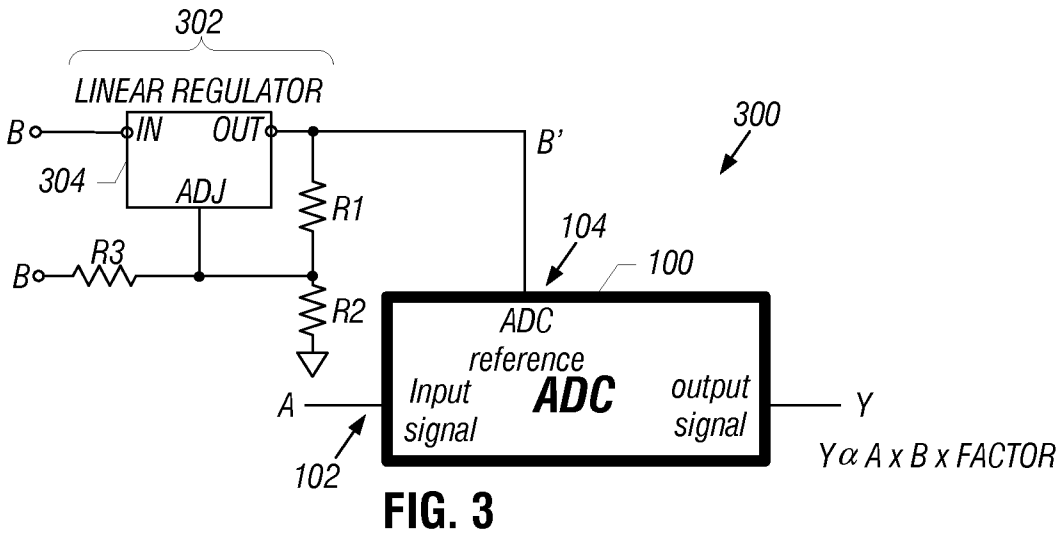

FIG. 3

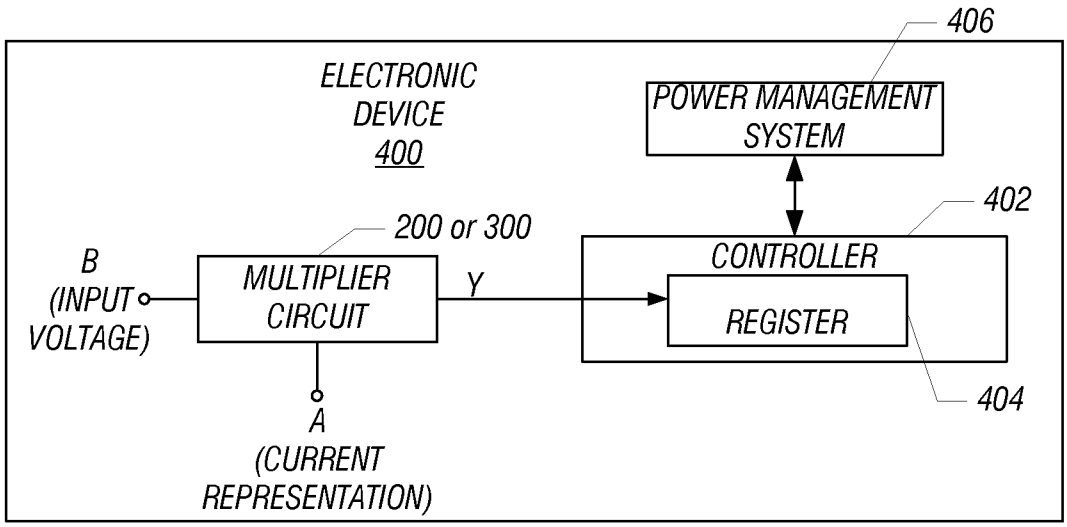

FIG. 4

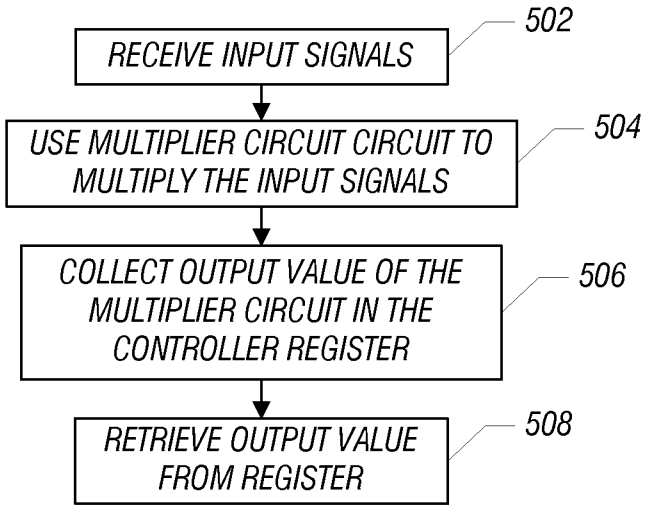

FIG. 5

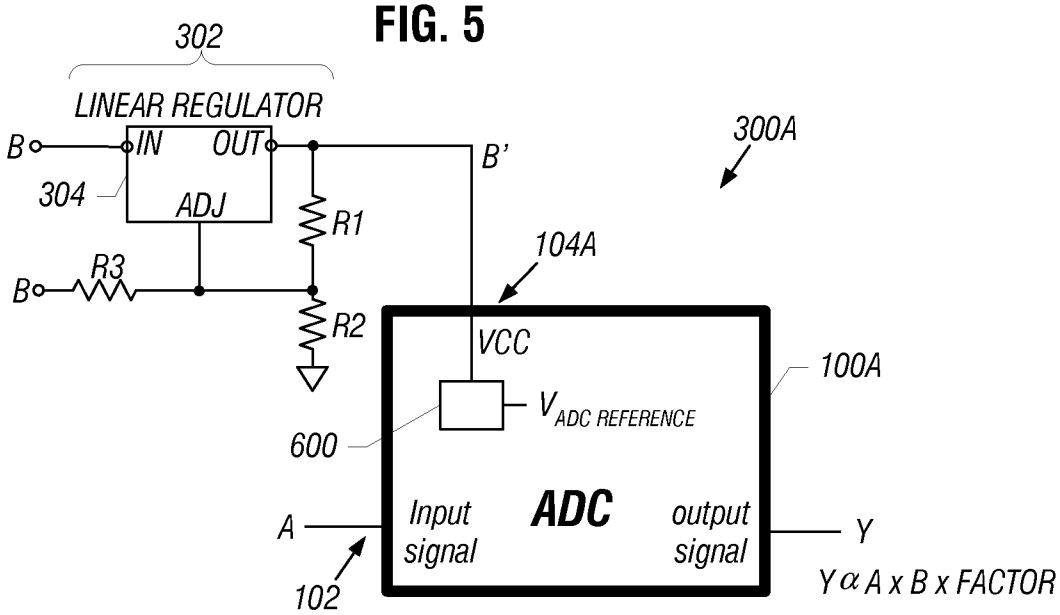

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2009/041980

A. CLASSIFICATION OF SUBJECT MATTER

G01R 31/00(2006.01)i, G06F 1/00(2006.01)i, G06F 17/00(2006.01)i, G02B 27/00(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 8 : G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean Utility models and applications for Utility models since 1975

Japanese Utility models and applications for Utility models since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS (KIPO internal)

"keywords : multiplier, cinverter, inverter"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 07446691 B2 (CHRISTOPHER PAUL) 04 NOVEMBER 2008 See abstract; claim 8; figure 8	1-7, 9-11, 13-15
A	US 2002-0125924 A1 (YASUHIRO KUROGOUCHI et al.) 12 SEPTEMBER 2002 See abstract; claim 3; figure 3	1-7, 9-11, 13-15
A	US 07184914 B2 (AKIO ATSUTA AND MASAHIKO IGAKI) 27 FEBRUARY 2007 See abstract	1-7, 9-11, 13-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 DECEMBER 2009 (24.12.2009)	**28 DECEMBER 2009 (28.12.2009)**
Name and mailing address of the ISA/KR Korean Intellectual Property Office Government Complex-Daejeon, 139 Seonsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	Authorized officer JEONG, So Yeon Telephone No. 82-42-481-5656

Form PCT/ISA/210 (second sheet) (July 2008)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2009/041980

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☒ Claims Nos.: 8,12
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required addtional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2009/041980

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 07446691 B2	04.11.2008	US 2008-238745 A1	02.10.2008
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