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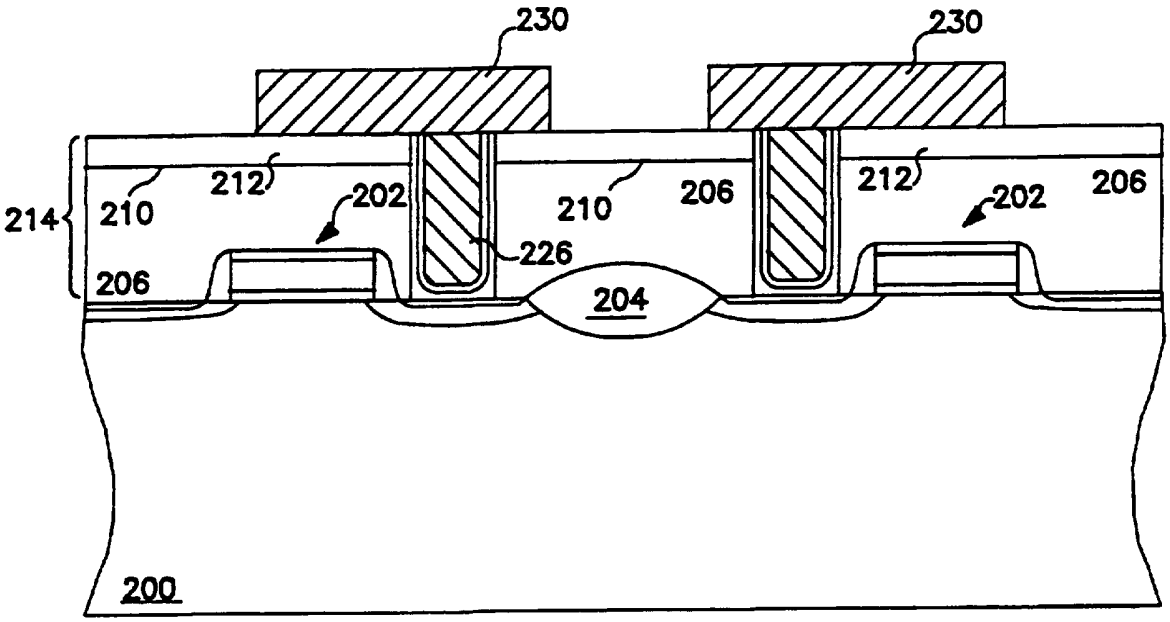

(57) Abstract

A method of forming a novel high density interconnection structure. According to the present invention, first an insulating layer (206) is formed over a semiconductor substrate. The first insulating layer is then planarized. Next, a second insulating layer (212) is formed above the first planarized insulating layer. An opening is then etched through the first and second insulating layers. A conductive material (226) is then deposited into the opening and onto the top surface of the second insulating layer. Next, the conductive material is polished back from the second insulating layer so as to form a conductively filled opening which is substantially planar with the second insulating layer.

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CAPPED INTERLAYER DIELECTRIC FOR CHEMICAL MECHANICAL POLISHING

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates to the field of semiconductor fabrication and more specifically to a method of forming an interconnect structure in an integrated circuit.

2. DISCUSSION OF RELATED ART

Today, integrated circuits are made up of literally millions of active devices formed in or on a silicon substrate or well. The active devices which are initially isolated from one another are later connected together to form functional circuits and components such as microprocessors. The devices are interconnected together through the use of well known multilevel interconnections. A cross-sectional illustration of an ideal multilevel interconnection structure 100 is shown in Figure 1. Interconnection structures normally have a first layer of metallization, an interconnection layer 102 (typically aluminum alloy with up to 3% copper), a second layer of metallization 104, and sometimes a third or even a fourth level of metallization. Interlevel dielectrics 106 (ILDs) such as silicon dioxide (SiO_2) are used to electrically isolate the different levels of metallization on silicon substrate or well 108. The electrical connections between different interconnection levels are made through the use of metallized vias 110 formed in ILD 106. In a similar manner, metal contacts 112 are used to form electrical connections between interconnection levels and devices formed in well 108. The metal vias 110 and contacts 112, hereinafter collectively referred to as

"vias" or "plugs", are generally filled with tungsten 114 and generally employ an adhesion layer 116 such as titanium.

A presently preferred interlevel dielectric film for ultra large scale integrated circuits is a borophosphosilicate glass (BPSG) film formed by atmospheric chemical vapor deposition (CVD). Atmospheric CVD BPSG layers are preferred because they can be formed very conformally and thereby can fill high aspect ratio gaps created by the high density placement of active devices on a semiconductor substrate. Atmospheric BPSG layers can fill high aspect ratio gaps without creating voids therein. Additionally, atmospheric BPSG layers are preferred because deposition machinery is relatively inexpensive as compared to other ILD equipment such as plasma enhanced chemical vapor deposition (PECVD) equipment. Additionally, atmospheric BPSG layers can be deposited relatively fast allowing for good wafer throughput.

A presently preferred method of forming plugs on vias 110 and 112 in an ultra large scale in an ULSI circuit is a tungsten plug process which utilizes chemical mechanical polishing. In a typical tungsten plug process, via holes are etched through an ILD to interconnection lines or semiconductor substrate formed below. Next, a thin adhesion layer such as titanium nitride is formed over the ILD and into the via hole. Next, a conformal tungsten film is blanket deposited over the adhesion layer and into the via. The deposition is continued until the via hole is completely filled with tungsten. Next, a metal film formed on top of the surface of the ILD is removed by chemical mechanical polishing to thereby form a metal via or plug. Such processes are preferred because they can fill high aspect ratio vias which are required to make electrical connection to densely packed active devices formed below.

A problem with tungsten plug processes and atmospheric BPSG ILD layers is that they are incompatible with one another. The problem is that tungsten polishing processes are not selective enough to atmospheric BPSG ILD layers. As such, when polishing back the tungsten layer, a substantial amount of ILD layer can be removed from

areas which clear tungsten first. If too much ILD is lost during the tungsten plug process, shorts can develop between active devices and the first level metallization or between levels of metallization. Thus, present processes which utilize both atmospheric BPSG layers and chemical mechanical tungsten plug processes are unreliable and unmanufacturable.

As such, what is desired is an interconnection scheme whereby an atmospheric BPSG layer and a tungsten plug process can be utilized together.

SUMMARY OF THE INVENTION

The present invention describes a method of forming a novel interconnection structure for an integrated circuit. According to the present invention, a first oxide layer comprising boron and phosphorous formed by atmospheric CVD is deposited over the semiconductor substrate. The first oxide layer is then chemically mechanically polished (CMP) to form a planarized surface. Next, a second undoped oxide layer formed by plasma enhanced CVD is deposited on the planarized first oxide layer. An opening is then etched through the first and second oxide layers. A conductive layer comprising tungsten is then deposited into the opening and over the second oxide layer. Finally, the conductive layer is polished back from the second oxide layer to form a filled opening which is substantially planar with the second oxide layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is an illustration of a cross-sectional view showing a prior art interconnection structure.

Figure 2a is an illustration of a cross-sectional view showing a semiconductor substrate having a plurality of devices formed thereon.

Figure 2b is a cross-sectional illustration of a semiconductor substrate showing the formation of a first interlayer dielectric on the substrate of Figure 2a.

Figure 2c is an illustration of a cross-sectional view showing the planarization of the first interlayer dielectric on the substrate of Figure 2b.

Figure 2d is a cross-sectional illustration showing the formation of a second interlayer dielectric on the substrate of Figure 2c.

Figure 2e is an illustration of a cross-sectional view showing the formation of openings in the substrate of Figure 2d.

Figure 2f is an illustration of a cross-sectional view showing the formation of a via fill material on the substrate of figure 2e.

Figure 2g is an illustration of a cross-sectional view showing the polishing of the via fill material on the substrate of Figure 2f to form filled contact openings.

Figure 2h is an illustration of a cross-sectional view showing the formation of a level of metallization on the substrate of Figure 2g.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

The present invention discloses a novel method of fabricating an interconnection structure in an integrated circuit. In the following description, numerous specific details such as specific process steps, materials, and dimensions, etc. are set forth in order to provide a thorough understanding of the present invention. It will be obvious, however, to one skilled in the art, that the present invention may be practiced without these specific details. In other instances, well known integrated circuit manufacturing steps and equipment have

not been set forth in detail in order to not unnecessarily obscure the present invention.

The present invention is a novel method of forming an interconnection structure for an integrated circuit. The preferred embodiment of the present invention enables an atmospheric chemical vapor deposited BPSG layer to be used with a tungsten plug process utilizing chemical mechanical polishing (CMP) to provide a manufacturable, high density interconnect structure.

According to the preferred embodiment of the present invention, a semiconductor substrate 200 is provided. Devices 202, such as metal oxide semiconductor (MOS) transistors are formed in the semiconductor substrate 200. Preferably, silicide is formed by a self-aligned process on the source, drain, and poly gates of the MOS devices to improve contact resistance and device performance. The active devices are initially isolated from one another by field oxide regions 204. Although only MOS transistors are shown, substrate 200 may contain other completed or partially completed active and passive devices such as, but not limited to, bipolar transistors, thin film transistors, capacitors, and resistors, etc. Additionally, although semiconductor substrate 200 is preferably a monocrystalline silicon substrate, substrate 200 can comprise other semiconductor material such as, but not limited to, gallium arsenide and germanium and may contain additional deposited semiconductor materials such as epitaxial silicon layers.

The first step according to the present invention, as shown in Figure 2b, is to form an interlayer dielectric (ILD) 206 over substrate 200 and devices 202 formed thereon. The purpose of ILD 206 is to electrically isolate devices 202 from subsequently formed metallization used to interconnect the devices into a functional circuit. ILD 206 is preferably a borophosphosilicate glass (BPSG) formed by atmospheric chemical vapor deposition (CVD). An atmospheric BPSG layer is preferred because it can be formed conformally to the underlying topography and therefore fill small gaps between adjacent devices 202 without creating voids therein. ILD 206 is preferably formed by

atmospheric CVD in a WJ999 TEOS machine using a tetraethyl orthosilicate (TEOS), oxygen (O_2), phosphine (PH_3) and diborane (B_2H_6) chemistry to produce a silicon dioxide (SiO_2) film with an approximately 3% boron and 6.3% phosphorous concentration. An approximately 18,000Å oxide layer is formed.

Next, ILD 206 is preferably densified using rapid thermal processing (RTP). One of the goals of densifying ILD 206 is to accelerate the incorporation of dopants into the oxide to stabilize it. By using a RTP process, steam flow processing can be eliminated. The use of steam flow processing is undesirable because it grows a thin oxide at the BPSG/silicide interface which consumes a substantial portion of the silicide during its growth. By utilizing a RTP process with an N_2 ambient for densification, no oxide grows at the BPSG/silicide interface, enabling the scaling of silicide thickness formed on the source drain regions to accompany scaling of the source drain junction depths. The use of RTP for densification improves the thermal budget, and in turn, transistor performance over steam furnace glass flow cycles. Additionally, the RTP process is preferably performed at a temperature less than 875° in order to prevent agglomeration of the silicides. That is silicide 203 cannot tolerate higher densification temperatures.

As shown in Figure 2b, the top surface 208 of ILD 206 is nonplanar due to the underlying topography created by devices 202 and isolation regions 204. The nonplanar topography is due to the conformal deposition nature of BPSG layer 206. Additionally, the nonplanar topography is also due to the fact that steam flow processing is preferably not used in the present invention. Steam flow steps generally help to smooth or planarize the topography of BPSG layers. Because the top surface 208 of ILD 206 is nonplanar, it is planarized as shown in Figure 2c. ILD 206 is preferably planarized by chemical mechanical polishing because it creates global planarization as opposed to only local planarization associated with reflow and etch back processes. ILD 206 is preferably polished back from 18,000Å to approximately 4500Å ± 1500Å over devices 202 to form a planar

surface 210. By initially forming ILD 206 very thick, a good amount of margin is provided for the chemical mechanical polishing process.

According to the preferred embodiment of the present invention, ILD 206 is chemically mechanically polished using a slurry comprising silica in a solution of potassium hydroxide and water ($KOH + H_2O$) using a Westech 372M polisher. It is to be appreciated however, that any well known CMP process can be used to planarize ILD 206.

Global planarization of ILD 206 is desired because it forms a very planar ILD surface 210 which enables the shrinking of metal lines, as well as increasing the number of metallization layers which may be used in a process. It is to be appreciated that the stacking of additional interconnection layers on top of one another produces a more rugged topography. Because of the planarization of ILD 206, fabrication problems such as poorly resolved contact/via openings, and/or metal lines, poor metal step coverage, electromigration, and metal stingers are reduced in the present invention. Additionally, the use of chemical mechanical planarization achieves global planarity which sets up a series of positive repercussions such as enabling subsequent use of very planar tungsten plug polishing technology for contact/via filling which in turn allows metal 1 dimensions to be more uniform and subsequent ILD thicknesses to be minimized.

Next, according to the present invention, a second ILD layer 212 is deposited onto ILD layer 206 as shown in Figure 2d. ILD 212 is formed of a different dielectric material than ILD 206. As will be described in more detail below, ILD 212 is a material which polishes significantly slower (8x) than does ILD 206 during a subsequent polishing step for plug formation. ILD 212 and ILD 206 together form a composite ILD 214 which is used to isolate subsequent electrical connections. As such, the final total thickness of composite ILD 214 must be sufficient to electrically isolate subsequently formed metallization from devices 202. Because ILD 212 is formed thin, approximately 2000Å, and is formed on a planarized surface 210 of ILD

206, composite dielectric 214 exhibits a very planar top surface 215 without any additional planarization.

In the preferred embodiment of the present invention where ILD 206 comprises an atmospheric CVD deposited BPSG layer, ILD 212 is preferably an undoped oxide layer formed by plasma enhanced chemical vapor deposition (PECVD) utilizing TEOS and O_2 source gases in an AMAT 5000 deposition machine. It is to be appreciated that plasma enhanced undoped TEOS oxide layers cannot be formed conformally enough to fill high aspect ratio gaps associated with modern high density integrated circuits. PECVD undoped oxide layer 214, however, can be formed uniformly and consistently enough to provide a planar capping layer 212 for planarized ILD layer 206 used to fill the high aspect gaps between adjacent devices 202. A valuable characteristic of plasma enhanced CVD processes is that they form dense dielectric layers. Dense oxide layers tend to polish at a slower rate than do less dense oxide layers such as doped atmospherically deposited CVD oxide layers.

Next, as shown in Figure 2e, openings 216 are formed through ILD 206 and ILD 212. Openings 216 provide vias or contact openings to allow electrical connections through ILD 206 and ILD 212 to devices 202 formed below. Any well known method can be used to form openings 216 such as reactive ion etching (RIE) in a LAM Research 4500 etcher with a freon based chemistry.

Because the goal of the present invention is to fabricate high density integrated circuits, devices 202 must be packed closely together necessitating the formation of narrow (approximately 0.4 microns wide) and closely spaced contact/via openings 216. Since composite ILD 214 must be sufficiently thick to isolate devices 202 and because of the desire to form narrow openings, high aspect ratio (i.e. deep and narrow openings) are preferably formed. The best method presently available to fill such high aspect ratio openings is to use plug technology.

Next, as shown in Figure 2e, a contact fill material 218 is blanket deposited over undoped oxide layer 212 and into opening 216. The

preferred contact fill material 218 is tungsten because it can be formed very conformally allowing for the filling of high aspect ratio openings without the creation of voids therein. When using a tungsten layer for via filling, it is preferable to form an adhesion layer before tungsten deposition. Adhesion layers help tungsten adhere to the composite ILD, lowers contact resistance, and provides a good ohmic contact.

According to the preferred embodiment of the present invention, a thin composite titanium/titanium nitride adhesion layer is used. First, an approximately 200Å titanium layer 222 is sputter deposited by well known means over ILD 212 and along the sidewalls and bottom of openings 216. Next, an approximately 600Å titanium layer 224 is sputter deposited by well known means over titanium layer 222. Next, a conformal layer of tungsten 220 is formed by first forming an initial seed layer of (approximately 300Å) of tungsten by CVD using a silane (SiH_4) reduction of tungsten hexafluoride (WF_6) followed by the formation of the bulk (approximately 4500Å) of the tungsten layer by CVD using a hydrogen (H_2) reduction of WF_6. Thus, according to the preferred embodiment of the present invention, contact fill material 218 preferably comprises a tri-layer metal comprising titanium, titanium nitride, and tungsten. It is to be appreciated that other contact fill materials a combination of materials may be used to fill openings 216.

Next, as shown in Figure 2g, contact fill material 218 is chemically mechanically polished back to remove contact fill material 218 from the top surface of ILD 212 and to thereby form a filled opening or plug 226 which is substantially planar with the top surface of ILD 214. When the contact fill material is tungsten, the tungsten layer is preferably chemically mechanically polished back using a chemistry comprising 0.01 to 0.3 molar potassium fericyanide ($K_3Fe(CN_6)$) and 1-25% silica by weight. A water diluted version (9:1) of the tungsten slurry can be used to polish off titanium nitride adhesion layer 224. Additionally, a slurry comprising approximately 0.5 molar potassium fluoride and approximately 0.5% silica by weight

is preferably used to polish off titanium adhesion layer 222 from ILD 212. The above specified slurries are preferred in the present invention because they allow for uniform and consistent polishing of tungsten layer 220 and adhesion layers 222 and 224 and the formation of a plug 226 without substantially recessing plug 226 beneath ILD 212 or without causing an "etch out" of plug 226. Details on the methodology and slurries for polishing tungsten, titanium nitride and titanium film utilizing the above specified slurries are described in full in U.S. Patent No. 5,340,370 assigned to the present assignee, which is hereby incorporated by reference.

An important aspect of the present invention is for the plug polishing process to be selective to ILD capping layer 212. That is, it is important for ILD capping layer 212 to polish at a rate significantly slower than contact fill material 218. In this way, nonuniformities exists across substrate 300, those areas which clear contact material first to reveal ILD 212 will essentially stop polishing (or least retard the polishing) while other areas with contact fill material still present will continue to polish. Capping layer 212 allows "overpolishing" to be utilized in the present invention to assure substantially complete removal of contact fill material 218 across the entire substrate 300 without significantly polishing away local areas of ILD 214. In this way, a plug polishing process can be reliably utilized without worrying about overpolishing causing excessive ILD loss. It is to be noted that on some areas of substrate 200 where high polish rates are experienced or thin layers formed, capping layer 212 can be completely polished off during plug formation. Capping layer 212 should provide enough selectivity to sufficiently retard the polishing process to preserve enough ILD to fabricate reliable interconnects. In the preferred embodiment of the present invention, the tungsten polishing process exhibits about a 32:1 tungsten to PECVD oxide selectivity. The use of ILD capping layer 212 makes the interconnection process of the present invention both manufacturable and reliable.

It is to be noted that the polish rates and selectivities provided herein were calculated by polishing thin films blanket deposited over

an entire wafer. Selectivities on portions of the substrate will actually be much lower due to a "dishing" effect which occurs during plug polishing. "Dishing" is due to the fact that ILDs between densely placed contacts polish much faster than do ILDs between less densely placed contacts. As such, "dishing" causes a substantial reduction in polish selectivity in areas with a high density of contacts. Thus, care should be taken to ensure that capping layer 212 provides enough selectivity to counter any "dishing" effect.

In the preferred embodiment of the present invention, ILD capping layer 212 is an undoped oxide layer formed by plasma enhanced CVD. Plasma enhanced CVD processes produce dense oxide layers. While atmospheric CVD processes produce oxide layers which are substantially less dense. Additionally, doped oxide layers tend to be less dense than undoped oxide layers. Dense oxide layers generally polish at slower rates than do less dense oxide layers. In the preferred embodiment of the present invention, undoped PECVD oxide capping layer 212 polishes about eight times slower during tungsten plug polishing than does doped atmospheric CVD oxide layer 206 used for the bulk of composite ILD 214.

Thus, by placing undoped PECVD oxide capping layer 212 on doped atmospheric CVD oxide layer 206, the tungsten plug polishing process is much more selective to composite ILD 214 than if only a doped atmospheric CVD oxide layer were utilized. It is to be appreciated, that although atmospheric BPSG layers are incompatible with tungsten polishing processes, they are required to fill small aspect ratio gaps created by high density placement of devices 202. Additionally BPSG layers formed by atmospheric CVD are significantly more economical than PECVD oxides because they require less expensive machinery and because they can be formed faster (i.e. they provide better wafer throughput). The use of a thin undoped PECVD oxide capping layer 212 enables the use of a low density, high aspect ratio filling atmospheric CVD BPSG layer with a tungsten plug process.

It is to be appreciated that both atmospheric CVD BPSG layers and tungsten plug processes are required to fabricate modern ultra high density integrated circuits. Atmospheric BPSG layers are used to fill high aspect ratio gaps created by dense placement of devices 202 and tungsten plugs are used to fill high aspect ratio contact openings necessary to make contact to the densely placed devices 202.

Next, as shown in Figure 2h, metal interconnects are formed on ILD capping layer 212 and over an electrical contact with plug 226. Interconnects 230 can be formed by any well known means such as by blanket depositing an aluminum layer (and adhesion layers if desired) over ILD 212 and plugs 226 and then etching the aluminum layers into individual metal lines 230 utilizing well known photolithographic techniques. At this point, the interconnection structure of the present invention is complete.

As is readily apparent in Figure 2h, a very planar high density interconnection structure has been fabricated. Because plug 226 is substantially planar with ILD 214, a planar interconnection layer 230 is formed. It is to be appreciated that the present invention can be utilized to form additional interconnection and via/contact layers if desired. Because of the very planar nature of the interconnect scheme of the present invention and almost unlimited number of metallization layers can be fabricated allowing for the interconnection of a large number of discrete devices formed in a semiconductor substrate such as required in ULSI circuits. Additionally, although the present invention has been described with respect to a preferred embodiment where a PECVD oxide capping layer is formed over an atmospheric CVD BPSG layer in order to increase the ILD selectivity to a tungsten plug process, it is expected that the concepts of the present invention may be applied to other semiconductor processes. That is, the present invention can generally be applied to any process which utilizes a chemical mechanical polishing (CMP) process to polish back one material to fill an opening in a second material and where the selectivity of the polishing process is not sufficiently selective to the second material to provide a robust process. In such cases, a suitable

capping layer is provided to increase the selectivity of the polishing process to provide a reliable process. For example, the present invention can be used to form interconnects, such as interconnects 230, by blanket depositing an aluminum layer over an ILD with an opening formed therein and then polishing back the aluminum layer to form metal interconnects. Additionally, the present invention can be used to increase the selectivity in a CMP process used to fill trenches for isolation or to form capacitors.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention. The present invention is not expected to be limited to the specific dimensions, materials, and slurries described herein. The specification and drawings are accordingly to be regarded in an illustrative rather than a restrictive sense.

Thus, a method and structure for enabling the use of a BPSG layer with a tungsten plug chemical mechanical polishing process has been described.

IN THE CLAIMS

We claim:

1. A method of fabricating an interconnection structure comprising the steps of:

forming a first insulating layer;

planarizing said first insulating layer;

forming a second insulating layer above said first planarizing insulating layer;

forming an opening in said first and second insulating layer;

depositing a conductive material into said opening and onto said second insulating layer; and

polishing said conductive material from said second insulating layer so as to form a conductive filled opening which is substantially planar with said second insulating layer, wherein said polishing step utilizes a polishing process which polishes said first insulating layer faster than said second insulating layer.

2. The method of Claim 1 wherein said second insulating layer comprises a plasma enhanced CVD layer.

3. The method of Claim 1 wherein said first insulating layer is a BPSG layer formed by atmospheric chemical vapor deposition utilizing a TEOS source gas.

4. The method of Claim 1 wherein said second insulating layer comprises an undoped oxide layer formed by plasma enhanced chemical vapor deposition utilizing a TEOS source gas.

5. The method of Claim 5 wherein said conductive layer comprises tungsten.

6. The method of Claim 1 wherein said first insulating layer is an atmospheric CVD oxide layer and said second insulating layer is a plasma enhanced CVD oxide layer.

7. A method of forming an interconnection structure on a semiconductor substrate comprising the steps of:

forming a first oxide layer comprising boron and phosphorous above said substrate;

planarizing said first oxide layer;

forming oxide layer on said planarized first oxide layer;

forming an opening in said first oxide layer and said undoped oxide layer;

depositing a conductive layer comprising tungsten in said opening and over said undoped oxide layer; and

polishing said conductive layer so as to remove said conductive layer from said undoped oxide layer to thereby form a filled opening which is substantially planar with said undoped oxide layer.

8. The method of Claim 7 wherein said first oxide layer is formed by atmospheric chemical vapor deposition utilizing a TEOS source gas.

9. The method of Claim 7 wherein said undoped oxide layer is formed by plasma enhanced chemical vapor deposition utilizing a TEOS source gas.

10. The method of Claim 7 further comprising the step of:

forming an interconnection over said undoped oxide layer and over said filled opening.

11. The method of Claim 7 wherein said polishing step utilizes a slurry which polishes said first oxide layer faster than said second oxide layer.

12. The method of Claim 11 wherein said slurry comprises (?).

13. The method of Claim 7 further comprising the steps of:

rapid thermal processing prior to planarizing said first oxide layer in a N_2 ambient to densify said first oxide layer.

14. The method of Claim 7 wherein said first oxide layer is planarized by chemical mechanical polishing.

15. A method of forming contacts to devices formed on a semiconductor substrate, said method comprising the steps of:

forming a first oxide layer on said substrate and over said devices, said first oxide layer comprising boron and phosphorous and formed by atmospheric CVD utilizing a TEOS source gas;

chemical mechanical polishing said first oxide layer to form a planarized first oxide layer;

depositing a capping oxide layer on said planarized first oxide layer, said capping oxide layer being substantially undoped and formed by plasma enhanced chemical vapor deposition utilizing a TEOS source gas;

etching contact openings through said capping layer and said planarized first oxide layer to said devices;

blanket depositing a conductive fill material comprising tungsten over said capping layer and into said contact opening; and

chemical mechanical polishing said conductive fill material so as to remove said conductive fill material from said capping layer to form filled contacts, wherein said chemical mechanical polishing of said conductive fill material polishes said first oxide layer faster than said capping oxide layer.

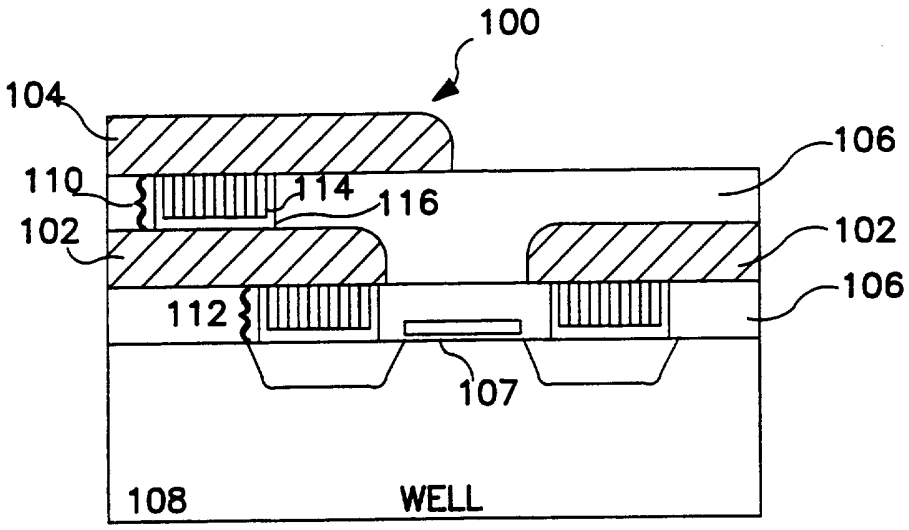

FIG. 1
PRIOR ART

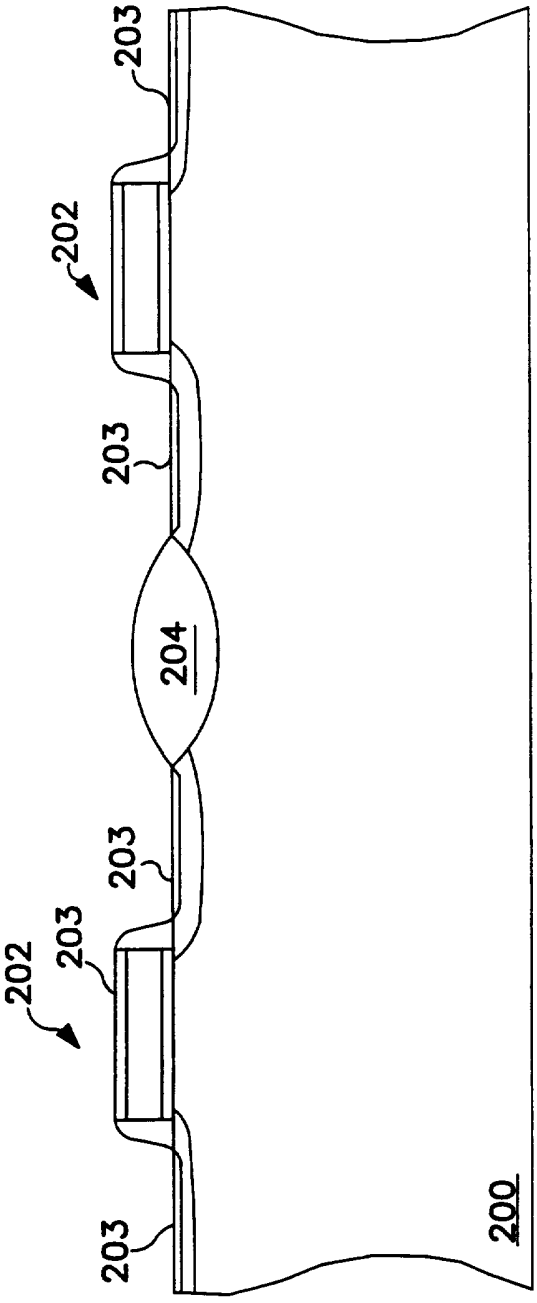

FIG. 2A

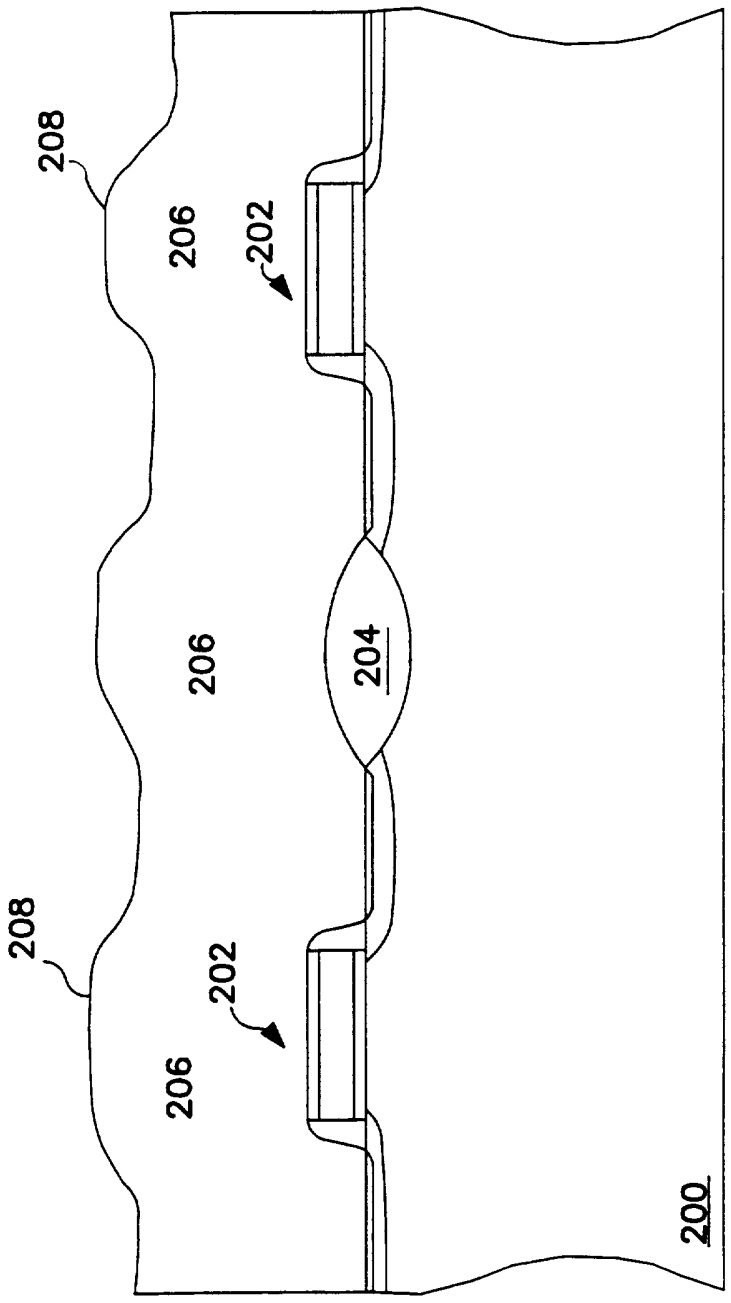

FIG. 2B

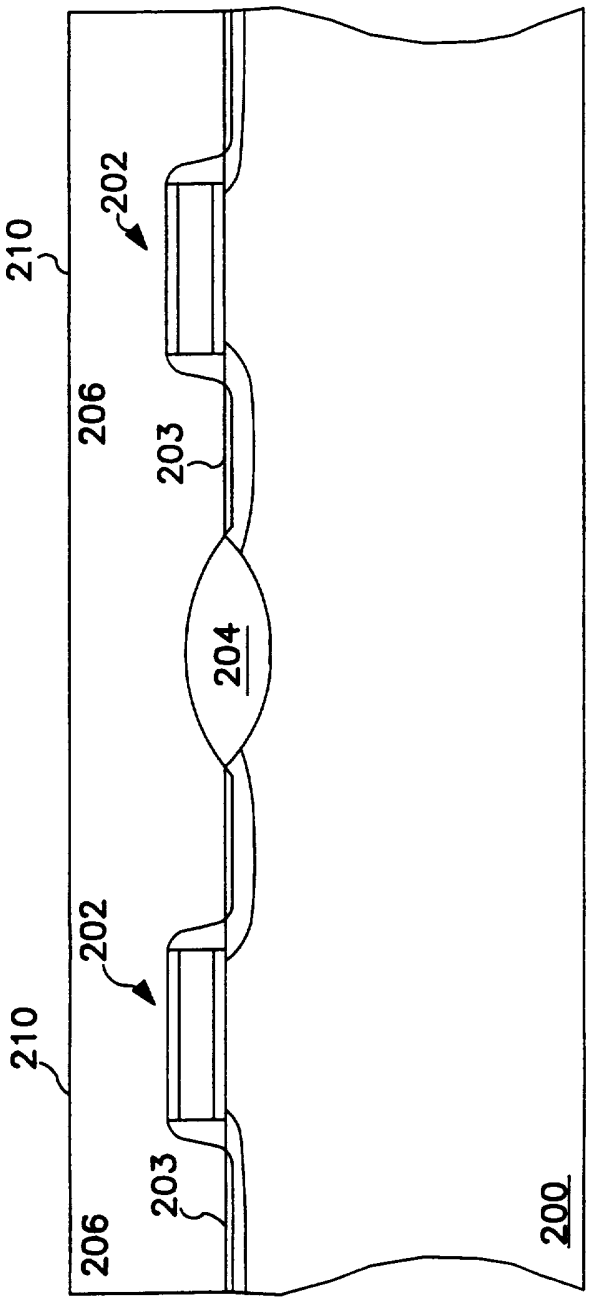

FIG. 2C

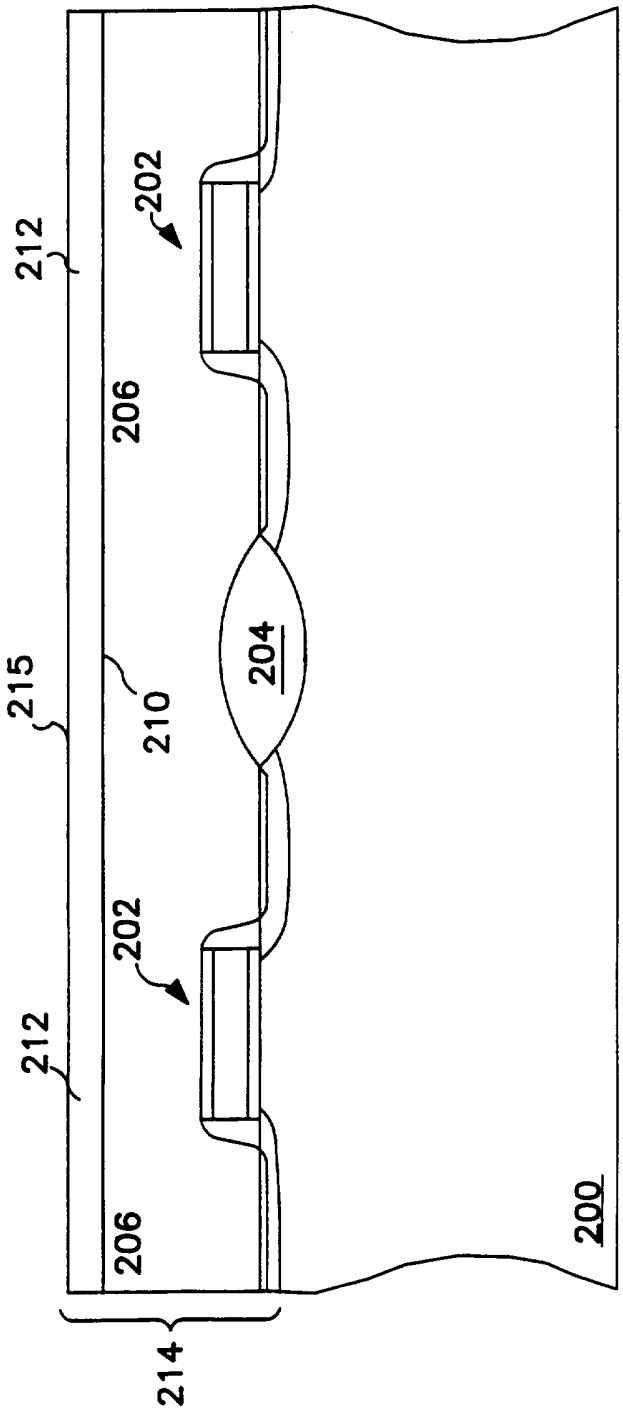

FIG. 2D

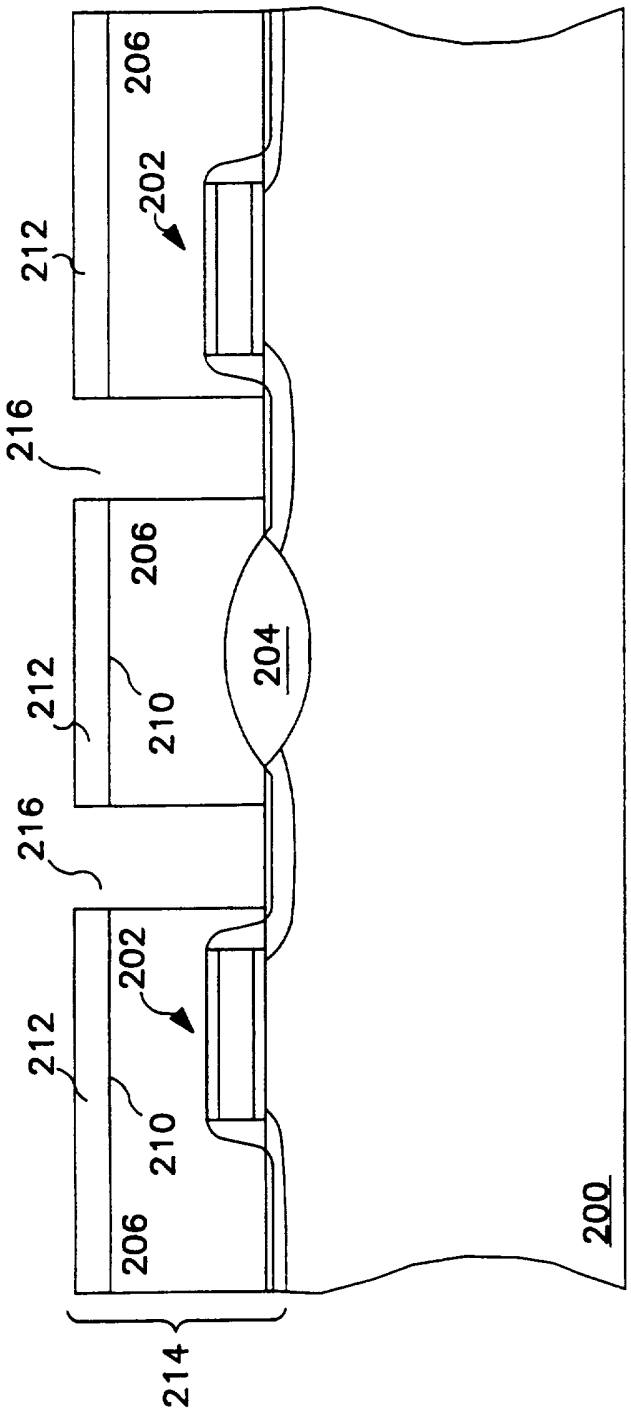

FIG. 2E

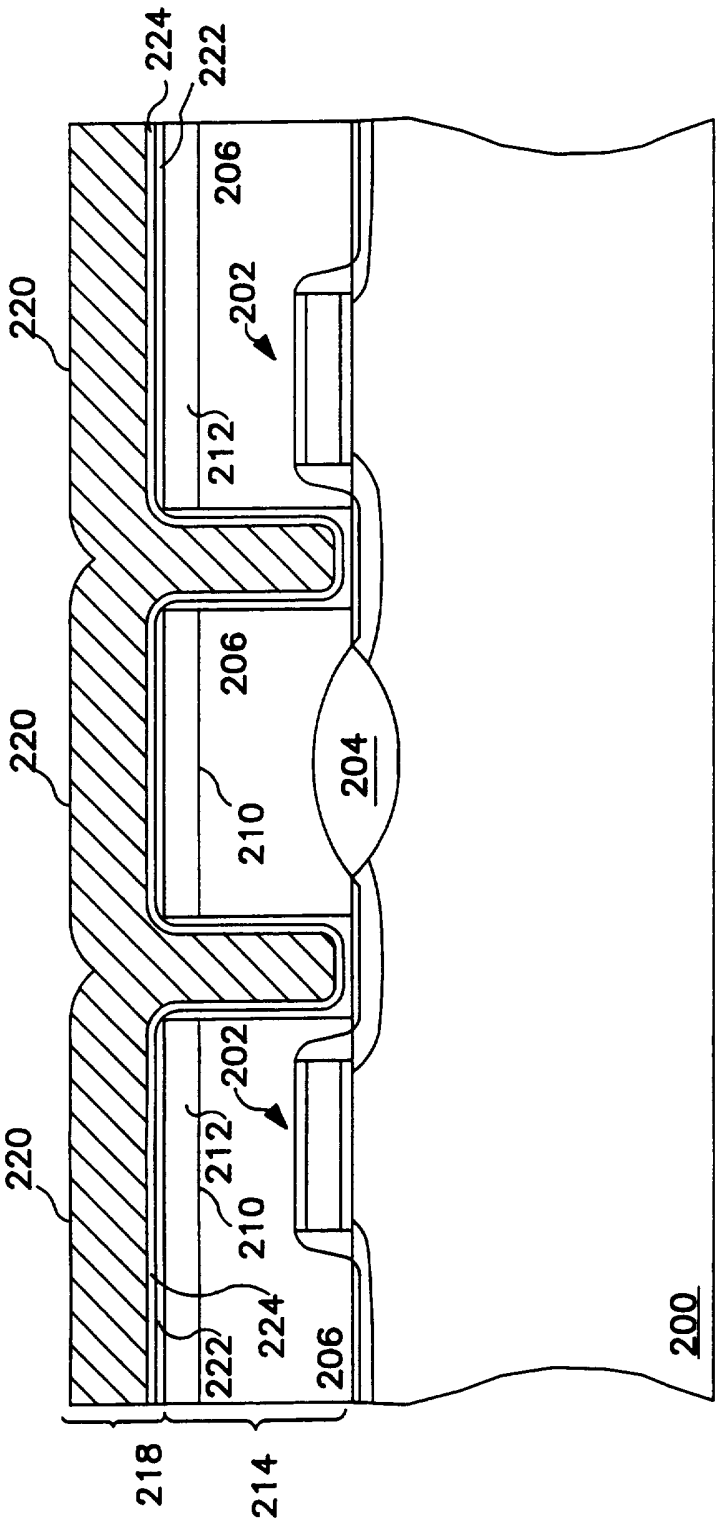
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FIG. 2F

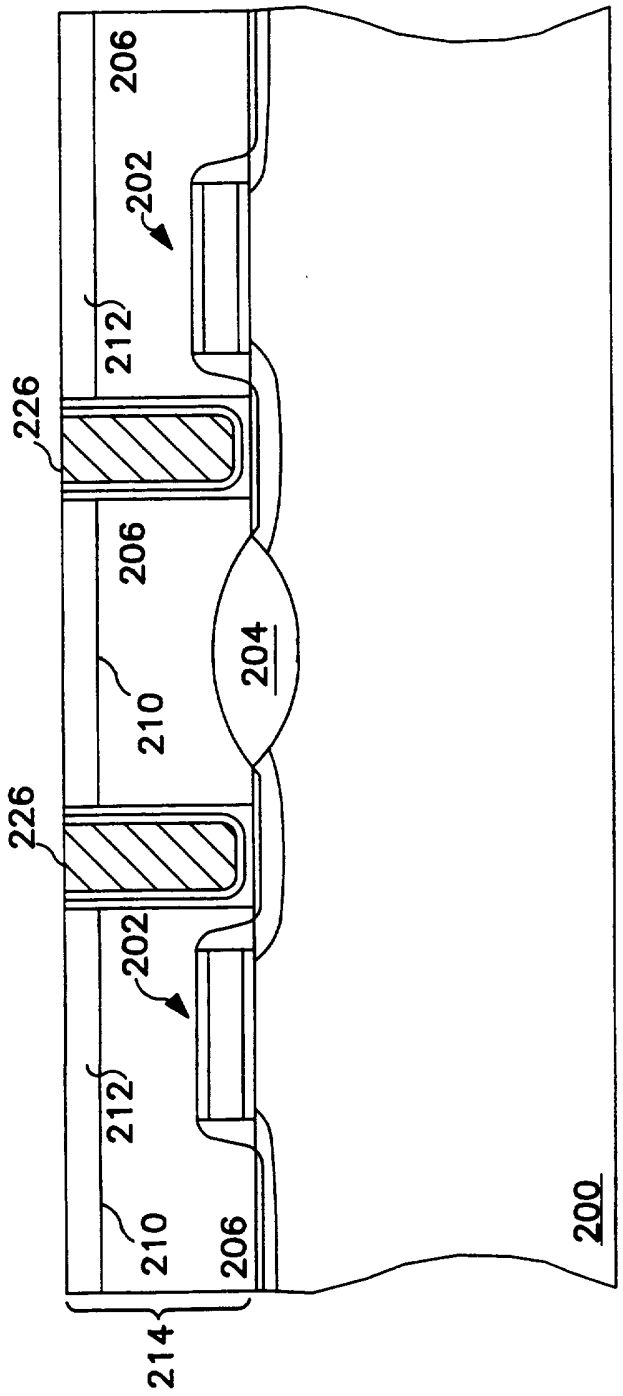

FIG. 2G

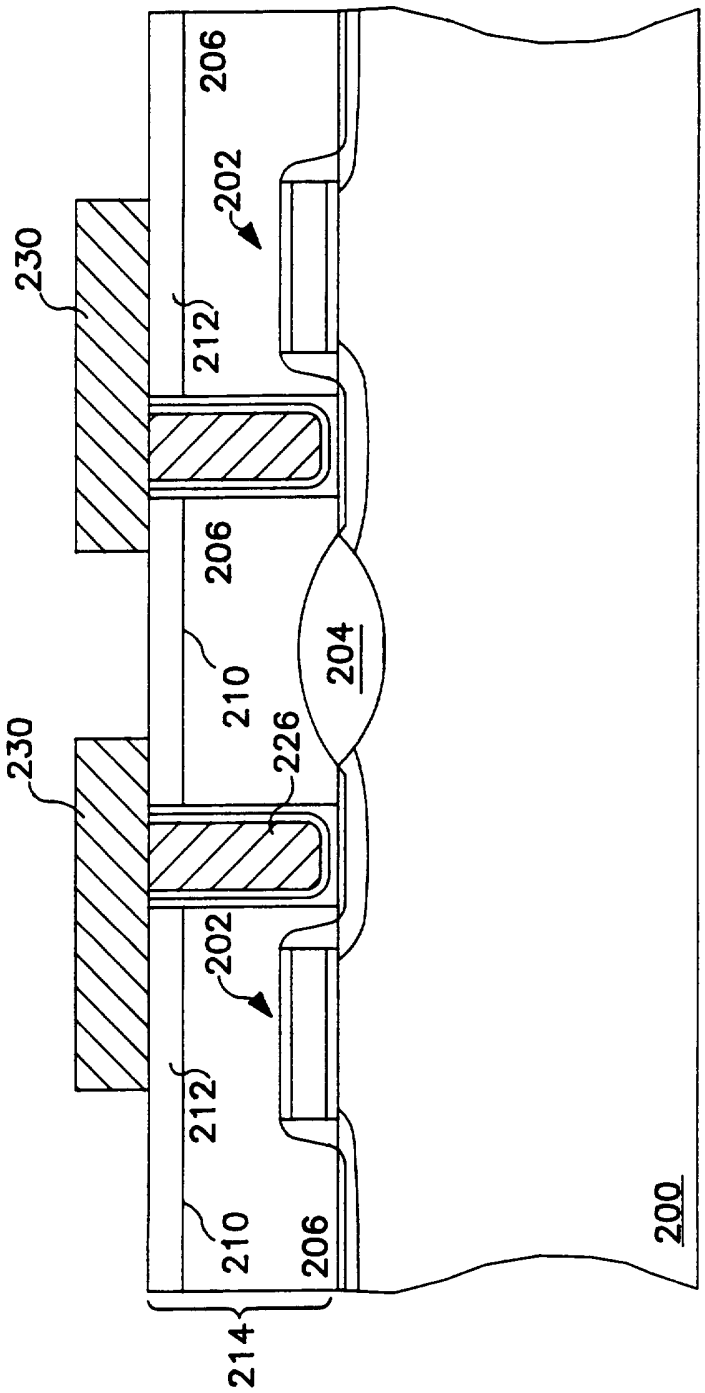

FIG. 2H

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/15201

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 21/44
US CL :437/192, 195
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 437/192, 195, 228, 238, 240; 156/636.1

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

WOLF, STANLEY, SILICON PROCESSING FOR THE VLSI ERA, VOL. 2

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS: USPAT, JPO

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X ---- Y	US 5,275,963 A (CEDERBAUM ET AL.) 04 JANUARY 1994, COL. 7, LINE 7 TO COL. 8, LINE 47.	1, 2, 5, 6 ---------- 3, 4, 7-15
Y	US 5,420,074 A (OHSHIMA) 30 MAY 1995, COL. 4, LINE 65 TO COL. 5, LINE 5.	1, 7, 15
Y	US 5,244,837 A (DENNISON) 14 SEPTEMBER 1993, COL. 4, LINES 40-47.	3, 7, 15
Y	US 5,409,858 A (THAKUR ET AL.) 25 APRIL 1995, COL. 4, LINES 3-33.	13
Y	US 5,164,340 A (CHEN ET AL.) 17 NOVEMBER 1992, COL. 3, LINES 5-15.	13

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 27 NOVEMBER 1996	Date of mailing of the international search report 27 FEB 1997
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer Matthew Whipple Telephone No. (703) 308-2521

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/15201

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WOLF, STANLEY, SILICON PROCESSING FOR THE VLSI ERA, VOL. 2, (1990) PAGES 194-195 AND 198.	3, 4, 7-9, 15

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/15201

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 12
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

THE CLAIM IS NOT COMPLETE AND DOES NOT CONTAIN ANY LIMITATIONS OTHER THAN THE PREAMBLE.

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.