(54) Title: METHOD AND APPARATUS FOR SCHEDULING THE ISSUE OF INSTRUCTIONS IN A MICROPROCESSOR USING MULTIPLE PHASES OF EXECUTION

(57) Abstract: A microprocessor configured to execute programs divided into discrete phases, comprising: a scheduler for scheduling program instructions to be executed on the processor; a plurality of resources for executing programming instructions issued by the scheduler; wherein the scheduler is configured to schedule each phase of the program only after receiving an indication that execution of the preceding phase of the program has been completed. By splitting programs into multiple phases and providing a scheduler that is able to determine whether execution of a phase has been completed, each phase can be separately scheduled and the results of preceding phases can be used to inform the scheduling of subsequent phases.

[Continued on next page]
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— with international search report (Art. 21(3))

— with amended claims (Art. 19(1))
Method and Apparatus for Scheduling the Issue of Instructions in a Microprocessor using Multiple Phases of Execution

Field of the invention

The present invention relates to the field of microprocessors and is particularly advantageous for single instruction multiple data (SIMD) processors.

Background to the invention

With some types of data, such as graphics data, large blocks of data often need to undergo the same processing operations. One example is when changing the brightness of an image. SIMD processing is advantageous for this process. An SIMD processor is a microprocessor with execution units, caches and memories as with any other processor, but additionally incorporates the concept of parallel execution of multiple data streams. Instead of individually fetching data instances, a single fetch instruction can be used to fetch a block of data. A single instruction can then be used to operate on the fetched data block, such as an "add" operation. SIMD processing therefore reduces the load on the processor as compared with traditional single instruction single data (SISD) processing.

However, SIMD processing can only be used in limited circumstances. For example, even in situations where large blocks of data are initially to be processed in the same way, programs often contain conditional instructions or branch instructions that result in some data in a block being operated on by one branch of instructions and the remaining data by another branch of instructions. It is very often not possible to predict in advance how many data instances will need to be processed by one branch and how many by another.

Typically in an SIMD processor, a scheduler is used to schedule the execution of a program, allocating the resources required by the program at the outset. One solution for programs in which different parts of a data set are processed by different instruction during a portion of the program has been to execute
each branch on all of the data and then discard the unwanted results. Clearly this is an inefficient use of processor resources and time.

Accordingly, it would be desirable to be able better allocate resources during the execution of programs in an SIMD processor, both to reduce power consumption and to optimise resource usage.

Summary of the invention

In a first aspect, the invention provides a multithreaded, SIMD microprocessor configured to execute programs divided into discrete phases of programming instructions and configured such that a plurality of data instances can be processed by a single thread of programming instructions, comprising: a scheduler for scheduling program instructions to be executed on the processor; and a plurality of resources for executing programming instructions issued by the scheduler; wherein the scheduler is configured to schedule each phase of the program only after receiving an indication that execution of the preceding phase of the program has been completed, and is configured during scheduling of each phase of the program to determine a number of data instances to be allocated to each thread for that phase of the program.

The scheduler is configured to recalculate an SIMD ratio for each phase of the program. The SIMD ratio is the number of data instances processed by a single instruction.

The processor includes a feedback loop to the scheduler through which the completion of each phase of the program is communicated to the scheduler.

Preferably the scheduler maintains a record for each phase of the program that is scheduled, during execution of that phase of the program.

Preferably, the processor further includes a thread finished counter, wherein when each thread finishes a phase of the program an indication is sent to the thread finished counter, and the processor is configured such that the
scheduler schedules a next phase of the program only when the thread finished counter indicates that all threads for a preceding phase of the program have finished. The thread finished counter may be part of the scheduler or provided as a separate component. The thread finished counter may comprise a memory storing a number of threads for each phase of a program and the thread finished counter decremented each time a thread finishes a phase, and configured such that when the thread finished counter reaches zero, the scheduler is instructed to schedule the next phase of the program.

The thread finished counter may store a record of a number of data instances for each thread of a phase of a program.

Preferably, the scheduler is configured to dynamically allocate the number of threads for each phase of the program based on the results of a preceding phase.

In a second aspect, the invention provides a method for scheduling programs in a multithreaded SIMD microprocessor, the microprocessor comprising a scheduler for scheduling programs of programming instructions, the programs being divided into discrete phases of programming instructions, the method comprising the steps of:

scheduling a first phase of a program to be executed on the processor, including the step of determining how many data instances to allocate to each of a plurality of threads in the first phase;

executing the first phase of the program scheduled by the scheduler;

when execution of the first phase of the program is complete, providing an indication to the scheduler that execution of the first phase of the program is complete; and

scheduling a second phase of the program after the scheduler has received the indication that execution of the first phase of the program is complete, including the step of determining how many data instances to allocate to each of a plurality of threads in the second phase.

Preferably, the method further comprises maintaining a record for each phase of the program that is scheduled, during execution of that phase of the
program.

Preferably, the method further comprises updating the record when each thread finishes a phase of the program, and scheduling a next phase of the program only when the record indicates that all threads for a preceding phase of the program have finished.

Preferably, the method further comprises storing a record of a number of data instances for each thread of a phase of a program.

Preferably, the method further comprises dynamically allocating the number of threads for each phase of the program based on the results of a preceding phase.

In a third aspect, the invention provides a computer program product, comprising computer executable code in the form a program executable on an SIMD processor, wherein the program is divided into a plurality of phases by phase instructions, the phase instructions being provided at points in the program where branches may occur and allowing a scheduler to schedule each phase of the program separately. At these points the SIMD ratio may need to change. An example of a point at which the SIMD ratio may need to change is following a branch instruction or conditional instruction. Another example is a sub-routine for alpha blending or anti-aliasing in a graphics processing program.

**Brief Description of the Drawings**

Embodiments of the invention will now be described in detail, by way of example only, with reference to the accompanying drawings, in which:

Figure 1 is a schematic illustration of a processor in accordance with the present invention;

Figure 2 is a schematic illustration of a program scheduling scheme in accordance with the present invention;
Figure 3 is a flow diagram illustrating the steps carried out by the scheduler of Figure 2; and

Figure 4 is a flow diagram illustrating the process carried out by the scheduler for scheduling new threads.

Detailed Description

Figure 1 is a schematic illustration of a multi-threaded SIMD processor 10 in accordance with an embodiment of the present invention. The processor is configured to schedule and execute individual phases of each program, separately to one another, rather than scheduling a complete program all at once and then executing it.

As with conventional processors, following scheduling by the scheduler 100, instructions are fetched from memory by the instruction fetch units 110. Fetched instructions are decoded by the instruction decode unit 120 and fed to the issue logic 130. The issue logic feeds the instructions and fetched data to the arithmetic logic units (ALUs) 140 and the results are stored in registers or memory 150.

The ALUs 140 are also configured to feedback thread finished instructions to the scheduler 100. As will be explained, thread finished instructions are provided at the end of each phase of a program.

New programs are provided to the scheduler 100 divided into multiple phases. The way in which the programs are divided is determined by the programmer but typically a new phase will begin at a point in the program when the resource requirements of the program may change.

For example, a program may include a conditional instruction such that if a data value is less than a threshold it is processed by one branch of instructions otherwise it is processed by another branch of instructions. It may not be possible to determine whether all data instances being processed by the program will be processed by a single branch or whether the data will be split
between the two branches and if so, how many data instances will go down which branch. So at the point of the conditional instruction the number of threads required and the number of instruction fetches required may change in a way that cannot be reliably predicted. By splitting a program at such points, resource scheduling can be managed dynamically in response to the data results.

Another example of an advantageous point for a new program phase is a routine for blending background colour with a transparent foreground object in a graphics program. A foreground object may have a uniform colour and so the data instances for the entire object can be processed in the same way for a colour calculation. However, the background over which the object sits may have variable colour and so different portions of the object must be processed differently in a blending routine. The blending routine may therefore be advantageously placed in a separate phase of the program to the colour routine.

A further example of an advantageous point for a new program phase is an anti-aliasing routine. Anti-aliasing is used when representing a high resolution image on a lower resolution screen. To remove undesirable artefacts, such as jagged edges, an anti-aliasing routine is used to smooth out the image. But anti-aliasing is only required at the edges of graphics objects. If a block of uniform colour is in the image, it is not necessary to process the bulk of it at high resolution and perform anti-aliasing. Only at the boundaries with other objects is it necessary. So a program might include a branch instruction so that edge portions of image data are processed using the anti-aliasing routine while larger blocks of data are processed in a much less computationally expensive way.

The programs are divided into phases by the inclusion of "phase completed" instructions at the end of each phase of the program. The phase completed instructions when executed feed back to the scheduler 100 an indication that a phase as been completed. The phase completed instructions include a program identifier.
The program instructions also include an indication of the resource requirements of the program, but instead of being provided at the start of the program to cover the entire program, they are provided at the beginning of each phase of the program. The scheduler 100 can then assess if there are sufficient resources available to execute the phase. Because the resources required may depend on the outcome of a preceding phase, the indication of the resources required may be in the form an algorithm to calculate the resources required. This dynamic calculation of resource requirements removes the need to always provision for the worst case scenario and leads to more efficient resource allocation.

The scheduler 100 includes a multi-phased execution control unit or thread finished counter 160 that stores a record for each program scheduled, and the number of threads scheduled for the current phase. At the start of a new program the scheduler creates a new record in the thread finished counter 160, and updates it every time a new phase of that program is scheduled. As each thread finishes a phase the thread finished counter receives an indication and adjusts the record for the number of threads executing for that program. The count of threads for a program is simply decremented each time a thread finishes until the thread count reaches zero. When the thread count for a program reaches zero, a new phase of that program can be scheduled. The thread finished counter may be provided as part of the scheduler or as a separate component.

Figure 2 is a schematic illustration of scheduling and execution process in accordance with the present invention showing the content of a program queue and a thread finished counter. A stream of programs is provided in a program queue as an input to a scheduler. The programs 200 are each divided into phases as described above, and each has a predetermined number of data instances, indicated as the value I in the program queue. The number of instances per thread is indicated by the value R. The scheduler 100 schedules individual phases of a program and waits for an indication that that phase is complete before scheduling the next phase. In the example shown in Figure 2 there are three programs in the program queue not yet scheduled and two programs, program A and program B currently being executed, but with further
phases remaining to be scheduled. The number of instances per thread, R, is known for the initial phase of each program but may be altered for subsequent phases of the program depending on the outcome of preceding phases. So the value of R is not known for the phases of programs A and B yet to be scheduled.

The phase of program A being executed has 17 threads, indicated in the thread finished counter 160 by the value T. Each thread contains a single data instance, so R=1. The phase of program B being executed has 2 threads each with 5 instances per thread. Figure 2 shows multiple threads scheduled by the scheduler entering the execution pipeline 210. The execution pipeline comprises the instruction fetch, issue logic and ALU's shown in Figure 1.

As already described with reference to Figure 1, the thread finished counter 160 stores a record for each program scheduled, and the number of threads scheduled for the current phase. As each thread finishes a phase the thread finished counter 160 receives an indication 220 from the end of the execution pipeline 210 and adjusts the record for the number of threads executing for that program. The count of threads T for a program is simply decremented each time a thread finishes until the thread count reaches zero. When the thread count for a program reaches zero, a new phase of that program can be scheduled.

Figure 3 is a flow diagram showing the process steps carried out by the scheduler in deciding how to schedule new threads. In step 300 the scheduler first checks if there are threads available for running to program from the program queue that are available to run. If there no threads available, the scheduler continues to check until there are threads available.

If there are threads available to run the first program in the queue is evaluated in step 310. In step 320, the scheduler checks if the first program already has a phase running and the scheduler is waiting for feedback to indicate that the phase is completed. If so then in step 325, the next program in the queue is evaluated in the same manner. If the scheduler is not awaiting feedback from a phase of the first program, then in step 330 the scheduler assesses whether
there are any further phases to execute. If there are no further phases the program is removed from the queue, as shown in step 340, and its record removed from thread finished counter.

If there are more phases left to run the scheduler determines whether the program is still running in step 350. If the program is still running, the scheduler moves to step 320 and next program in the queue is evaluated. If the program is not still running, the scheduler creates new threads for the next phase of the program, as indicated by step 360. Following the creation of new threads, the scheduler returns to the step 300 to check if there is room for any further threads.

Figure 4 shows in detail the steps taken by the scheduler to create new threads in step 360. In a first step, step 400, the scheduler checks that there is space for a new thread. If not, the scheduler continues to check until space becomes available. When space for a new thread is available, the scheduler creates a new thread, shown as step 410. The number of data instances in the new thread is the lesser of the maximum number of instances allowed per thread (which is limited by the hardware) and the number of data instances left.

Once the new thread has been created, a record for the thread is created or updated in the multi phased execution control unit, shown as step 420.

In step 430 the scheduler assesses whether there are further data instances to be run in the phase. If so, the scheduler attempts to create a further thread or threads to accommodate them. If not, the thread creation process ends in step 440 and the scheduler returns to step 300.

The present invention allows the SIMD ratio of programs to be dynamically altered during program execution. By splitting programs into multiple phases and providing a scheduler that is able to determine whether execution of a phase has been completed, each phase can be separately scheduled and the results of preceding phases can be used to inform the scheduling of subsequent phases.
Claims

1. A multithreaded single instruction multiple data (SIMD) microprocessor configured to execute programs divided into discrete phases of programming instructions, and configured such that a plurality of data instances can be processed by a single thread of programming instructions, comprising: a scheduler for scheduling phases of program instructions to be executed on the processor; and a plurality of resources for executing programming instructions issued by the scheduler; wherein the scheduler is configured to schedule each phase of the program only after receiving an indication that execution of a preceding phase of the program has been completed, and is configured during scheduling of each phase of the program to determine a number of data instances to be allocated to each thread for that phase of the program.

2. A microprocessor according to any preceding claim, wherein the scheduler is configured to determine the number of data instances per thread for each phase of the program based on a result of a preceding phase of the program.

3. A microprocessor according to claim 1 or 2, wherein the scheduler maintains a record for each program that is scheduled, during execution of that program.

4. A microprocessor according to any preceding claim, further including a thread finished counter, wherein when each thread finishes a phase of the program an indication is sent to the thread finished counter, and wherein the processor is configured such that the scheduler schedules a next phase of the program only when the thread finish counter indicates that all threads for a preceding phase of the program have finished.

5. A microprocessor according to claim 4, wherein the thread finished counter is part of the scheduler.
6. A microprocessor according to claim 4 or 5, wherein the thread finished counter comprises a memory storing a number of threads for each phase of a program and the microprocessor is configured such that the thread finished counter is decremented each time a thread finishes a phase, and when the thread counter reaches zero, the scheduler is instructed to schedule the next phase of the program.

7. A microprocessor according to claim 4, 5 or 6, wherein the thread finished counter stores a record of a number of data instances for each thread of a phase of a program.

8. A method for scheduling programs in a multithreaded, single instruction multiple data microprocessor, the microprocessor comprising a scheduler for scheduling programs of programming instructions, the programs divided into discrete phases of programming instructions, the method comprising the steps of:
   scheduling a first phase of a program to be executed on the processor, including the step of determining how many data instances to allocate to each of a plurality of threads in the first phase;
   executing the first phase of the program scheduled by the scheduler;
   when execution of the first phase of the program is complete, providing an indication to the scheduler that execution of the first phase of the program is complete; and
   scheduling a second phase of the program after the scheduler has received the indication that execution of the first phase of the program is complete, including the step of determining how many data instances to allocate to each of a plurality of threads in the second phase.

9. A method according to any one of claims 9 to 12, wherein the step of determining how many data instances to allocate to each thread for the second phase of the program is based on a result of the first phase of the program.

10. A method according to claim 8 or 9, further comprising maintaining a record for each phase of the program that is scheduled, during execution of that phase of the program.
11. A method according to claim 10, further comprising updating the record when each thread finishes a phase of the program, and scheduling a next phase of the program only when the record indicates that all threads for a preceding phase of the program have finished.

12. A method according to claim 8, 9, 10 or 11, further comprising storing a record of a number of data instances for each thread of a phase of a program.

13. A method according to any one of claims 8 to 12, further comprising dynamically allocating the number of threads for the second phase of the program based on a result of the first phase of the program.

14. A computer program product, comprising computer executable code in the form a computer program executable on an SIMD processor, the program being divided into a plurality of phases by phase instructions, the phase instructions being provided at points in the program where branches may occur and allowing a scheduler to schedule each phase of the program separately and to determine how many data instances to allocate to each thread for each phase of the program.
AMENDED CLAIMS

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Claims

1. A multithreaded single instruction multiple data (SIMD) microprocessor configured to execute programs divided into discrete phases of programming instructions, and configured such that a plurality of data instances can be processed by a single thread of programming instructions, comprising:
   a scheduler for scheduling phases of programming instructions to be executed on the processor; and
   a plurality of resources for executing programming instructions issued by the scheduler;

   wherein the scheduler is configured to schedule each phase of the program only after receiving an indication that execution of a preceding phase of the program has been completed, and is configured during scheduling of each phase of the program to determine a number of data instances to be allocated to each thread for that phase of the program based on a result of a preceding phase of the program.

2. A microprocessor according to claim 1, wherein the scheduler maintains a record for each program that is scheduled, during execution of that program.

3. A microprocessor according to any preceding claim, further including a thread finished counter, wherein when each thread finishes a phase of the program an indication is sent to the thread finished counter, and wherein the processor is configured such that the scheduler schedules a next phase of the program only when the thread finish counter indicates that all threads for a preceding phase of the program have finished.

4. A microprocessor according to claim 3, wherein the thread finished counter is part of the scheduler.

5. A microprocessor according to claim 3 or 4, wherein the thread finished counter comprises a memory storing a number of threads for each phase of a program and the microprocessor is configured such that the thread finished counter is decremented each time a thread finishes a phase, and when the thread counter reaches zero, the scheduler is instructed to schedule the next
phase of the program.

6. A microprocessor according to claim 3, 4 or 5, wherein the thread finished counter stores a record of a number of data instances for each thread of a phase of a program.

7. A method for scheduling a program in a multithreaded, single instruction multiple data microprocessor, the microprocessor comprising a scheduler for scheduling programs of programming instructions, the programs divided into discrete phases of programming instructions, the method comprising the steps of:
   - scheduling a first phase of a program to be executed on the processor, including the step of determining how many data instances to allocate to each of a plurality of threads in the first phase;
   - executing the first phase of the program scheduled by the scheduler;
   - when execution of the first phase of the program is complete, providing an indication to the scheduler that execution of the first phase of the program is complete; and
   - scheduling a second phase of the program after the scheduler has received the indication that execution of the first phase of the program is complete, including the step of determining how many data instances to allocate to each of a plurality of threads in the second phase based on a result of the first phase of the program.

8. A method according to claim 7, further comprising maintaining a record for each phase of the program that is scheduled, during execution of that phase of the program.

9. A method according to claim 8, further comprising updating the record when each thread finishes a phase of the program, and scheduling a next phase of the program only when the record indicates that all threads for a preceding phase of the program have finished.

10. A method according to claim 7, 8 or 9, further comprising storing a record of a number of data instances for each thread of a phase of a program.
11. A method according to any one of claims 7 to 10, further comprising dynamically allocating the number of threads for the second phase of the program based on a result of the first phase of the program.

12. A computer program product, comprising computer executable code in the form of a computer program executable on an SIMD processor, the program being divided into a plurality of phases by phase instructions, the phase instructions being provided at points in the program where branches may occur and allowing a scheduler to schedule each phase of the program separately and to determine how many data instances to allocate to each thread for each phase of the program.
PROGRAM E  I=33  
Not Started  R=11

PROGRAM D  I=6  
Not Started  R=4

PROGRAM C  I=21  
Not Started  R=5

PROGRAM B  I=10  
Awaiting Feedback  R=?

PROGRAM A  I=17  
Awaiting Feedback  R=?
ARE THERE AVAILABLE THREADS TO RUN PROGRAMS?

- If No, return to previous step.
- If Yes, proceed to EVALUATE FIRST PROGRAM IN QUEUE.

EVALUATE FIRST PROGRAM IN QUEUE

AWAITING FEEDBACK?

- If Yes, proceed to EVALUATE NEXT PROGRAM IN QUEUE.
- If No, proceed to MORE PHASES?

MORE PHASES?

- If Yes, proceed to PROGRAM STILL RUNNING?
- If No, remove program from queue.

PROGRAM STILL RUNNING?

- If Yes, create threads.
- If No, return to previous step.
IS THERE SPACE FOR A NEW THREAD?

CREATE NEW THREAD WITH LESSER OF (INSTANCES PER THREAD) OR (_INSTANCES LEFT) Instances

UPDATE MULTI PHASED EXECUTION CONTROL-INCREMENT RUNNING THREADS

ARE THERE ANY INSTANCES LEFT TO RUN?

FINISHED
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F9/38 G06F9/30 G06F15/80 G06T1/20 G06F9/48
G06F9/50
ADD.

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
G06F G06T

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
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X Further documents are listed in the continuation of Box C. X See patent family annex.

* Special categories of cited documents:

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<th>Category*</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
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</thead>
<tbody>
<tr>
<td>Patent document cited in search report</td>
<td>Publication date</td>
<td>Patent family member(s)</td>
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<td>----------------------------------------</td>
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<tr>
<td>US 7836116 B1</td>
<td>16-11-2010</td>
<td>NONE</td>
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<td></td>
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<td>CN 1484786 A</td>
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<td>JP 2004513455 A</td>
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<td>TW 563063 B</td>
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<td>US 6732253 B1</td>
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<td>US 2004158691 A1</td>
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<td></td>
<td>WO 0239271 A1</td>
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</tbody>
</table>