March 14, 1967 C. GILKER 3,309,571

REPEATING CIRCUIT INTERRUPTER HAVING RESET CONTROL MEANS RESPONSIVE TO LINE CONDITION

Filed March 9, 1964 2 Sheets-Sheet 1

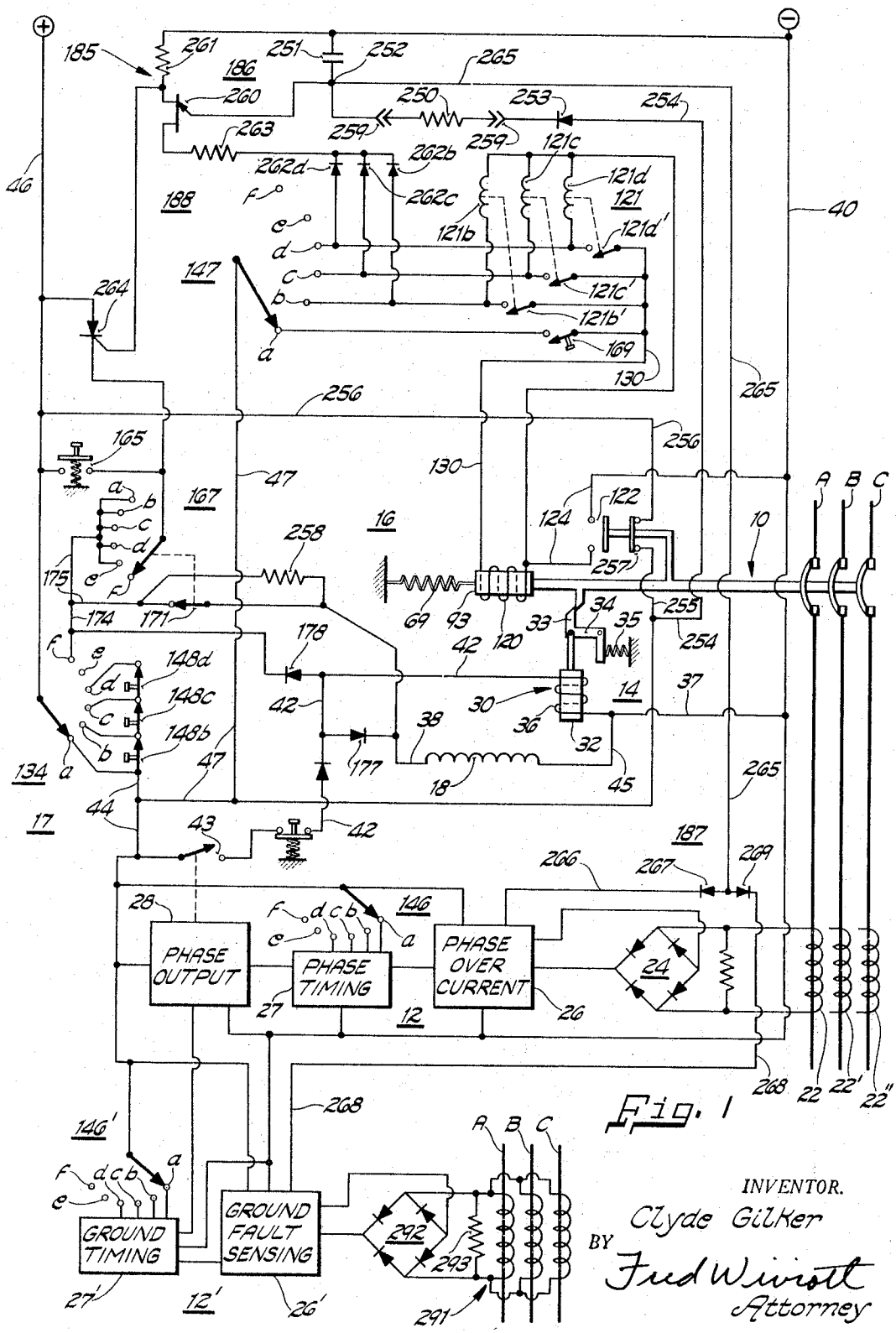

Fig. 1

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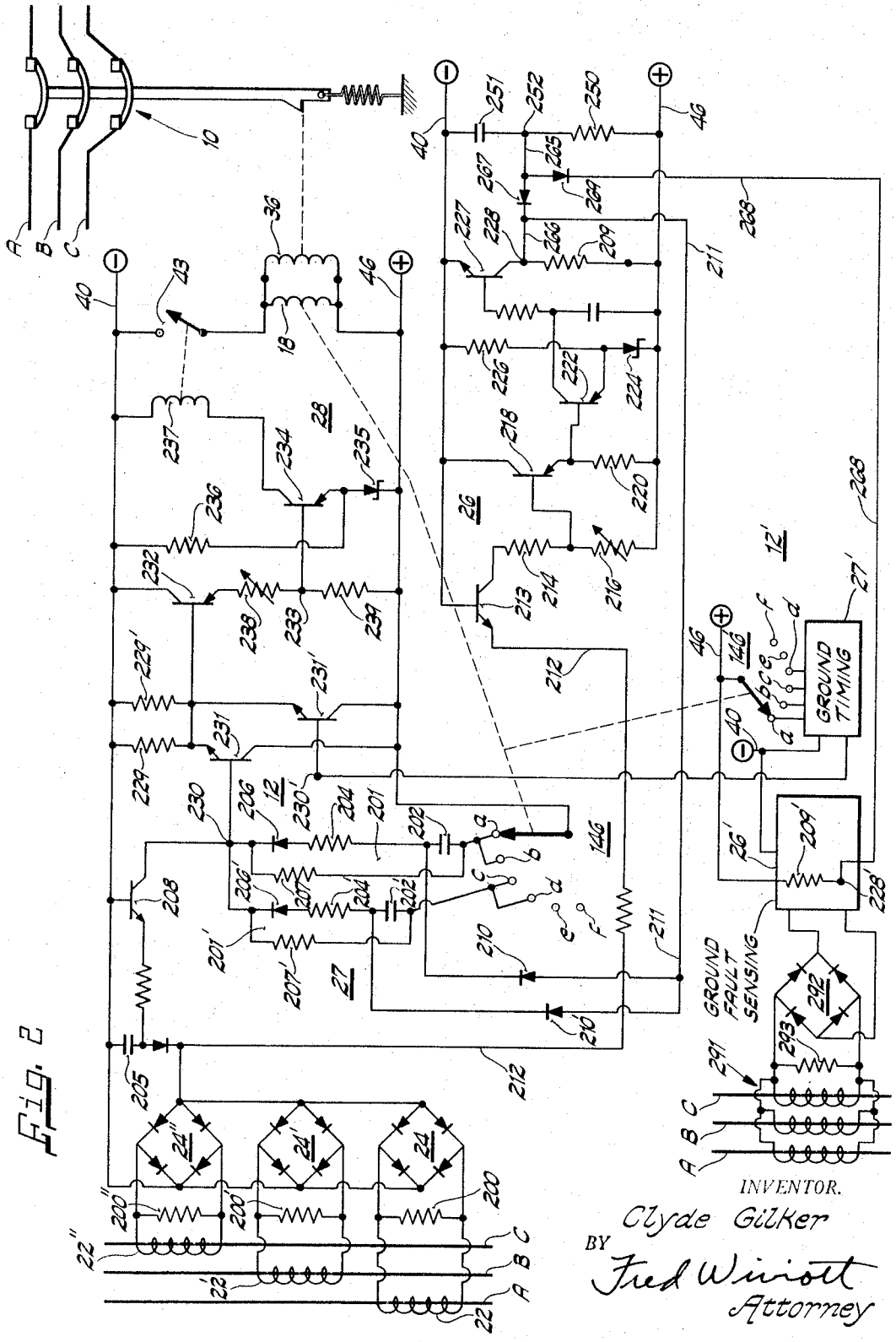

Fig. 2

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United States Patent Office 3,309,571 Patented Mar. 14, 1967

3,309,571

REPEATING CIRCUIT INTERRUPTER HAVING RESET CONTROL MEANS RESPONSIVE TO LINE CONDITION

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Filed Mar. 9, 1964, Ser. No. 350,195
20 Claims. (Cl. 317—22)

This invention relates to repeating circuit interrupters and, more particularly, to new and improved reset timing means for repeating circuit interrupters having step-acting operation counting and sequencing means.

A repeating circuit interrupter or recloser may be characterized as a circuit protective device having abnormal condition sensing means connected to the systems being protected and which is responsive to abnormal circuit conditions to initiate a switch opening operation, switch reclosing means operable after each opening operation, opening time delay means, and operation counting and lockout means which is operable to initiate time delayed switch opening after a first predetermined number of operations and to prevent reclosing after a second predetermined number of operations.

Because of the majority of faults in this type of system are temporary in nature and will clear in a relatively short period of time, it is common to arrange the switch opening means of the repeating circuit interrupter to execute a series of rapid opening operations so that the period in which the system remains energized is shorter than the time necessary for backup protective devices, such as fuses, to operate. In addition, the circuit interrupter contacts should not be closed immediately in order to allow the backup fuses to cool. If the fault does not clear during this initial series of rapid operations, the time delay means is actuated by the operation counting means so that there follows a second series of operations in which the recloser's contacts remain closed for a period of sufficient length to allow the backup protective devices to operate. If the fault still has not cleared after a predetermined number of such time delayed operations, it is considered permanent and the operation counting means prevents the actuation of the reclosing means so that the device is locked open. On the other hand, should the fault be cleared during any of the rapid or time delayed operations, it is necessary for the operation counting means to be reset in its initial position so that upon the occurrence of a subsequent fault, the recloser will execute the full number of rapid and time-delayed operations prior to locking the device open.

Prior art reclosers having electroresponsive step-acting operation counting means perform the resetting operation by energizing the electroresponsive means when the operation counting means is in a position other than its initial or lockout positions. However, because certain of the recloser's opening and/or closing operations are time delayed, it was necessary for the resetting means to be time delayed for a period longer than the sum of these time-delayed operations.

It is an object of the invention to provide a new and improved resetting means for the electroresponsive sequencing means of a repeating circuit interrupter.

Another object of the invention is to provide time-delayed resetting means for the sequencing means of a recloser which is independent of opening and/or reclosing time delay of the device.

A more specific object of the invention is to provide a repeating circuit interrupter having sequencing means wherein resetting means are operative during normal circuit conditions to reset the sequencing means to its initial position.

Another more specific object of the invention is to provide a repeating circuit interrupter having sequencing means and resetting means normally operative to reset said sequencing means wherein said resetting means is rendered inoperative during abnormal circuit conditions.

These and other objects and advantages of the instant invention will become more apparent from the detailed description thereof taken with the accompanying drawings, in which:

FIG. 1 schematically illustrates a repeating circuit interrupter incorporating the instant invention; and

FIG. 2 schematically illustrates in greater detail a portion of the repeating circuit interrupter shown in FIG. 1.

Referring now to the drawings in greater detail, FIG. 1 shows a repeating circuit interrupter or recloser having main interrupting switches **10**, overload responsive means **12**, switch opening means **14**, switch closing means **16**, and sequencing means **17**. In general terms, the overcurrent responsive means **12** is operable to actuate the switch opening means **14** upon the occurrence of an overload in the system being protected so that the interrupting switches **10** will each be moved to its open position. Upon this event, the reclosing means **16** is made operable to return the interrupting switches **10** to their closed position. The sequencing means **17** which performs the operation counting and lockout functions, includes a stepping relay coil **18** and step switches **134**, **146**, **146'**, **147** and **167**.

For a more complete description of the circuit breaker operating mechanism usable with the illustrated control mechanism, reference is made to copending Application S.N. 56,259 filed September 15, 1960, now abandoned and assigned to the assignee of the instant invention.

The overcurrent responsive means **12** is shown coupled to each phase of the polyphase system being protected and includes a phase overcurrent sensing portion **26**, a phase timing portion **27** and a phase output portion **28**. In addition, a ground fault responsive means **12'** is provided and includes a ground fault sensing portion **26'** coupled to each of the phases A, B and C and a ground timing portion **27'** coupled to the ground fault sensing portion **26'** and to the phase output portion **28**.

The overcurrent responsive means **12** and the ground fault responsive means **12'** will be discussed in greater detail below, it being sufficient at this point to state that when a predetermined overcurrent is sensed by the overcurrent sensing portion **26** or a predetermined unbalance current is sensed by the ground fault sensing portion **26'**, a signal is provided to their respective timing portions **27** or **27'**. Upon the receipt of this signal, the timing portions **27** or **27'** initiate a timing operation, and, after a predetermined interval, provide a signal to the output portion **28** which initiates an opening operation of the interrupting switches **10** by closing normally open contacts **43**.

The switch opening means **14** is shown in FIG. 1 to include an electromagnetic tripper **30** having a plunger **32** and a coil **36**. The plunger **32** is mechanically coupled to a latch crank **33** which is normally urged in a clockwise direction about pivot point **34** by a reset spring **35** to hold the main switches **10** in closed position against the influence of an opening spring **69**. The coil **36** is connected by a conductor **37** to the negative power supply bus **40** and by a conductor **42** to the contacts **43**. A conductor **44** connects the other side of contacts **43** to the positive bus **46** through the step switch **134** which is initially on contact *a*.

As stated hereinabove, contacts **43** are closed upon the occurrence of an abnormal circuit condition. This energizes coil **36** which in turn rotates crank **33** counterclockwise to release the main switches **10** for movement toward their open position under the influence of opening

spring 69. When the main switches are open, contacts 43 are returned to their normal open position to de-energize coil 36 so that crank 33 may be returned to its initial position by reset spring 35. The trip portion 14 is thereby reset in a position to relatch the main switches 10 when they are returned to their closed positions.

Before continuing with the discussion of the mechanical portion of the device, the operation of the sequencing means 17 will be mentioned briefly. Sequencing means 17 is schematically illustrated to include a stepping relay coil 18 and step switches 134, 146, 146,' 147 and 167 although any well known type of mechanical or static stepping device may be employed. The sequencing means 17 has a plurality of sequentially operable stages symbolized by the coil 18 and a movable wiper and taps or stages *a–f* for each of the step switches. Each time coil 18 is energized it is operable to simultaneously advance each wiper one tap from *a–f* and back to *a*. While it may appear from the schematically illustrated step switches that the circuit through each will be momentarily opened when their respective wipers are between positions, in actual practice the switches are of a type wherein the wiper bridges over to the next contact before moving off of a previous one so that circuit integrity is maintained. For this reason contacts 171 are provided in the relay coil 18 energizing circuit and are arranged to open and reclose each time the coil 18 advances the step switches so that coil 18 will be de-energized and drop out in preparation for a succeeding stepping operation.

Because the stepping relay coil 18 is connected by conductors 37, 38, 42 and 45 in parallel with the trip coil 36, said coil 18 will be energized when contacts 43 are closed. Thus, each time the recloser executes an opening operation, the coil 18 will advance each of the switches 134, 146, 146', 147 and 167.

The reclosing assembly 16 includes a closing coil 120, a time delay relay bank 121 and normally open contacts 122, which are mechanically connected to the main switches 10. Conductor 124 connects one side of the closing coil 120 to the negative bus 40 through contacts 122 and conductor 130 connects the other side thereof to the time delay relay bank 121, which, in turn, is connected to the positive bus 46 through switch 147, conductors 47 and 44 and switch 134. When the main switches 10 are in their closed position, contacts 122 are open so that the closing coil 120 and the time relay bank 121 are de-energized When the main switches 10 reach their fully open position, the contacts 122 close to complete an energizing circuit through the time delay relay bank 121 causing a predetermined one of the time delay relays in bank 121 to complete an energizing circuit through the closing coil 120. This moves the magnetic plunger 93 toward the right as seen in FIG. 1 to close the main switches 10 and extend the opening spring 69 thereby storing energy for the succeeding opening operation. In addition, contacts 122 are opened to de-energize the closing coil 120 and the time delay relay bank 121.

FIG. 2 shows the details of the overcurrent sensing portion 26, the timing portion 27 and the output portion 28 of the overload responsive means 12. Circuit 12 is coupled to the phases A, B and C by current transformers 22, 22' and 22'' respectively and corresponding full wave rectifiers 24, 24' and 24'' whose output terminals are connected in parallel. Resistors 200, 200' and 200'' are connected across each of the secondaries of current transformers 22, 22' and 22'' respectively so that a voltage will be derived across each which is proportional to the current in their respective phases and the largest of these drops will appear across capacitor 205.

The ground fault sensing portion 26' is coupled to phases A, B and C by a three-phase current transformer 291 which has a resistor 293 connected in its neutral leg so that a voltage drop will appear across resistor 293 which is proportional to the ground fault or unbalance current flowing in the phases A, B and C. Full wave rectifier 292 couples the resistor 293 to the ground fault sensing circuit 26'.

The timing portion 27 of circuit 12 includes a first timing circuit 201 connected to taps *a* and *b* of switch 146 and a second timing circuit 201' connected to taps *c* and *d* of said switch. The timing circuits 201 and 201' are identical except for the size of their components, which determine their time delay characteristics, and, accordingly, only timing circuit 201 will be discussed in detail, for the sake of brevity. Circuit 201 is shown to include a timing capacitor 202 connected in series with a timing resistor 204 and a diode 206 and the series combination connected in parallel with a second timing resistor 207. As more fully described in copending application Serial No. 800,567, filed Mar. 19, 1959, and assigned to the assignee of the instant invention, the impedance values of capacitor 202 and resistors 204 and 207 determine the charging time for any given fault current. Under normal operating conditions, tap switch 146 will be initially connected to tap *a*, so that timing circuit 201 will govern the first opening operation.

In operation, the current flowing to the collector of the charging transistor 208, which is a function of the voltage across capacitor 205, will split between the parallel paths defined by the timing resistor 207 and the series combination of timing resistor 204 and timing capacitor 202. When there is no fault in any of the phases, capacitor 202 is prevented from charging, because it is shunted by a leakage resistor 209 in overcurrent sensing portion 26 to which it is connected by diode 210 and conductor 211. As a result of this leakage current the terminal 228 of resistor 209 has some positive potential.

The current flowing to the overcurrent sensing portion 26 through conductor 212 is also proportional to the highest peak current in any of the phases A, B or C and results in a proportional transistor 213 collector current flowing through resistors 214 and 216. This produces a potential on the base of transistor 218 which is also proportional to said peak current. Transistor 218 draws emitter current proportional to this potential through a resistor 220 so that its emitter potential is also proportional to said peak current. The emitter of a signal comparing transistor 222 is held at a fixed potential by a Zener diode 224 and a resistor 226 while its base is connected to the emitter of transistor 218. Thus, by a proper selection of components, transistor 222 can be rendered conductive when the current of any of the phases A, B or C equals or exceeds the desired minimum actuating current of the device.

Upon the occurrence of an overcurrent in the system therefore, transistor 222 becomes conductive, passing current to the base of an output transistor 227. Upon the latter event, transistor 227 will become conductive to connect the leakage resistor 209 to the negative bus 40. This, in turn, causes terminal 228 to assume a negative potential so that leakage current can no longer flow from capacitor 202. As a result, timing capacitor 202 is prevented from discharging through leakage resistor 209 and, therefore, begins charging. In this manner, the timing operation is initiated. Diode 210 performs the function of preventing reverse current flow from junction point 228 to charging capacitor 202.

As timing capacitor 202 charges up, the potential at the junction point 230 between diode 206 and the base of a coupling transistor 231 will begin raising so that the transistor 231 emitter current through resistor 229 will be proportional to the voltage at junction point 230. As a result, a second transistor 232, whose base is connected to resistor 229, will draw proportional current through resistors 238 and 239 so that the potential of junction point 233 will also follow the potential of junction point 230. The base of a signal comparing transistor 234 is connected to junction point 233 while its emitter is held at a constant potential by a Zener diode 235 and

a resistor 236 connected across the power supply buses 40 and 46.

After timing capacitor 202 has charged for a predetermined time, which is the time delay for the first operation of the device, the potential at junction point 233 will reach the point where transistor 234 is rendered conductive. Relay 237 will thus be energized to close contacts 43 and thereby initiate an opening operation of the main switches 10 in the manner described hereinabove. In addition, stepping relay 18 will also be energized so that step switch 146 will be moved to tap *b*, so that the time delay circuit 201 will be effective during the second switch opening operation. Should the fault persist, requiring a third and a fourth opening operation, the switch 147 will be moved to taps *c* and *d*, so that the time delay circuit 201' will be effective, whereby the third and fourth operations may have a longer time delay than the initial operations.

Because the ground fault sensing circuit 26' and the ground timing circuit 27' are identical with the phase overcurrent circuit 26 and the phase timing circuit 27, except for the size of certain components, they will not be discussed in detail, for the sake of brevity. It is sufficient, for an understanding of the invention, to state that when a ground fault occurs in a system, it is sensed by the ground fault sensing circuit 26' in the same manner that an overcurrent is sensed by the phase overcurrent sensing circuit 26. The appropriate capacitor in the ground fault timing circuit 27' will begin charging so that after a time delay the emitter potential of transistor 231' will be sufficient to cause the energization of relay 237 in the manner discussed above. Contacts 43 are thereby closed to initiate a switch opening operation.

The time delay relay bank 21 is shown in FIG. 1 to include three time delay relay means symbolized by coils 121*b*, 121*c* and 121*d*, although it will be appreciated by those skilled in the art that any type of electroresponsive relay may be employed. Each coil 121*b*, 121*c* and 121*d* is connected between the corresponding taps *b*, *c* and *d* on switch 147, and the negative supply bus 40, and each coil is operative upon being energized, and after a time delay, to close the appropriate contacts 121*b*', 121*c*' or 121*d*' to complete the energizing circuit between the closing coil 120 and taps *b*, *c* and *d* of switch 147.

Upon the initial operation of the repeating circuit interrupter, each of the switches 134, 146, 146' and 147 will be on tap *a*, so that the contacts 43 will be closed after a relatively short time delay when a phase fault or overcurrent or a ground fault or overcurrent is sensed by the abnormal current sensing circuits 26 or 26'. This energizes trip coil 36 which opens the main contacts 10, and also energizes the stepping relay 18 which moves the switches 134, 146, 146' and 147 to their *b* taps. The movement of switch 147 to its tap *b* completes an energizing circuit through time delay relay 121*b*, which, after a time delay, closes contacts 121*b*' to energize the closing coil 120 through switches 134 and 147, conductors 44, 47, 130, 124 and contacts 122, which are closed when the main switches 10 are open.

Should the fault persist, the output portion 28 will again be energized after a short time delay to close the contacts 43. This will again energize trip coil 36 and stepping relay 18, so that switches 134, 146, 146' and 147 will each be moved to their taps *c*, whereupon time delay coil 121*c* will be energized to closed contacts 121*c*' after a time delay, thereby energizing closing coil 120 to initiate a second closing operation. Similarly, should the fault persist after the second reclosing operation, trip coil 36 will be energized after a relatively long time delay to again open the main switches 10. In a like manner, after the third opening operation, stepping relay 18 will move each of the switches 134, 146, 146' and 147 to their *d* taps, whereupon closing coil 120 will be energized through contacts 121*d* after a time delay. If the fault continues after the third closing operation, switch 43 will again be closed to energize the trip coil 36 and the stepping relay 18, which will then move each of the switches to their open taps *e*.

It can be seen that because tap *e* of switch 134 is unconnected, closing coil 120 is now open circuited, even though contacts 122 are closed when the main switch 10 is open. As a result, the main switches 10 will not reclose. In this manner, the recloser is locked in open position after a predetermined number of opening and closing operations. If it is desired to lock the recloser open after a lesser number of operations, this can be accomplished by opening the appropriate one of the switches 148*b*, 148*c* and 148*d*, disposed between the taps of switch 134. For example, if switch 148*b* is open, conductor 44 and the energizing circuit of the coil 120 will be open-circuited from the positive bus 46 when the stepping switch 134 advances from tap *a* to tap *b*. As a result, the recloser will be locked out after a single operation. Similarly, the opening of switch 148*c* will lock the recloser open after two operations while the opening of switch 148*d* will lock the recloser open after three operations.

Resetting of the recloser after it has been locked open in the manner described above is accomplished by means of a manual reset button 165 and stepping switch 167. It will be remembered that after lockout, each of the step switches 134, 146, 146' and 147, as well as 167, will be connected to taps *e*. When the reset button 165 is closed, stepping relay coil 18 will be energized from the positive bus 46 to the negative bus 40 through a path defined by tap *e* of step switch 167, conductor 175, switch 171 and conductors 38, 45 and 37. Stepping relay 18 then moves each of the switches to their position *f*, whereby an energizing circuit to stepping relay 18 is completed through the tap *f* on switch 134, conductors 174, 175, switch 171 and conductors 38, 45 and 37. The stepping relay 18 then moves each of the switches to their *a* taps, whereupon they are in position for a switch closing operation. Diodes 177 and 178 between stepping relay 18 and trip coil 36 prevent energization of the latter during the resetting operation just described.

After the step switches have been cycled to their *a* taps by reset button 165, the main switches 10 may be reclosed by closing switch 169, which completes an energizing circuit to closing coil 120 around the time delay relay bank 121.

It will be recalled that the recloser will cycle itself to lock out only if the fault current persists for a predetermined number of opening and closing operations. In order to reset the device should the fault clear after a lesser number of opening and reclosing operations, a resetting circuit 185 according to the instant invention is provided. This includes a time delay circuit 186, a system coupling circuit 187 and a switching circuit 188.

The timing circuit 186 includes a resistor 250 and a capacitor 251 which have a common terminal 252. The other side of resistor 250 is connected to the positive bus by a diode 253, conductors 254, 255, 256 and contacts 257 which are closed when the main contacts 10 are in their closed position, while the other side of capacitor 251 is connected to the negative bus 40.

The switching circuit 188 includes a uni-junction transistor 260 having its base-one electrode connected to the negative bus through resistor 261 and its base-two electrode connected to taps *b*, *c*, *d*, *e* and *f* of step switch 147 through resistor 263 and diodes 262*b*, 262*c*, 262*d*, 262*e* and 262*f*, respectively, so that the base-one-base-two electrodes will be in circuit between the positive bus 46 and the negative bus 40 only when switch 147 is on taps *b*, *c*, *d*, *e* or *f*. The switching circuit 188 also includes a controlled rectifier 264 whose gate electrode is connected to the junction between resistor 261 and the base-one electrode of uni-junction transistor 260. The anode and cathode of controlled rectifier 264 are respectively connected to the positive bus 46 and the wiper of step switch 167.

The common terminal 252 between resistor 250 and capacitor 251 is connected by conductors 265 and 266 and diode 267 to the terminal 228 between the collector of transistor 227 and a resistor 209 in the overcurrent sensing portion of the overload responsive means 12 (see FIG. 2). In addition, conductors 265 and 268 and diode 269 connect terminal 252 to the corresponding point in the ground fault sensing circuit 26'.

It will be recalled that when there is no overcurrent in the system being protected, terminal 228 will have some positive potential as a result of the voltage drop across resistor 209. Accordingly, junction point 252 between resistor 250 and capacitor 251 will be isolated from terminal 228 by blocking diode 267 but will also have a positive potential as a result of its being connected to the positive bus 46 by conductors 254, 255 and 256 and contacts 257, so that charge may accumulate on capacitor 251. It will be further recalled that when a fault current appears in the system, transistor 227 will become conductive, thereby connecting terminal 228 to the negative bus 40 so that the capacitor 251 is short circuited. It can therefore be seen that during normal circuit conditions charge may accumulate on capacitor 251 and that during abnormal circuit conditions charge is prevented from accumulating on capacitor 251.

It can also be seen that the junction point 252 between capacitor 251 and resistor 250 is also connected to the terminal 228' of the ground fault sensing circuit 26' and in a similar manner this point will be positive during the absence of ground fault currents and will be negative upon the occurrence of a ground fault. It can therefore be seen that capacitor 251 will be prevented from charging when either a phase overcurrent or a ground overcurrent flows in the system and will be permitted to charge only when normal circuit conditions prevail.

It will be appreciated that after the first opening operation the switches 134, 146, 146', 147 and 167 will each be advanced from tap *a* to tap *b*. Should the phase or ground overcurrent reappear in the system upon reclosure of the main switches 10, capacitor 251 will be short circuited in the manner discussed above and no charge can accumulate. As a result uni-junction transistor 260 remains inactive and normal opening and reclosing operations will continue until lockout or until the abnormal circuit condition disappears.

Assume, for example, that a fault occurs in one of the phases A, B or C and that after two opening and two reclosing operations, the abnormal circuit condition disappears. It will be appreciated that each of the switches 134, 146, 146', 147 and 167 will be on their tap *c*. When the main switches 10 close, normal circuit conditions will prevail so that transistor 227 becomes nonconductive. Upon this event terminal 228 of resistor 209 will be disconnected from the negative bus 40 and will assume a positive potential so that it is isolated by diode 267 from junction 252. As a result capacitor 251 begins charging from the positive bus 46 through resistor 250, conductors 254, 255, 256 and contacts 257. After a time delay predetermined by the relative sizes of resistor 250 and capacitor 251, the firing potential of uni-junction transistor 260 will be reached and it will conduct emitter current through resistor 261 and provide gate current to controlled rectifier 264 which will become conductive thereby energizing the stepping relay 18 through a path which includes positive bus 46, the wiper and tap *c* of switch 167, conductors 175, 38, 45 and 37, while diode 177 prevents the energization of trip coil 36. Resistor 258 is provided in shunt with contacts 171, which open each time the stepping relay 18 operates, so that the controlled rectifier 264 will not be open circuited as the tap switches are operated from taps *c* to taps *d*. As a result, relay coil 18 will be immediately re-energized when contacts 171 close to move each of the step switches from their taps *d* to their taps *e* and so on successively until they return to their taps *a*. The resistance of resistor 258 will, of course, be sufficiently great to insure that relay coil 18 will drop out whenever contacts 171 open.

It can be seen that when the step switch 147 is on its *a* tap the base-two electrode of uni-junction 260 is open circuited so that it cannot provide gate current to the controlled rectifier 264 even though capacitor 251 may be charged. Similarly, when the recloser is in its lockout position, step switch 147 will be on tap *e* so that the base-two electrode of 260 is similarly open circuited, although charge will not be accumulating on capacitor 251 because contacts 257 will be open when the main contacts 10 are open. Thus, the resetting circuit, according to the instant invention, will recycle the recloser control to its initial position whenever the main contacts are closed, when both the overcurrent sensing circuit 26 and the ground fault sensing circuit 26' sense normal circuit conditions, and when the step switches are in any position other than their initial or home position or lockout position. Because the resetting time delay circuit operates only when normal circuit conditions prevail, its time delay can be independent of the time delay of the phase timing circuit 27 and the ground timing circuit 27' because these circuits operate only when abnormal circuit conditions prevail. In addition, the time delay of the resetting circuit 185 is also independent of the time delay relay bank 121 because the latter is operative only when the main contacts 10 are open and there is no system current flowing.

It will be further appreciated that the time delay of the resetting circuit according to the instant invention can be modified by changing the resistance of the resistor 250. This can be accomplished by making resistor adjustable or by providing for its removal and replacement by another resistor. The latter can be accomplished by making resistor 250 insertable into the circuit by plug-in connectors 259.

While only a single embodiment of the disclosed invention has been described, it is not intended to be limited thereby but only by the scope of the appended claims.

I claim:

1. A repeating circuit interrupter including main switch means in circuit with an electrical system, means for opening said main switch means when an abnormal condition exists in said system, switch closing means, sequencing means having a plurality of stages and being operable to a successive one of said stages upon each switch opening operation, the operation of said sequencing means from an initial stage to each of a predetermined number of successive stages being operable to initiate the actuation of said switch closing means, the operation of said sequencing means to the next succeeding stage after said predetermined number being ineffective to initiate the actuation of said switch closing means so that said main switch means is not reclosed, resetting means coupled to said system and responsive to the return of normal circuit conditions to effect the return of said sequencing means to said initial stage if said sequencing means is in one of its predetermined number of stages.

2. The repeating circuit interrupter set forth in claim 1 and including condition responsive means coupled to said system for opening said main switch means when an abnormal condition exists in said system, and wherein said resetting means is coupled to said condition responsive means, said condition responsive means being operative when normal circuit conditions return to said system to initiate the operation of said resetting means to return said sequencing means to said initial stage if said sequencing means is in one of its predetermined number of stages, said condition responsive means being inoperative to actuate said resetting means during abnormal circuit conditions.

3. The repeating circuit interrupter set forth in claim 2 wherein said condition responsive means is operative to produce an electrical signal during normal circuit conditions in said system, said resetting means being coupled

to said condition responsive means and responsive to said electrical signal for effecting the return of sequencing means to said initial stage if said sequencing means is in one of its predetermined number of stages, said resetting means being rendered inoperative when said sequencing means is in said initial stage.

4. The repeating circuit interrupter set forth in claim 3 wherein said condition responsive means is operable to produce a second electrical signal when an abnromal condition exists in said system and includes circuit means responsive to said second electrical signal for opening said main switch means, said second electrical signal rendering said resetting means nonresponsive.

5. The device set forth in claim 1 wheerin said switch closing means includes electroresponsive means and including a source of electrical energy, wherein a predetermined number of said successive stages are in circuit between said energy source and said electroresponsive means, the next succeeding stage after said predetermined number being open circuited, said sequencing means being sequentially operable during each opening operation of said main switch means to connect said electroresponsive means to said energy source through successive ones of said predetermined number of stages to effect the reclosure of said main switch means, the connection of said electroresponsive means to the next succeeding stage after said predetermined number open circuiting said electroresponsive means to prevent further reclosure of said main switch means.

6. The repeating circuit interrupter set forth in claim 2 wherein said resetting means includes first time delay circuit means having energy storage means coupled to said abnormal condition responsive means, said abnormal condition responsive means initiating the charging of said energy storage means when normal circuit conditions return to said system, said resetting means also including circuit means coupled to said energy storage means and to said sequencing means and being operative to return said sequencing means to said initial stage when the energy stored therein exceeds a predetermined value, said sequencing means open circuiting said time delay circuit means when said sequencing means is in said initial stage, and means for rendering said circuit means ineffective when said main switch means is open.

7. The repeating circuit interrupter set forth in claim 6 wherein said switch opening means includes second time delay circuit means having second energy storage means, means coupled to said system for providing charging current to said second energy storage means which is functionally related to the current in said system, said abnormal condition responsive means being connected to said second energy storage means to initiate the charging thereof when an abnormal circuit condition exists in said system, and means coupled to said second energy storage means for opening said main switch means when the energy stored therein reaches a predetermined value, the time delay period of said first time delay circuit means being independent of the time delay period of said second time delay circuit means.

8. A repeating circuit interrupter including main switch means in circuit with an electrical system, switch actuating means for operating said main switch means through a succession of opening and closing operations when an abnormal condition exists in said system, sequencing means having a plurality of stages and being successively operable from an initial one of said stages through a predetermined number of intermediate stages to a subsequent one of said stages upon each operation of said switch actuating means, the operation of said sequencing means to said subsequent one of said stages being effective to prevent the reclosure of said main switch means, and resetting means normally operative to effect the return of said sequencing means to the initial one of said stages if said abnormal circuit condition disappears while said sequencing means is in one of its intermediate stages, said resetting means being coupled to said system for being rendered nonoperative upon the occurrence of an abnormal circuit condition.

9. The repeating circuit interrupter set forth in claim 8 wherein said switch actuating means includes condition responsive means coupled to said system for opening said main switch means when an abnormal condition exists in said system, and wherein said condition responsive means is coupled to said resetting means for rendering said resetting means inoperative during abnormal circuit conditions.

10. The repeating circuit interrupter set forth in claim 9 wherein said condition responsive means is operable to produce an electrical signal when an abnormal condition exists in said system and includes circuit means responsive to said electrical signal for opening said main switch means, said electrical signal rendering said resetting means nonresponsive.

11. The repeating circuit interrupter set forth in claim 9 wherein said resetting means includes time delay circuit means having energy storage means coupled to said abnormal condition responsive means, said abnormal condition responsive means providing a leakage path for said energy storage means when an abnormal circuit condition exists in said system and being ineffective to provide said leakage path when normal circuit conditions return to said system, said resetting means also including circuit means coupled to said energy storage means and to said sequencing means and being operative to return said sequencing means to said initial stage when the energy stored therein exceeds a predetermined value, said sequencing means open circuiting said time delay circuit means when said sequencing means is in said initial stage, and means for rendering said circuit means ineffective when said main switch means is open.

12. The repeating circiut interrupter set forth in claim 11 wherein said abnormal condition responsive means includes impedance means normally having a first polarity and means for changing said polarity upon the occurrence of an abnormal circuit condition, said impedance means providing a leakage path for said energy storage means when the polarity of said impedance means is changed and being ineffective to provide said leakage path when said impedance means has said first polarity.

13. The repeating circuit interrupter set forth in claim 11 wherein said sequencing means includes a step acting relay and said circuit means includes switching circuit means coupled to said energy storage means and to said step acting relay and being operative to complete an energizing circuit to said relay to return said step acting relay to its initial one of said stages if said sequencing means is in one of its intermediate stages, said step acting relay open circuiting said time delay circuit means when said step acting relay is in said initial one of said stages, and means coupled to said main switch means for rendering said switching circuit means ineffective when said main switch means is open.

14. The repeating circuit interrupter set forth in claim 8 wherein said switch actuating means includes first time delay means for delaying at least one of said opening and closing operations and wherein said resetting means includes second time delay means for delaying the return of said sequencing means to the initial one of its stages, the delay period of said second time delay means being independent of the delay period of said first time delay means.

15. The repeating circuit interrupter set forth in claim 12 wherein said switch actuating means includes second time delay circuit means having second energy storage means, means coupled to said system for providing charging current to said second energy storage means proportional to the current in said system, said second energy storage means being connected to said impedance means to provide a leakage path for said system proportional current when said impedance means has said first polarity and being ineffective to provide said leakage path when

said polarity is changed, and means coupled to said second energy storage means for opening said main switch means when the energy stored therein reaches a predetermined value, the time delay period of said first time delay circuit means being independent of the time delay period of said second time delay circuit means.

16. The repeating circuit interrupter set forth in claim 1 and including first time delay means for delaying at least one of said switch opening or switch closing operations, and second time delay means for delaying the operation of said resetting means, the time delay period of said second time delay means being independent of the time delay period of said first time delay means.

17. The repeating circuit interrupter set forth in claim 13 and including a source of electrical energy, said actuating means including electroresponsive switch closing means, and wherein said sequencing means is operative when in its intermediate stages to complete an energizing circuit between said energy source and said electroresponsive means to effect the reclosure of said main switch means, said sequencing means being inoperative when in its subsequent stage to complete said energizing circuit to prevent reclosure of said main switch means.

18. A repeating circuit interrupter having main switch means in circuit with an electrical system, control means operable in response to an abnormal circuit condition in said system for performing a succession of opening and reclosing operations of said switch means until the termination of said condition, step acting means operable from a first position through successive intermediate positions during each operation of said control means to a lockout positions wherein the reclosure of said switch means is prevented if normal conditions do not return after a plurality of said opening and closing operations, and reset means coupled to said system and to said sequencing means for sensing the return of normal conditions in said system before the operation of said sequencing means to said lockout position for returning said sequencing means to its first position.

19. The repeating circuit interrupter set forth in claim 18 wherein said control means includes first time delay means for delaying at least one of said switch opening and closing operations and wherein said resetting means includes second time delay means for delaying the return of said sequencing means to its first position, the delay period of said second time delay means being independent of the delay period of said first time delay means.

20. The repeating circuit interrupter set forth in claim 19 wherein said control means includes electroresponsive switch closing means, and wherein said step acting means is operative when in its intermediate positions to complete an energizing circuit to said electroresponsive means to effect the reclosure of said main switch means, said sequencing means being inoperative to complete said energizing circuit when in its lockout position to prevent reclosure of said main switch means.

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