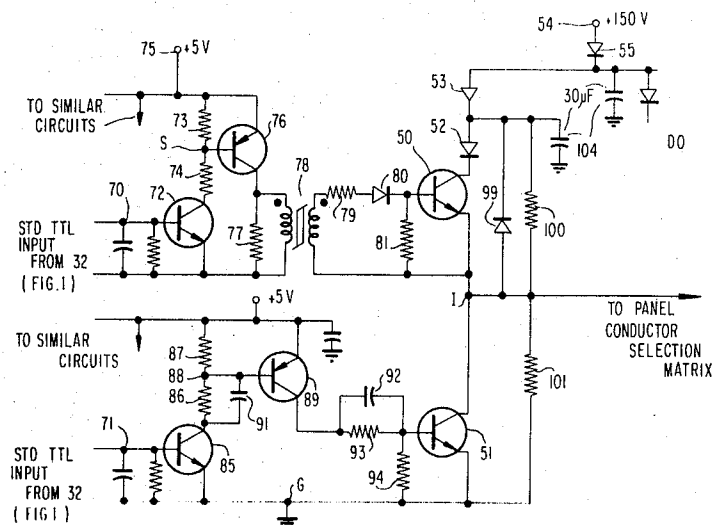


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|-----------|--------|-------------------|------------|
| 3,343,128 | 9/1967 | Rogers | 315/169 R |
| 3,499,167 | 3/1970 | Baker et al. | 315/169 TV |

- 5 Claims, 6 Drawing Figures**



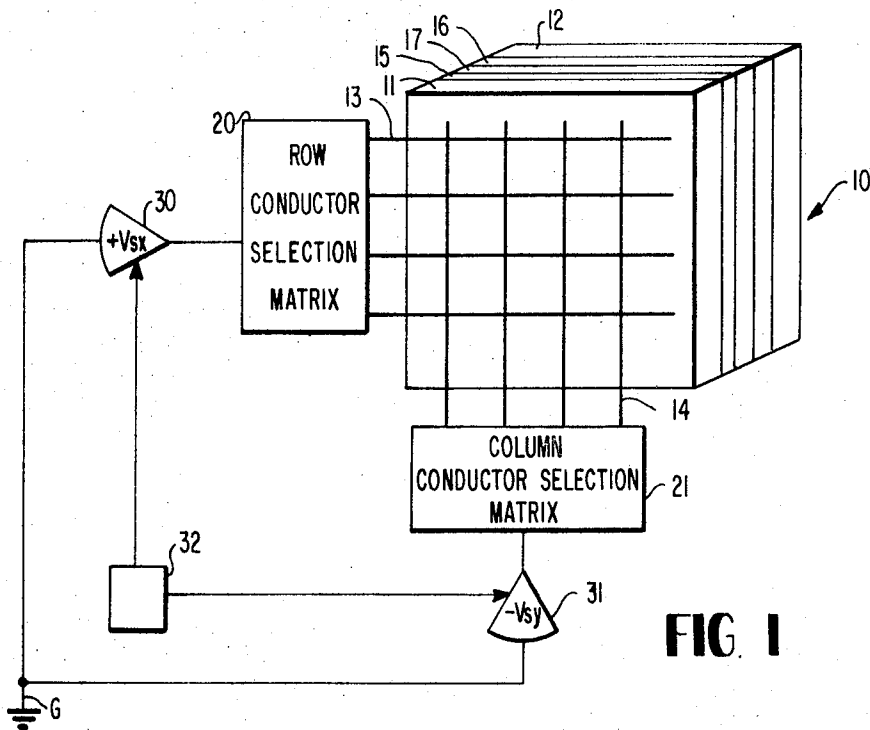


FIG. 1

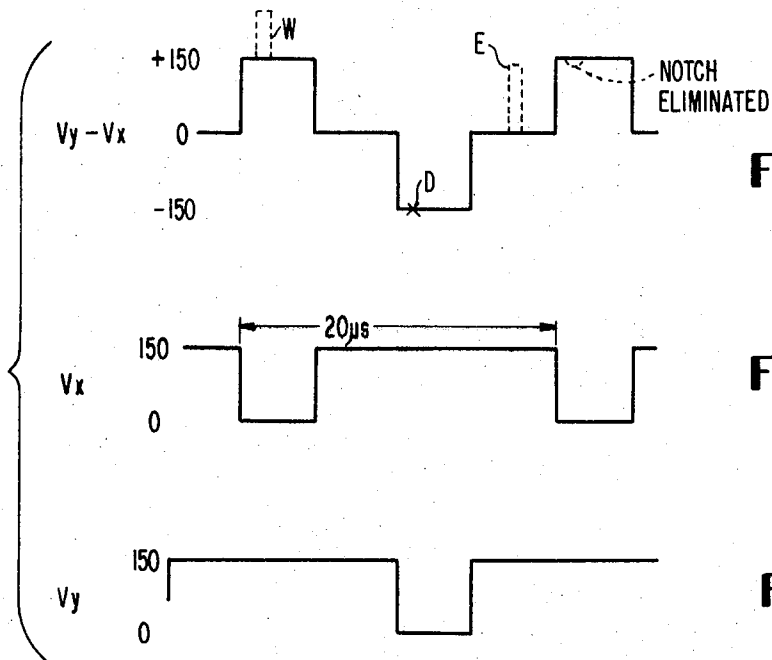


FIG. 2a

FIG. 2b

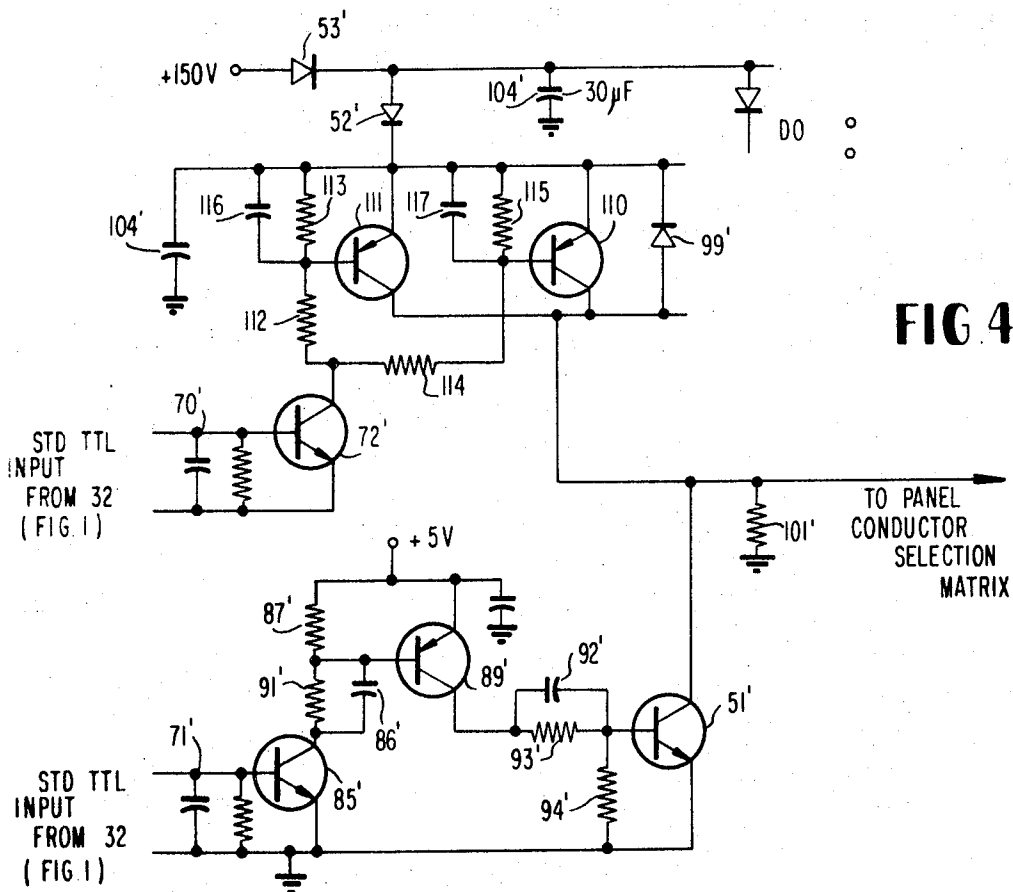
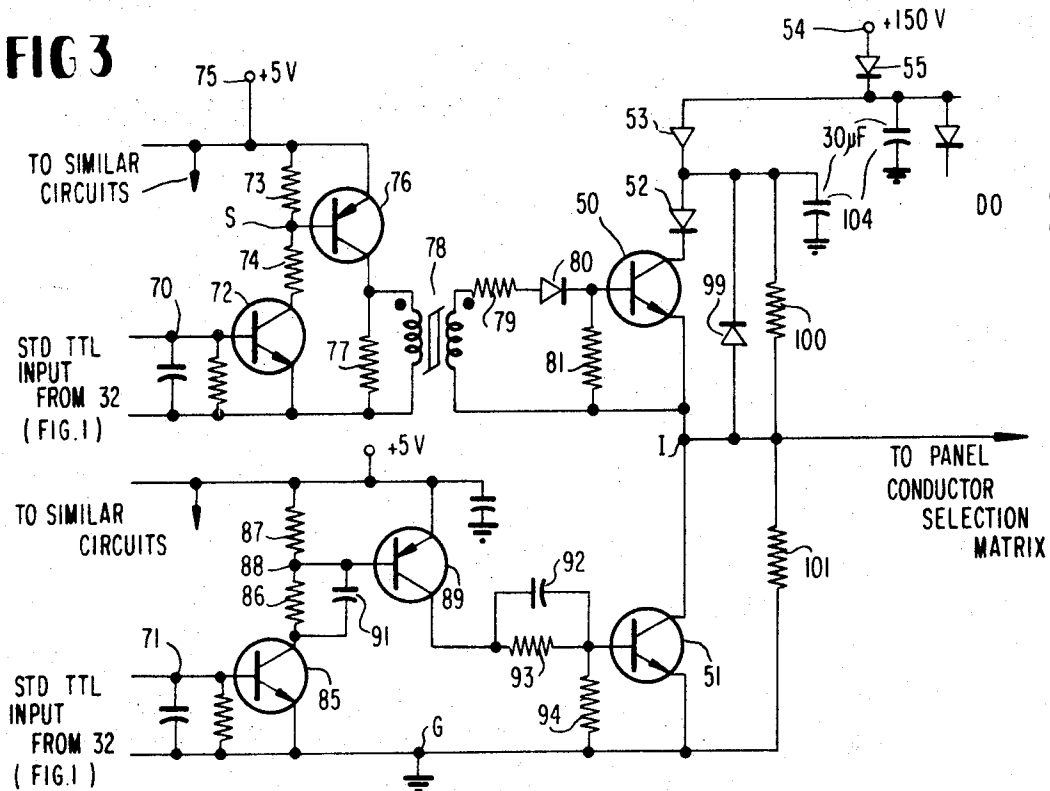
FIG. 2c

FIG. 2

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FIG 3



SUSTAINER VOLTAGE GENERATORS FOR DRIVING GASEOUS DISCHARGE DISPLAY PANELS

The present invention is directed to sustaining voltage generators uniquely designed and adapted for driving gaseous discharge display panels of the type disclosed in Baker et al. U.S. Pat. No. 3,499,167 and is an improvement on sustaining voltage generators disclosed in E. M. Murley application Ser. No. 846,555. As used herein, the sustaining voltage generator is intended to be a device which supplies the operating power to a gaseous discharge device of the type disclosed in the aforementioned Baker et al. patent. Some aspects of its design are dictated by power, voltage and frequency requirements of the panel, the frequency now being in the range of about 50KHZ. Because of the non-linearity of the impedance presented to the generator by the gaseous discharge panel, unusual design approaches are required for such generators. The present invention is directed to sustaining generators which are relatively simple in design for driving large numbers of conductors in such panels at 50KHZ and which circuits are directly interfaceable with the logic system for controlling the operation of such a generator and, also for the miniaturization of such circuits to make them more compact and reliable and to minimize notch distortion as seen by the panel. As used herein, notch distortion means the distortion in the sustainer voltage wave form caused by the firing of a large number of discreet sites served by a common sustaining generator.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, advantages and features of the invention will become more apparent in light of the following specification taken with the accompanying drawings wherein:

FIG. 1 is a diagrammatic illustration of a gaseous discharge display panel to which the invention has been applied,

FIGS. 2A, 2B and 2C are wave form diagrams which have been included to facilitate an understanding of the operation of the sustainer generators according to the invention,

FIG. 3 is a circuit diagram of a preferred form of one-half of sustaining generator according to the invention and

FIG. 4 is a circuit diagram of a second embodiment of the invention showing sustaining generator for supplying either row or common conductors of a gaseous discharge panel shown in FIG. 1.

Referring to FIG. 1, a gaseous discharge display panel 10, generally of the type disclosed in Baker et al. U.S. Pat. No. 3,499,167 is constituted by a pair of support plates 11 and 12 on which are placed row conductors 13 and column conductors 14, the conductor arrays having dielectric or insulative coatings 15 and 16 applied thereto. The respective plates are joined in spaced apart relation by a spacer sealant means 17 to form a thin gaseous discharge chamber in which may be placed a neon-argon gas mixture as is disclosed in Nolan application Ser. No. 764,577. other gaseous discharge mediums may likewise be incorporated in the panel but the improvement achieved by use of the gas mixture recited above permits the panels to be operated in 30-50KHZ range without being damaged by thermal shock and, at the same time with good light output and good memory margins. The individual con-

ductors in row conductors 13 are preferably driven by a row conductor selection matrix 20 and the column conductors are driven by column conductor selection matrix 21 such selection matrices being generally of the type disclosed in Johnson application Ser. No. 60,402 filed Aug. 5, 1970 and entitled "Selection and Addressing Circuitry For Matrix Type Gas Display Panel." However, instead of a selection matrix operating on multiplex principles, individual pulsing circuits may be used for selecting individual ones of the row and column and conductors, respectively. The selection matrices 20 and 21 receive signal inputs from a signal source, not shown, but which may be computer, key set, tape, reader or other data source.

A pair of sustaining generator voltage sources 30 and 31 are provided for supplying opposite phase or opposite polarity sustaining potentials to the row conductors 13 and column conductors 14 in the panel 10, voltages having the wave forms shown in FIGS. 2B and 2C, respectively with the resultant wave form shown in FIG. 2A being the voltage wave form (idealized) as seen by the gas in the discharge gap between the row and column conductors at the cross points thereof. Essentially, one-half of the sustainer potential is applied to the panel 10 is applied to the row conductors and the other one-half of the sustainer potential is applied to the column conductors. It will be particularly noted that the sustaining generators 30 and 31 have a common point or terminal G (but not necessarily electrical ground) so that in the arrangement shown, the potentials generated in or produced by row conductor selection matrix 20 floats or are referenced to the potential from sustainer generator source 30 and, similarly, the potentials generated in the column conductor selection matrix are in series with and have as a reference the instantaneous voltage from sustaining generator 31. Moreover, both sustaining generators 30 and 31 receive controlling logic signal inputs from a source 32 which, if desired, may be a free running multivibrator or other signal source from the computer. Thus, it may be desirable at times to erase the panel in which case one of the signals applied to one of sustaining generators 30 and 31 may simply be removed for a certain time interval to thereby permit bulk erasing of all information on the panel or it may be desirable to vary the sustaining rate by varying signal rate from control circuit 32.

Referring to the wave form diagrams of FIG. 2, it will be noted that the wave form of the voltage appearing between row conductors 13 and column conductors 14, shown at line A of FIG. 2 rises or is "pulled up" from 0 to about 150 volts, stays at the 150 volt level for a selected time interval, is then returned or "pulled down" to the 0 volt level, where it stays for a selected time interval and then is driven to a negative 150 volt level, stays there for the same time interval as at the positive level and, then is returned to the 0 level where it remains for a selected time interval and then repeats itself. Such voltage wave form (FIG. 2A) is, in effect, the difference between the two voltage wave forms applied to the X Y conductors and shown in lines B and C of FIG. 2. The time interval shown is merely exemplary. Referring further to FIG. 2, line A, it will be noted that positive pulse W is a firing voltage pulse (from the selection matrix) which is on or referenced to the sustainer voltage wave form. This voltage, when added at the time interval shown, will be sufficient to initiate a discharge at the selected cross point as de-

finished by the row-column conductor matrix. Subsequently thereto and on the next half cycle, there will be subsequent discharge indicated at the point X on the negative half of the sustainer wave form, assuming a past history of discharges at the selected site, and hence assuming stored charges and a memory, the discharges will repeat and at substantially the same point in the cycle. Because the discharge once initiated occur at substantially the same point on the sustainer, care must be taken that no notch distortion occurs. Erase is accomplished by many techniques and preferably by applying an erased pulse, which is essentially the "write" pulse but applied at the point indicated by the numeral E on wave form FIG. 2A.

In the preferred embodiment shown in FIG. 3, a pair of NPN transistors 50 and 51 have their emitter-collector circuits connected in series and through decoupling or blocking diodes 52, 53 and 54 to a high voltage output terminal 55 of the direct current supply and to a ground or common point G. The intermediate point I between the collector of transistor 51 and the emitter of transistor 50 constitutes the output terminal for the sustaining generator and is connected to the panel conductor selection matrix shown in FIG. 1. The arrangement of transistor switches 50 and 51 is such that when transistor 50 is turned "on" or made fully conductive, the capacitive load constituted by the panel 10 is charged and has applied thereto the +150 volt level and when transistor 51 is rendered conductive, and transistor 50 rendered non-conductive, the panel discharges its capacitance to return to the 0 volt level. This constitutes one-half of the periodic sustainer potential which is applied to the panel 10. As indicated above, the resultant wave form shown in FIG. 2A is constituted by two operations like as just described, the terminals of the direct current supply being reversely connected as is suggested by the wave forms shown in FIGS. 2B and 2C, respectively. In other words, the circuitry shown in FIG. 3 is identical for the sustaining generator 30 and the sustaining generator 31, only the polarity of potential applied to the panel each sustaining generator being reversed.

The timing of the occurrences of the charging of the panel and the discharging of same, both on the negative and positive excursions of the V_x and V_y wave forms shown in FIG. 2B and FIG. 2C, respectively, is controlled by the output from control circuit 32. Control circuit 32 can, for example, be the output of a free running multivibrator as is shown in the above referenced Murley application. On the other hand, and preferably, the output voltages from control circuit 32 can be variable in order to vary the timing and hence the widths of the sustainer voltage square pulse wave form. In FIG. 3 (as well as FIG. 4) the output from source 32 is labeled as "STD TTL Input From 32" which is intended to imply that this is standard transistor logic or gate output potentials (from typical integrated type) which are coupled through shaping networks 70 and 71, respectively, each of which is composed of a parallel capacitor and resistor circuit.

Referring now to the shaping circuit 70, the signal therefrom is applied to the base of transistor 72 which has its collector connected through a voltage divider, constituted by resistors 73 and 74, to the low voltage supply 75. The intermediate point S between resistors 73 and 74 is connected to drive the base circuit of transistor 76 to turn this transistor "on." Transistor 76 is a

PNP transistor having its collector connected through the primary winding of transformer 78, a fairly large resistor 77 is connected in parallel with the transformer primary winding to reduce the ringing voltage when the drive voltage is removed. The output voltage generated in the secondary of transformer 78 is coupled through a dropping resistor 79 and coupling diode 80 to the base of transistor 50. A small resistor 81 is connected between the base-emitter electrodes of transistor 50. Diode 80 is used to increase the repetition rate of the transformer 78 and also make the secondary thereof appear as an open circuit or high impedance to the base of circuit of transistor 50. Summarizing the function of the circuit just described, the appearance of a signal pulse voltage at shaping circuit 70 is effective to turn on or render fully conductive switching transistor 50 which, in effect, connects the high voltage positive supply directly to the panel conductors via intermediate point I in the panel conductor selection matrix. During this time switching transistor 51 is maintained non-conductive so that charging current flows to the panel 10.

The low voltage logic signals from source 32 applied to a second shaping circuit 71 are coupled to the base of transistor 85 which has its emitter connected to ground or common point G and its collector connected through a voltage divider constituted by resistors 86 and 87 to the low voltage supply. The intermediate point 88 of this voltage divider is connected to the base electrode of transistor 89, a speed up capacitor 91 being connected in shunt with resistor 86. The output signal from transistor 89 is connected through capacitor 92 to the base of switching transistor 51, and capacitor 92 being in parallel with resistor 93, which resistor serves to discharge the capacitor 92 between pulses. A very small resistor 94 is connected between the base-emitter electrodes of switching transistor 51.

There may be a number of circuits similar to that described which are indicated by the repeating sign "DO:" on the high voltage circuit and "to similar circuits" for the logic inputs. In other words, for large panels, the supply potentials may be split between several like but similarly controlled sustaining voltage generator circuits. Moreover, as disclosed in the aforementioned Baker et al. patent, the border discharge sites may be lighted "on" at all times so as to provide "conditioning" for the panel and a separate supply sustainer supply may be used for this purpose. Diodes 99 are used to handle displacement currents through panel 10 and the resistors 100 and 101 are included for the purpose of helping to turn off transistors 50 and 51 respectively. Diodes 52, 53 and 55 in the 150 volt supply lines tend to reduce ringing on the power supply lines, which is interpreted as "notch" on the panel 10. For the same reason large capacitors 104 are connected to the 150 volt line to help eliminate notch distortion, the capacitors serving as storage devices to aid in supplying currents during discharge.

The embodiment shown in FIG. 4 differs from the circuit of FIG. 3 mainly in that the silicon NPN transistor 50 of FIG. 3 is replaced by at least a pair of parallel PNP transistors 110 and 111. The signal from shaping circuit 70' is applied to the base of transistor 72' as in the embodiment of FIG. 3. However, the collector circuit of transistor 72' now includes a pair of voltage dividers 112-113 and 114-115, the intermediate points of which are connected to the base electrodes of

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switching transistor pair 111 and 110, respectively. Small capacitors (0.1MF) 116 and 117 form a low impedance path to keep the emitter currents of transistors 111 and 110 minimized when the collector voltage is switched on energization of switching transistor 51'. Thus, transistor 111 and 112 are turned on by a low base drive which is easily done and still performs well due to the fact that fast turn-on is not important in a sustainer which is normally high. It is also noted that the circuit of FIG. 4 is capable of being made in hybrid form and better lends itself to miniaturization (there is no transformer in the generator per se) and therefore to a more compact and reliable circuit.

It is apparent that many other embodiments and modifications are possible and within the scope of the claims appended hereto.

What is claimed is:

1. In a system for supplying square wave sustaining potentials to transversely related conductor arrays in a capacitive load type gas discharge panel wherein the crossing points of said conductor arrays locates a discharge site in the panel, a high voltage direct current voltage source having a pair of output terminals, a first pair of normally open switch means connected in series across said high voltage source and having a point intermediate said pair of switches connected to one of said conductor arrays, a second pair of normally open switch means connected in series across said high voltage source and having a point intermediate said second pair of switches connected to the other one of said conductor arrays, a switch control means for controlling the alternate closing and opening of said pair of switch

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means at selected times such that said high voltage source is first connected to said conductor arrays respectively, to supply charging current thereto and secondly to said point of reference potential common to said sources to discharge said conductor arrays, the improvement comprising:

each of said switches in a pair of switches being constituted by at least one switching transistor circuit, and wherein said switch control means includes a separate control circuit for each switching transistor to control the time duration of each square wave potential, a source of low level logic signal voltage, and means connecting each said control circuit to receive said low level logic signal voltage from said source thereof.

2. The invention defined in claim 1 wherein said switching transistors are of the NPN type.

3. The invention defined in claim 1 including compensating capacitor means connected between the base of the switching transistors connecting said conductor arrays to said point of reference potential to discharge said conductor arrays and the said switch control means therefor.

4. The invention defined in claim 1 wherein one of the switches in each pair is an NPN switching transistor and the other switch of said pair is constituted by at least a pair of parallel connected PNP switching transistors.

5. The invention defined in claim 1 including diode means in said high voltage current source for reducing notch distortion in the voltage supplied to said panel.

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