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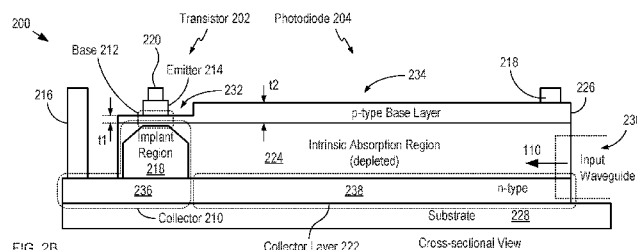
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(54) Title: DECOUPLED ABSORPTION/GAIN REGION BIPOLAR PHOTOTRANSISTOR



(57) Abstract: A phototransistor capable of exhibiting a high gain-bandwidth product as well as fast carrier collection is presented. Phototransistors in accordance with the present invention include a transistor region whose base/ collector junction also serves as the PIN region of an integrated photodiode formed in a photodiode region of the device. The base layer is common to both the transistor region and the photodiode region; however, in the transistor region, the thickness of the base layer is thinner than in the photodiode region. By providing a base layer that is thinner in the transistor region than in the photodiode region, the base/collector junction depth is kept thin in the transistor region while remaining much deeper in the photodiode region. As a result, the transistor region is characterized by a short transit time, ensuring high f_t , while the photodiode region is characterized by a large depleted carrier collection region having low capacitance.



Decoupled Absorption/Gain Region Bipolar Phototransistor

Statement Regarding Federally-Sponsored Research

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Field of the Invention

[0002] The present invention relates to optical detectors in general, and, more particularly, to phototransistors.

Background of the Invention

[0003] Optical communications links are critical elements in many applications, such as modern telecommunications and data communications systems. An optical communications link includes an optical source (*i.e.*, transmitter) that sends an optical signal to an optical detector (*i.e.*, receiver) via an optical path, such as an optical fiber, integrated-optics waveguide, or free space. The receiver then generates an electrical signal based on the optical signal received from the transmitter. The performance of an optical communications link is strongly dependent upon the sensitivity of its receiver. Historically, conventional receivers have been based on photodetectors such as avalanche photodetectors (APDs), PIN photodiodes, and phototransistors.

[0004] Telecommunications and data communications applications, in particular, require receivers that have very fast response times to enable high-bandwidth communications. The APD is an attractive choice in such applications due to its high bandwidth capability. Unfortunately, APDs have a number of drawbacks that have limited their adoption, such as a very high bias-voltage requirement (necessary for enabling avalanche amplification), high noise generation, and a strong sensitivity to temperature.

[0005] PIN photodiode-based receivers overcome some of the disadvantages of APD-based receivers. Unfortunately, the electrical signal generated by the photodiode is normally quite weak. As a result, it is usually necessary to amplify the output signal of the photodiode via one or more amplifier stages to enable its use in microelectronic circuits.

This is typically accomplished by connecting the photodiode to a conventional transistor via wire bonds, tab bonds, and the like. Unfortunately, this introduces large amounts of undesirable wire capacitance, which leads to a high energy cost for signal amplification.

[0006] Phototransistors avoid some of the wire capacitance associated with PIN-detector-based receivers by monolithically integrating the photodiode and a first stage of amplification, thereby providing the combined functionality of a photodiode and transistor. Perhaps the most common type of phototransistor is the bipolar phototransistor, which includes an emitter layer disposed on a base layer disposed on a collector layer. Light received by the device is absorbed in the base layer, the base-collector junction, and the collector layer. In these regions, the absorbed energy of the light gives rise to free-carrier pairs of electrons and holes. Holes generated in the base-collector junction are injected into the base and generate a photodiode current, which is amplified by the current gain of the transistor.

[0007] For use in high-bandwidth applications, a phototransistor must have low capacitance, high speed, and high efficiency. Unfortunately, for conventional bipolar phototransistors, these requirements are contradictory. The efficiency of a photodiode is a function of photon-absorption length, which in a typical semiconductor is on the order of microns. High efficiency, therefore, typically demands a large photon absorption volume. For high-speed operation, however, a very short transit region for amplified carriers is desirable - typically only a few tens of nanometers (nm) at most. As a result, there exists a 100x or greater mismatch in the desirable size of a phototransistor. In addition, increasing any dimension other than the transit direction results in prohibitively high capacitances.

[0008] The need for a high-speed, low-capacitance, efficient phototransistor suitable for use in communications links, or other high-bandwidth applications, remains unmet in the prior art.

Summary of the Invention

[0009] The present invention enables an optical receiver that can efficiently provide an electrical output signal suitable for use in microelectronic circuits. Phototransistors in accordance with the present invention include a base layer that serves as both a photon absorption region and a transistor gain region; however, the thickness of the photon absorption region is decoupled from the thickness of the transistor gain region.

Embodiments of the present invention are particularly well suited for use in cameras, sensors, and communications links, such as optical telecom, optical datacom, rack-to-rack links, chip-to-chip links, on-chip links, and the like.

[0010] Embodiments of the present invention comprise a phototransistor that includes a transistor region whose base/collector junction also serves as the PIN region of an integrated photodiode formed in a photodiode region of the device. Phototransistors in accordance with the present invention include a base layer that is common to both the transistor region and the photodiode region; however, in the transistor region, the thickness of the base layer is thinner than in the photodiode region. Specifically, the base/collector junction depth is kept shallow in the transistor region but is made much deeper in the photodiode region via an additional dopant implantation step. As a result, the transistor region is characterized by a short transit time, giving rise to a high f_t , while the photodiode region is characterized by a large depleted-carrier collection region having low capacitance.

[0011] In some embodiments, the phototransistor has a transistor region whose structure is that of a bipolar junction transistor. In some embodiments, the transistor region is that of a heterojunction bipolar transistor.

[0012] In some embodiments, the short transit time in the transistor region is enabled by a selectively implanted collector under the emitter of the transistor structure.

[0013] In some embodiments, the photodiode region is integrated with an integrated-optics waveguide. In some embodiments, the photodiode region is dimensioned and arranged to enable topside illumination through the base layer.

[0014] An embodiment of the present invention is a phototransistor (200) comprising: a first layer (226) that is a continuous layer having a first region (232) and a second region (234); a transistor region (206) comprising a transistor (202) that includes a collector (210), a base (212), and an emitter (214), the first region comprising the base; and a photodiode region (208) comprising a photodiode (204) that includes an absorption layer (224) and the second region; wherein the phototransistor is characterized by the first layer having a first thickness (t_1) in the first region (232) and a second thickness (t_2) in the second region (234), the second thickness being greater than the first thickness.

[0015] Another embodiment of the present invention is a method for forming a phototransistor (200) having a transistor region (206) and a photodiode region (208), the

method comprising: forming a collector layer (222) disposed on a substrate (228); forming a first layer (224) disposed on the collector layer, the first layer being substantially undoped; forming a base layer (226) disposed on the first layer, the base layer being a continuous layer having a first region (232) and a second region (234), the first transistor region including the first region and the photodiode region including the second region; forming an implant region (218) in the first layer, the implant region being in physical and electrical contact with the collector layer; and forming an emitter (214) disposed on the base layer; wherein the method is characterized by: formation of the base layer such that it has a first thickness (t1) in the first region and a second thickness (t2) in the second region, wherein the second thickness is greater than the first thickness.

Brief Description of the Drawings

[0016] FIG. 1 depicts a schematic drawing of a cross-sectional view of a phototransistor in accordance with the prior art.

[0017] FIGS. 2A-B depict schematic drawings of top and cross-sectional views, respectively, of a phototransistor in accordance with an illustrative embodiment of the present invention.

[0018] FIGS. 2C-D depict schematic drawings of enlarged cross-sectional views of transistor region **206** and photodiode region **208**, respectively, in accordance with the illustrative embodiment.

[0019] FIG. 3 depicts operations of a method suitable for fabricating a phototransistor in accordance with the illustrative embodiment.

[0020] FIGS. 4A-F depict schematic drawings of cross-sectional views of phototransistor **200** at different stages of its fabrication.

[0021] FIG. 5 depicts a schematic drawing of a cross-sectional view of the transistor region of a phototransistor in accordance with the present invention.

[0022] FIGS. 6A-B depict simulations of phototransistor **500**.

Detailed Description

[0023] FIG. 1 depicts a schematic drawing of a cross-sectional view of a phototransistor in accordance with the prior art. Phototransistor **100** is an npn bipolar phototransistor that includes collector **102**, base **104**, and emitter **106**. Base **104** includes detector region **108**, which is dimensioned and arranged such that it can receive light signal **110** such that its optical energy can be absorbed in the material of the base region.

[0024] In operation, phototransistor is biased such that the base-collector junction is reverse biased. Prior to the incidence of light signal **110** on detector region **108**; therefore, substantially no current flows between emitter **106** and collector **102**. When light signal **110** is incident on detector region **108**, however, the energy of the light liberates charge carriers that give rise to a macroscopically detectable current between collector **102** and emitter **106**.

[0025] Prior-art phototransistors, such as phototransistor **100**, have significant drawbacks – particularly with respect to their use in high-bandwidth applications. The speed of operation of the phototransistor (*i.e.*, its frequency response) is an inverse function of the length of transit region, t_a . In order to enable high-speed operation, therefore, it is desirable that t_a be short (preferably, tens of nm). A short carrier transit region also mitigates recombination of charge carriers before they can add to the photocurrent output, thereby improving efficiency of phototransistor **100**. Unfortunately, photon absorption is dependent upon the depth of base **104**, t_b , which determines the length over which incident light interacts with the absorptive material (*i.e.*, the absorption length). To ensure good photon absorption, t_b is preferably large - on the order of few microns. Unfortunately, in addition to increasing the length of the transit region, a deep base region further impairs high-speed operation because it gives rise to high capacitance for the device.

[0026] It is an aspect of the present invention, however, that high photon absorption and high speed can be enabled in a phototransistor by forming its base region such that its photon absorption region thickness is decoupled from the thickness of the transistor gain region. As a result, the structure of each region can be independently tailored to improve its desired functionality.

[0027] FIGS. 2A-B depict schematic drawings of top and cross-sectional views, respectively, of a phototransistor in accordance with an illustrative embodiment of the

present invention. Phototransistor **200** comprises transistor **202** and photodiode **204**, which are formed in transistor region **206** and photodiode region **208**, respectively. Phototransistor **200** is dimensioned and arranged to provide an electrical output signal in response to light signal **110**, which is received at photodiode region **208** via optical fiber **230**. In some embodiments, photodiode region **208** receives light signal **110** via a different means, such as via an integrated-optics waveguide, or via free-space optical coupling.

[0028] Transistor **202** is an npn heterojunction bipolar transistor (HBT) that includes collector **210**, base **212**, and emitter **214**. As discussed below and with respect to FIGS. 4A-F, base **212** comprises region **232** of base layer **226**, while collector **210** comprises implant region **218** and region **236** of collector layer **222** (also referred to as a "sub-collector" layer). Electrical connectivity to the collector, base, and emitter of transistor **202** is made via contact pads **216**, **218**, and **220**, respectively. In some embodiments, transistor **202** is a bipolar junction transistor (BJT). In some embodiments, transistor **202** is a pnp transistor.

[0029] Photodiode **204** is a PIN photodiode that includes region **234** of base layer **226**, absorption layer **224**, and region **238** of collector layer **222**. In the illustrative embodiment, photodiode **204** is formed on substrate **228** such that it is optically coupled with input waveguide **230**, enabling phototransistor **200** to detect light signal **110** as it is received from the waveguide. In some embodiments, photodiode **204** is dimensioned and arranged to detect light incident on its top surface.

[0030] As is the case in a conventional phototransistor, base layer **226** is a continuous layer that is included in both transistor region **206** and photodiode region **204**. As a result, base layer **226** forms a portion of each of transistor **202**, and also gives rise to a base/collection junction that also serves as the PIN region of photodiode **204**. It accordance with the present invention, however, the thickness of base layer **226** is much thinner in transistor region **206** than in photodiode region **208**, thereby tailoring the layer more appropriately for its role in each of the transistor and photodiode. Specifically, base layer **226** has thickness, **t1**, in transistor region **206** and thickness, **t2**, in photodiode region **208**, where **t1** is much thinner than **t2**. As a result, the base/collection junction depth in transistor region **206** is very shallow while the junction depth in photodiode region **208** is very deep (typically substantially equal to the thickness of absorption layer **224**).

[0031] FIGS. 2C-D depict schematic drawings of enlarged cross-sectional views of transistor region **206** and photodiode region **208**, respectively, in accordance with the illustrative embodiment.

[0032] The thin base/collector junction depth in transistor region **206** gives rise to a depletion region (*i.e.*, **dr1**) having a very shallow depletion layer width, **w1**. The shallow depletion layer width in transistor region **206** enables transistor **202** to have a very short carrier transit time, thereby ensuring a high f_t .

[0033] At the same time, the deep base/collector junction depth gives rise to depletion region, **dr2**, having large depletion region width, **w2**, in photodiode region **208**. As a result, photodiode **204** has a large depleted-carrier collection region having low capacitance. It also provides a thicker 'extrinsic' base region in photodiode region **208**, which reduces the base resistance for the collected carriers in the photodiode. Still further, since the base/collector depletion region is much larger in photodiode region **208**, its capacitance per unit area is drastically reduced, enabling the photon collection volume to be large compared to the dimension of transistor region **206** without having excess capacitance.

[0034] The present invention, therefore, enables phototransistors with:

- a transistor region having a short depletion region, short transit time (*i.e.*, large f_t), and/or small area (*i.e.*, low capacitance); and
- a photodiode region having a long depletion region, low capacitance per area, fast carrier collection (*i.e.*, drift-driven carrier collection), large area for improved light absorption, and/or a thicker base layer having lower resistance.

[0035] As a non-limiting example of the present invention, fabricating transistor **202** using the 22-nanometer node ITRS projection for BiCMOS HBT technologies would yield a transistor having a capacitance of approximately 60 attoFarads (aF). For a base layer thickness, **t2**, of 250 nm in photodiode region **208**, where the photodiode is germanium-based, the absorption area of photodiode **204** can be greater than 200x the transistor area without exceeding a capacitance of 60 aF.

[0036] One skilled in the art would recognize after reading this Specification, however, that a phototransistor fabricated using presently available manufacturing

processes would result in transistor **202** having a capacitance in the range of 10s of femtoFarads. It should be noted that a transistor capacitance in this range would still afford embodiments of the present invention significant advantages in many applications.

[0037] FIG. 3 depicts operations of a method suitable for fabricating a phototransistor in accordance with the illustrative embodiment. Method **300** begins with operation **301**, wherein collector layer **222** is grown on substrate **228**.

[0038] FIGS. 4A-F depict schematic drawings of cross-sectional views of phototransistor **200** at different stages of its fabrication. Method **300** is described with continuing reference to FIGS. 2A-B and FIGS. 4A-F.

[0039] Substrate **228** is a conventional silicon substrate suitable for use in planar processing. In some embodiments, substrate **228** comprises a material other than silicon. Materials suitable for use in substrate **228** include, without limitation, germanium, silicon compounds (e.g., silicon carbide, silicon germanium, etc.), III-V or II-VI compound semiconductors (e.g., gallium arsenide, indium phosphide, etc.), glass, and the like. One skilled in the art will recognize that the choice of materials for one or more of the constituent layers of phototransistor **200** are typically based on the choice of material for substrate **228**, as well as other factors such as the wavelength of operation, etc.

[0040] Collector layer **222** is a layer of silicon that is heavily doped with an appropriate n-type dopant, such as phosphorous, arsenic, antimony, etc. Typically, collector layer **222** is formed via an epitaxial growth process, such as molecular-beam epitaxy (MBE), atomic-layer epitaxy (ALE), vapor-phase epitaxy (VPE), liquid-phase epitaxy (LPE), and the like. In some embodiments, collector layer is formed via another suitable growth method, such as rapid-melt growth, and the like. It will be clear to one skilled in the art, after reading this Specification, how to specify, make, and use collector layer **222**.

[0041] FIG. 4A depicts phototransistor **200** after deposition of collector layer **222**.

[0042] At operation **302**, intrinsic layer **224** is formed on collector layer **222** using growth methods analogous to those described above. Intrinsic layer **224** is a layer of substantially undoped germanium. In some embodiments, intrinsic layer **224** comprises a suitable substantially intrinsic semiconductor other than germanium.

[0043] At operation **303**, nascent base layer **402** is formed on intrinsic layer **224** via epitaxial growth. The growth of nascent base layer **402** is analogous to the growth of

collector layer **222**, as described above. Nascent base layer **402** is a p-doped layer of germanium grown to a thickness of **t1**, which is the desired thickness of base layer **226** in transistor region **206**. Typically, thickness **t1** is within the range of approximately 20 nm to approximately 200 nm. In the depicted example, **t1** is approximately 50 nm. One skilled in the art will recognize, however, that any suitable value of thickness, **t1**, can be used without departing from the scope of the present invention.

[0044] At operation **304**, intrinsic layer **224** and nascent base layer **402** are patterned in conventional fashion to expose a portion of region **236** of collector layer **222**. Region **236** is substantially the portion of collector layer **222** that lies within transistor region **206**.

[0045] FIG. 4B depicts phototransistor **200** after the formation and patterning of intrinsic layer **224** and nascent base layer **402**.

[0046] At operation **305**, mask layer **404** is formed over nascent base layer **402** and the exposed portion of region **236**. Mask layer **404** is a layer of silicon oxide that includes window **406**, which exposes region **232** of nascent base layer **402**. Region **232** is a portion of nascent base layer **402** that lies within transistor region **206**.

[0047] At operation **306**, implant region **218** is formed in intrinsic layer **224** by implanting n-type dopants, such as phosphorous, etc., into the layer through window **406** and region **232**. Implant region **218** is a heavily n-doped region that extends substantially through the thickness of intrinsic layer **224** such that it is physically and electrically connected with region **236**. As a result, implant region **218** and region **236** collectively define collector **210** of transistor **202**. Implant region **218** also preferably substantially abuts region **232** of p-doped nascent base layer **402**, which gives rise to a p-n junction at the interface between them. One skilled in the art will recognize that the top edge of implant region **218** is not defined by an abrupt change in dopant concentration but, rather, an exponential decrease in dopant concentration as a result of the implantation process itself. As a result, implant region **218** is depicted as being separated from region **232** by a thin portion of intrinsic layer **224**; however, it should be noted that implant region **218** and region **232** still collectively give rise to depletion region **dr1**. The interface between implant region **218** and region **232** defines base **212**.

[0048] FIG. 4C depicts phototransistor **200** after the formation of mask layer **404** and implant region **218**.

[0049] At operation **307**, emitter **214** is formed in window **406** via conventional epitaxial growth and patterning techniques. In the depicted example, emitter **214** is a layer of n-doped germanium; however, one skilled in the art will recognize, after reading this Specification, that many different materials can be used to form emitter **214** without departing from the scope of the present invention.

[0050] FIG. 4D depicts phototransistor **200** after the formation of emitter **214**.

[0051] At operation **308**, mask layer **408** is formed and mask layers **404** and **408** are patterned to protect emitter **214** and expose the top surface of region **234** of nascent base layer **402** (*i.e.*, the region of nascent base layer **402** that is within photodiode region **208**). Like mask layer **404**, mask layer **408** is a layer of silicon oxide formed and patterned in conventional fashion.

[0052] At operation **309**, the thickness of base layer **226** in photodiode region **208** is increased to **t2**. The thickness of the base layer is increased by growing layer **410** on the exposed surface of nascent base layer **402** within region **234** via conventional selective-area epitaxial growth. In the depicted example, layer **410** is a layer of p-doped germanium grown to thickness **t3**, where the sum of thicknesses **t1** and **t3** is equal to the desired thickness, **t2**, of base layer **226** in photodiode region **208**. Typically, thickness **t2** is within the range of approximately 200 nm to approximately 2 microns. In the depicted example, **t2** is approximately 250 nm. One skilled in the art will recognize, however, that any suitable value of thickness, **t2**, can be used without departing from the scope of the present invention.

[0053] At the conclusion of operation **309**, base layer **226** comprises regions **232** and **234**, whose thicknesses are tailored for the use of base layer **226** in transistor **202** and photodiode **204**, respectively.

[0054] One skilled in the art will recognize that, since nascent base layer **402** is an epitaxially grown crystalline layer, its exposed surface acts as a crystal template that enables defect-free growth of layer **410**, which gives rise to a substantially homogeneous layer of base layer material in photodiode region **208**. In some embodiments, the thickness

of base layer **226** is increased in photodiode region **208** via another conventional method, such as non-selective-area epitaxial growth and patterning.

[0055] FIG. 4E depicts phototransistor **200** after the desired thickness of base layer **226** has been achieved in each of transistor region **206** and photodiode region **208**.

[0056] In some embodiments, base layer **226** is grown to an initial thickness of **t2** and subsequently thinned to a thickness of **t1** in transistor region **206** using conventional etching methods.

[0057] At operation **310**, contact pads **216**, **218**, and **220** are formed on collector **210**, base **212**, and emitter **214**, respectively, in conventional fashion. One skilled in the art will recognize that, in some cases, the contact pads must be formed in multiple operations since forming ohmic contacts to n-type semiconductors and p-type semiconductors can require different metals and processes.

[0058] Providing contact pads **216**, **218**, and **220** enables base **212** to be biased with an external current source. In some embodiments, however, phototransistor **200** is operated with a floating base and, therefore, contact pad **220** is not necessary.

[0059] FIG. 4F depicts phototransistor **200** after the formation of its contact pads.

[0060] It should be noted that the materials and layers described above are merely exemplary and that many alternatives are possible without departing from the scope of the present invention. For example, semiconductor materials suitable for use in the substrate and/or any of the layers of phototransistor **200**, in any combination, include, without limitation, silicon, silicon compounds (e.g., SiC, Si-Ge, etc.), germanium, III-V semiconductors (e.g., GaAs, InP, etc.), III-V semiconductor compounds (e.g., AlGaAs, InGaAsP, InGaAs, etc.), II-VI semiconductors (e.g., CdS, ZnSe, etc.), and II-VI semiconductor compounds. Further, phototransistor **200** can include semiconductor layers grown using techniques such as selective epitaxy or rapid-melt growth, or incorporate some silicon either in the base or the emitter, to benefit from gains already proven in heterojunction bipolar transistors. Ultimately, phototransistor **200** can be used in any system that requires an ultra-sensitive receiver. By altering silicon content, bandgap engineering and strain engineering can be utilized as they are already known to improve the performance of conventional BiCMOS transistors.

[0061] It should be noted that some embodiments of the present invention lead to increased manufacturing complexity; however, fabrication processes only slightly different from those used to fabricate conventional BiCMOS devices are possible without departing from the scope of the present invention. Further, the requirement that the transistor and photodiode are made of the same material can also be disadvantageous in some cases, since it reduces flexibility. In some such instances, however, emitter **214** can still contain a heterostructure.

[0062] FIG. 5 depicts a schematic drawing of a cross-sectional view of the transistor region of a phototransistor in accordance with the present invention. Phototransistor **500** is analogous to phototransistor **200** described above.

[0063] Phototransistor **500** is 2 micron wide HBT that includes collector **502**, base **504**, and emitter **506**, arranged as shown.

[0064] Collector **502** includes region **508** of collector layer **222** and implant region **510**. Collector **502** is a region of heavily doped (10^{19} cm^{-3}) n-type silicon. Implant region **510** is a region of intrinsic layer **512** that has been heavily implanted n-type dopants. In the depicted example, implant region **510** is a region of intrinsic layer **512** that has been implanted with a 200 keV implant dose of phosphorous (10^{15} cm^{-2} dose); however, it will be clear to one skilled in the art, after reading this Specification, that myriad dopant levels and dopants can be used to form implant region **510** without departing from the scope of the present invention.

[0065] Intrinsic layer **512** is a layer of undoped germanium having a thickness within the range of approximately 100 nm to approximately 2 microns. In the depicted example, intrinsic layer has a thickness of approximately 300 nm.

[0066] Base **504** comprises region **516** of base layer **514**. In the depicted example, base layer **514** is a p-doped base layer having a thickness of approximately 30 nm and a doping level of approximately $2 \times 10^{18} \text{ cm}^{-3}$.

[0067] Mask layer **518** is a layer of silicon oxide having a thickness of 100 nm, which is formed on the top surface of base layer **514**. Mask layer **518** is etched to form mask opening **520**. In the depicted example, mask opening **520** is a 100 nm-wide opening that defines the region of emitter **506**, as well as an opening through which implant region **510** is formed. In some embodiments, mask layer **518** has a different thickness suitable for

providing sufficient masking capabilities for ion implantation. In some embodiments, mask layer **518** comprises a suitable material other than silicon oxide.

[0068] Emitter **506** is a region of n+ polysilicon that is deposited and patterned to define the emitter structure. It should be noted that emitter **506** is typically diffused slightly into base layer **514** (not shown) via rapid thermal annealing.

[0069] Embodiments of the present invention in accordance with exemplary phototransistor **500** mitigate some of the cost and complexity associated with the formation of prior-art phototransistors by forming the emitter, base, and collector in a self-aligned manner through mask opening **520**.

[0070] Contact pads **220** are formed in regions opened on the sides of oxide layer **512** to expose regions of base **504**.

[0071] FIGS. 6A-B depict simulations of phototransistor **500**.

[0072] Plot **600** depicts an electrical simulation of phototransistor **500** with a 1 volt bias applied to collector **502**. The bias on the base-emitter was optimized for gain and bandwidth. Plot **600** shows a peak of 120 GHz electrical gain-bandwidth product with a bias of 0.59 volts on the base-emitter voltage with a current gain of 6 (15.5 dB).

[0073] Plot **602** shows the optical response of transistor **500** under uniform illumination. Plot **602** evinces that the same optimal bias point gives a bandwidth of 18 GHz.

[0074] It can be seen from FIGS. 6A-B that a phototransistor in accordance with the present invention can exhibit both high gain-bandwidth product and fast carrier collection.

[0075] It is to be understood that the disclosure teaches just one example of the illustrative embodiment and that many variations of the invention can easily be devised by those skilled in the art after reading this disclosure and that the scope of the present invention is to be determined by the following claims.

What is claimed is:

- 1.** A phototransistor (200) comprising:
 - a first layer (226) that is a continuous layer having a first region (232) and a second region (234);
 - a transistor region (206) comprising a transistor (202) that includes a collector (210), a base (212), and an emitter (214), the first region comprising the base; and
 - a photodiode region (208) comprising a photodiode (204) that includes an absorption layer (224) and the second region;wherein the phototransistor is characterized by the first layer having a first thickness (t1) in the first region (232) and a second thickness (t2) in the second region (234), the second thickness being greater than the first thickness.
- 2.** The phototransistor of claim 1 wherein the collector comprises:
 - a second layer (222) comprising a third region (236) and a fourth region (238); and
 - an implant region (218), the implant region including a portion of the absorption layer (224), wherein the implant region and the first region (232) collectively give rise to a first depletion region (dr1) having a first width (w1).
- 3.** The phototransistor of claim 2 wherein the second region (234), the absorption layer (224), and the fourth region (238) collectively give rise to a second depletion region (dr2) in the photodiode region (208), the second depletion region having a second width (w2) that is larger than the first width (w1).
- 4.** The phototransistor of claim 1 wherein the transistor (202) is a heterojunction bipolar transistor having a capacitance that is less than or equal to 100 femtoFarads.
- 5.** The phototransistor of claim 4 wherein the transistor (202) has a capacitance within the range of approximately 20 attoFarads to approximately 100 attoFarads.
- 6.** The phototransistor of claim 4 wherein the transistor has a capacitance of approximately 60 attoFarads.
- 7.** The phototransistor of claim 1 wherein the transistor is a bipolar junction transistor having a capacitance that is less than or equal to 100 femtoFarads.
- 8.** The phototransistor of claim 7 wherein the transistor has a capacitance within the range of approximately 20 attoFarads to approximately 100 attoFarads.

9. The phototransistor of claim 7 wherein the transistor has a capacitance of approximately 60 attoFarads.

10. A method for forming a phototransistor (200) having a transistor region (206) and a photodiode region (208), the method comprising:

forming a collector layer (222) disposed on a substrate (228);

forming a first layer (224) disposed on the collector layer, the first layer being substantially undoped;

forming a base layer (226) disposed on the first layer, the base layer being a continuous layer having a first region (232) and a second region (234), the first transistor region including the first region and the photodiode region including the second region;

forming an implant region (218) in the first layer, the implant region being in physical and electrical contact with the collector layer; and

forming an emitter (214) disposed on the base layer;

wherein the method is characterized by:

formation of the base layer such that it has a first thickness (t1) in the first region and a second thickness (t2) in the second region, wherein the second thickness is greater than the first thickness.

11. The method of claim 10 wherein the implant region and base layer are formed such that they give rise to a first depletion region (dr1) having a first depletion region width (w1) in the transistor region, and wherein the base layer, first layer, and collector layer are formed such that they give rise to a second depletion region (dr2) having a second depletion region width (w2) in the photodiode region.

12. The method of claim 10 wherein the base layer (226) is formed by operations including:

forming a first sub-layer (402) on the first layer (224), the first sub-layer having the first thickness (t1), and the first sub-layer being located in each of the transistor region and the photodiode region; and

forming a second sub-layer (410) on the first sub-layer, the second sub-layer having a third thickness (t3), the second sub-layer being in the photodiode region and not in the transistor region;

wherein the sum of the first thickness (t1) and third thickness (t3) equals the second thickness (t2).

13. The method of claim 12 wherein the second sub-layer (410) is formed via selective-area epitaxial growth.

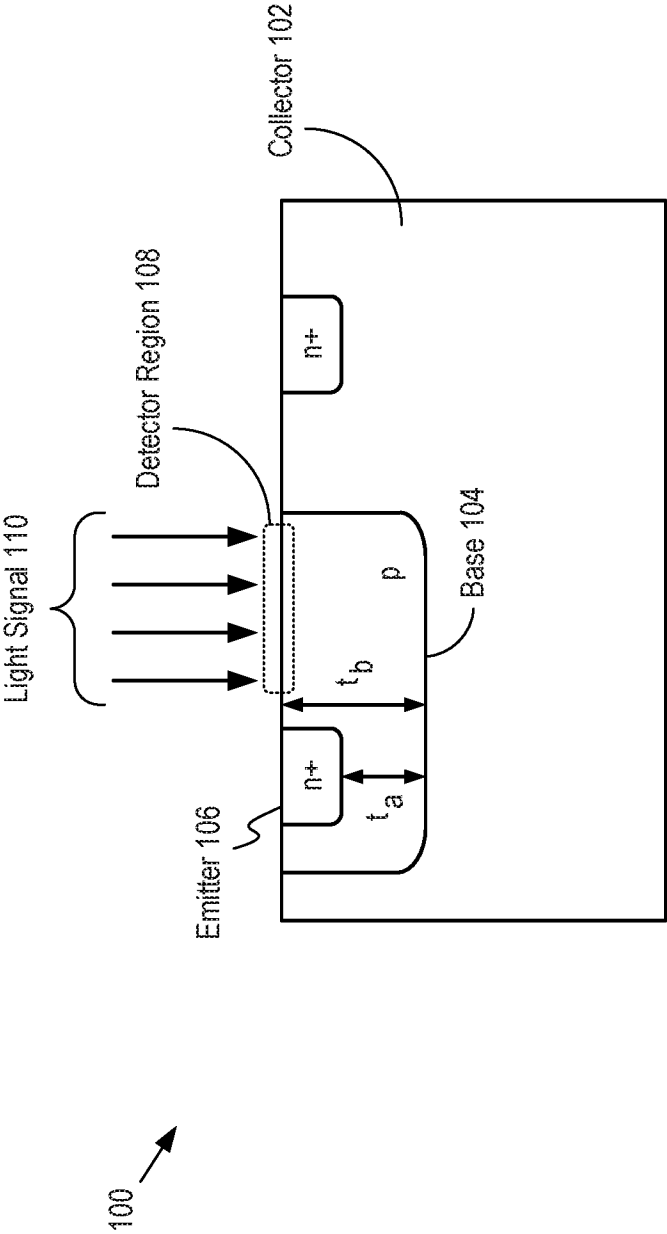
14. The method of claim 10 wherein the base layer is formed by operations including:

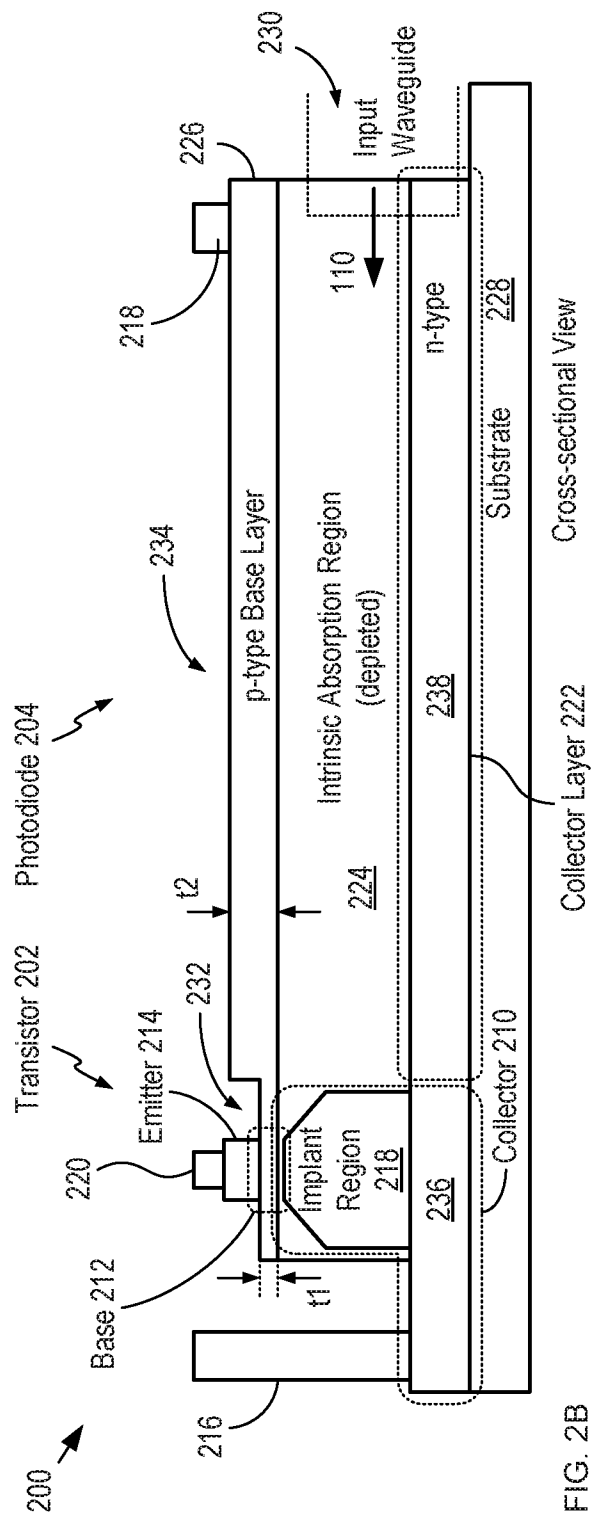
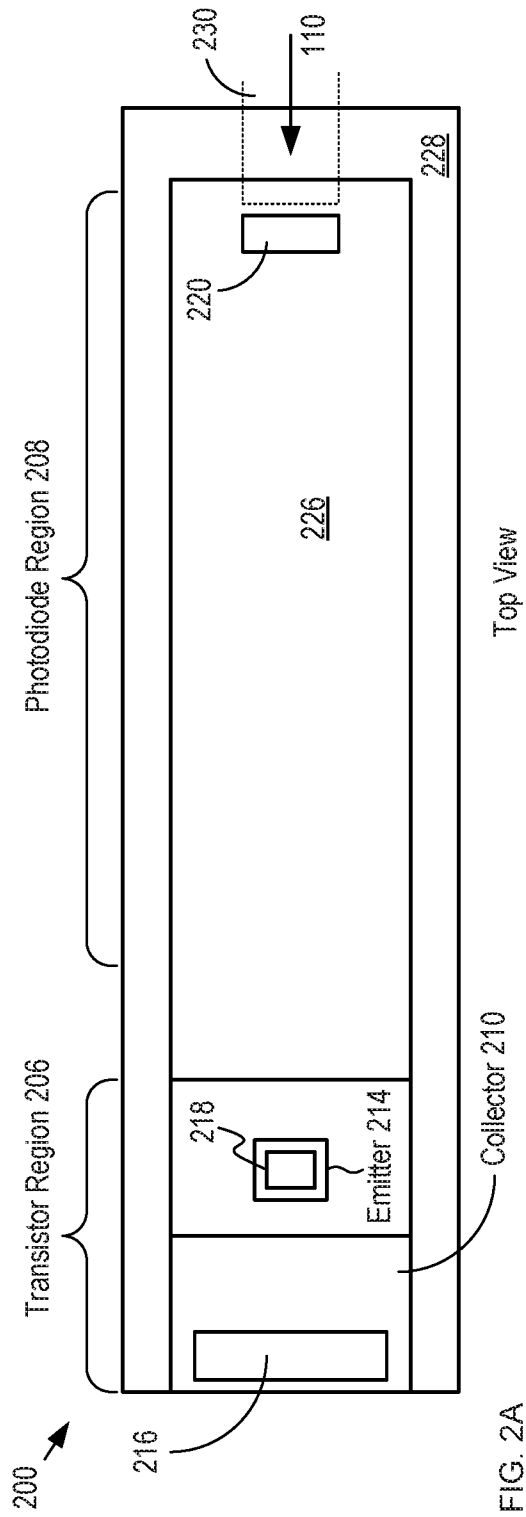
forming the base layer (226) such that it is located each of the transistor region and the photodiode region, the base layer being formed with the second thickness (t2); and

reducing the thickness of the base layer in the transistor region to the first thickness (t1).

15. The method of claim 10 wherein the phototransistor is formed such that the transistor region (206) includes a transistor (202) that is a heterojunction bipolar transistor having a capacitance that is less than or equal to 100 femtoFarads.

FIG. 1 (Prior Art)





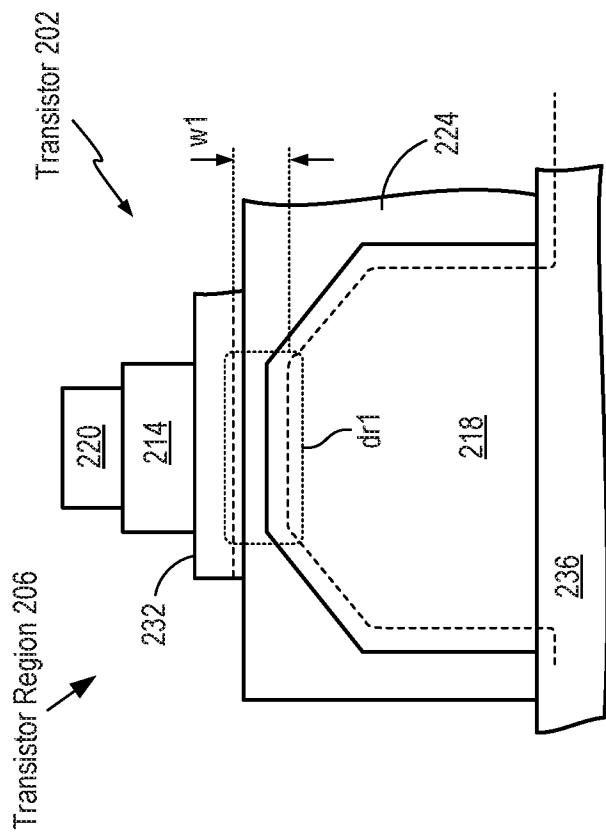


FIG. 2C

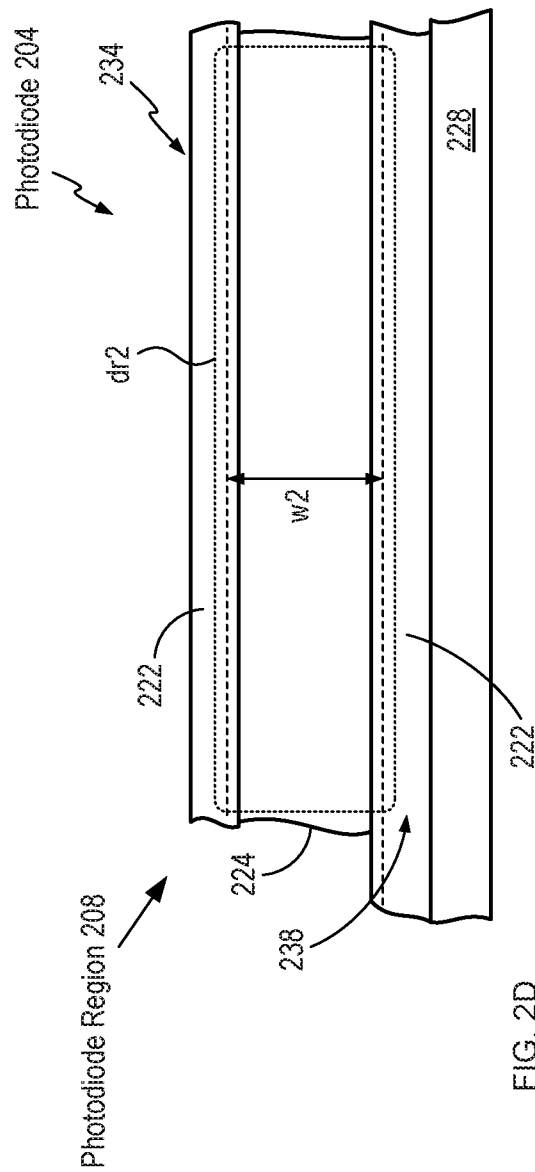
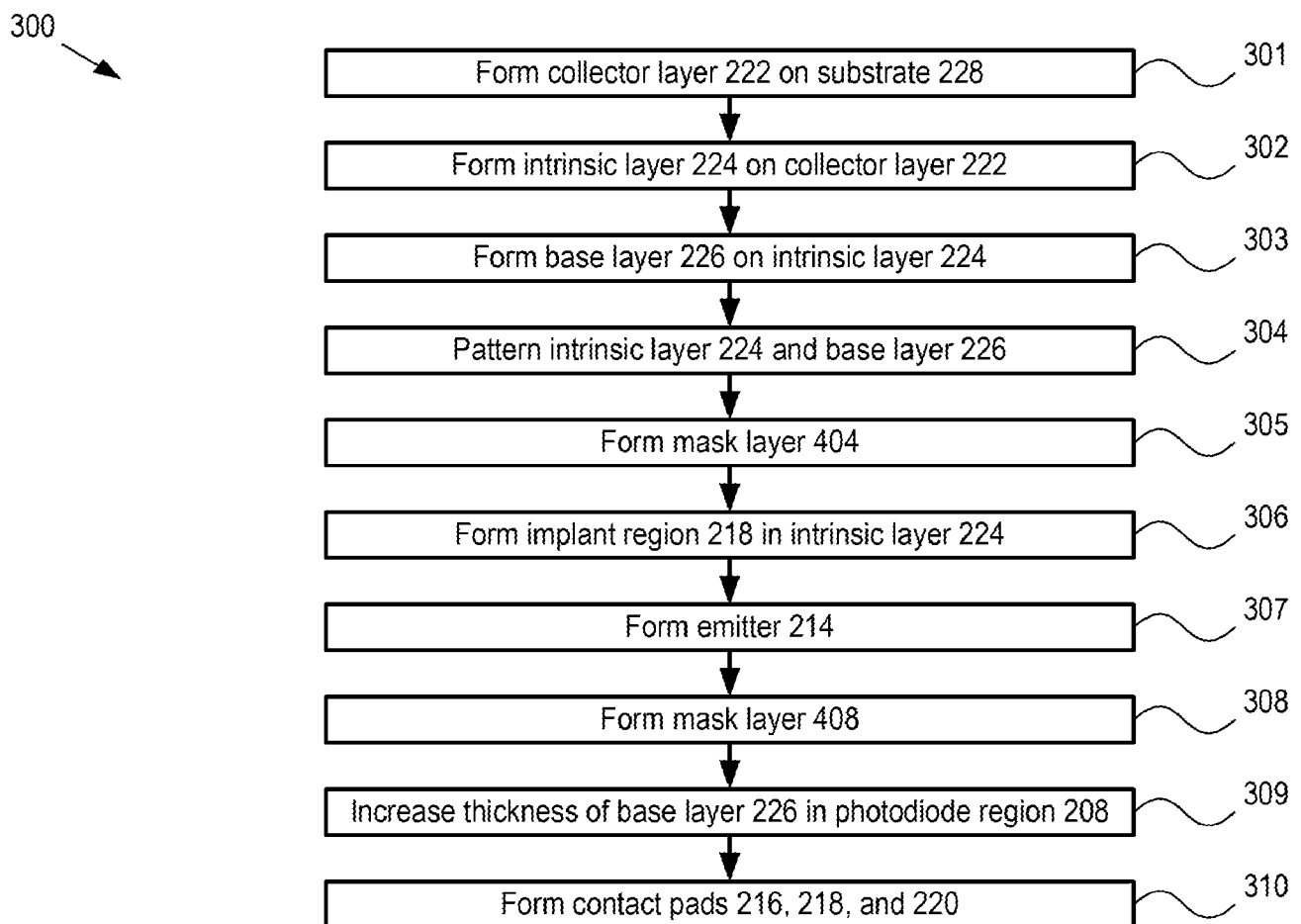


FIG. 2D

FIG. 3



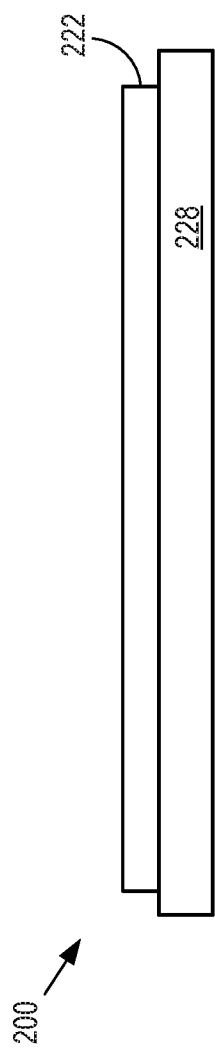


FIG. 4A

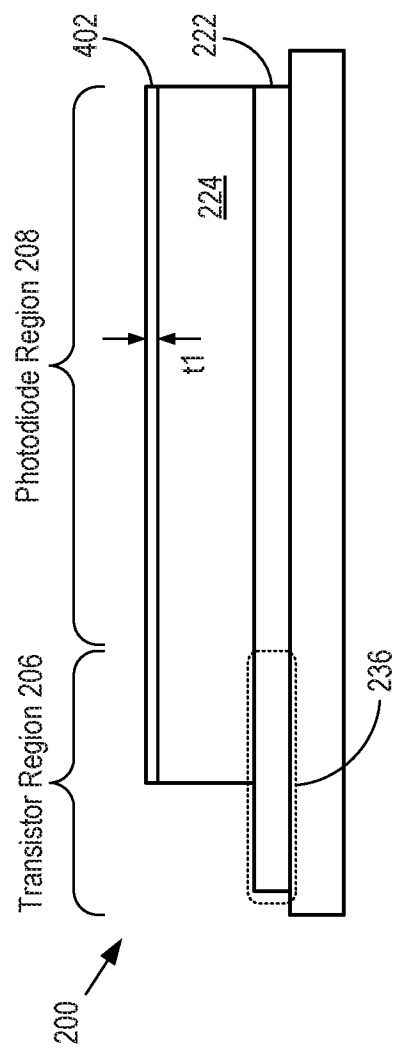


FIG. 4B

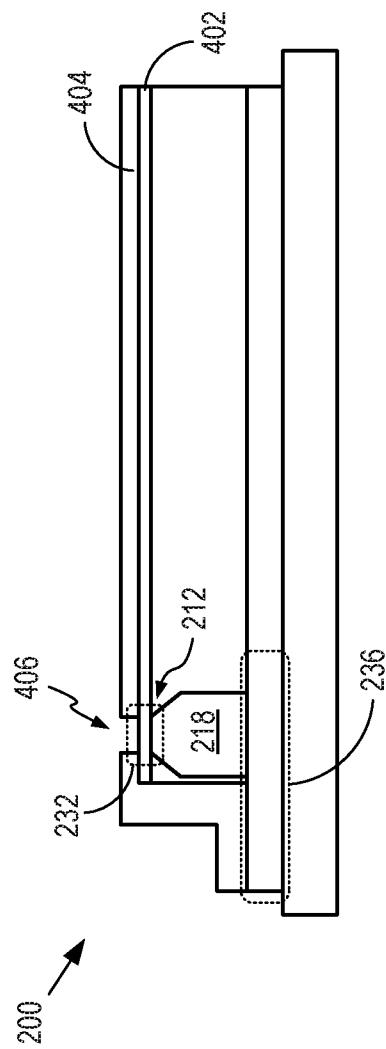


FIG. 4C

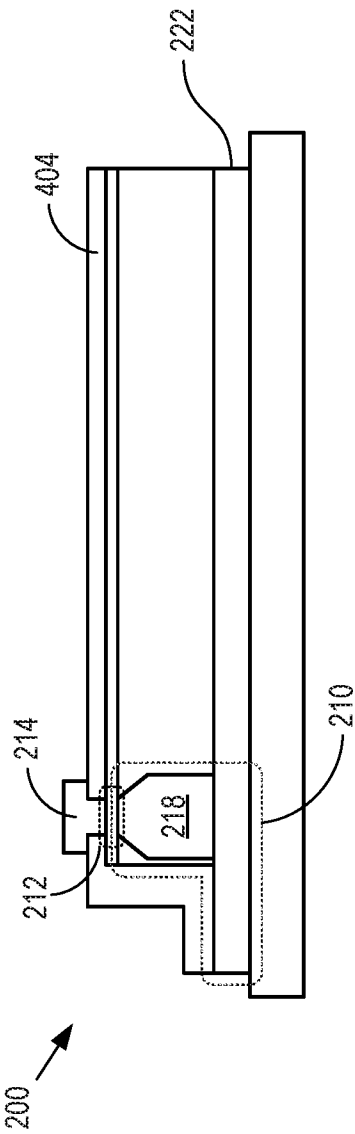


FIG. 4D

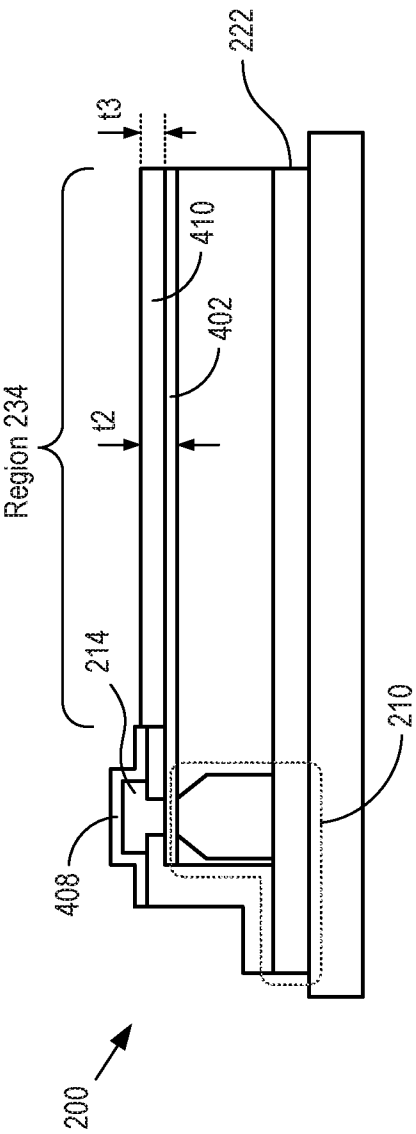


FIG. 4E

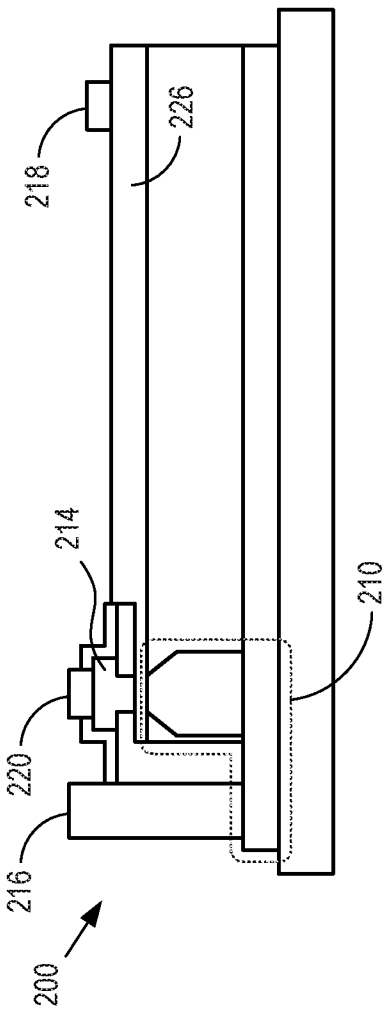


FIG. 4F

FIG. 5

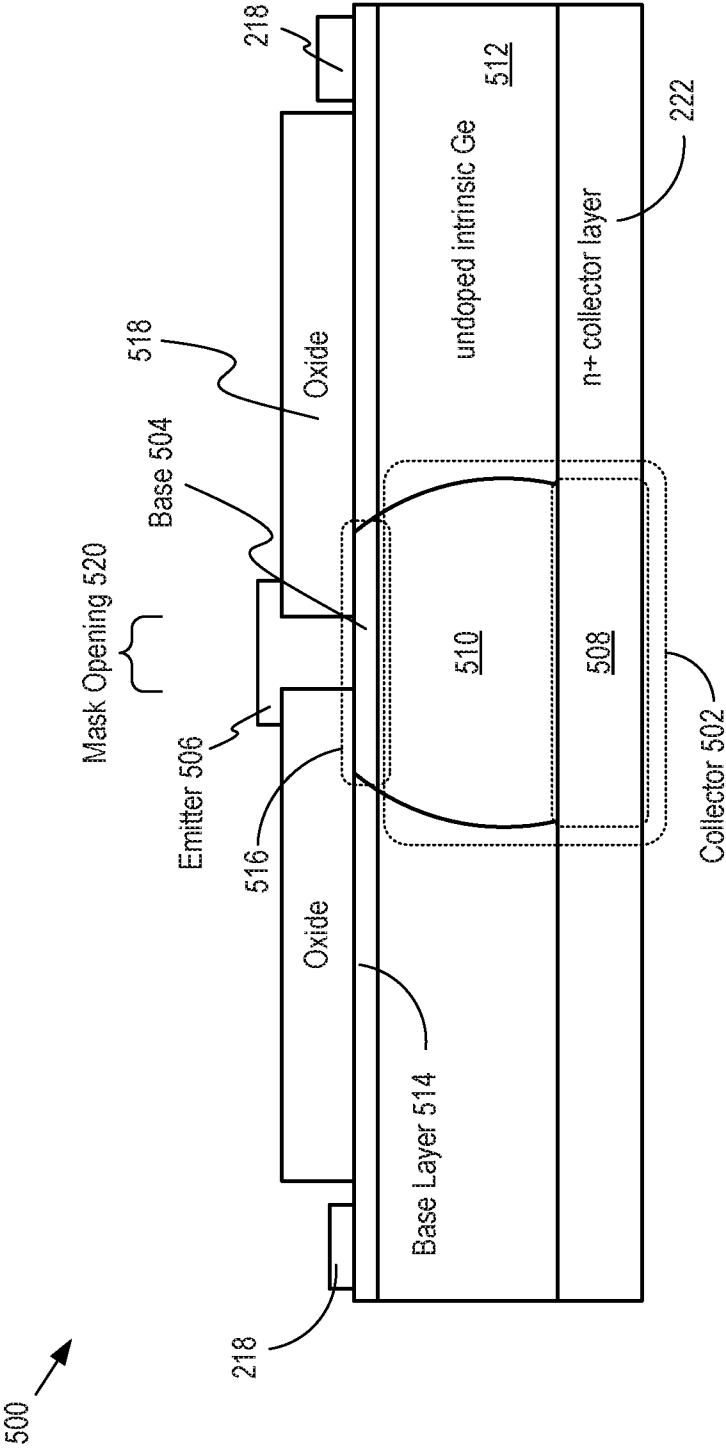


FIG. 6A

600

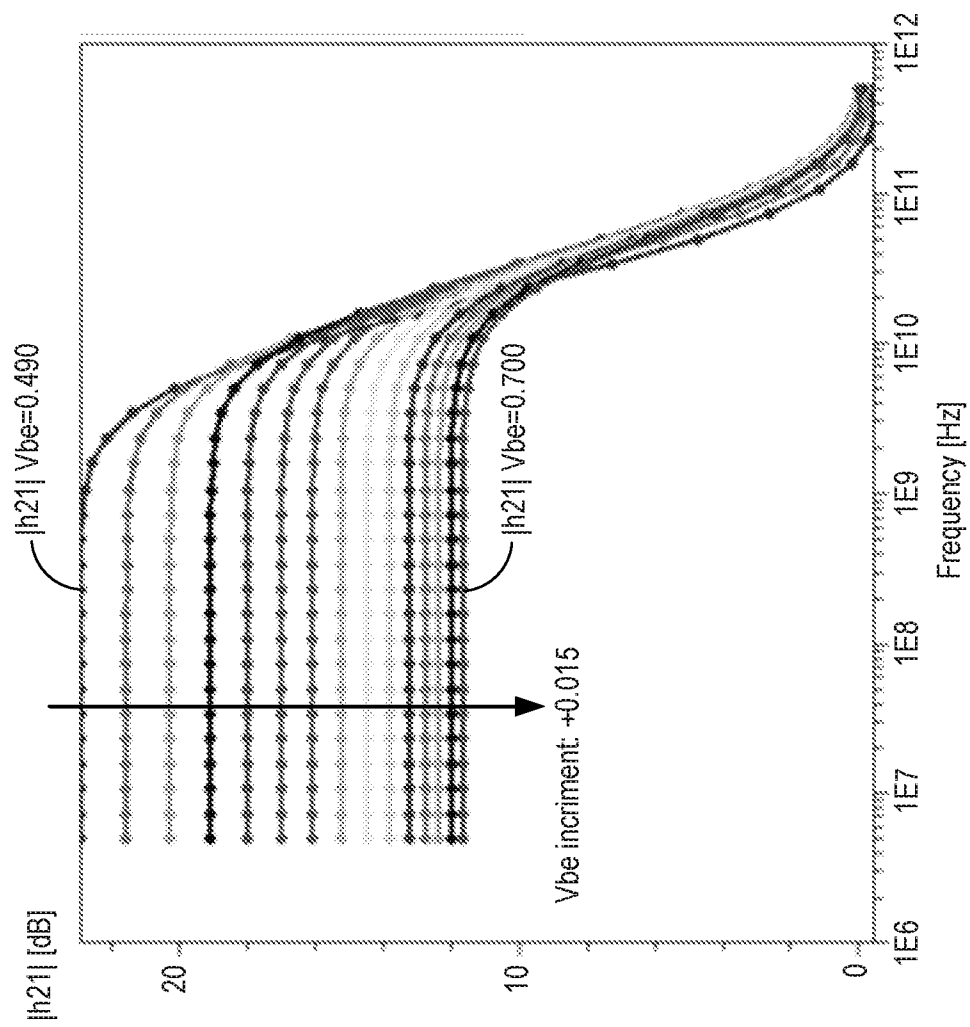
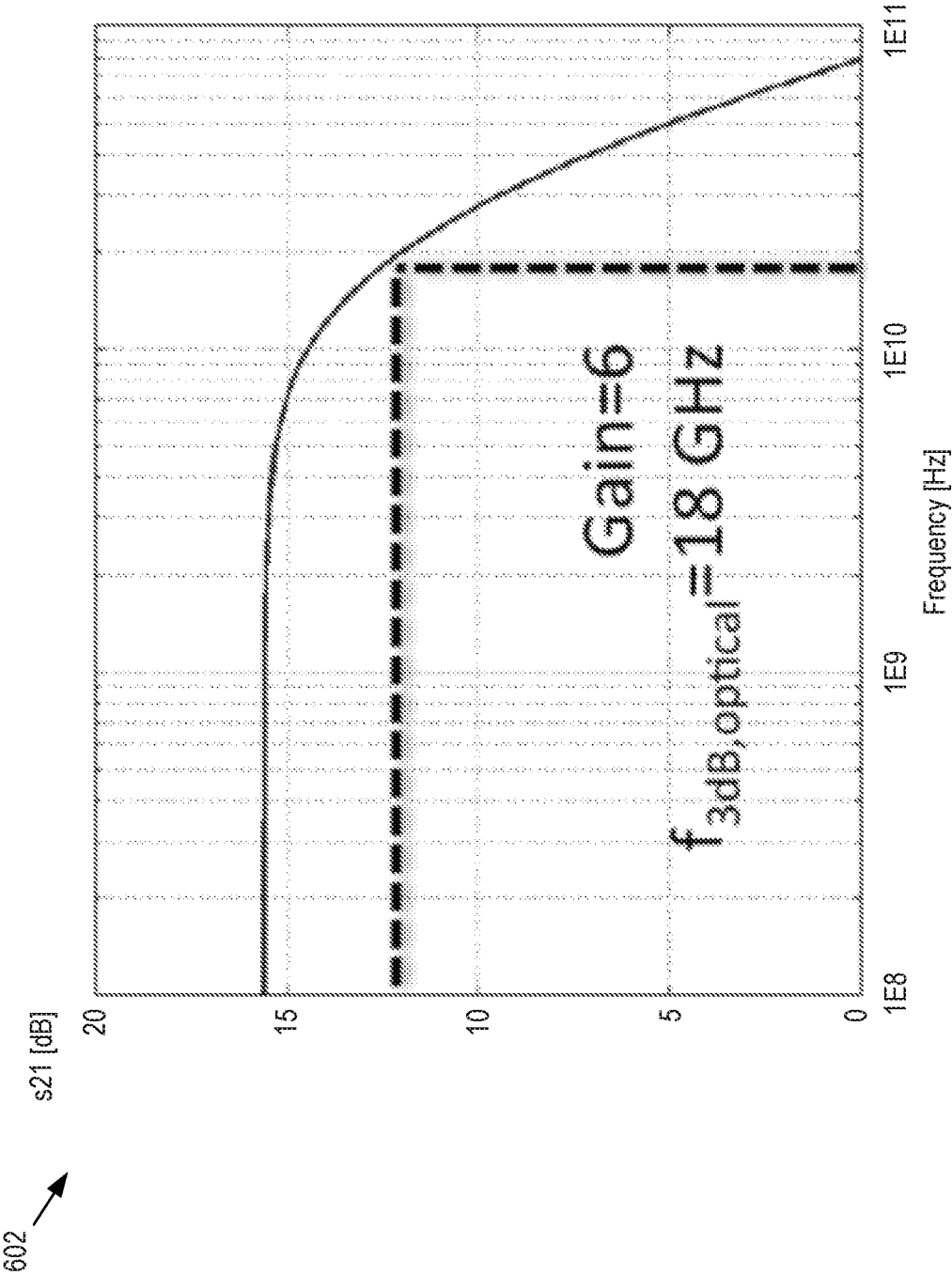


FIG. 6B



INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2016/028069

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H01L 27/14; H01L 27/102; H01L 31/101; H01L 31/18 (2016.01)

CPC - H01L 27/14; H01L 27/1022; H01L 31/101; H01L 31/18 (2016.05)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC(8) - C30B 25/04; G02B 6/12; H01L 27/102; H01L 27/14; H01L 29/225; H01L 31/10; H01L 31/101; H01L 31/105; H01L 31/18
CPC - C30B 25/04; G02B 6/12; H01L 27/1022; H01L 27/14; H01L 29/225; H01L 31/10; H01L 31/101;
H01L 31/105; H01L 31/105; H01L 31/18 (2016.05)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

USPC - 257/446; 257/458; 357/30; 357/43; 438/59 (keyword delimited)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Patbase, Google Patents, Google

Search terms used: phototransistor, pin diode, npn transistor, monolithic

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,410,175 A (KYOMASU et al) 25 April 1995 (25.04.1995) entire document	1-15
Y	US 3,677,280 A (WECKLER) 18 July 1972 (18.07.1972) entire document	1-15
Y	US 2006/0289960 A1 (WU) 28 December 2006 (28.12.2006) entire document	2, 3, 10-15
Y	US 5,063,426 A (CHANDRASEKHAR et al) 05 November 1991 (05.11.1991) entire document	4-6, 15
Y	US 4,622,093 A (TSANG) 11 November 1986 (11.11.1986) entire document	13
A	US 2007/0014508 A1 (CHEN et al) 18 January 2007 (18.01.2007) entire document	1-15
A	US 5,101,253 A (MIZUTANI et al) 31 March 1992 (31.03.1992) entire document	1-15
A	US 5,027,177 A (VASUDEV) 25 June 1991 (25.06.1991) entire document	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

19 June 2016

Date of mailing of the international search report

26 JUL 2016

Name and mailing address of the ISA/

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