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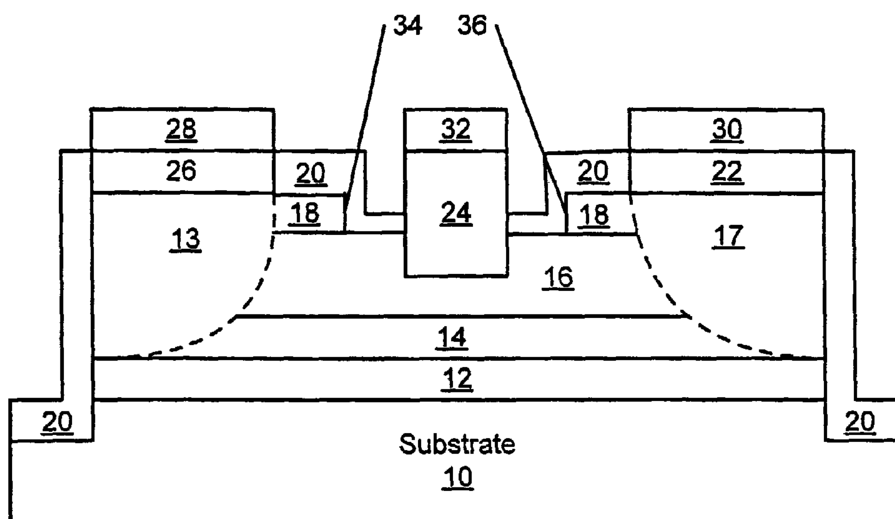

(57) Abstract: The present invention provides a unit cell of a metal-semiconductor field-effect transistor (MESFET). The unit cell of the MESFET includes a delta doped silicon carbide MESFET having a source (13), a drain 817) and a gate (24). The gate (24) is situated between the source (13) and the drain (17) and extends into a doped channel layer (16) of a first conductivity type. Regions of silicon carbide adjacent to the source (13) and the drain (17) extend between the source (13) and the gate and the drain (17) and the gate (24), respectively. The regions of silicon carbide have carrier concentrations that are greater than a carrier concentration of the doped channel layer (16) and are spaced apart from the gate (24).

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

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DELTA DOPED SILICON CARBIDE METAL-SEMICONDUCTOR FIELD EFFECT TRANSISTORS AND METHODS OF FABRICATING THEM

Field of the Invention

The present invention relates to microelectronic devices and more particularly to metal-semiconductor field-effect transistors (MESFETs) formed in silicon carbide.

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Background of the Invention

Electrical circuits requiring high power handling capability (>20 watts) while operating at high frequencies such as radio frequencies (500 MHz), S-band (3 GHz) and X-band (10 GHz) have in recent years become more prevalent. Because of the increase in high power, high frequency circuits there has been a corresponding
10 increase in demand for transistors which are capable of reliably operating at radio frequencies and above while still being capable of handling higher power loads. Previously, bipolar transistors and power metal-oxide semiconductor field effect transistors (MOSFETs) have been used for high power applications but the power handling capability of such devices may be limited at higher operating frequencies.
15 Junction field-effect transistors (JFETs) were commonly used for high frequency applications but the power handling capability of previously known JFETs may also be limited.

Recently, metal-semiconductor field effect transistors (MESFETs) have been developed for high frequency applications. The MESFET construction may be
20 preferable for high frequency applications because only majority carriers carry current. The MESFET design may be preferred over current MOSFET designs because the reduced gate capacitance permits faster switching times of the gate input. Therefore, although all field-effect transistors utilize only majority carriers to carry

current, the Schottky gate structure of the MESFET may make the MESFET more desirable for high frequency applications.

In addition to the type of structure, and perhaps more fundamentally, the characteristics of the semiconductor material from which a transistor is formed also affects the operating parameters. Of the characteristics which affect a transistor's operating parameters, the electron mobility, saturated electron drift velocity, electric breakdown field and thermal conductivity may have the greatest effect on a transistor's high frequency and high power characteristics.

Electron mobility is the measurement of how rapidly an electron is accelerated to its saturated velocity in the presence of an electric field. In the past, semiconductor materials which have a high electron mobility were preferred because more current could be developed with a lesser field, resulting in faster response times when a field is applied. Saturated electron drift velocity is the maximum velocity which an electron can obtain in the semiconductor material. Materials with higher saturated electron drift velocities are preferred for high frequency applications because the higher velocity translates to shorter times from source to drain.

Electric breakdown field is the field strength at which breakdown of the Schottky junction and the current through the gate of the device suddenly increases. A high electric breakdown field material is preferred for high power, high frequency transistors because larger electric fields generally can be supported by a given dimension of material. Larger electric fields allow for faster transients as the electrons can be accelerated more quickly by larger electric fields than by smaller.

Thermal conductivity is the ability of the semiconductor material to dissipate heat. In typical operations, all transistors generate heat. In turn, high power and high frequency transistors usually generate larger amounts of heat than small signal transistors. As the temperature of the semiconductor material increases, the junction leakage currents generally increase and the current through the field effect transistor generally decreases due to a decrease in carrier mobility with an increase in temperature. Therefore, if the heat is dissipated from the semiconductor, the material will remain at a lower temperature and be capable of carrying larger currents with lower leakage currents.

In the past, most high frequency MESFETs have been manufactured of n-type III-V compounds, such as gallium arsenide (GaAs) because of their high electron mobilities. Although these devices provided increased operating frequencies and

moderately increased power handling capability, the relatively low breakdown voltage and the lower thermal conductivity of these materials have limited their usefulness in high power applications.

Silicon carbide (SiC) has been known for many years to have excellent physical and electronic properties which should theoretically allow production of electronic devices that can operate at higher temperatures, higher power and higher frequency than devices produced from silicon (Si) or GaAs. The high electric breakdown field of about 4×10^6 V/cm, high saturated electron drift velocity of about 2.0×10^7 cm/sec and high thermal conductivity of about 4.9 W/cm-°K indicate that SiC would be suitable for high frequency, high power applications. Unfortunately, difficulty in manufacturing has limited the usefulness of SiC for high power and high frequency applications.

Recently, MESFETs having channel layers of silicon carbide have been produced on silicon substrates (*see* U.S. Pat. Nos. 4,762,806 to Suzuki *et al.* and 4,757,028 to Kondoh *et al.*). Because the semiconductor layers of a MESFET are epitaxial, the layer upon which each epitaxial layer is grown affects the characteristics of the device. Thus, a SiC epitaxial layer grown on a Si substrate generally has different electrical and thermal characteristics then a SiC epitaxial layer grown on a different substrate. Although the SiC on Si substrate devices described in U.S. Pat. Nos. 4,762,806 and 4,757,028 may have exhibited improved thermal characteristics, the use of a Si substrate generally limits the ability of such devices to dissipate heat. Furthermore, the growth of SiC on Si generally results in defects in the epitaxial layers which result in high leakage current when the device is in operation.

Other MESFETs have been developed using SiC substrates. U.S. patent application Ser. No. 07/540,488 filed Jun. 19, 1990 and now abandoned, the disclosure of which is incorporated entirely herein by reference, describes a SiC MESFET having epitaxial layers of SiC grown on a SiC substrate. These devices exhibited improved thermal characteristics over previous devices because of the improved crystal quality of the epitaxial layers grown on SiC substrates. However, to obtain high power and high frequency it may be necessary to overcome the limitations of SiC's lower electron mobility.

Similarly, commonly assigned United States Patent No. 5,270,554 to Palmour describes a SiC MESFET having source and drain contacts formed on n^+ regions of SiC and an optional lightly doped epitaxial layer between the substrate and

the n-type layer in which the channel is formed. United States Patent No. 5,925,895 to Sriram *et al.* also describes a SiC MESFET and a structure which is described as overcoming "surface effects" which may reduce the performance of the MESFET for high frequency operation. Sriram *et al.* also describes SiC MESFETs which use n^+ source and drain contact regions as well as a p-type buffer layer. However, despite the performance reported in these patents, further improvements may be made in SiC MESFETs.

For example, conventional SiC FET structures may provide the constant characteristics during the entire operating range of the FET, *i.e.* from fully open channel to near pinch-off voltage, by using a very thin, highly doped channel (a delta doped channel) offset from the gate by a lightly doped region of similar conductivity type. Delta doped channels are discussed in detail in an article by Yokogawa *et al.* entitled *Electronic Properties of Nitrogen Delta-Doped Silicon Carbide Layers*, MRS Fall Symposium, 2000 and an article by Konstantinov *et al.* entitled *Investigation of Lo-Hi-Lo and Delta Doped Silicon Carbide Structure*, MRS Fall Symposium, 2000. The structures discussed in these articles utilize delta doped channels and provide high breakdown voltages which is desirable for high power applications. However, these devices also have increased source and drain resistances due to the lower mobility of the delta doped channel, which is not desirable. The increased source and drain resistances cannot, typically, be overcome by simply increasing the carrier concentration of the delta doped channel because this may decrease the breakdown voltage, which may be an important device characteristic as discussed above.

Summary of the Invention

Embodiments of the present invention provide a unit cell of a metal-semiconductor field-effect transistor (MESFET). The unit cell of the MESFET includes a delta doped silicon carbide MESFET having a source, a drain and a gate. The gate is situated between the source and the drain and extends into a doped channel layer of a first conductivity type. Regions of silicon carbide adjacent to the source and the drain extend between the source and the gate and the drain and the gate, respectively. The regions of silicon carbide have carrier concentrations that are greater than a carrier concentration of the doped channel layer. The regions of silicon carbide are also spaced apart from the gate.

In further embodiments of the present invention, the delta doped silicon carbide MESFET and the regions of silicon carbide include a silicon carbide substrate and a delta doped layer of a first conductivity type silicon carbide on the substrate. The doped channel layer of the first conductivity type silicon carbide on the delta 5 doped layer has a carrier concentration that is less than at least one carrier concentration of the delta doped layer. Ohmic contacts on the doped channel layer may respectively define the source and the drain. A cap layer of the first conductivity type silicon carbide on the doped channel layer has a carrier concentration that is greater than the carrier concentration of the doped channel layer. A first recess is 10 positioned between the source and the drain. The first recess has a first floor that extends through the cap layer into the doped channel layer a first distance. The gate is in the first recess and extends into the doped channel layer. A second recess is positioned between the source and the drain and has a second floor that extends a second distance, less than the first distance, through the cap layer to the doped 15 channel layer. The second recess has respective sidewalls which are between respective ones of the source and the gate and the drain and the gate and are spaced apart from the gate, the source and the drain so as to define regions of the cap layer extending between respective ones of the source and the gate and the drain and the gate to provide the regions of silicon carbide.

20 In further embodiments of the present invention, the second floor of the second recess extends into the doped channel layer a third distance. The silicon carbide substrate may be a semi-insulating silicon carbide substrate. The first conductivity type silicon may be n-type conductivity silicon carbide or p-type conductivity silicon carbide.

25 In still further embodiments of the present invention the regions of silicon carbide may be implanted regions. In other embodiments of the present invention, the regions of silicon carbide are grown in a single growth step with the delta doped layer and the doped channel layer. In further embodiments of the present invention, the delta doped layer, the doped channel layer and the cap layer are grown on the 30 substrate.

In additional embodiments of the present invention, the cap layer may have a carrier concentration of from about 3×10^{17} cm^{-3} to about 6×10^{17} cm^{-3} and a thickness of from about 500 Å to about 1000 Å. The delta doped layer may have a carrier concentration from about 2×10^{18} cm^{-3} to about 3×10^{18} cm^{-3} and a thickness

from about 200 Å to about 300 Å. The doped channel layer may have a carrier concentration of from about 1×10^{16} cm^{-3} to about 5×10^{16} cm^{-3} and a thickness of from about 1800 Å to about 3500 Å.

In further embodiments of the present invention, the MESFET further includes
5 a buffer layer of a second conductivity type silicon carbide between the substrate and the delta doped layer. For a p-type buffer layer, the buffer layer may have a carrier concentration of about 1.0×10^{16} cm^{-3} to about 6×10^{16} cm^{-3}, but typically about 1.5×10^{16} cm^{-3}. The buffer layer may have a thickness of from about 0.2 μm to about 0.5 μm. For an n-type buffer layer, the buffer layer may have a carrier concentration of
10 about 1×10^{15} cm^{-3} or less and a thickness of about 0. 25 μm. The second conductivity type silicon carbide may be p-type conductivity silicon carbide, n-type conductivity silicon carbide or undoped silicon carbide.

In still further embodiments of the present invention, the MESFET may further include regions of first conductivity type silicon carbide under the source and
15 the drain which has a carrier concentration that is greater than the carrier concentration of the doped channel layer. The region of first conductivity type silicon carbide may have a carrier concentration of at least about 1×10^{19} cm^{-3}. In other embodiments of the present invention, the MESFET may further include an oxide layer on the cap layer and the doped channel layer.

20 In further embodiments of the present invention the ohmic contacts comprise nickel contacts. The MESFET may further comprise an overlayer on the ohmic contacts. In still further embodiments of the present invention, the delta doped layer and the doped channel layer form a mesa having sidewalls which define the periphery of the transistor and which extend through the delta doped layer and the
25 doped channel layer. The sidewalls of the mesa may or may not extend into the substrate.

In additional embodiments of the present invention, the first distance may be from about 0.07 μm to about 0.25 μm and the second distance may be from about 500 Å to about 1000 Å. The gate may include a first gate layer of chromium on the doped
30 channel layer and an overlayer on the first gate layer that comprises platinum and gold. Alternatively, the gate may include a first gate layer of nickel on the doped channel layer and an overlayer on the first gate layer, wherein the overlayer comprises gold. The gate may have a length from about 0.4 μm to about 0.7 μm. The distance from the source to the gate may be from about 0.5 μm to about 0.7 μm. The distance

from the drain to the gate may be from about 1.5 μm to about 2 μm. The distance between the source and a first one of the sidewalls of the second recess may be from about 0.1 μm to about 0.4 μm and the distance between the drain and a second one of the sidewalls of the second recess may be from about 0.9 μm to about 1.7 μm. The distance between a first one of the sidewalls of the second recess and the gate may be from about 0.3 μm to about 0.6 μm and the distance between a second one of the sidewalls of the second recess and the gate may be from about 0.3 μm to about 0.6 μm. The distance from a first gate in a transistor comprising a plurality of unit cells to a second gate may be from about 20 μm to about 50 μm.

While the present invention is described above primarily with reference to SiC MESFETs, methods of fabricating SiC MESFETs are also provided.

Brief Description of the Drawings

FIG. 1 is a cross-sectional view of a metal-semiconductor field effect transistor (MESFET) according to embodiments of the present invention; and

FIGs. 2A through **2H** illustrate processing steps in the fabrication of MESFETS according to embodiments of the present invention.

Detailed Description of the Invention

The present invention will now be described with reference to the **Figures 1** and **2A-2H** which illustrate various embodiments of the present invention. As illustrated in the Figures, the sizes of layers or regions are exaggerated for illustrative purposes and, thus, are provided to illustrate the general structures of the present invention. Furthermore, various aspects of the present invention are described with reference to a layer being formed on a substrate or other layer. As will be appreciated by those of skill in the art, references to a layer being formed on another layer or substrate contemplates that additional layers may intervene. References to a layer being formed on another layer or substrate without an intervening layer are described herein as being formed "directly" on the layer or substrate. Like numbers refer to like elements throughout.

Embodiments of the present invention will now be described in detail below with reference to **FIGs. 1** and **2A-2H** which illustrate various embodiments of the present invention and various processes of fabricating embodiments of the present invention. A metal-semiconductor field effect transistor (MESFET) is provided

having a delta doped layer, *i.e.* very thin, highly doped layer, offset from the gate by a doped channel layer that is lightly doped relative to the delta doped layer. As described in detail below, a double recessed gate structure is provided which may increase breakdown voltage and lower source and drain resistances relative to conventional MESFETs. MESFETs according to embodiments of the present invention may be fabricated using existing fabrication techniques as discussed below. MESFETs according to embodiments of the present invention may be useful in, for example, high efficiency linear power amplifiers, such as power amplifiers for base stations using complex modulation schemes such as code division multiple access (CDMA) and/or Wideband CDMA (WCDMA).

Referring to **FIG. 1**, metal-semiconductor field effect transistors (MESFETs) according to embodiments of the present invention will now be described in detail. As seen in **FIG. 1**, a single crystal bulk silicon carbide (SiC) substrate **10** of either p-type or n-type conductivity or semi-insulating is provided. The substrate may be formed of silicon carbide selected from the group of 6H, 4H, 15R or 3C silicon carbide.

An optional buffer layer **12** of p-type silicon carbide may be provided on the substrate **10**. The optional buffer layer **12** is preferably formed of p-type conductivity silicon carbide of 6H, 4H, 15R or 3C polytype. The buffer layer may have a carrier concentration of about 1.0×10^{16} cm^{-3} to about 6×10^{16} cm^{-3}, but typically about 1.5×10^{16} cm^{-3}. Suitable dopants include aluminum, boron and gallium. The buffer layer **12** may have a thickness of from about 0.2 μm to about 0.5 μm. Although the buffer layer **12** is described above as p-type silicon carbide, the invention should not be limited to this configuration. Alternatively, the buffer layer may be undoped silicon carbide or a very low doped n-type conductivity silicon carbide. If a low doped silicon carbide is utilized for the buffer layer **12**, it is preferred that the carrier concentration of the buffer layer **12** be less than about 5×10^{15} cm^{-3}. If an undoped or n-type buffer layer **12** is utilized, the substrate **10** is preferably a semi-insulating silicon carbide substrate.

The buffer layer **12** may be disposed between the substrate **10** and a delta doped layer **14** which may be either n-type or p-type silicon carbide. The delta doped layer **14** typically has doping impurities that are uniformly distributed within a very thin, two-dimensional layer and typically has a high carrier concentration. However,

the delta doped layer **14** may also have a doping profile, *i.e.* a representation of the carrier concentrations of different portions of the delta doped layer **14** typically having varying depths, with one or more spikes having a higher carrier concentration in the profile.

5 The delta doped layer **14**, a doped channel layer **16** and a cap layer **18**, all of n-type silicon carbide, may be provided on the substrate **10**, as shown in **FIG. 1.** Thus, the doped channel layer **16** is on the delta doped layer **14** and the cap layer **18** is on the doped channel layer **16**. If the optional buffer layer **12** is provided on the substrate **10**, the delta doped layer **14**, the doped channel layer **16** and the cap layer **18**
10 may be provided on the optional buffer layer **12.** Because the delta doped layer may contain a single spike or multiple spikes in its doping profile as discussed above, the doped channel layer **16** has a carrier concentration that is less than the carrier concentration of at least one of the spikes in the doping profile of the delta doped layer **14.** The carrier concentration of the doped channel layer **16** is also less than the
15 carrier concentration of the cap layer **18.** Thus, the doped channel layer **16** is lightly doped, *i.e.* has a smaller carrier concentration, relative to both the delta doped layer **14** and the cap layer **18.**

The delta doped layer **14** may be formed of n-type conductivity silicon carbide of 6H, 4H, 15R or 3C polytype. N-type carrier concentrations of the delta doped n-
20 type layer from about 2×10^{18} cm^{-3} to about 3×10^{18} cm^{-3} are suitable. Suitable dopants include nitrogen and phosphorous. The delta doped layer **14** may have a thickness from about 200 Å to about 300 Å. The doped channel layer **16** may have a carrier concentration of from about 1×10^{16} cm^{-3} to about 5×10^{16} cm^{-3} and may be formed of n-type conductivity silicon carbide of 6H, 4H, 15R or 3C polytype. The
25 doped channel layer **16** may further have a thickness of from about 1800 Å to about 3500 Å. Finally, the cap layer **18** may have a carrier concentration of from about 3×10^{17} cm^{-3} to about 6×10^{17} cm^{-3} and a thickness of from about 500 Å to about 1000 Å.

Although the delta doped layer **14**, the doped channel layer **16** and the cap layer **18** are described above as being of n-type conductivity silicon carbide, it will be
30 understood that the present invention is not limited to this configuration.. Alternatively, for example, in a complementary device, the delta doped layer **14**, the doped channel layer **16** and the cap layer **18** may be of p-type conductivity silicon carbide.

As further illustrated in **FIG. 1**, n^+ regions **13** and **17** are provided in the

source and drain regions of the device, respectively. As used herein, "n^+ " or "p^+ " refer to regions that are defined by higher carrier concentrations than are present in adjacent or other regions of the same or another layer or substrate. Regions **13** and **17** are typically of n-type conductivity silicon carbide and have carrier concentrations that are greater than the carrier concentration of the doped channel layer **16**. For the n^+ regions **13** and **17**, carrier concentrations of about 1 x 10^{19} cm^{-3} are suitable, but carrier concentrations as high as possible are preferred.

Ohmic contacts **26** and **22**, may be provided on the implanted regions **13** and **17**, and are spaced apart so as to provide a source contact **26** and a drain contact **22**. The ohmic contacts **26** and **22** are preferably formed of nickel or other suitable metals. An oxide layer **20** may be further provided on the exposed surface of the device.

MESFETs according to embodiments of the present invention include a first recessed section and a second recessed section. The first recessed section has a floor that extends through the cap layer **18** a distance of from about 500 Å to about 1000 Å to the doped channel layer **16**. The second recessed section is provided between the sidewalls **34, 36** of the first recessed section. A first sidewall **34** of the first recessed section is between the source **26** and the gate **24** and a second sidewall **36** of the first recessed section is between the drain **22** and the gate **24**. The floor of the second recessed section extends into the doped channel layer **16** a distance of from about 0.07 μm to about 0.25 μm. The floor of the first recessed section may also extend further into the doped channel layer **16**, for example, about 100 Å further, but does not extend as far into the doped channel layer **16** as the floor of the second recessed section. Furthermore, the distance between the source **26** and the first sidewall **34** of the first recessed structure may be from about 0.1 μm to about 0.4 μm. The distance between the drain **22** and the second sidewall **36** of the first recessed structure may be from about 0.9 μm to about 1.7 μm. The distance between the first sidewall **34** of the first recessed section and the gate **24** may be from about 0.3 μm to about 0.6 μm. The distance between the second sidewall **36** of the first recessed section and the gate **24** is from about 0.3 μm to about 0.6 μm.

It will be understood that although the recessed sections described above are termed first and second recessed sections, these recessed sections should not be limited by these terms. These terms are only used to distinguish one recessed section

from another recessed section. Thus, the first recessed section discussed above could be termed the second recessed section, and similarly, the second recessed section above could be termed the first recessed section.

A gate contact **24** is provided in the second recessed section between the
5 sidewalls **34, 36** of the first recessed section. The gate contact **24** may be formed of chromium, platinum, or platinum silicide, nickel, or TiWN, however, other metals such as gold, known to one skilled in the art to achieve the Schottky effect, may be used. However, the Schottky gate contact **24** typically has a three layer structure. Such a structure may have advantages because of the high adhesion of chromium
10 (Cr). For example, the gate contact **24** can optionally include a first gate layer of chromium (Cr) contacting the doped channel layer **16**. The gate contact **24** may further include an overlayer of platinum (Pt) and gold **46** or other highly conductive metal. Alternatively, the gate contact **24** may include a first layer of nickel on the floor of the second recessed section on the doped channel layer **16**. The gate contact
15 **24** may further include an overlayer on the first layer of nickel which includes a layer of gold. As illustrated, optional metal overlayers **28, 30** and **32** may be provided on the source and drain contacts **26** and **22** and the gate contact **24**. The overlayers **28, 30** and **32** may be gold, silver, aluminum, platinum and copper. Other suitable highly conductive metals may also be used for the overlayer.

20 The thickness of the n-type conductivity regions beneath the gate contact defines the cross-sectional height of the channel region of the device and is selected based on the desired pinch-off voltage of the device and the carrier concentration. Given the carrier concentrations of the doped channel layer and the delta doped layer, the depths of these layers for a given pinch-off voltage may be readily calculated
25 using methods known to one skilled in the art. Accordingly, it is desirable for the thickness and carrier concentrations of the doped channel layer to be selected to provide a pinch-off voltage of greater than -3 volts and preferably greater than -5 volts. The pinch off voltage may also be from between about -3 volts and -20 volts, but typically between about -5 volts and -15 volts.

30 In selecting the dimensions of the MESFET, the width of the gate is defined as the dimension of the gate perpendicular to the flow of current. As shown in the cross-section of **FIG. 1**, the gate width runs into and out of the page. The length of the gate is the dimension of the gate parallel to the flow of current. As seen in the cross-sectional views of **FIG. 1**, the gate length is the dimension of the gate **24** which is in

contact with the doped channel layer **16**. For example, the gate length of the MESFET according to embodiments of the present invention may be from about 0.4 μm to about 0.7 μm. Another important dimension is the source to gate distance which is shown in the cross-section of **FIG. 1**, as the distance from the source contact **26** or n^+ region **13**, to the gate contact **24**. The source to gate distance according to embodiments of the present invention may be from about 0.5 μm to about 0.7 μm. Furthermore, the distance from the drain **22** to the gate **24** may be from about 1.5 μm to about 2 μm. Embodiments of the present invention may further include a plurality of unit cells of MESFETS, and the distance from a first gate of the unit cells to a second gate may be from about 20 μm to about 50 μm.

FIGs. 2A through **2H** illustrate the fabrication of FETs according to embodiments of the present invention. As seen in **FIG. 2A**, an optional buffer layer **12** may be grown or deposited on a SiC substrate **10**. The substrate **10** may be a semi-insulating SiC substrate, a p-type substrate or an n-type substrate. The optional buffer layer **12** may be of p-type conductivity silicon carbide having carrier concentration of about 1.5×10^{16} cm^{-3} or less. Alternatively, the buffer layer may be n-type silicon carbide or undoped silicon carbide.

If the substrate **10** is semi-insulating it may be fabricated as described in commonly assigned and co-pending United States Patent Application Serial No. 09/313,802 entitled "Semi-insulating Silicon Carbide Without Vanadium Domination", the disclosure of which is hereby incorporated by reference herein as if set forth in its entirety. Such a semi-insulating substrate may be produced by providing silicon carbide substrates with sufficiently high levels of point defects and sufficiently matched levels of p-type and n-type dopants such that the resistivity of the silicon carbide substrate is dominated by the point defects. Such a domination may be accomplished by fabricating the silicon carbide substrate at elevated temperatures with source powders which have concentrations of heavy metals, transition elements or other deep level trapping elements of less than about 1×10^{16} cm^{-3} and preferably less than about 1×10^{14} cm^{-3}. For example, temperatures between about 2360 °C and 2380 °C with the seed being about 300 °C to about 500 °C lower may be utilized. Thus, it is preferred that the semi-insulating substrate be substantially free of heavy metal, transition element dopants or other deep level trapping elements, such as vanadium, such that the resistivity of the substrate is not dominated by such heavy metals or transition elements. While it is preferred that the semi-insulating substrate

be free of such heavy metal, transition element dopants or deep level trapping elements, such elements may be present in measurable amounts while still benefiting from the teachings of the present invention if the presence of such materials does not substantially affect the electrical properties of the MESFETs described herein.

5 As seen in **FIG. 2B**, a delta doped layer **14**, a doped channel layer **16** and a cap layer **18** are grown or deposited on the optional buffer layer **12**. It will be understood that if the buffer layer **12** is not included, the delta doped layer, doped channel layer **16** and cap layer **18** may be grown or deposited on the substrate **10**. The delta doped layer **14** is formed on the buffer layer **12**, the doped channel layer **16**

10 is formed on the delta doped layer **14** and the cap layer **18** is formed on the doped channel layer **16** as illustrated in **FIG. 2B**. It will be understood that the delta doped layer **14**, the doped channel layer **16** and the cap layer **18** may be grown in a single growth step by changing the source material concentration a first time to grow the doped channel layer **16** and a second time to grow the cap layer **18**. The delta doped

15 layer **14**, the doped channel layer **16** and the cap layer **18** may also be grown in multiple growth steps. Alternatively, the cap layer **18** may be formed by ion implantation.

As illustrated in **FIG. 2C**, a mask **45** may be formed for implanting n+ regions **13** and **17**. Regions **13** and **17** are typically formed by ion implantation of, for

20 example, nitrogen (N) or phosphorus (P), followed by a high temperature anneal. Suitable anneal temperatures may be from about 1100 to about 1600 ° C. The ion implantation may be performed on the regions which are not covered by the mask **45** to form n^+ regions **13** and **17** as illustrated in **FIG. 2D**. Thus, the ions are implanted in portions of the delta doped layer **14**, the doped channel layer **16** and the cap layer

25 **16** to provide highly doped regions of n-type conductivity silicon carbide having higher carrier concentrations than the doped channel layer **16**. Once implanted, the dopants are annealed to activate the implant.

As seen in **FIG. 2D**, the substrate **10**, buffer layer **12**, delta doped layer **14**, doped channel layer **16**, cap layer **18** and n+ regions **13** and **17** may be etched to form

30 an isolation mesa which defines the periphery of the device. The substrate **10**, the delta doped layer **14**, the doped channel layer **16**, the cap layer **18** and n^+ regions **13** and **17** form a mesa having sidewalls which define the periphery of the transistor. The sidewalls of the mesa extend downward past the delta doped layer **14** of the device. Typically, the mesa is formed to extend into the substrate **10** of the device as

shown in **FIG. 2C**. The mesa may extend past the depletion region of the device to confine current flow in the device to the mesa and reduce the capacitance of the device. If the depletion region of the device extends below the level of the mesa then it may spread to areas outside the mesa, resulting in larger capacitance. The mesa is preferably formed by reactive ion etching the above described device, however, other methods known to one skilled in the art may be used to form the mesa. Furthermore, if a mesa is not utilized the device may be isolated using other methods such as proton bombardment, counterdoping with compensating atoms or other methods known to those skilled in the art.

FIG. 2D further illustrates the formation of a first recess **43** of the MESFET. The first recess **43** may be formed by forming a mask **47** for the first recess **43** and then etching through the cap layer **18** a distance of from about 500 Å to about 1000 Å to form the recess according to the mask **47**. The cap layer **18** is etched through at least to the doped channel layer **16** to form the first recess **43**. The first recess **43** may be formed by an etching process, such as a dry or wet etch process. Alternatively, the etch may continue into the doped channel layer **16**, for example, about 100 Å further. Etching the first recess so that the recess extends into the doped channel layer **16** is preferred to not reaching the doped channel layer **16**.

FIG. 2E illustrates the formation of an oxide layer **20** after the first recess **43** has been formed as discussed above. The oxide layer may be grown or deposited over the exposed surface of the existing structure, *i.e.* on the isolation mesa, n^+ regions **13** and **17**, the cap layer **18** and the doped channel layer **16** in the first recess **43**. The oxidation process removes SiC that may have been damaged by the etch process and also smoothes out roughness that may have been created on the surface by the etch. This may enable the etch of the second recess discussed below, performed prior to formation of the gate metalization, to be much shallower, minimizing the sub-surface damage and surface roughness that, typically, cannot be removed.

Contact windows may be etched through the oxide layer **20** to the n+ regions **13** and **17**. Nickel may then be evaporated to deposit the source and drain contacts **26** and **22** and annealed to form the ohmic contacts as illustrated in **FIG. 2F**. Such a deposition and annealing process may be carried out utilizing conventional techniques known to those of skill in the art. For example, the ohmic contacts may be annealed at a temperature of about 1050 ° C for about 2 minutes. However, other times and

temperatures, such as temperatures of from about 800 to about 1150 ° C and times from about 30 seconds to about 10 minutes may also be utilized.

FIG. 2G illustrates the formation of a second recess for the gate structure of the MESFET. The second recess **40** may be formed by forming a mask **49** for the second recess and then etching the recess according to the mask **49**. The doped channel layer **16** may be etched into a distance of from about 0.07 μm to about 0.25 μm to form the recess **40**. It will be understood that these distances of the etch into the doped channel layer **16** do not include the etch through the oxide layer **20**.

The first and second recesses **43** and **40** discussed above may be formed by dry etching, for example, Electron Cyclotron Resonance (ECR) or Inductively Coupled Plasma (ICP) etching. Alternatively, the recesses discussed above may be formed in two steps with a double recess process. For example, the Schottky gate contact **24** may be formed in the second recessed section through an oxide layer **20** and into the doped channel layer **16**. The oxide layer **20** may be first etched through and then a second etch performed to etch into the doped channel layer **16**. The depth of the first etch can be all the way through the oxide layer **20**, or it may be only partially through the oxide layer **20**. The preferred depth into the doped channel layer **16** for the second etch is from about 0.07 μm to about 0.25 μm. Similarly, the first recessed section may be etched in a two step etch, first etching through the cap layer **18** extending to or into the doped channel layer **16** as discussed above.

The two etch approach may have a number of advantages over a single etch process. One advantage may be that the first etch can be performed prior to any metalization on the wafer, allowing a thermal oxide to be grown subsequent to etching with respect to the first recessed section. The thermal oxidation process removes SiC that may have been damaged by the etch process and also smoothes out roughness that may have been created on the surface by the etch. This may enable the second etch of the second recessed section, performed prior to formation of the gate metalization, to be much shallower, minimizing the sub-surface damage and surface roughness that, typically, cannot be removed. Another advantage of the two etch approach may be that the shallower second etch may reduce the amount of gate contact to the etched sidewall. This minimizes the contact area with potentially damaged material and the reduced contact area may also reduce the gate capacitance and, therefore, improve the frequency response of the transistor.

FIG. 2H illustrates the formation of the gate contact **24** and the optional overlayers **28, 30** and **32** as discussed above. For example, a layer of chromium may be deposited in the second recess **40**. Typically, the chromium layer is formed by evaporative deposition. The gate structure may then be completed by deposition of
5 platinum and gold. As will also be appreciated by those of skill in the art, the overlayers **28** and **30** may be formed either before or after formation of the gate structure. In fact, if the titanium/platinum/gold structure is utilized, the platinum and gold portions of the overlayer may be formed in the same processing steps as the platinum and gold portions **32** of the gate structure. Accordingly, the overlayers **28**
10 and **30** may be formed prior to the formation of a gate contact or after the formation of a gate contact.

As is briefly described above, MESFETs according to embodiments of the present invention provide a double recessed gate structure which may simultaneously increase breakdown voltage and reduce source and drain resistances relative to
15 conventional MESFETs. This may provide an advantage over conventional field effect transistors utilizing delta doped layers that sacrifice source and drain resistance to obtain a high breakdown voltage.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are
20 used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

THAT WHICH IS CLAIMED IS:

1. A unit cell of a metal-semiconductor field-effect transistor (MESFET), comprising:

a delta doped silicon carbide MESFET having a source, a drain and a gate, the gate being between the source and the drain and extending into a doped
5 channel layer of a first conductivity type; and

regions of silicon carbide adjacent to the source and the drain and extending between respective ones of the source and the gate and the drain and the gate, having a carrier concentration that is greater than a carrier concentration of the doped channel layer and being spaced apart from the gate.

10

2. A MESFET according to Claim 1, wherein the delta doped silicon carbide MESFET and the regions of silicon carbide comprise:

a silicon carbide substrate;

a delta doped layer of a first conductivity type silicon carbide on the substrate;

15 the doped channel layer of the first conductivity type silicon carbide on the delta doped layer having a carrier concentration that is less than at least one carrier concentration of the delta doped layer;

ohmic contacts on the doped channel layer that respectively define the source and the drain;

20 a cap layer of the first conductivity type silicon carbide on the doped channel layer and having a carrier concentration that is greater than the carrier concentration of the doped channel layer;

a first recess between the source and the drain having a first floor that extends through the cap layer into the doped channel layer a first distance;

25 the gate in the first recess and extending into the doped channel layer; and

a second recess between the source and the drain having a second floor that extends a second distance, less than the first distance, through the cap layer to the doped channel layer and having respective sidewalls which are between respective ones of the source and the gate and the drain and the gate and spaced apart from the
30 gate, the source and the drain so as to define regions of the cap layer extending between respective ones of the source and the gate and the drain and the gate to provide the regions of silicon carbide.

3. A MESFET according to Claim 2, wherein the second floor of the second recess extends into the doped channel layer a third distance.

4. A MESFET according to Claim 2, wherein the silicon carbide substrate
5 comprises a semi-insulating silicon carbide substrate.

5. A MESFET according to Claim 1, wherein the first conductivity type silicon carbide comprises n-type conductivity silicon carbide.

10 6. A MESFET according to Claim 1, wherein the first conductivity type silicon carbide comprises p-type conductivity silicon carbide.

7. A MESFET according to Claim 1, wherein the regions of silicon carbide are implanted regions.

15

8. A MESFET according to Claim 1, wherein the regions of silicon carbide are grown in a single growth step with the delta doped layer and the doped channel layer.

20 9. A MESFET according to Claim 2, wherein the delta doped layer, the doped channel layer and the cap layer are deposited on the substrate.

10. A MESFET according to Claim 2, wherein the cap layer has a carrier concentration of from about 3×10^{17} cm^{-3} to about 6×10^{17} cm^{-3}.

25

11. A MESFET according to Claim 2, wherein the cap layer has a thickness of from about 500 Å to about 1000 Å.

12. A MESFET according to Claim 2, wherein the delta doped layer has a
30 carrier concentration from about 2×10^{18} cm^{-3} to about 3×10^{18} cm^{-3}.

13. A MESFET according to Claim 2, wherein the delta doped layer has a thickness from about 200 Å to about 300 Å.

14. A MESFET according to Claim 2, wherein the doped channel layer has a carrier concentration of from about 1×10^{16} cm^{-3} to about 5×10^{16} cm^{-3}.

15. A MESFET according to Claim 2, wherein the doped channel layer has
5 a thickness of from about 1800 Å to about 3500 Å.

16. A MESFET according to Claim 2 further comprising:

a buffer layer of a second conductivity type silicon carbide between the substrate and the delta doped layer.

10

17. A MESFET according to Claim 16, wherein the buffer layer has a carrier concentration of about 1.0×10^{16} cm^{-3} to about 6×10^{16} cm^{-3}.

18. A MESFET according to Claim 16, wherein the buffer layer has a
15 thickness of about 0.5 μm.

19. A MESFET according to Claim 16, wherein the second conductivity type silicon carbide is p-type conductivity silicon carbide.

20 20. A MESFET according to Claim 16, wherein the second conductivity type silicon carbide is n-type conductivity silicon carbide.

21. A MESFET according to Claim 16, wherein the second conductivity type silicon carbide is undoped silicon carbide.

25

22. A MESFET according to Claim 2, further comprising:

regions of first conductivity type silicon carbide under the source and the drain and having a carrier concentration that is greater than the carrier concentration of the doped channel layer.

30

23. A MESFET according to Claim 22, wherein the region of first conductivity type silicon carbide has a carrier concentration of at least about 1×10^{19} cm^{-3}.

24. A MESFET according to Claim 2, further comprising an oxide layer on the cap layer and the doped channel layer.

25. A MESFET according to Claim 2, wherein the ohmic contacts
5 comprise nickel contacts.

26. A MESFET according to Claim 2, further comprising an overlayer on the ohmic contacts.

10 27. A MESFET according to Claim 2, wherein the delta doped layer and the doped channel layer form a mesa having sidewalls which define the periphery of the transistor and which extend through the delta doped layer and the doped channel layer.

15 28. A MESFET according to Claim 27, wherein the sidewalls of the mesa extend into the substrate.

29. A MESFET according to Claim 2, wherein the first distance is from about 0.08 μm to about 0.25 μm.

20

30. A MESFET according to Claim 2, wherein the gate comprises a first gate layer of chromium on the doped channel layer.

31. A MESFET according to Claim 30, wherein the gate further comprises
25 an overlayer on the first gate layer, wherein the overlayer comprises platinum and gold.

32. A MESFET according to Claim 2, wherein the gate comprises a first gate layer of nickel on the doped channel layer.

30

33. A MESFET according to Claim 32, wherein the gate further comprises an overlayer on the first gate layer, wherein the overlayer comprises gold.

34. A MESFET according to Claim 1, wherein the gate has a length from about 0.4 μm to about 0.7 μm.

35. A MESFET according to Claim 1, wherein a distance from the source
5 to the gate is from about 0.5 μm to about 0.7 μm.

36. A MESFET according to Claim 1, wherein a distance from the drain to the gate is from about 1.5 μm to about 2 μm.

10 37. A MESFET according to Claim 2, wherein the second distance is from about 500 Å to about 1000 Å.

38. A MESFET according to Claim 2, wherein a distance between the source and a first one of the sidewalls of the second recess is from about 0.1 μm to
15 about 0.4 μm; and

wherein a distance between the drain and a second one of the sidewalls of the second recess is from about 0.9 μm to about 1.7 μm.

39. A MESFET according to Claim 2, wherein a distance between a
20 first one of the sidewalls of the second recess and the gate is from about 0.3 μm to about 0.6 μm; and

wherein a distance between a second one of the sidewalls of the second recess and the gate is from about 0.3 μm to about 0.6 μm.

25 40. A MESFET comprising a plurality of unit cells according to Claim 1, wherein a distance from a first gate to a second gate is from about 20 μm to about 50 μm.

41. A method of forming a metal-semiconductor field-effect transistor
30 (MESFET), comprising:

forming a delta doped silicon carbide MESFET having a source, a drain and a gate, the gate being between the source and the drain and extending into a doped channel layer of a first conductivity type; and

forming regions of silicon carbide adjacent to the source and the drain and extending between respective ones of the source and the gate and the drain and the gate, having a carrier concentration that is greater than a carrier concentration of the doped channel layer and being spaced apart from the gate.

5

42. A method according to Claim 41, wherein forming a delta doped silicon carbide MESFET and forming regions of silicon carbide comprise:

forming a delta doped layer of a first conductivity type silicon carbide on a silicon carbide substrate;

10 forming the doped channel layer of the first conductivity type silicon carbide on the delta doped layer having a carrier concentration that is less than at least one carrier concentration of the delta doped layer;

forming ohmic contacts on the doped channel layer that respectively define the source and the drain;

15 forming a cap layer of the first conductivity type silicon carbide on the doped channel layer and having a carrier concentration that is greater than the carrier concentration of the doped channel layer;

forming a first recess between the source and the drain having a first floor that extends through the cap layer into the doped channel layer a first distance;

20 forming the gate in the first recess and extending into the doped channel layer; and

forming a second recess between the source and the drain having a second floor that extends a second distance, less than the first distance, through the cap layer to the doped channel layer and having respective sidewalls which are between

25 respective ones of the source and the gate and the drain and the gate and spaced apart from the gate, the source and the drain so as to define regions of the cap layer extending between respective ones of the source and the gate and the drain and the gate to provide the regions of silicon carbide.

30 43. A method according to Claim 42, wherein the steps of forming a delta doped layer, a doped channel layer and a cap layer comprises the step of epitaxially growing the delta doped layer, the doped channel layer and the cap layer in a single growth step.

44. A method according to Claim 43, wherein a source material concentration in the single growth step is changed a first time to grow the doped channel layer and changed a second time to grow the cap layer.

5 45. A method according to Claim 43:

wherein the step of forming a cap layer comprises implanting dopants of the first conductivity type in the doped channel layer.

46. A method according to Claim 42, wherein the steps of forming a delta 10 doped layer, a doped channel layer and a cap layer comprise the steps of depositing the delta doped layer, depositing the doped channel layer and depositing the cap layer.

47. A method according to Claim 42, wherein the first conductivity type silicon carbide comprises n-type conductivity silicon carbide.

15

48. A method according to Claim 42, wherein the first conductivity type silicon carbide comprises p-type conductivity silicon carbide.

49. A method according to Claim 42, further comprising the step of 20 forming a buffer layer between the substrate and the delta doped layer.

50. A method according to Claim 49, wherein forming a buffer layer comprises the step of forming a p-type conductivity silicon carbide layer.

25 51. A method according to Claim 49, wherein forming a buffer layer comprises the step of forming an n-type conductivity silicon carbide layer.

52. A method according to Claim 49, wherein forming a buffer layer comprises the step of forming an undoped silicon carbide layer.

30

53. A method according to Claim 42, wherein the step of forming ohmic contacts comprises:

etching a contact window through the cap layer in a region adjacent a source region of the MESFET; and

forming the ohmic contact in the contact window.

54. A method according to Claim 42, further comprising:

implanting n-type dopants in regions under the source and drains so as to
5 provide a highly doped region of n-type conductivity silicon carbide having a higher carrier concentration than the doped channel layer;

wherein the step of forming ohmic contacts comprises forming ohmic contacts on the highly doped regions.

10 55. A method according to Claim 54, further comprising the step of etching the delta doped layer, the doped channel layer, the cap layer and the highly doped regions to form a mesa.

56. A method according to Claim 54, wherein the step of implanting n-
15 type dopants further comprises annealing the n-type dopants to activate the n-type dopants.

57. A method according to Claim 42, further comprising the step of growing an oxide layer on the MESFET.

20

58. A method according to Claim 42, further comprising the step of depositing an oxide layer on the MESFET.

59. A method according to Claim 42, wherein forming the second recess
25 comprises:

forming a mask on the cap layer for the second recess;

etching through the cap layer the second distance extending to the doped channel layer according to the mask.

30 60. A method according to Claim 42, wherein forming the second recess comprises:

forming a mask on the cap layer for the second recess;

etching through the cap layer extending into the doped channel layer the second distance according to the mask.

61. A method according to Claim 42, wherein forming the first recess comprises:

forming a mask for the first recess;

5 etching into the second floor the first distance according to the mask.

62. A method of forming a MESFET, comprising:

forming buffer layer of a second conductivity type on a silicon carbide substrate;

10 epitaxially growing a delta doped layer, a doped channel layer, and a cap layer all of a first conductivity type, in a single growth step changing a source material carrier concentration a first time to grow the doped channel layer and a second time to grow the cap layer;

forming a mask for a first conductivity type implant;

15 implanting first conductivity type implant and activating the first conductivity type implant with an anneal;

etching the delta doped layer, the doped channel layer, the cap layer and the first conductivity type implant to form a mesa;

forming a mask for a first recess and etching the first recess between a source

20 and a drain having a first floor that extends through the oxide layer and the cap layer and into the doped channel layer a first distance and having respective sidewalls which are between respective ones of the source and a gate and the drain and the gate;

growing an oxide layer on the cap layer and in the first recess;

opening windows for the source and the drain;

25 forming ohmic contacts on the windows;

forming a mask for a second recess;

etching a second recess that extends into the doped channel layer a second distance greater than the first distance; and

forming a gate in the second recess that extends into the doped channel layer.

30

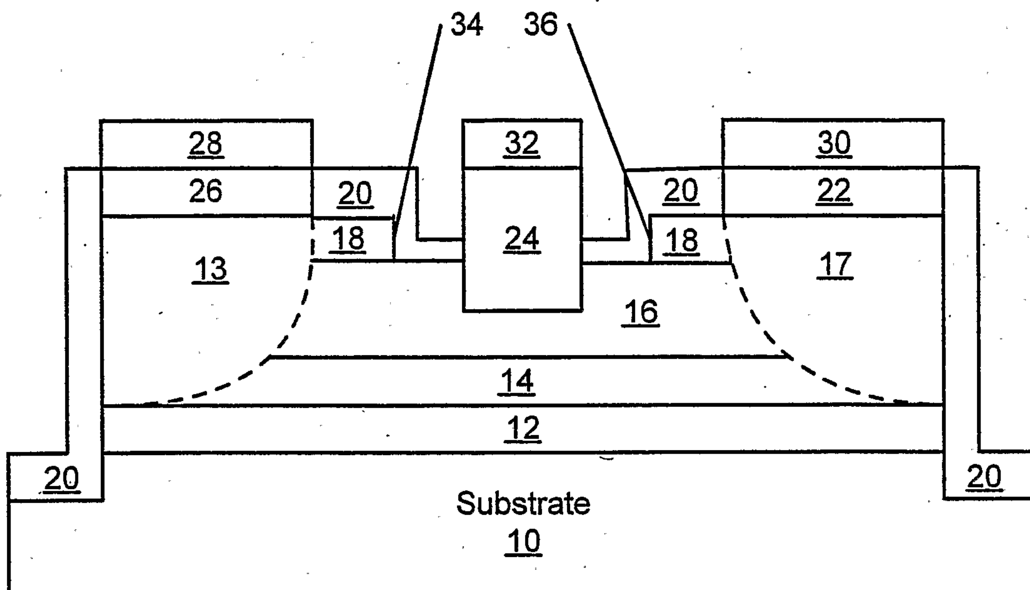

Fig. 1

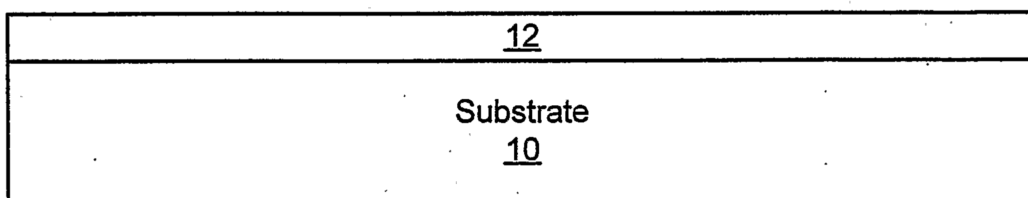

Fig. 2A

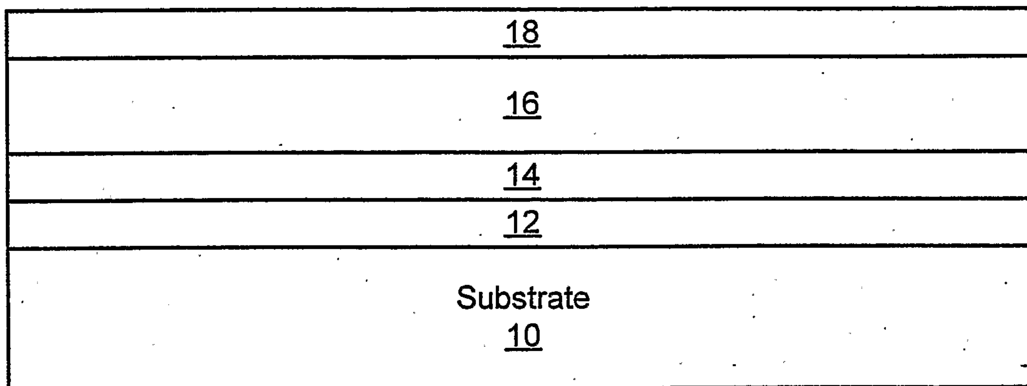

Fig. 2B

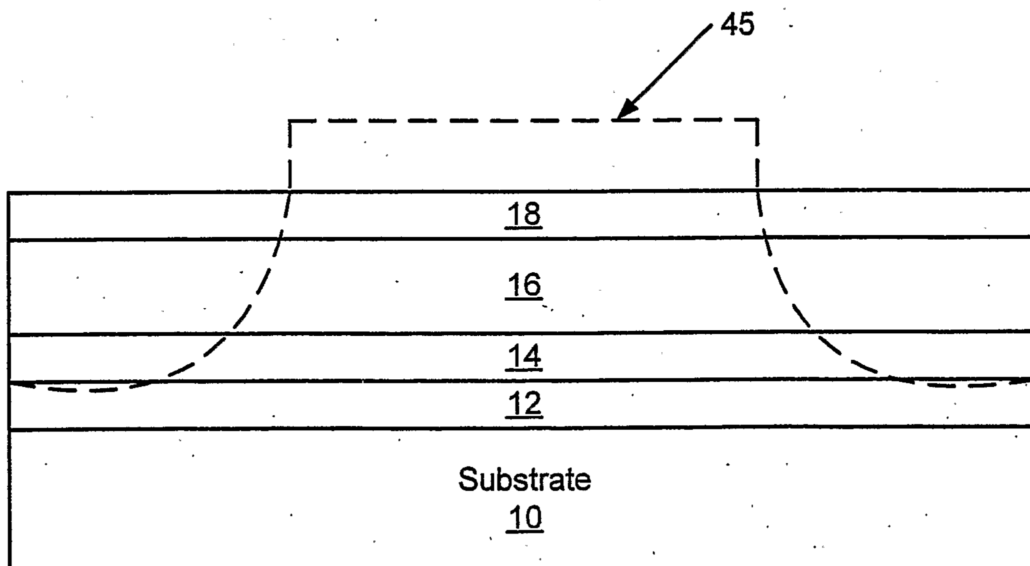

Fig. 2C

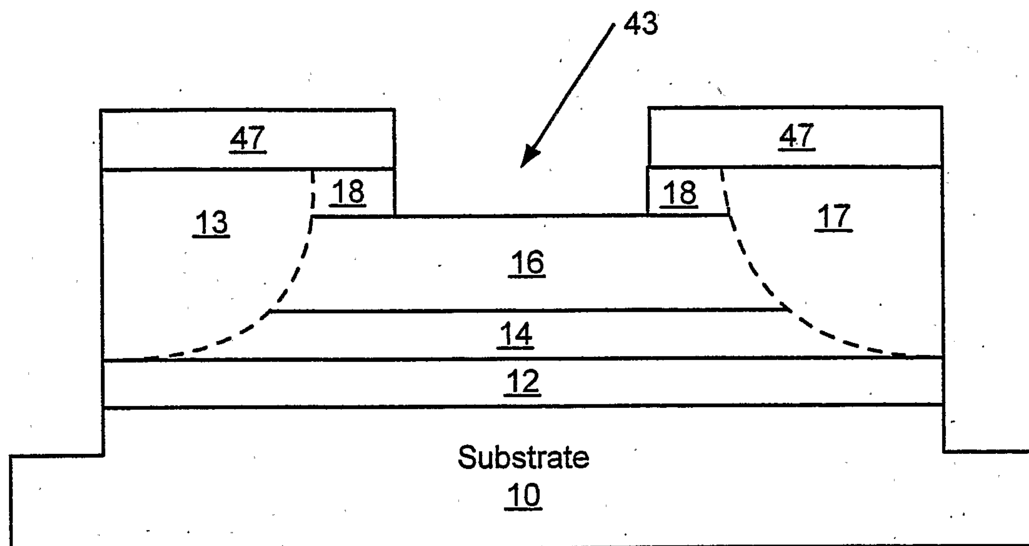

Fig. 2D

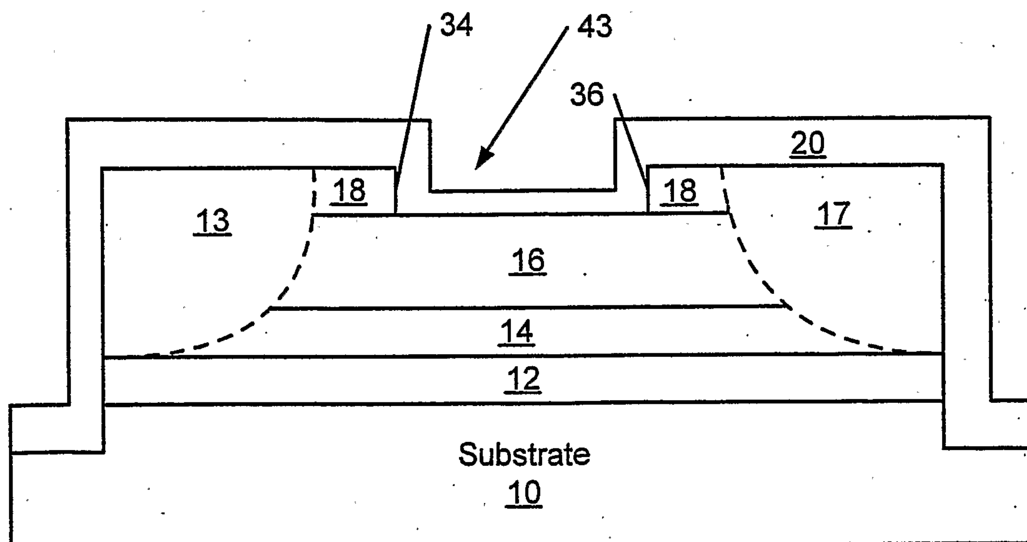

Fig. 2E

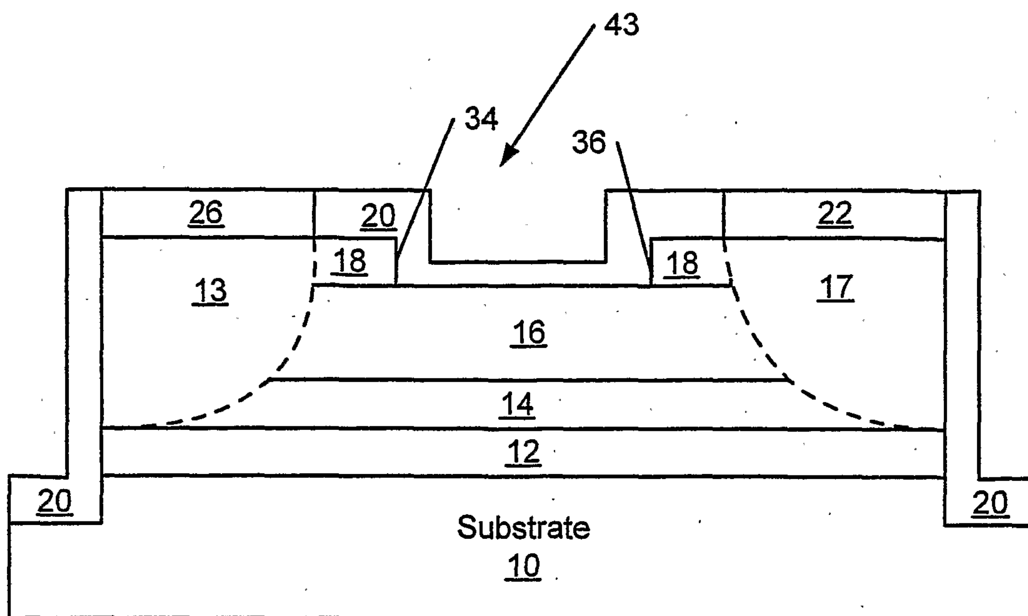

Fig. 2F

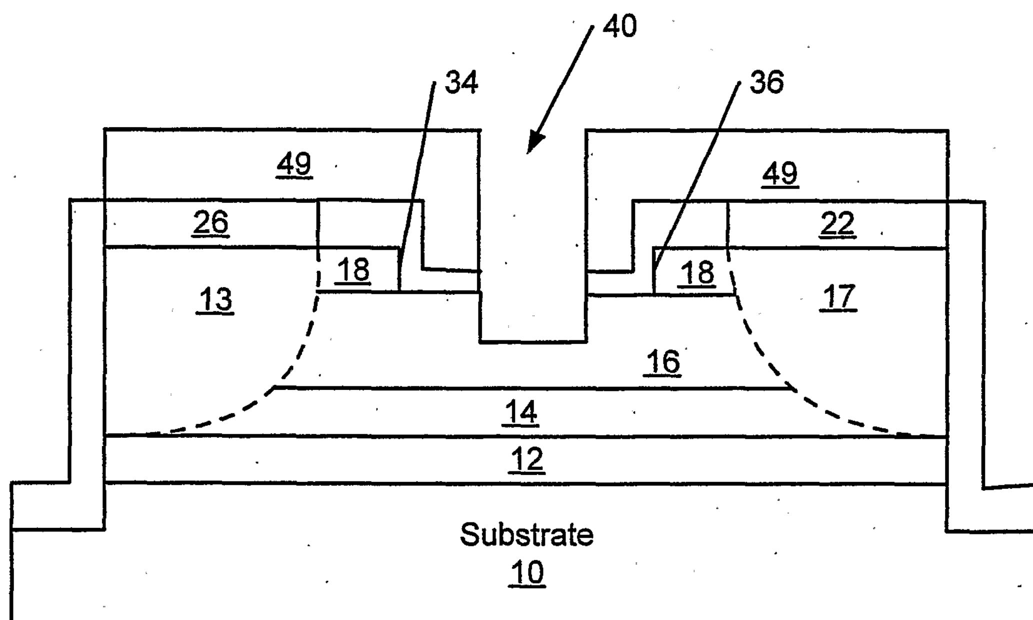

Fig. 2G

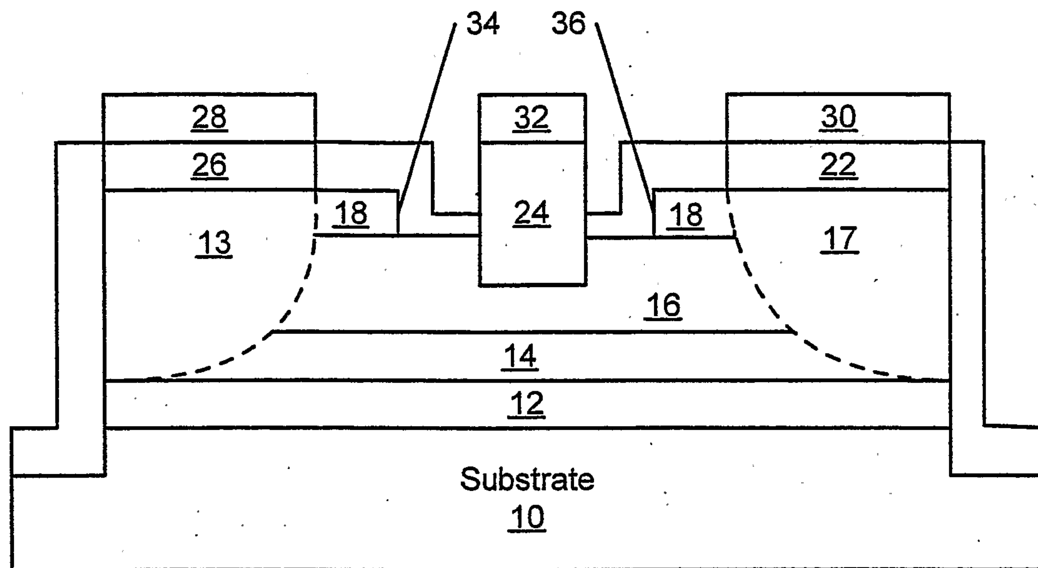

Fig. 2H

INTERNATIONAL SEARCH REPORT

Interna[illegible]l Application No
PCT/US 02/32204

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L29/812 H01L21/338 H01L29/36

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 270 554 A (PALMOUR) 14 December 1993 (1993-12-14) cited in the application	1,5-8, 34-36,41
A	the whole document	2-4, 9-33, 37-40, 42-62

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 February 2003	26/02/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Baillet, B

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 02/32204

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
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