

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
21 October 2010 (21.10.2010)

PCT

(10) International Publication Number
WO 2010/119456 A2

(51) International Patent Classification:
H03M 3/04 (2006.01)

(21) International Application Number:
PCT/IN2010/000257

(22) International Filing Date:
23 April 2010 (23.04.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
781/CHE/2009 3 April 2009 (03.04.2009) IN
995/CHE/2009 29 April 2009 (29.04.2009) IN

(71) Applicants (for all designated States except US): **SECRETARY, DEPARTMENT OF INFORMATION TECHNOLOGY (DIT)** [IN/IN]; Ministry of Communication and Information Technology, Government of India, Electronics Niketan, 6, CGO Complex, Lodhi Road, New Delhi 110 003 (IN). **INDIAN INSTITUTE OF TECHNOLOGY-MADRAS** [IN/IN]; I.I.T.Post office, Adyar, Chennai 600 036, Tamil Nadu (IN).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **YENDLURI SHANTHI PAVAN** [IN/IN]; Department of Electrical Engineering, Indian Institute of Technology-Madras, Chennai 600 036, Tamil Nadu (IN).

(74) Agent: **MOHAN DEWAN**; R. K. Dewan & Company, Trade Mark & Patent Attorneys, Podar Chambers, S.A.Brelvi Road, Fort, Mumbai 400 001, Maharashtra (IN).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- as to the identity of the inventor (Rule 4.17(i))
- of inventorship (Rule 4.17(iv))

Published:

- without international search report and to be republished upon receipt of that report (Rule 48.2(g))
- the filing date of the international application is within two months from the date of expiration of the priority period (Rule 26bis.3)

(54) Title: METHOD AND APPARATUS FOR LOW POWER CONTINUOUS TIME DELTA SIGMA MODULATION

(57) Abstract: A Continuous Time Delta Sigma Modulator (CTDSM) comprising a set of opamp integrators and at least one feedback DAC is provided with an assistant connected between the input and output of at least one of the opamp integrators of the set to moderate the linearity and bandwidth requirements of the opamp integrators of the set and result in low power dissipation. The assistant comprises a transconductor adapted to moderate the current demanded from the set of opamp integrators and a replica DAC adapted to steer the moderated current. This assisted opamp technique may be used with both single bit and multi bit CTDSMs.



WO 2010/119456 A2

METHOD AND APPARATUS FOR LOW POWER CONTINUOUS TIME DELTA SIGMA MODULATION

FIELD OF THE INVENTION

The present invention relates to the field of signal processing.

Particularly, the present invention relates to the field of analog to digital signal conversion.

DEFINITIONS OF TERMS USED IN THE SPECIFICATION

The terms used in this specification have definitions as provided herein below:

- **Integrators** are devices which perform the mathematical operation of integration. Electronic integrators are constructed to perform integration (usually with respect to time) of signals. This operation is a form of first-order low-pass filter, which can be performed in the continuous-time (analog) domain or approximated (simulated) in the discrete-time (digital) domain.
- The **Transconductance** is a property of certain electronic components. Conductance is the reciprocal of resistance and transconductance is the ratio of the current at the output port and the

voltage at the input port and is given by the formula, $g_m = \frac{\Delta I_{out}}{\Delta V_{in}}$

or $g_m = \frac{i_{out}}{v_{in}}$.

- An **Operational transconductance amplifier (OTA)** is an amplifier whose differential input voltage produces an output current. Thus, it is a voltage controlled current source (VCCS). There is usually an additional input for a current to control the amplifier's transconductance. The OTA is similar to a standard operational amplifier in that it has a high impedance differential input stage and it can be used with a negative feedback.
- A **digital-to-analog converter (DAC)** is a device for converting a digital (usually binary) signal to an analog signal (current, voltage or electric charge). An analog-to-digital converter (ADC) performs the reverse operation.
- **Feedforward** is a term describing an element or pathway within a system which passes a controlling signal from a source in the system's external environment, often a command signal from an external operator, to a load elsewhere in its external environment.
- **Feedback** is a term describing an element or pathway within a system which passes part or whole of the information from the load (output) of a system to the source (input) of the system. If the signal is inverted on its way round the control loop, the system is said to have negative feedback; otherwise, the feedback is said to be positive. Negative feedback is often deliberately introduced to increase the stability and accuracy of a system by correcting unwanted changes.
- **The Miller effect** is an increase in the equivalent input capacitance of an inverting voltage amplifier due to amplification of capacitance between the input and output terminals. Although Miller effect normally refers to capacitance, any impedance connected between the

input and another node exhibiting high gain can modify the amplifier input impedance because of the Miller effect. This increase in input capacitance is given by $C_M = C(1 - A_v)$, where A_v is the gain of the amplifier and C is the feedback capacitance.

- **Replica** is a copy that is relatively indistinguishable from the original.
- **Linearity** of an opamp implies that the output of opamp varies linearly with the input.
- **Bandwidth** of the opamp refers to the upper cutoff frequency measured in Hertz.
- **Single bit modulation** is a technique wherein a higher sampling rate is traded for a lower number of bits. Only a single bit is needed for each sample. A **Multibit modulator** requires multi bits for each sample.
- **NRZ DAC** refers to a DAC using Non Return to Zero type of encoding in which 1's are represented by one significant condition (usually a positive voltage) and 0's are represented by some other significant condition (usually a negative voltage), with no other neutral or rest condition.
- **SCR DAC** refers to a Switched-Capacitor-Resistor DAC which produces an exponentially decaying pulse.

These definitions are in addition to those expressed in the art.

BACKGROUND OF THE INVENTION AND PRIOR ART

Delta-Sigma ($\Delta\Sigma$) modulators belong to a class of noise-shaping linear encoders which transform an analog (continuous-time) signal to an

oversampled bit stream. Oversampling is the process of sampling a signal with a sampling frequency significantly higher than twice the bandwidth or the highest frequency of the signal being sampled. Oversampling of the continuous-time signal before quantization reduces the quantization noise density by a factor of the Over Sampling Ratio (OSR) which is defined as a ratio of the sampling rate to twice the signal bandwidth (Nyquist rate). Quantization is the process of approximating a continuous range of values (or a very large set of possible discrete values) by a relatively small set of discrete symbols or integer values. The quantization level is specified in bits. Delta- Sigma modulators are most commonly used in low-speed high-resolution applications.

Continuous-time delta-sigma modulators (CTDSM) have several attractive features like free anti-aliasing, relaxed speed requirements on the active elements and resistive input impedance. There are two types of CTDSMs based on the quantizer configuration. They are single bit CTDSM and multi bit CTDSM. A single bit CTDSM employs a single bit quantizer and a multi bit CTDSM employs a multi bit quantizer. Several modulators targeting the audio range have been proposed, where power reduction is the main motivation for choosing CTDSMs over their discrete-time counterparts.

When compared to single-bit CTDSMs, multibit designs are less sensitive to clock jitter and relax the linearity requirements of the loop filter. However, a single-bit design has several attractive features. The quantizer is simple, resulting in a reduced area/power for the loop ADC. Dynamic Element Matching (DEM) circuitry is not needed, further reducing area and complexity. A single bit quantizer also results in a smaller excess loop delay.

To leverage the implementation advantages of a single-bit design, one needs to address the issues of clock jitter sensitivity and loop filter linearity requirements. FIGURES 1 and 2 illustrate a Non Return to Zero (NRZ) DAC and a Switched Capacitor Resistor (SCR) DAC feedback waveforms respectively. Jitter effects the performance of CTDSMs by perturbing the width of the feedback DAC pulse, making an NRZ DAC preferable to an RZ DAC. If the modulator output sequence and the jitter in the n^{th} clock edge are denoted by $y[n]$ and $\Delta T[n]$ respectively, an NRZ DAC injects an error proportional to $\Delta T[n](y[n]-y[n-1])$, as shown in FIGURE 1. One way of reducing noise due to clock jitter is through appropriate Phase locked Loop (PLL) design. The full scale jumps in the feedback DAC signals also demand excellent linearity of a first integrator in the loop filter (thereby increasing power dissipation). Another way of addressing clock jitter is to inject a fixed charge into the loop filter using an impulsive DAC (implemented using a Switched Capacitor Resistor (SCR), FIGURE 2). It can be shown that noise due to clock jitter is first-order noise shaped, and is therefore negligible in the signal band. An SCR DAC is more problematic for the linearity of the first integrator than a NRZ DAC, since the first integrator has to now source/sink impulsive currents. A compromise is to use an exponentially decaying DAC pulse, generated as shown in FIGURE 3.

FIGURE 3 illustrates a schematic representation of an SCR DAC and the exponentially decaying pulse produced by the DAC. The integrator operation can be explained with respect to two phases given by ϕ_1 and ϕ_2 . Phase ϕ_1 is the phase when the integrating capacitors discharge and during phase ϕ_2 , the DAC capacitors are charged to V_{ref} and $-V_{\text{ref}}$, wherein V_{ref} is the

reference voltage given to the DAC. In ϕ_1 , the capacitor C_D (which has been previously charged to V_{ref} during ϕ_2) discharges into the virtual ground of the opamp through a resistor R_D with a time-constant $\tau = C_D R_D$. The initial (peak) current injected by the DAC is $I_0 = V_{ref} / R_D$, decaying to $I_1 = I_0 \exp(-T/2\tau)$. If $I_1 \ll I_0$, the average current is given by $C_D V_{ref} f_s$ (which is the height of the equivalent NRZ DAC pulse), and $I_1 < C_D V_{ref} f_s$. The noise introduced by this DAC due to clock jitter is proportional to I_1 , and is controlled by T/τ . Choosing a small τ (small R_D) reduces jitter sensitivity, but results in an increased peak current, which in turn increases the linearity requirements of the first integrator. The choice of R_D , therefore, involves a tradeoff between linearity and jitter noise.

FIGURE 4 illustrates a schematic representation of a conventional integrator along with its waveforms. A single-ended circuit, assuming an NRZ feedback DAC is shown for simplicity – the same arguments hold for an SCR DAC. The input given to the integrator is a sinusoid (V_{in}), with an amplitude V_{max} . The feedback DAC waveform (V_{dac}) takes on one of the two values $\pm V_{ref}$. If the opamp is ideal, the current i_1 flowing through the integrating capacitor is as shown in the figure. The peak-to-peak value of this current is almost $4 V_{ref} / R$, where R is the integrating resistor value. The current consists of a very high frequency content, due to the voltage steps introduced by the feedback DAC. If the opamp is ideal, the virtual ground voltage remains at zero, and the in-band component of V_{dac} equals $-V_{in}$.

A real opamp, however, cannot respond fast enough to the sharp steps of the DAC feedback voltage. This effect manifests as jumps in the virtual ground potential whenever the feedback DAC switches. If the opamp is linear, these

jumps do not result in distortion. With a practical opamp, the large jumps at the virtual ground node result in nonlinear behaviour and degrade the performance of the modulator. The conventional way of addressing this issue is to bias the opamps with large currents, so that the bandwidth and slew rate of the opamp are enhanced. It is thus seen that the inability of the opamp to source or sink large currents instantaneously is responsible for the nonlinearity in the modulator.

A single bit CTDSM has several drawbacks including higher in-band quantization noise, noise due to clock jitter and higher slew rate requirement of loop filter employed in the CTDSM. A multi bit CTDSM overcomes these disadvantages as explained below:

Lower In-band Quantization Noise: A multi bit quantizer has inherently low quantization noise for the same Noise Transfer Function (NTF). The in-band quantization noise decreases by 6 dB for every extra quantizer bit. Also, the multi bit quantizer allows the use of a more aggressive NTF, resulting in further reduction of in-band quantization noise.

Lower Noise due to Clock Jitter: Clock jitter results in increased in-band quantization noise due to the modulation of the width of a DAC feedback pulse (assuming a Non Return to Zero DAC). The effect of jitter can be modeled as an additive sequence at the input of a jitter-free modulator. Since the difference between successive outputs of the modulator is smaller with a multi bit quantizer, the sensitivity to clock jitter is greatly reduced when compared with a single-bit design.

Lower Slew Rate Requirements in the Loop Filter: The input to the loop filter employed in a CTDSM is a shaped quantization noise. The amplitude of this noise is much lower in a multi bit design when compared to a single bit modulator. Therefore, the loop filter operational amplifiers need to have lower slew rates, which translate into reduced power dissipation for the entire modulator.

A single-bit CTDSM has the below mentioned advantages over its multi bit counterpart.

- The hardware is far less complex, thereby simplifying the design, reducing the area and power dissipation of an Analog to Digital Converter (ADC) in the loop.
- If resistive Digital to Analog Converters (DACs) are used, the area occupied by the DACs will be smaller.
- Dynamic Element Matching (DEM) circuitry needed in a multi bit loop to achieve adequate DAC linearity is no longer necessary in a single bit design, further reducing area and complexity.
- The simplicity of a single bit quantizer also results in reduced excess loop delay. While this might not be a concern in an audio design, it is a definite advantage in a high speed CTDSM.
- Only less time is required to run full transistor level simulations of a single bit modulator due to the smaller transistor count.

Several attempts have been made to improve the efficiency of both single bit and multi bit modulator implemented ADCs.

For instance, United States Patent Application US20080309535 A1 discloses a delta sigma analog- to-digital converter apparatus, wherein an additional direct feedforward path is introduced to compensate for peaking of feedforward structures while preserving frequency selectivity of the feedforward topology. In particular, the direct feedforward path is provided with a scaling by a direct feedforward coefficient greater than zero and less than one. As a result, overshoot or peaking of classical feedforward topologies can be suppressed while providing interferer immunity, anti-aliasing effects and loop stability. However, the current demand on the integrator opamp employed in the ADC is large and hence the output linearity is affected.

Also, disclosures in PCT Application No. WO2005043331, PCT Application No. WO2004042932, United States Patent No. 6972705 and United States Patent No. 7176821 have attempted to reduce the power consumption of the delta sigma modulators. However, there were issues of large circuit area and component count apart from clock jitter noise and slew rate that still needed to be addressed.

Several methods have been proposed to address the problem of jitter in CTDSMs. The most popular among these approaches is to employ a Switched-Capacitor Digital to Analog Converter (SCDAC). Disclosures in patent documents like United States Patent No. 7102557 and United States Patent No. 7102558 have made attempts to use SCDACs with CTDSMs. However the use of switched capacitor DAC in a continuous time delta

sigma modulator results in stringent bandwidth and slew rate requirements for the first operational amplifier of the loop filter of the modulator.

None of the abovementioned prior art documents disclose methods to meet the large source and sink current requirements on the modulator opamp. Therefore there is felt a need for a CTDSM with:

- the advantages of both single bit and multi bit quantizers;
- adequate linearity and low power dissipation;
- a simplified design;
- reduced circuit area;
- reduced component count;
- reduced jitter sensitivity; and
- enhanced slew rate.

OBJECTS OF THE INVENTION

An object of the invention is to provide a continuous time delta sigma modulation system with a single bit modulator.

Another object of the invention is to provide a continuous time delta sigma modulation system that can also be applied to multi bit modulators.

Still another object of the invention is to provide a continuous time delta sigma modulation system with an adequately linear output.

Yet another object of the invention is to provide a continuous time delta sigma modulation system with low power dissipation.

One more object of the invention is to provide a continuous time delta sigma modulation system with a simplified design.

Another object of the invention is to provide a continuous time delta sigma modulation system with reduced circuit area and component count.

Still another object of the invention is to provide a continuous time delta sigma modulation system with enhanced slew rate.

Yet another object of the present invention is to provide a continuous time delta sigma modulation system with low jitter sensitivity.

SUMMARY OF THE INVENTION

In accordance with the present invention, there is provided a Continuous Time Delta Sigma Modulator (CTDSM) comprising a set of opamp integrators and at least one feedback digital to analog converter (DAC); characterized in that at least one assistant is connected between the input and output of at least one of the opamp integrators of the set, the assistant being adapted to moderate the linearity and bandwidth requirements of the opamp integrators of the set,

the assistant comprising:

- a transconductor adapted to moderate the current demanded from the set of opamp integrators; and
- a replica digital to analog converter (DAC) adapted to steer the moderated current.

Typically, in accordance with this invention, the assistant is adapted to provide a good replica of the current injected by the feedback DAC into the connected opamp integrator of the set.

Typically, in accordance with this invention, the set of opamp integrators includes a single stage operational amplifier.

Typically, in accordance with this invention, the set of opamp integrators includes at least one Operational Transconductance Amplifier (OTA).

Typically, in accordance with this invention, the set of opamp integrators includes at least one Miller compensated two stage Operational Transconductance Amplifier (OTA).

Preferably, in accordance with this invention, the set of opamp integrators includes at least one two stage feed forward Operational Transconductance Amplifier (OTA).

Preferably, in accordance with this invention, the set of opamp integrators includes a Cascade of Integrators with Feed Forward (CIFF) structure.

Typically, in accordance with this invention, the set of opamp integrators includes a Cascade of Integrators with Feedback (CIFB) structure.

Typically, in accordance with this invention, the set of opamp integrators includes modulator structures other than Cascade of Integrators with Feed Forward (CIFF) and Cascade of Integrators with Feedback (CIFB).

Typically, in accordance with this invention, the set of opamp integrators is adapted to drive a capacitive load.

In accordance with the present invention, there is provided a method for providing a Continuous Time Delta Sigma Modulator (CTDSM) comprising a set of opamp integrators and at least one feedback digital to analog converter (DAC), the method comprising the following steps:

- connecting at least one assistant between the input and output of at least one of the opamp integrators of the set;
- moderating the current demanded from the set of opamp integrators;
- steering a good replica of the moderated current into the connected opamp integrator of the set; and
- moderating linearity and bandwidth requirements of the opamp integrators of the set.

Typically, in accordance with this invention, the feedback digital to analog converter (DAC) is adapted to generate arbitrary DAC pulse shapes.

Typically, in accordance with this invention, the feedback digital to analog converter (DAC) is adapted to generate Non Return to Zero (NRZ) DAC pulse shapes.

Typically, in accordance with this invention, the feedback digital to analog converter (DAC) is adapted to generate Switched Capacitor Resistor (SCR) DAC pulse shapes.

Typically, in accordance with this invention, the Continuous Time Delta Sigma Modulator (CTDSM) is a multibit modulator.

Typically, in accordance with this invention, the Continuous Time Delta Sigma Modulator (CTDSM) is a single bit modulator.

Typically, in accordance with this invention, the Continuous Time Delta Sigma Modulator (CTDSM) includes an exponentially decaying pulse generator.

Typically, in accordance with this invention, each of the opamp integrators in the set of opamp integrators can be arbitrarily selected from a group of opamp integrators having arbitrary topologies.

BRIEF DESCRIPTION OF ACCOMPANYING DRAWINGS

The invention will now be described in relation to the accompanying drawings, in which:

FIGURE 1 illustrates a Non Return to Zero (NRZ) DAC feedback waveform;

FIGURE 2 illustrates a Switched Capacitor Resistor (SCR) DAC feedback waveform;

FIGURE 3 illustrates a schematic representation of a Switched Capacitor Resistor (SCR) DAC and the exponentially decaying pulse produced by the DAC;

FIGURE 4 illustrates a schematic representation of a conventional integrator along with its waveforms;

FIGURE 5 illustrates a delta sigma modulator in accordance with an embodiment of the present invention;

FIGURE 6 illustrates a schematic representation of an assisted opamp integrator in accordance with the present invention;

FIGURE 7 illustrates an equivalent circuit of an assisted opamp integrator in accordance with the present invention;

FIGURE 8 illustrates an implementation of an assisted opamp integrator with a single stage Operational Transconductance Amplifier (OTA) in accordance with the present invention;

FIGURE 9 illustrates an implementation of an assisted opamp integrator with a feedforward compensated Operational Transconductance Amplifier (OTA) in accordance with a preferred embodiment of the present invention;

FIGURE 10 illustrates an implementation of an assisted opamp integrator with a Miller compensated Operational Transconductance Amplifier (OTA) in accordance with the present invention;

FIGURE 11 illustrates a schematic of a transconductor used in the assistant circuit in accordance with the present invention;

FIGURE 12 illustrates a schematic of a Switched Capacitor Resistor (SCR) assistant DAC in accordance with the present invention;

FIGURE 13 illustrates a simplified schematic of the bias current generator;

FIGURE 14 illustrates a graphical representation of a low frequency Power Spectral Density (PSD) of Non Return to Zero (NRZ) modulators designed using conventional integrators and assisted opamp integrators with the same power consumption;

FIGURE 15 illustrates a graphical representation of a low frequency Power Spectral Density (PSD) of Switched Capacitor Resistor (SCR) modulators designed using conventional integrators and assisted opamp integrators with the same power consumption;

FIGURE 16 illustrates a simulated performance of modulators employing assisted integrators with Non Return to Zero (NRZ) and Switched Capacitor Resistor (SCR) DACs with $\pm 5\%$ mismatch between the feedback and assistant DACs in accordance with the present invention;

FIGURE 17 illustrates a simulated performance of modulators employing assisted integrators with Non Return to Zero (NRZ) and Switched Capacitor Resistor (SCR) DACs with $\pm 1\text{ns}$ ($0.6\% T_s$) skew between the feedback and assistant DACs in accordance with the present invention;

FIGURE 18 illustrates a graphical representation of measured Signal to Noise Ratio (SNR) and Signal to Noise and Distortion Ratio (SNDR) for a modulator with a Non Return to Zero (NRZ) DAC;

FIGURE 19 illustrates a graphical representation of measured Signal to Noise Ratio (SNR) and Signal to Noise and Distortion Ratio (SNDR) for a modulator with a Switched Capacitor Resistor (SCR) DAC;

FIGURE 20 illustrates a modulator output spectrum for a 6kHz ton for a Non Return to Zero (NRZ) DAC based modulator with -2.2 dBFS input;

FIGURE 21 illustrates a modulator output spectrum for a 6kHz ton for a Switched Capacitor Resistor (SCR) DAC based modulator with -2.1 dBFS input; and

FIGURE 22 illustrates measured jitter performance of the Non Return to Zero (NRZ) and Switched Capacitor Resistor (SCR) DAC based modulators with an FM modulated sinewave clock source.

DETAILED DESCRIPTION OF THE ACCOMPANYING DRAWINGS

The invention will now be described with reference to the embodiment shown in the accompanying drawings. The embodiment does not limit the scope and ambit of the invention. The description relates purely to the exemplary preferred embodiment of the invention and its suggested application.

In accordance with the present invention, there is envisaged a means to provide a low power continuous time delta sigma modulator that also meets its high bandwidth and linearity requirements. The description provided herein is with reference to a Continuous Time Delta Sigma Modulator (CTDSM) comprising a set of opamp integrators, typically in a Cascade of

Integrators with Feed Forward (CIFF) structure or a Cascade of Integrators with Feedback (CIFB) structure and at least one feedback digital to analog converter (DAC), typically a Non Return to Zero (NRZ) DAC or a Switched Capacitor Resistor (SCR) DAC.

The system in accordance with the present invention however, can be also extended to any type of modulator (other than CIFF and CIFB structure) known in the art including an arbitrary digital to analog converter (DAC) waveform and / or an exponentially decaying pulse generator.

Each of the opamp integrators in the set of opamp integrators can be arbitrarily selected from the group of opamp integrators having arbitrary topologies i.e. other than those described in various embodiments herein below.

FIGURES 1-4 have been described in detail herein above wherein, FIGURES 1 and 2 illustrate a Non Return to Zero (NRZ) DAC and a Switched Capacitor Resistor (SCR) DAC feedback waveforms respectively. FIGURE 3 illustrates a schematic representation of a Switched Capacitor Resistor (SCR) DAC and the exponentially decaying pulse produced by the DAC. FIGURE 4 illustrates a schematic representation of a conventional integrator along with its waveforms. This system has an advantage of simplicity, however, the DC gain of the integrator is low due to resistive loading of the integrator by other parts of the loop filter. Such a design would therefore need large values of transconductor G_m , thereby degrading the power efficiency.

The system in accordance with the present invention envisages a solution to this problem. FIGURE 5 illustrates a delta sigma modulator in accordance with an embodiment of the present invention wherein the first integrator represented by its gain A_1 is implemented along with an assistant. The assistant comprises: a transconductor g_m to moderate the current and a replica digital to analog converter DAC_r to steer the moderated current. The assistant moderates the large amount of current demanded from the first integrator by sourcing or sinking the current.

A_1 , A_2 and A_3 represent the gains of the respective integrators in the loop. V_{in} is the input source voltage given to the modulator. R_1 , R_2 and R_3 are the integrating resistors and C_1 , C_2 and C_3 are the integrating capacitors used in the three stages of the loop filter with gains A_1 , A_2 and A_3 respectively. A direct path is added from the modulator input to the loop filter output through R_d . This reduces the values of the integrating capacitors C_1 , C_2 and C_3 . For low noise and high linearity, active RC techniques are used to implement the integrators. Weighted addition of the integrator outputs is performed using a separate summing amplifier with gain A_4 . The gain of the loop filter can be scaled without affecting the Noise Transfer Function (NTF). The complex zeroes of the NTF are realized using R_x , R_{x1} and R_{x2} . R_a , R_b and R_c are the voltage dividing resistors at the input of the summing amplifier. R_f is the feedback resistor of the summing amplifier. D represents the quantizer output. The current flowing through the assistant DAC will be $\pm V_{ref}/R$ and that through the transconductor will be V_{in}/R . DAC represents the feedback DAC of the modulator which is typically either a NRZ DAC or an SCR DAC.

The operation of the assistant is further explained in detail with reference to FIGURE 6 wherein a schematic representation of an assisted opamp integrator in accordance with the present invention is illustrated. The inability of the opamp to source or sink large currents instantaneously is responsible for the nonlinearity in the modulator. V_{in} and V_{dac} provide the exact current demanded from the opamp. A transconductor g_m with value equal to the reciprocal of the value of an input resistor R and a current steering DAC with outputs $\pm V_{ref}/R$ (referred to as the assistant) pull current out of the opamp. Hence, the opamp does not have to supply a large current. Since the demands made on the opamp are now greatly relaxed, the excursions of the virtual ground voltage are reduced, resulting in low distortion operation. The increased current demand is no longer a problem since it is supplied by the assistant. In practice, the opamp has to supply any incidental difference between the integrator input current and the assistant current, as well as the current needed to drive subsequent stages in the loop filter. Since the current demand is small, the slew rate requirement of the opamp is greatly reduced. i_1 is the current through the integrating capacitor, C and R is the value of the integrating resistor.

FIGURE 7 illustrates an equivalent circuit of an assisted opamp integrator in accordance with the present invention. i_{in} and G_1 denote the Norton equivalent of the input and DAC circuits. C_x is the capacitance at the virtual ground v_x . C is the integrating capacitor, while C_L and G_L are the total load capacitance and conductance that the opamp needs to drive. The opamp itself is modeled as a frequency dependent transconductor $G_m(s)$. This is an accurate representation of a single stage and two-stage feedforward

compensated opamps. i_a denotes the assistant current. The distortion introduced by the integrator is dependent on the swing at the virtual ground.

Opamp assistance results in a dramatic reduction in the swing at the virtual ground node of the opamp, thereby significantly improving the distortion performance of the integrator (and in consequence, the modulator). Since the opamps do not source / sink any current because of the assistants, they can be designed with lower quiescent currents, thereby saving power.

FIGURE 8 illustrates an implementation of an assisted opamp integrator with a single stage Operational Transconductance Amplifier (OTA) in accordance with the present invention. FIGURE 9 illustrates an implementation of an assisted opamp integrator with a feedforward compensated Operational Transconductance Amplifier (OTA) in accordance with a preferred embodiment of the present invention. The assistant current i_a is realized using a transconductor (that provides the input component of the integrator current) and a current steering DAC (which provides the DAC component of the integrator current).

FIGURE 10 illustrates an implementation of an assisted opamp integrator with a Miller compensated Operational Transconductance Amplifier (OTA) in accordance with the present invention. In a Miller OTA based integrator, the voltage across the integrating and compensating capacitors are nearly identical if g_{m2} is sufficiently large. In an ideal case, the current that the second stage needs to supply is approximately $i_1 (1 + C_c / C)$ which is equal to $V_{in} / R (1 + C_c / C)$. The assistant needs to supply this current. The current supplied by the first stage g_{m1} , which is also flowing through C_c is of the value of about $i_1 C_c / C$. The current through DAC is $\pm V_{Ref} / R (1 + C_c / C)$.

This indicates that, using a single assistant that only compensates for the current supplied by g_{m2} is not sufficient to prevent excursions of the virtual ground node. It is also necessary to assist the first stage. The assistant for the first stage needs to supply current $i_1 C_c / C$ only with the current through g_{mx} as $V_{in} / R (C_c / C)$ and through DAC_x as $\pm V_{Ref} / R (C_c / C)$.

Apart from supplying the desired signal current, the assistant circuits also inject thermal and $1/f$ noise. In the single stage OTA case with assistance as illustrated in FIGURE 8, this extra noise source appears in parallel with the noise of the OTA. In a well designed integrator, $G_m \gg 1/R$, therefore it is seen that noise injected by the assistant degrades the input referred opamp noise only slightly. In the two stage opamp using feedforward compensation as illustrated in FIGURE 9, the noise due to the assistant appears in parallel with that of the second stage of the opamp. Thus, the noise due to the assistant (and g_{m2}) becomes negligible when referred to the opamp input. For a Miller compensated two stage opamp as illustrated in FIGURE 10, the noise injected by the assistant circuitry appears in parallel with that injected by g_{m1} and g_{m2} . The source occurring at the output of g_{m1} could be of potential concern. However, in a well designed integrator, the gain-bandwidth product of the opamp is chosen to be much higher than the unity gain bandwidth of the integrator, thereby eliminating this concern. Hence it is concluded that the assisted opamp technique has negligible impact on the in-band noise of the modulator.

In practice, the assistant transconductor is weakly nonlinear. Since the distortion tone is injected at the integrator output, it is 'absorbed' by the opamp. Simulations show that transconductor distortion levels of 0.1% are

adequate to achieve distortion free modulator performance. This is exploited by using a class-AB design for the transconductor. The current steering DAC, whose distortion is also attenuated by $G_m R$, is easy to design for low distortion operation.

A deviation in the magnitude of the assistant current from the desired value of $i_{in}(1+C_L/C)$, and timing skew due to finite bandwidth effects results in imperfect cancellation, and the swing at v_x will not be zero. The mismatch / skew can be tolerated, as long as the swing at v_x does not become large enough to push the transconductors into their strongly nonlinear regions of operation. This is ensured by making $G_m(s)$ large.

In a Miller compensated Operational Transconductance Amplifier (OTA), power is wasted in charging and discharging the compensating capacitor. Since there is no compensating capacitor in a feedforward opamp, such an OTA is fundamentally more power efficient when compared to a Miller opamp. Further, assisting a Miller opamp is more complicated, as seen from FIGURE 10. A single stage opamp is not preferred since the G_m realizable for a given bias current is small. Due to the reduced complexity of implementation and power efficiency, the feedforward compensated assisted integrator is considered to be a preferred embodiment of the present invention.

Although the opamp assistant has been described and illustrated as being connected to the first integrator, the same can be applied to any integrator in the modulator.

FIGURE 11 illustrates a schematic of a transconductor used in the assistant circuit in accordance with the present invention. It is a class AB design, comprising of complementary common gate stages M_2 and M_6 . M_4 and M_8 are chosen to be twice as large as M_3 and M_7 respectively. The distortion components generated by this transconductor are attenuated by the first integrator, and are of little consequence. The schematic illustrated in FIGURE 11 only exemplifies one implementation of a transconductor. Other implementations may be used in accordance with the present invention.

FIGURE 12 illustrates a schematic of a Switched Capacitor Resistor (SCR) assistant DAC in accordance with the present invention. FIGURE 13 illustrates a simplified schematic of the bias current generator. The feedback DAC consists of a capacitor C_D that discharges into the opamp virtual ground through R_D and the on resistance of two switches, denoted by $2R_s$. Typically, the first integrator uses an operational amplifier (opamp) with a PMOS (P-channel metal oxide semiconductor) input stage for low $1/f$ noise. The other integrators and the summing amplifier use operational amplifiers with NMOS (N-channel metal oxide semiconductor) input pairs.

The assistant DAC works as follows, where operation of the NMOS portion is explained. The PMOS portion operates in a similar fashion. M_2 , M_6 are N times wider than M_1 , which is biased with $I_{ref} = V_{ref} / N(R_D + 2R_s)$. During phase ϕ_2 , the capacitors denoted by nC_D (where n is a natural number) are discharged whereas during phase ϕ_1 , the switches at the sources of either M_2 or M_6 are turned on, depending on the quantizer decision D . The drain current of M_2 or M_6 (which should not go into the triode region during modulator operation) starts out at $V_{ref}/(R_D + 2R_s)$, and decays exponentially

toward zero with a time constant $(R_D + 2R_s)C_D$ as the capacitor nC_D keeps charging. Replica switches are used in series with the sources of M_1 and M_3 to match the peak current/time constant of the assistant and feedback DACs. The differential component of the current pulses injected by the feedback and assistant DACs have a good match when the injected current is large. At the end of phase ϕ_2 , the assistant pulse deviates from the feedback pulse due to the decreasing g_m of M_2 / M_6 . This is not a problem as the difference is small, the current in the second stage of the opamp is deliberately increased to be able to handle this mismatch. Capacitors C_b are needed for high frequency bypass, and are realized using MOS gates. The average current drawn by the assistant DAC from the supply can be shown to be $C_D V_{ref} f_s$. The system in accordance with the present invention is less sensitive to charge injection and device / layout conditions when compared to prior art, where the gate of a grounded source device is excited with an exponentially decaying pulse.

Though the illustration and description of the present invention is made with reference to a single bit modulator, the implementation of the assisted opamp integrator is also applicable to multi bit modulators.

TEST RESULTS

Power Reduction using the Assisted Opamp Integrator:

Simulations were run to estimate the benefit (power reduction) of using opamp assistance in the NRZ and SCR-DAC modulators. To do this, the modulator was simulated by replacing the assisted opamp integrator with a conventional active RC integrator. The two-stage feedforward topology of

FIGURE 9 was used for the opamp, with the second stage scaled to accommodate the current that the opamp needs to source / sink. The input to the modulator was a -5dBFS 6 kHz sine wave. In the NRZ case, the total power consumed by the assisted opamp integrator (opamp, assistant transconductor and DAC) is 27 μ A, and the simulated in-band SNDR is 107 dB (this is almost the simulated SNDR of a modulator with a linear loop filter). When the assistant is removed, and the quiescent current in the second stage of the opamp increased to 10 μ A per leg (so that the current consumption is the same as the assisted integrator), the inband SNDR is 89 dB. FIGURE 14 illustrates a graphical representation of a low frequency Power Spectral Density (PSD) of Non Return to Zero (NRZ) modulators designed using conventional integrators and assisted opamp integrators with the same power consumption. The inset in the figure shows the virtual ground waveforms in both cases. It is seen that the voltage excursions are considerably smaller with assistance. The second stage current was further increased (in the conventional integrator) to determine the improvement possible with enhanced power dissipation. The results are given in Table 1 herein below.

Table 1 - Performance of a CTDSM using a conventional integrator (NRZ DAC) as a function of current consumption.

Total Current (μ A)	Second Stage Current (μ A)	In-band SNDR (dB)
27	20	89
39	32	102
47	40	103.5

It is seen that significantly more current is needed to achieve low distortion operation when compared to the assisted opamp design (which needs only 27 μA).

The same experiments were run with the SCR-DAC based modulator. FIGURE 15 illustrates a graphical representation of a low frequency Power Spectral Density (PSD) of Switched Capacitor Resistor (SCR) modulators designed using conventional integrators and assisted opamp integrators with the same power consumption (about 35 μA). It is seen that using assistance improves the SNDR by about 23.5 dB. Table 2 gives the simulated performance of the SCR-DAC based modulator (without assistance) as a function of the total bias current, from which one can conclude that using the assisted opamp technique results in significant power savings.

Table 2 - Performance of a CTDSM using a conventional integrator (SCR DAC) as a function of current consumption.

Total Current (μA)	Second Stage Current (μA)	In-band SNDR (dB)
35	28	78
67	60	98
113	106	102

Mismatch and Timing Errors:

Since the assisted opamp integrator is based on cancellation of the swing at the virtual ground of the opamp, a potential problem is the sensitivity to

mismatch and timing skew errors between the currents injected by the feedback and assistant DACs. Mismatch and skew errors in the assistant current can be modeled as the sum of the ideal current and an error current injected at the opamp output. As long as these errors are small, it is seen that they should not significantly increase the swing at the virtual ground node, and should therefore not adversely affect the modulator performance. Further, the error current is injected at the output of the opamp, so its in-band component should be suppressed by the in-band $G_m(s)$ of the opamp, in a manner similar to the suppression of noise and distortion from the assistant. Since quantitative estimation of modulator performance with errors seems difficult, simulations incorporating mismatch ($\pm 5\%$) and timing skew ($\pm 0.6\%T_s = 1\text{ ns}$) between the feedback and feedforward DACs were run.

FIGURE 16 illustrates a simulated performance of modulators employing assisted integrators with Non Return to Zero (NRZ) and Switched Capacitor Resistor (SCR) DACs with $\pm 5\%$ mismatch between the feedback and assistant DACs in accordance with the present invention and FIGURE 17 illustrates a simulated performance of modulators employing assisted integrators with Non Return to Zero (NRZ) and Switched Capacitor Resistor (SCR) DACs with $\pm 1\text{ ns}$ ($0.6\% T_s$) skew between the feedback and assistant DACs in accordance with the present invention. It is seen from FIGURES 17 and 18 that the assisted opamp technique is robust in the face of practical nonidealities.

Measurement Results:

FIGURE 18 illustrates a graphical representation of measured Signal to Noise Ratio (SNR) and Signal to Noise and Distortion Ratio (SNDR) for a

modulator with a Non Return to Zero (NRZ) DAC and FIGURE 19 illustrates a graphical representation of measured Signal to Noise Ratio (SNR) and Signal to Noise and Distortion Ratio (SNDR) for a modulator with a Switched Capacitor Resistor (SCR) DAC. The SNR is determined using a 15 kHz sinewave input, while a 6 kHz tone is used for SNDR measurement. The peak SNR/SNDR are 91 dB/88 dB and 90.3 dB/89.1 dB for the NRZ/SCR modulators. The measured dynamic ranges are 92.5 dB and 91.5 dB respectively. FIGURE 20 illustrates a modulator output spectrum for a 6kHz ton for a Non Return to Zero (NRZ) DAC based modulator with -2.2 dBFS 6 kHz sinewave input (this is the amplitude that results in the best SNDR). It is seen that the harmonics are about 95 dB below the fundamental and no non harmonic tones are observed above the noise floor. The origin of the second harmonic is not clear. FIGURE 21 illustrates a modulator output spectrum for a 6kHz ton for a Switched Capacitor Resistor (SCR) DAC based modulator with -2.1 dBFS 6 kHz input. The third harmonic is seen to be about 97 dB below the fundamental. The observed distortion levels may be due to the input resistors, since their voltage dependence was not modeled in simulations. Two observations lend credence to this conclusion. Firstly, measurements showed that the second and third harmonic distortion levels were somewhat insensitive to the quiescent current in the first opamp. Further, about the same levels of distortion were observed in the multibit design in accordance with the present invention.

Jitter Sensitivity Measurements:

Since a controlled jitter injection setup was not available, the modulators were tested using an FM modulated sinusoidal clock source, which can be expressed as:

$$V_{clk} = A_{clk} \sin(2\pi f_s t + \frac{\Delta f}{f_m} \sin(2\pi f_m t))$$

where f_s and f_m refer to the sampling and modulating frequencies, and Δf denotes the peak frequency deviation. f_m was chosen to be 2.5MHz.

FIGURE 22 illustrates measured jitter performance of the Non Return to Zero (NRZ) and Switched Capacitor Resistor (SCR) DAC based modulators with an FM modulated sinewave clock source.

With an SCR DAC, jitter effects the position of the DAC pulse, as well as its width. It is well known that pulse-position jitter is first order noise shaped out of the signal band, and that pulse-width jitter causes the inband jitter noise to be white. The measured in-band noise with jitter is shown (denoted by squares) in the figure and seen to be significantly smaller than that in the NRZ case, indicating the superior performance of the SCR-DAC, when there is clock jitter.

A summary of measured performance is given in Table 3 herein below.

Table 3 – Summary of Measured performance of the NRZ and SCR Modulators.

	NRZ Modulator	SCR Modulator
Signal Bandwidth / Clock Rate	24kHz/6.144MHz	24kHz/6.144MHz
Quantizer Range	3.6V _{pp,diff}	3.6V _{pp,diff}

Input Swing for peak SNR	-1.6dBFS	-2dBFS
Dynamic Range / SNR / SNDR	92.5dB/91dB/88dB	91.5dB/90.3dB/89.1dB
Active Area	0.24mm ²	0.26mm ²
Process/Supply Voltage	0.18μm MOS/1.8V	0.18μm CMOS/1.8V
Power Dissipation (Modulator + References)	110μW	122μW
Figure of Merit	66.5 fJ/level	82.7 fJ/level

The Figure of Merit (FOM) of the converter is determined as:

$$FOM = \frac{P}{2 \times f_B \times 2^{(DR-1.76)/6.02}}$$

where P, f_B and DR denote the power dissipation, signal bandwidth and dynamic range respectively. The FOMs are close to that achieved in the multibit design but with one-third the active area.

Comparison with other works:

Table 4 compares the performance of several $\Sigma - \Delta$ modulators known in the art with NRZ and SCR feedback DAC modulators in accordance with the present invention.

Reference	B/W (kHz)	OSR	Cont. Time or Disc. Time	Dynamic Range (dB)	Power (μW)	Tech. (μm)	Supply (V)	FOM (pJ/level)
discrete time -3 level design	24	64	DT	92	1500	0.13	0.9	0.96
discrete time single bit converter	20	100	DT	88	140	0.090	1.0	0.17

single-bit multiple NRZ feedback continuous- time design	25	48	CT	80	135	0.35	1.5	0.25
single-bit multiple SCR feedback continuous- time design	25	48	CT	81	250	0.35	1.5	0.45
four-bit quantizer, hybrid continuous- time,switched- capacitor loop filter	20	128	CT	106	18000	0.35	3.3	2.79
design in a 65 nm CMOS process	20	300	CT	95	2200	0.065	1.5	1.20
single-bit modulator intended for voice applications	3.4	64	CT	80	210	0.50	2.2	3.77
single-bit design in a 0.5V supply	25	64	CT	74	300	0.18	0.5	1.16
15-bit multibit continuous- time design	24	64	CT	93.5	121	0.18	1.8	0.065
Present invention(NRZ)	24	128	CT	92.5	110	0.18	1.8	0.066
Present invention(SCR)	24	128	CT	91.5	122	0.18	1.8	0.083

The power dissipation in the first opamp of a conventional single bit continuous-time oversampled converter is large due to high bandwidth and linearity requirements. This becomes an even bigger problem when a SCR feedback DAC is used. The assisted opamp integrator as described herein above enables low distortion operation without effecting noise performance, with a significant reduction in the opamp's bias current. This technique was applied to the design of audio frequency third order CTDSMs (with NRZ and SCR feedback DACs) implemented in a 0.18 μm CMOS technology. The NRZ/SCR ADCs have a dynamic range of 92.5 dB/91.5 dB while dissipating 110 μW /122 μW from a 1.8V supply, with a power efficiency comparable to the best multibit modulators reported with similar specifications.

TECHNICAL ADVANCEMENTS

The system in accordance with the present invention described herein above has several technical advantages including but not limited to the realization of:

- a continuous time delta sigma modulation system with a single bit modulator;
- a continuous time delta sigma modulation system that can also be applied to multi bit modulators;
- a continuous time delta sigma modulation system with an adequately linear output;
- a continuous time delta sigma modulation system with low power dissipation;

- a continuous time delta sigma modulation system with a simplified design;
- a continuous time delta sigma modulation system with reduced circuit area and component count;
- a continuous time delta sigma modulation system with enhanced slew rate; and
- a continuous time delta sigma modulation system with low jitter sensitivity.

While considerable emphasis has been placed herein on the particular features of this invention, it will be appreciated that various modifications can be made, and that many changes can be made in the preferred embodiments without departing from the principles of the invention. These and other modifications in the nature of the invention or the preferred embodiments will be apparent to those skilled in the art from the disclosure herein, whereby it is to be distinctly understood that the foregoing descriptive matter is to be interpreted merely as illustrative of the invention and not as a limitation.

Claims:

1. A Continuous Time Delta Sigma Modulator (CTDSM) comprising a set of opamp integrators and at least one feedback digital to analog converter (DAC); characterized in that at least one assistant is connected between the input and output of at least one of the opamp integrators of said set, said assistant being adapted to moderate the linearity and bandwidth requirements of the opamp integrators of said set, said assistant comprising:
 - a transconductor adapted to moderate the current demanded from said set of opamp integrators; and
 - a replica digital to analog converter (DAC) adapted to steer said moderated current.
2. The Continuous Time Delta Sigma Modulator (CTDSM) as claimed in claim 1, wherein said assistant is adapted to provide a good replica of the current injected by the feedback DAC into the connected opamp integrator of said set.
3. The Continuous Time Delta Sigma Modulator (CTDSM) as claimed in claim 1, wherein the set of opamp integrators includes a single stage operational amplifier.
4. The Continuous Time Delta Sigma Modulator (CTDSM) as claimed in claim 1, wherein the set of opamp integrators includes at least one Operational Transconductance Amplifier (OTA).

5. The Continuous Time Delta Sigma Modulator (CTDSM) as claimed in claim 1, wherein the set of opamp integrators includes at least one Miller compensated two stage Operational Transconductance Amplifier (OTA).
6. The Continuous Time Delta Sigma Modulator (CTDSM) as claimed in claim 1, wherein the set of opamp integrators includes at least one two stage feed forward Operational Transconductance Amplifier (OTA).
7. The Continuous Time Delta Sigma Modulator (CTDSM) as claimed in claim 1, wherein the set of opamp integrators includes a Cascade of Integrators with Feed Forward (CIFF) structure.
8. The Continuous Time Delta Sigma Modulator (CTDSM) as claimed in claim 1, wherein the set of opamp integrators includes a Cascade of Integrators with Feedback (CIFB) structure.
9. The Continuous Time Delta Sigma Modulator (CTDSM) as claimed in claim 1, wherein the set of opamp integrators is adapted to drive a capacitive load.
10. A method for providing a Continuous Time Delta Sigma Modulator (CTDSM) comprising a set of opamp integrators and at least one feedback digital to analog converter (DAC), said method comprising the following steps:
 - connecting at least one assistant between the input and output of at least one of the opamp integrators of the set;
 - moderating the current demanded from the set of opamp integrators;

- steering a good replica of said moderated current into the connected opamp integrator of the set; and
- moderating linearity and bandwidth requirements of the opamp integrators of the set.

11.The Continuous Time Delta Sigma Modulator (CTDSM) as claimed in claim 1, wherein the feedback digital to analog converter (DAC) is adapted to generate arbitrary DAC pulse shapes.

12.The Continuous Time Delta Sigma Modulator (CTDSM) as claimed in claim 1, wherein the feedback digital to analog converter (DAC) is adapted to generate Non Return to Zero (NRZ) DAC pulse shapes.

13.The Continuous Time Delta Sigma Modulator (CTDSM) as claimed in claim 1, wherein the feedback digital to analog converter (DAC) is adapted to generate Switched Capacitor Resistor (SCR) DAC pulse shapes.

14.The Continuous Time Delta Sigma Modulator (CTDSM) as claimed in claim 1, wherein, said Continuous Time Delta Sigma Modulator (CTDSM) is a single bit modulator.

15.The Continuous Time Delta Sigma Modulator (CTDSM) as claimed in claim 1, wherein, said Continuous Time Delta Sigma Modulator (CTDSM) is a multibit modulator.

16. The Continuous Time Delta Sigma Modulator (CTDSM) as claimed in claim 1, which includes an exponentially decaying pulse generator.
17. The Continuous Time Delta Sigma Modulator (CTDSM) as claimed in claim 1, wherein each of the opamp integrators in the set of opamp integrators can be arbitrarily selected from the group of opamp integrators having arbitrary topologies.

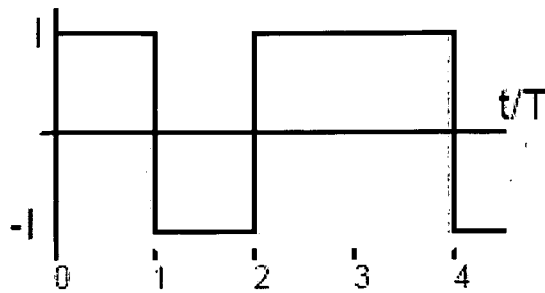


FIGURE 1

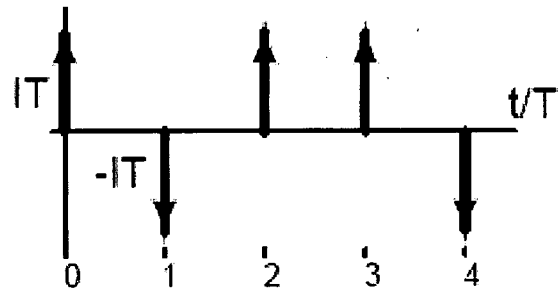


FIGURE 2

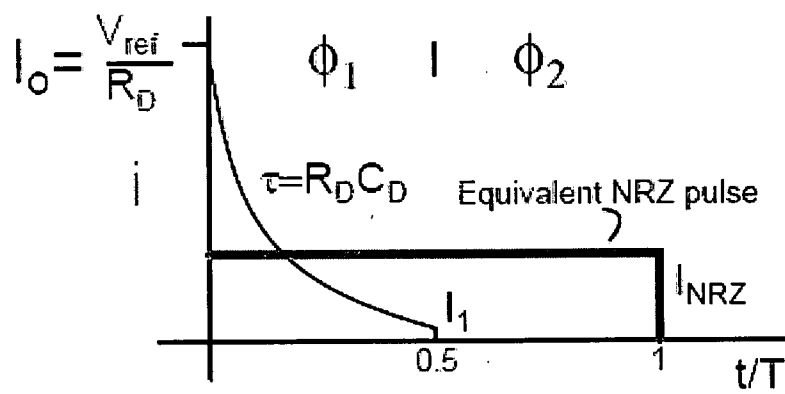
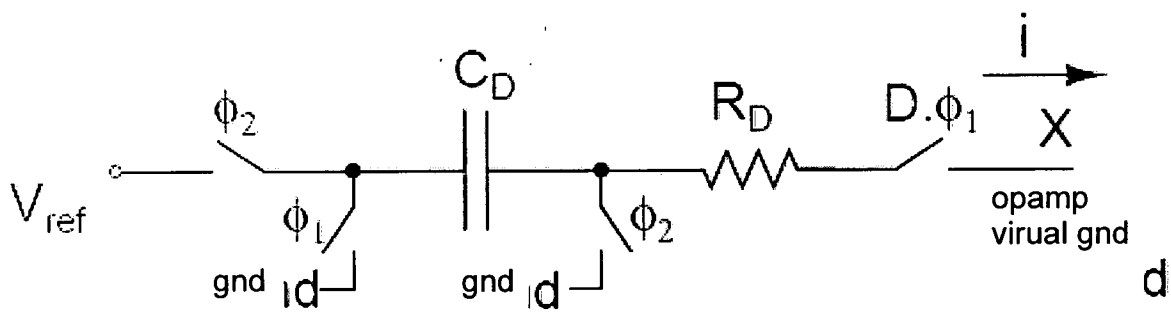


FIGURE 3

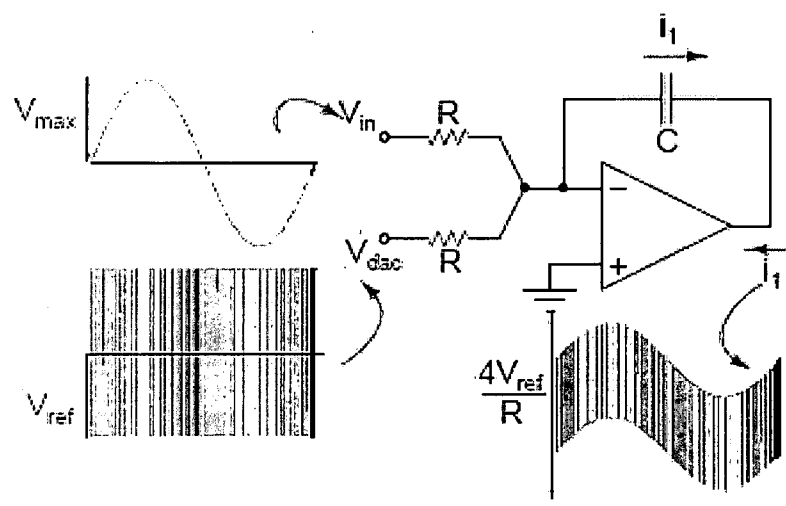


FIGURE 4

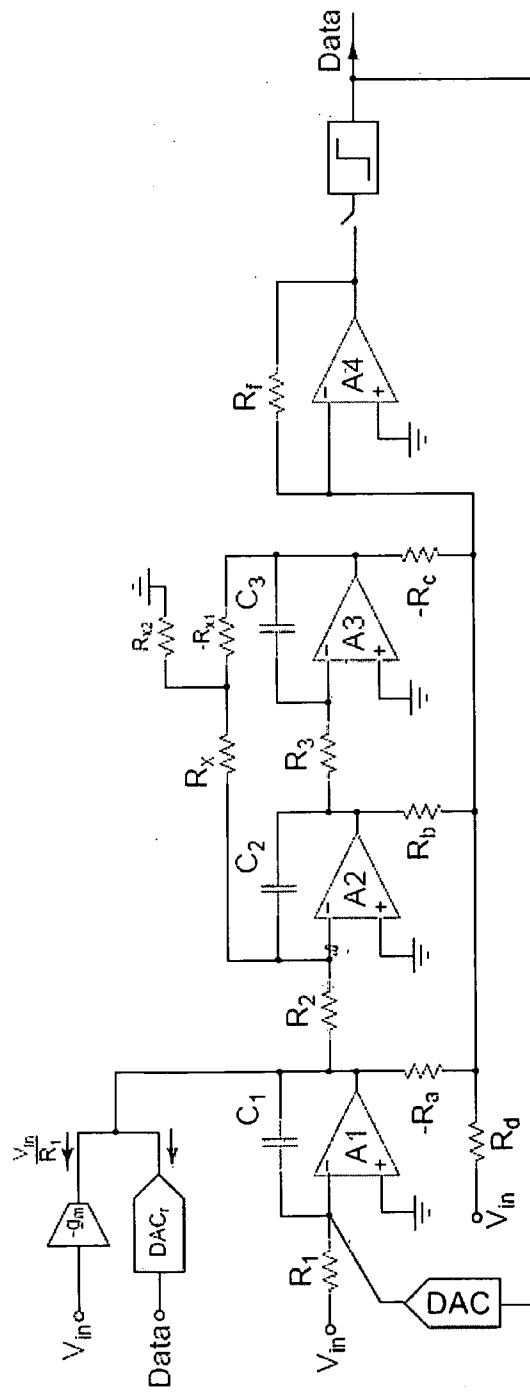


FIGURE 5

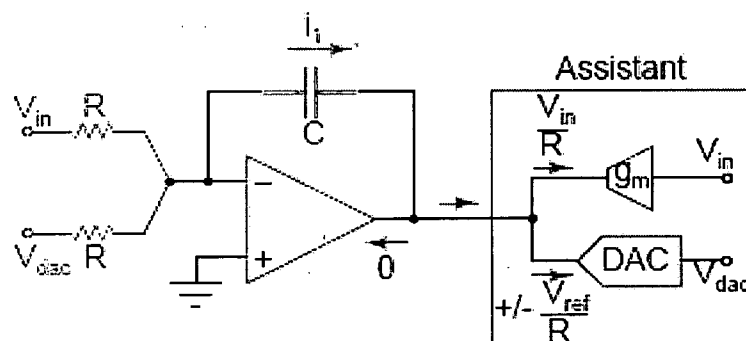


FIGURE 6

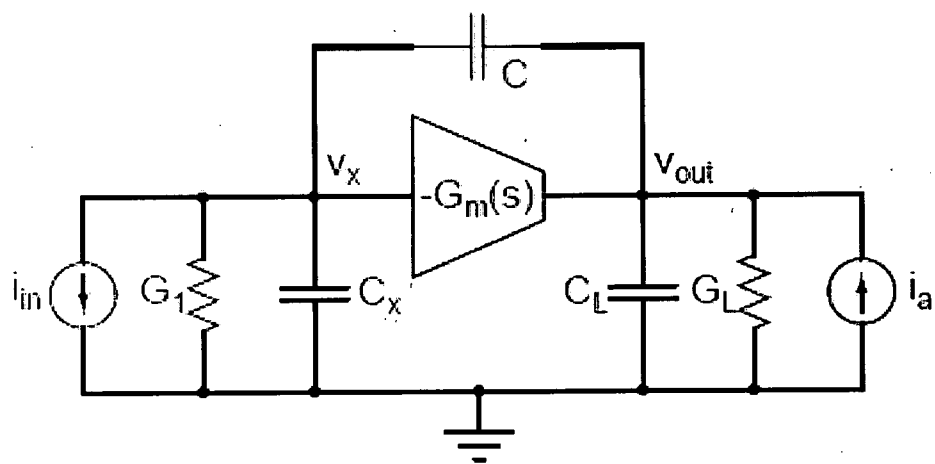


FIGURE 7

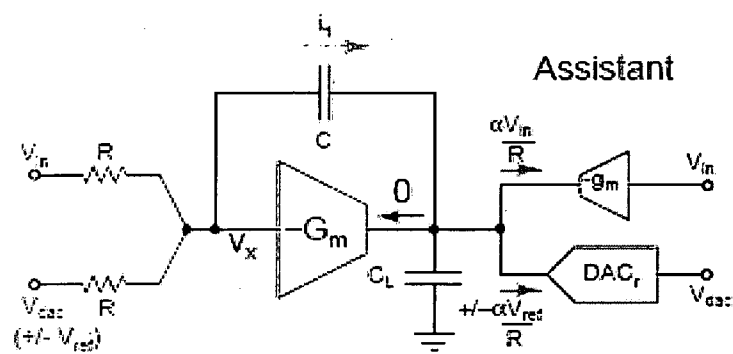


FIGURE 8

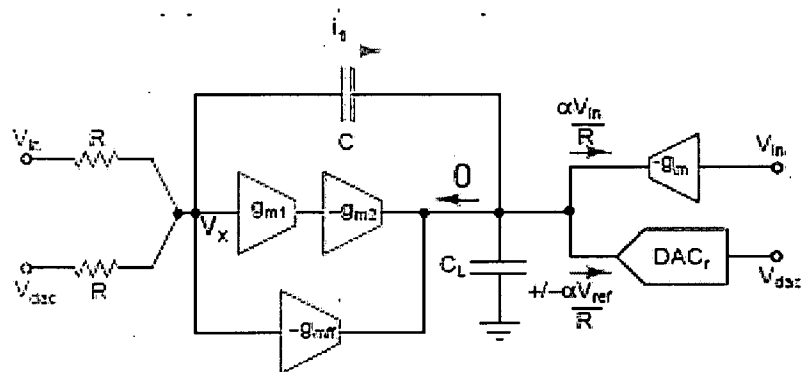


FIGURE 9

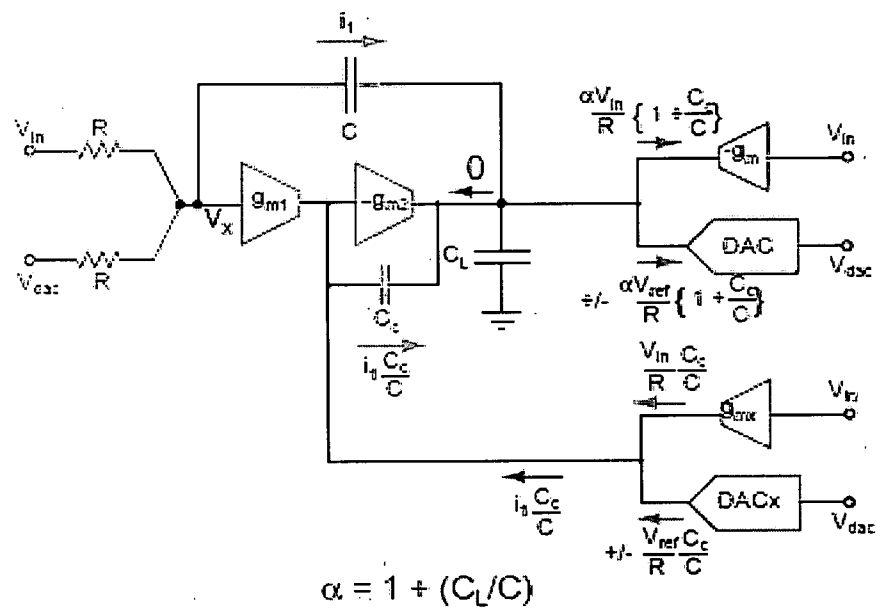


FIGURE 10

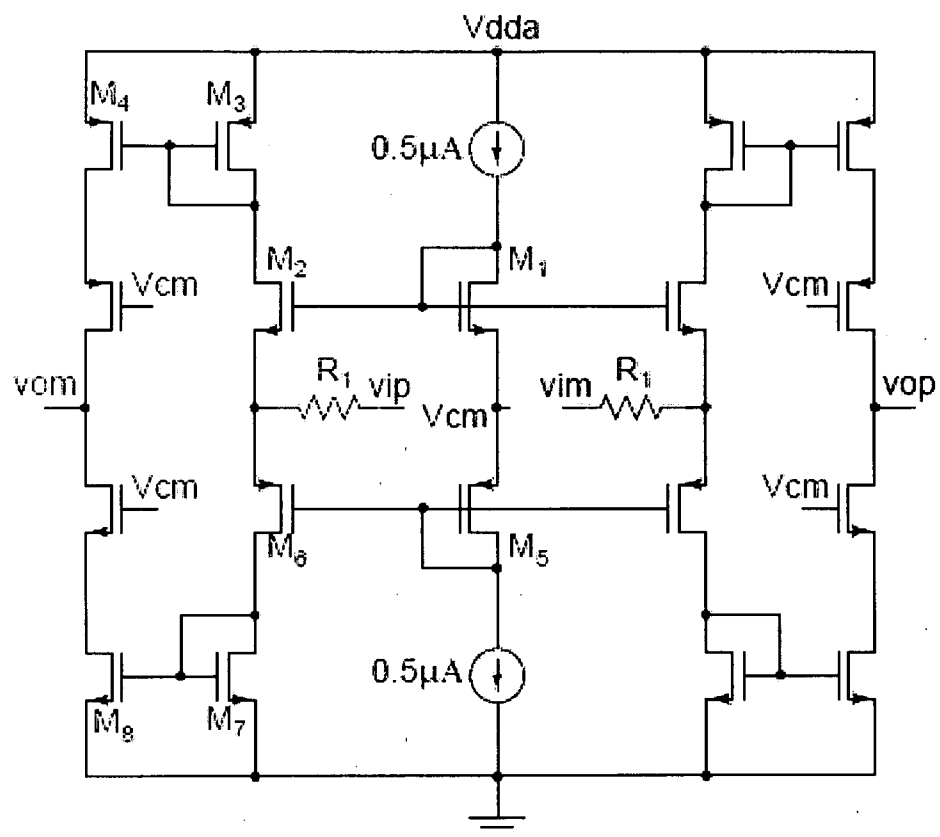


FIGURE 11

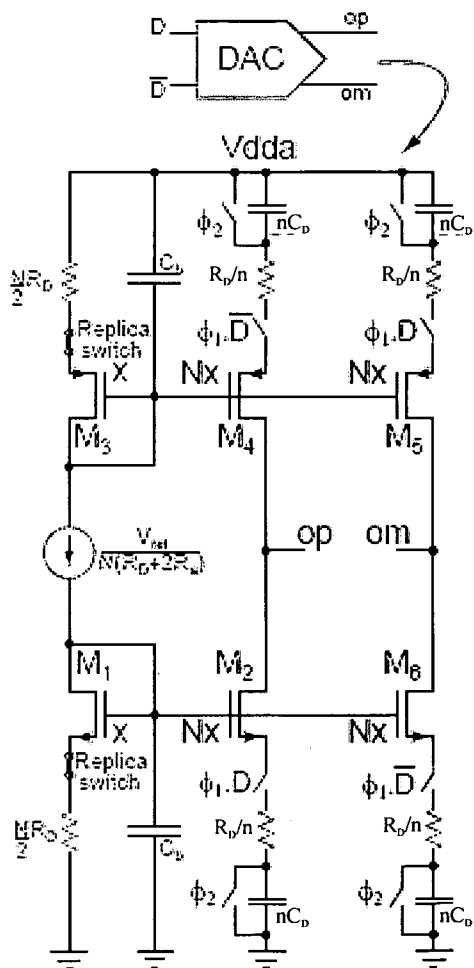


FIGURE 12

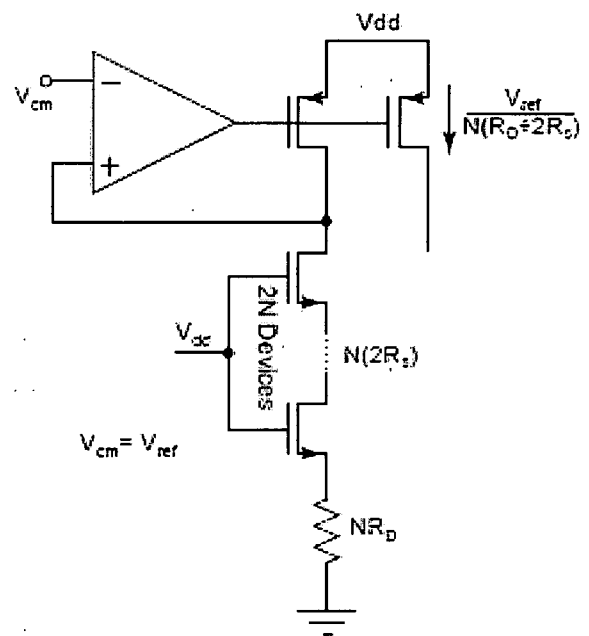


FIGURE 13

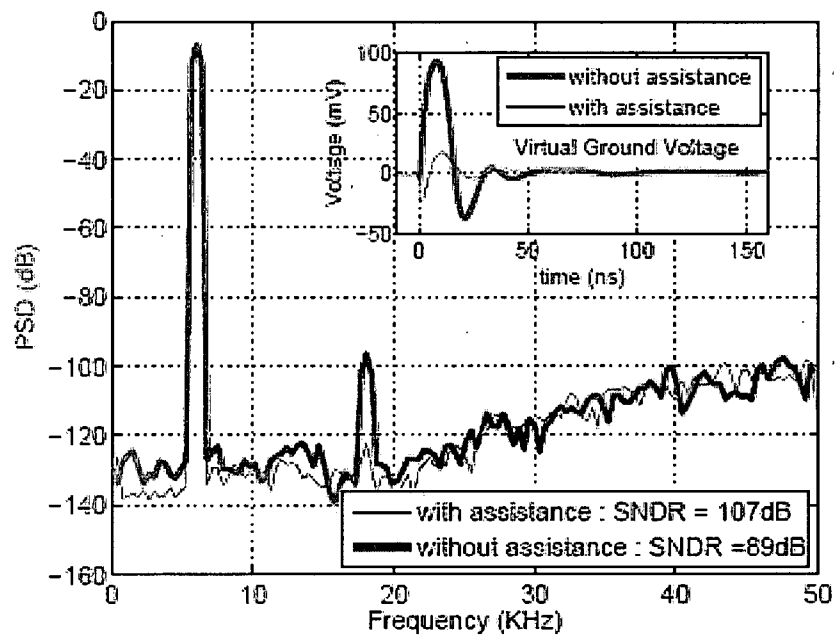


FIGURE 14

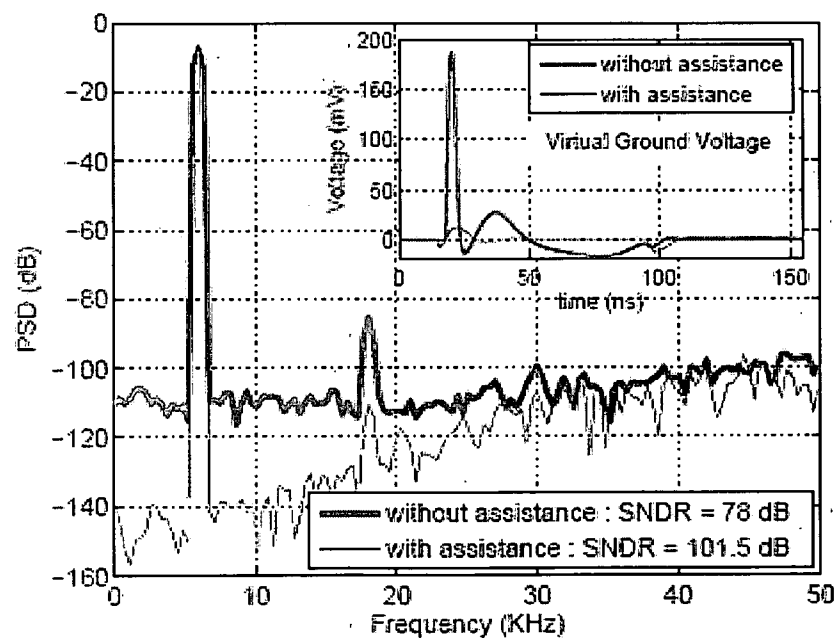


FIGURE 15

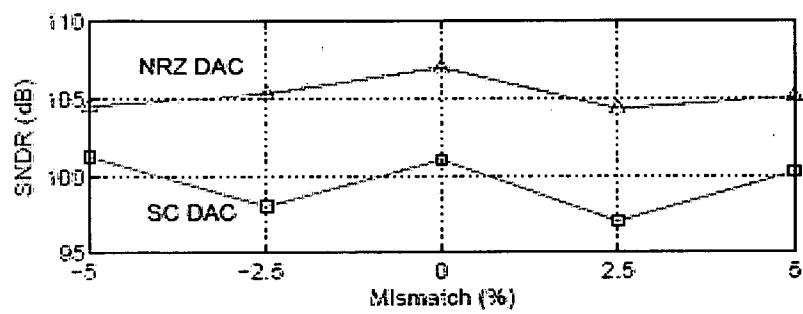


FIGURE 16

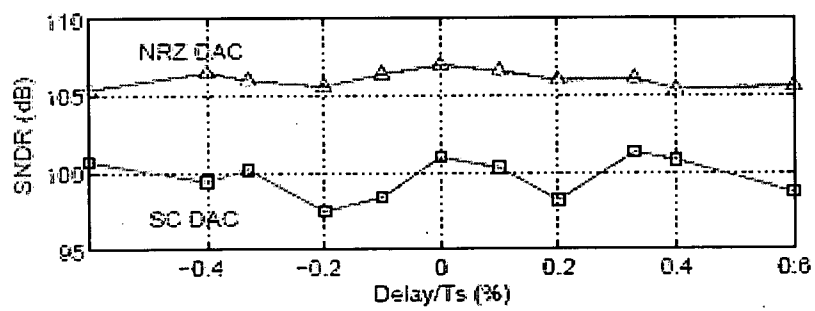


FIGURE 17

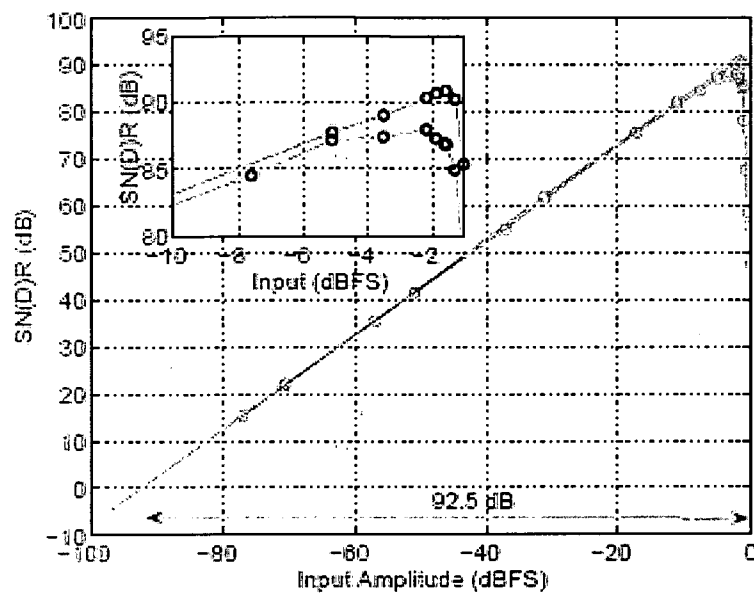


FIGURE 18

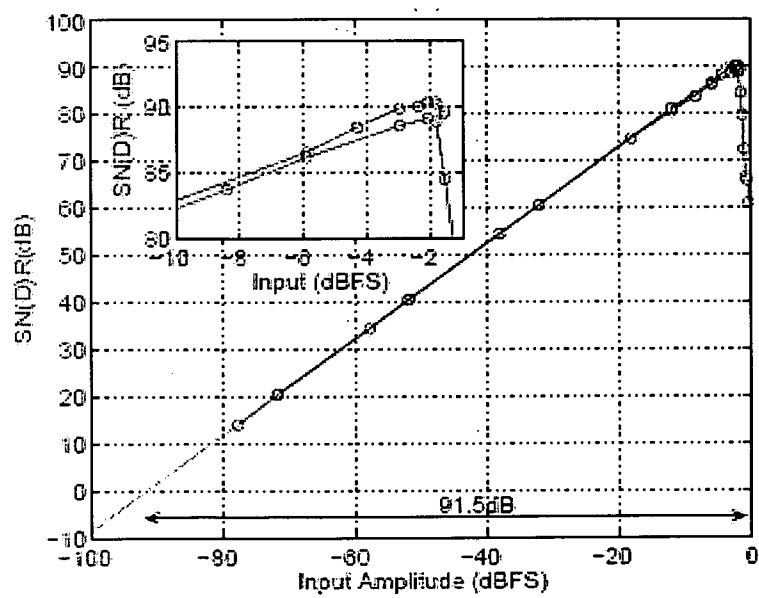


FIGURE 19

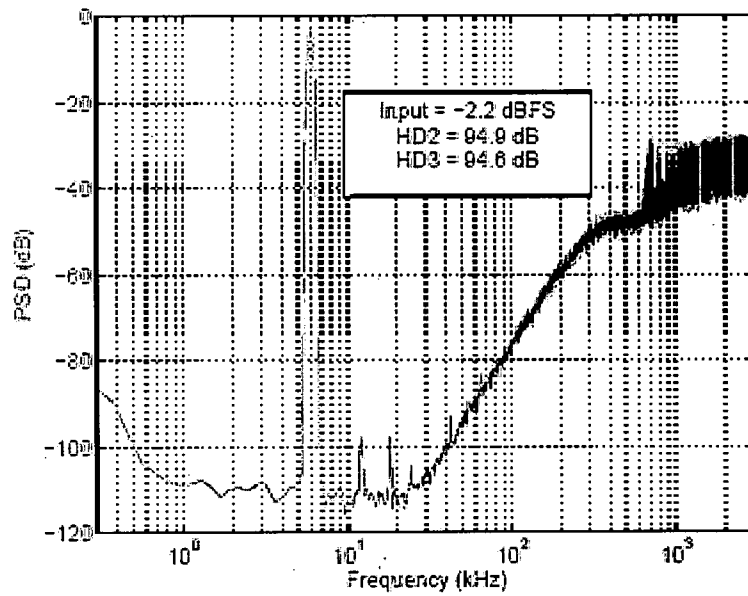


FIGURE 20

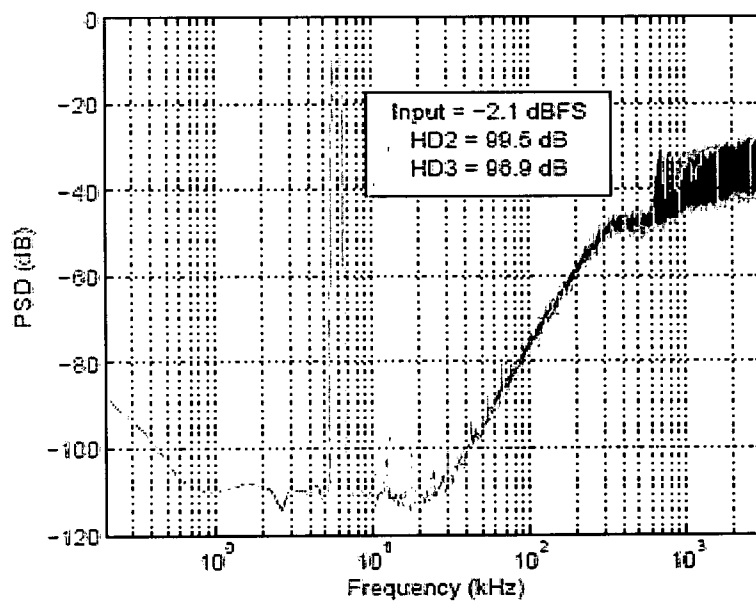


FIGURE 21

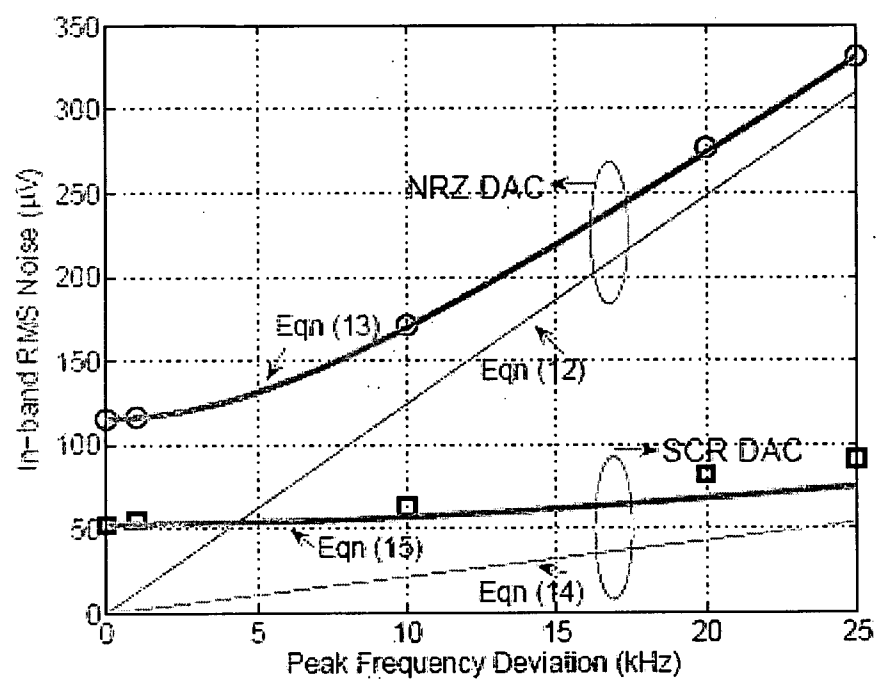


FIGURE 22