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[Continued on next page]

(54) Title: FAIL-SAFE FOR SHARED PIN

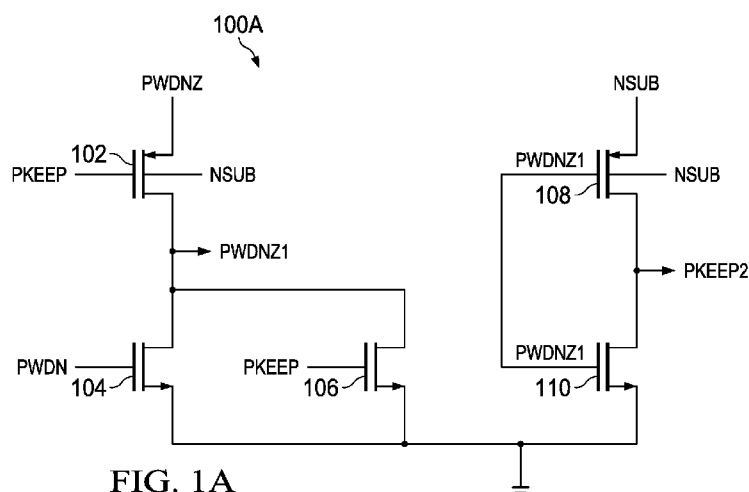


FIG. 1A

(57) Abstract: In described examples, an integrated circuit IC (100A) provides an improved fail-safe signal (PKEEP2) to a module sharing a fail-safe pin at which a voltage can be greater than a voltage of an upper rail. The IC (100 A) includes: a first circuit segment (102, 104, 106) that receives a first fail-safe signal (PKEEP) and a first power-down signal (PWDN) and provides an intermediate signal (PWDNZ1), wherein the first fail-safe signal (PKEEP) indicates when the voltage at the fail-safe pin is greater than the upper rail, and the first power-down signal (PWDN) indicates when the module is powered down; and a second circuit segment (108, 110) connected to receive the intermediate signal (PWDNZ1) and to provide the improved fail-safe signal (PKEEP2) to the module.



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## FAIL-SAFE FOR SHARED PIN

**[0001]** This relates generally to fail-safe circuits, and more particularly to a fail-safe circuit for use with a shared pin.

### BACKGROUND

**[0002]** A node or pin in a system is a fail-safe pin when it is possible for the voltage at the pin to be greater than  $V_{DD}$ , a condition that should be protected against. To manage this problem, a fail-safe circuit generates a fail-safe signal to prevent the flow of current towards  $V_{DD}$ . When a fail-safe pin is shared by multiple circuit blocks, undesired interactions can occur in certain situations. A circuit block that is in power-down mode can still affect settling time in other blocks sharing the same fail-safe pin.

### SUMMARY

**[0003]** In described examples, an integrated circuit includes: a first circuit segment that receives a first fail-safe signal and a first power-down signal and provides an intermediate signal, wherein the first fail-safe signal indicates when a voltage at a fail-safe pin is greater than an upper rail, and the first power-down signal indicates when a module is powered down; and a second circuit segment connected to receive the intermediate signal and to provide an improved fail-safe signal to the module.

**[0004]** In another example, an integrated circuit includes: a plurality of circuit blocks that share a common pin, wherein a voltage at the common pin can be greater than a voltage of an upper rail; a first circuit block of the plurality of circuit blocks, the first circuit block comprising a PMOS transistor coupled in series between the common pin and the upper rail; and a fail-safe circuit that receives the voltage at the common pin and a power-down signal for the first circuit block and provides a first fail-safe signal that turns off the PMOS transistor whenever the voltage at the common pin is greater than the upper rail and also when the first circuit block is in power-down mode.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. 1A depicts a circuit for modifying a fail-safe signal to provide an improved fail-safe signal according to an embodiment.

[0006] FIG. 1B depicts a circuit for providing a fail-safe signal when the voltage on a given pad is greater than the upper rail according an embodiment.

[0007] FIG. 2 depicts a system having multiple blocks that share a fail-safe pin.

[0008] FIG. 3A depicts a circuit section that uses a fail-safe signal.

[0009] FIG. 3B depicts a circuit section having an improvement to the use of a fail-safe signal.

## DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0010] In the drawings, like references indicate similar elements. Further, if a particular feature, structure, or characteristic is described in connection with an embodiment, then such feature, structure, or characteristic may also be effected in connection with other embodiments irrespective of whether explicitly described.

[0011] In this description, the term "couple" or "coupled" means either an indirect or direct electrical connection, unless qualified as in "communicably coupled" (which may include wireless connections). For example, if a first device couples to a second device, that connection may be through a direct electrical connection, or through an indirect electrical connection via other devices and connections.

[0012] Preferably, a block in power-down mode would have no effect on blocks that share a fail-safe pin. A module is described herein that modifies an existing fail-safe signal, so that the modified fail-safe signal is asserted when a voltage at the fail-safe pin is greater than  $V_{DD}$  and also when a circuit block that receives the modified fail-safe signal is in power-down mode. The modified fail-safe signal prevents switching of the fail-safe signal during power-down mode, eliminating interference with other circuit blocks.

[0013] The following circuits are described with reference to complementary metal oxide semiconductor (CMOS) transistors, which include n-type MOS (NMOS) and p-type MOS (PMOS). These names (CMOS, PMOS, NMOS) originated when those transistors were made using metal gates and oxide passivation layers, but other materials can be used instead of those specific materials. Also, other types of transistors can be used, such as junction gate field-effect transistor (JFET), and bipolar junction transistors.

**[0014]** Referring first to FIG. 2, the problem encountered in blocks sharing a fail-safe pin is described in greater detail. System 200, which may for example be a system on chip (SOC), discloses three IPs: IP-1 202, IP-2 204 and IP-3 206; the three IPs share a Fail-Safe Pin 208 that has a voltage  $V_{OUT}$ . Herein, an IP refers to an internal circuitry core or block of circuitry within the overall system; only portions of each IP are illustrated for simplicity. Similarly, a pin is a node that provides input or output to an IP. IP1 202 supplies an alternating current (AC) having a voltage  $V_{STEP}$  to Fail-Safe Pin 208 through Resistor  $R_{SOURCE}$ . IP2 204 contains Resistor 224 and Capacitor 222 and a Node 210, which has a voltage  $V_{STEP_{OUT}}$ , between Resistor 224 and Capacitor 222. A second terminal of Capacitor 222 is coupled to ground. IP-3 206 shares Fail-Safe Pin 208 with IP2 204 and in this example, contains a digital-to-analog converter (DAC), the details of which are not shown. IP-3 206 has a power-down mode in which the IP is not active. When IP3 206 is in power-down mode, this IP still affects the settling time at Node 210 in IP2 whenever  $V_{OUT}$  goes higher than  $V_{DD}$ . The configuration in FIG. 2 is an example and does not limit the circuits that can benefit from the described modified fail-safe signal.

**[0015]** To describe how this effect occurs, FIG. 3A shows one example of a fail-safe switch in use. Circuit 300A provides an example section of circuit that may be a part of an IP coupled to the shared Fail-Safe Pin 208. In this example, PMOS Transistor 310 has a source coupled to the upper rail, e.g.,  $V_{DD}$ , while NMOS Transistor 314 has a source coupled to the lower rail, e.g., ground, with a connection to Fail-Safe Pin 208 being provided between the drain of PMOS Transistor 310 and the drain of NMOS Transistor 314. As shown in FIG. 3A, PMOS Transistor 310 and NMOS Transistor 314 have their respective gates controlled by differential signals  $V_{IN+}$  and  $V_{IN-}$ . Given that the voltage  $V_{OUT}$  at Fail-Safe Pin 208 may be greater than the upper rail at times, PMOS Transistor 312 is coupled between the drain of PMOS Transistor 310 and Fail-Safe Pin 208, with the gate of PMOS Transistor 312 being controlled by a signal PKEEP. When the voltage  $V_{OUT}$  on Fail-Safe Pin 208 is less than or equal to  $V_{DD}$ , i.e., the circuit is able to operate normally, PKEEP is equal to the lower rail, e.g., ground. When the voltage  $V_{OUT}$  becomes greater than  $V_{DD}$ , PKEEP is driven to a value equal to  $V_{OUT}$ , as described hereinbelow, turning off Transistor 312. In this manner, PMOS Transistor 312 prevents a direct connection of Fail-Safe Pin 208 to the drain of PMOS Transistor 310 when  $V_{OUT}$  is greater than  $V_{DD}$ . Circuit 300A can be placed in a power-down mode by Signal PWDNZ, which is high during normal operation and low when the IP is in power-down mode. Transistor 316 is coupled between the

upper rail and the gate of Transistor 310 such that when PWDNZ goes low during power-down, the gate of PMOS Transistor 310 is pulled toward the upper rail, turning off PMOS Transistor 310.

**[0016]** If Circuit 300A is part of IP-3, then the switching of PMOS Transistor 312 (when  $V_{OUT}$  becomes greater than  $V_{DD}$ ) affects the settling time of voltage  $V_{STEP_{OUT}}$  at Node 210 in IP-2 204, even when IP-3 206 is in power-down mode. Preferably, as described hereinabove, when IP-3 is in power-down mode, IP-3 would not affect other IPs that share Fail-Safe Pin 208. One method of managing this issue is shown in FIG. 3B.

**[0017]** Circuit 300B is identical to Circuit 300A except for the addition of PMOS Transistor 318 between the drain of PMOS Transistor 312 and Fail-Safe Pin 208. Signal PWDN, which controls the gate of PMOS Transistor 318, is the inverse of PWDNZ and thus is high whenever the module is in power-down mode. This turns off PMOS Transistor 318 during power-down, isolating Fail-Safe Pin 208 from switching at PMOS Transistor 312 and preventing an effect on settling at Node 210. However, the addition of PMOS Transistor 318 introduces additional problems. PMOS Transistor 318 would need to be large, as the switch size required will be high, and the addition of another PMOS Transistor will increase the voltage drop, making the circuit less efficient.

**[0018]** Instead of adding a new switch, at least one embodiment modifies the fail-safe signal PKEEP such that the modified fail-safe signal will be high whenever  $V_{OUT}$  is greater than  $V_{DD}$  and also when the IP receiving PKEEP is in power-down mode, thus isolating Fail-Safe Pin 208 from the drain of PMOS Transistor 310 during these times. An embodiment that creates a modified PKEEP signal is described: first, with reference to FIG. 1B, which discloses a circuit for providing a fail-safe signal; and second, with reference to FIG. 1A, which discloses an embodiment in which the original fail-safe signal is modified to prevent issues during power-off.

**[0019]** In FIG. 1B, Circuit 100B receives voltage rails  $V_{DD}$  and  $V_{SS}$  and voltage  $V_{PAD}$  from Shared Pin 208; Circuit 100B provides two outputs: PKEEP, which is the original fail-safe signal, and NSUB, which as we will see is the greater of the value of  $V_{PAD}$  and  $V_{DD}$ . In the embodiment shown,  $V_{DD}$  and  $V_{SS}$  are received at Tie-Cell 118. For smaller technologies, e.g., 90 nanometer and smaller, the fixed inputs cannot be implemented by directly connecting the gate inputs to the power rails, as the high voltages and currents received from the rails are able to destroy the gates. Tie-cell 118 can connect additional resistors between the gate inputs and the

rails to protect the gates. For purposes of this description, the signals Tie<sub>High</sub> and Tie<sub>Low</sub>, which are output from Tie-Cell 118, are equivalent to  $V_{DD}$  and  $V_{SS}$  respectively; however, the values of Tie<sub>High</sub> and Tie<sub>Low</sub> can be adjusted to accommodate smaller technologies or different reference voltages. References in this description to ground, GND, are a reference to the local ground  $V_{SS}$ .

**[0020]** PMOS Transistor 120, PMOS Transistor 122 and NMOS Transistor 124 are coupled in series between Shared Pin 208, and the lower rail. The gates of PMOS Transistor 120 and NMOS Transistor 124 are each controlled by Tie<sub>High</sub> and the gate PMOS Transistor 122 is controlled by Tie<sub>Low</sub>. The output PKEEP is taken from a point between the drains of PMOS Transistor 122 and NMOS Transistor 124. PMOS Transistor 126 and PMOS Transistor 128 are also coupled in series between  $V_{PAD}$  and  $V_{DD}$ . The gate of PMOS Transistor 126 is controlled by Tie<sub>High</sub> and the gate of PMOS Transistor 128 is controlled by the signal, PKEEP. The signal NSUB is taken from a point between PMOS Transistor 126 and PMOS Transistor 128. Also, the substrates of PMOS Transistors 120 and 122 are coupled to a point between PMOS 126 and PMOS 128 and thus are also connected to NSUB.

**[0021]** The operation of Circuit 100B is as follows. When  $V_{PAD}$  is greater than  $V_{DD}$ , PMOS Transistors 120 and 122 turn on due to their negative gate-source voltage,  $V_{GS}$ , which pulls Node 125 towards  $V_{PAD}$ . NMOS Transistor 124 will remain on; however, this transistor has been made weaker than PMOS Transistor 120, such that NMOS Transistor 124 is overpowered when PMOS Transistor 120 is on. PKEEP then has a value of  $V_{PAD}$ , which turns off PMOS Transistor 128; PMOS Transistor 126 is also on due to its negative  $V_{GS}$ , so that NSUB has a value of  $V_{PAD}$ .

**[0022]** When  $V_{PAD}$  is less than  $V_{DD}$ ,  $V_{GS}$  at PMOS Transistor 120 is positive, so that PMOS Transistor 120 is turned off. NMOS Transistor 124 is on, pulling Node 125 to the lower rail, e.g., GND, giving PKEEP a value of zero. Because  $V_{PAD}$  is less than  $V_{DD}$ , PMOS transistor 126 is off, PMOS transistor 128 is on, and NSUB will be equal to  $V_{DD}$ .

**[0023]** As described hereinabove, Circuit 100B provides the fail-safe signal PKEEP, which is equal to the voltage  $V_{PAD}$  at Fail-Safe Pin 208 whenever  $V_{PAD}$  is greater than  $V_{DD}$  and is equal to GND when  $V_{PAD}$  is less than  $V_{DD}$ . However, we now want the transistor controlled by PKEEP to also turn off when its circuit is in power-down mode. Accordingly, the modified fail-safe signal PKEEP2 would preferably have the values shown in Table 1.

Table 1

| Power-Down | $V_{PAD}$ Value    | PKEEP2            |
|------------|--------------------|-------------------|
| PWDN=0     | $V_{PAD} < V_{DD}$ | PKEEP2=GND        |
| PWDN=0     | $V_{PAD} > V_{DD}$ | PKEEP2= $V_{PAD}$ |
| PWDN=1     | $V_{PAD} < V_{DD}$ | PKEEP2= $V_{DD}$  |
| PWDN=1     | $V_{PAD} > V_{DD}$ | PKEEP2= $V_{PAD}$ |

**[0024]** Referring to FIG. 1A, Circuit 100A discloses a circuit to provide the desired values for modified fail-safe signal PKEEP2. Circuit 100A receives inputs PKEEP, PWDN, PWDNZ (the inverse of PWDN), and NSUB and provides a modified fail-safe signal PKEEP2. Circuit 100A includes PMOS Transistor 102 coupled in series with NMOS Transistor 104 between Signal PWDNZ and the lower rail. NMOS Transistor 106 is also coupled in series with PMOS Transistor 102 (between Signal PWDNZ and the lower rail) and in parallel with NMOS Transistor 104. The gates of PMOS Transistor 102 and NMOS Transistor 106 are each controlled by PKEEP and the gate of NMOS Transistor 104 is controlled by PWDN. An intermediate signal PWDNZ1 is taken from a point between the drain of PMOS Transistor 102 and the drains of NMOS Transistors 104, 106 and provided to the gates of PMOS Transistor 108 and NMOS Transistor 110, which are coupled in series between signal NSUB and the lower rail. Modified fail-safe signal PKEEP2 is taken from a point between the drains of PMOS Transistor 108 and NMOS Transistor 110. PMOS Transistors 102, 108 have their substrate coupled to NSUB.

**[0025]** The operation of Circuit 100A will now be described. The four possible situations that can determine the value of modified fail-safe signal PKEEP2 are shown in Table 1, so the operation is described in the order of Table 1. In a first situation,  $V_{PAD}$  is less than  $V_{DD}$  and power-down is not active, so PWDN is equal to zero, PWDNZ is equal to one, and PKEEP is equal to the lower rail, which turns on PMOS Transistor 102 and turns off NMOS Transistor 106. PWDN being zero turns off NMOS 104. With both NMOS Transistor 104 and NMOS Transistor 106 turned off and PMOS Transistor 102 turned on, the value of PWDNZ1 is one. PWDNZ1 then turns off PMOS Transistor 108 and turns on NMOS Transistor 110, so that PKEEP2 is equal to the lower rail.

**[0026]** In the second situation,  $V_{PAD}$  is greater than  $V_{DD}$  and Circuit 200A is not in power

down mode. As described hereinabove, both PKEEP and NSUB are equal to  $V_{PAD}$ , PWDN is equal to zero and PWDNZ1 is equal to one. At PMOS Transistor 102, the gate-source voltage  $V_{GS}$  is positive, so PMOS Transistor 102 is off. NMOS Transistor 104 is turned off and NMOS Transistor 106 is turned on, setting PWDNZ1 to GND. PWDNZ1 then turns on PMOS Transistor 108 and turns off NMOS Transistor 110 so that PKEEP2 is equal to NSUB, which in this instance is equal to  $V_{PAD}$ .

**[0027]** In the third case,  $V_{PAD}$  is less than  $V_{DD}$  and Circuit 200A is in power down mode. PKEEP is equal to ground, PWDN is equal to one and PWDNZ is equal to zero. PMOS Transistor 102 will not turn on, because the gate-source voltage  $V_{GS}$  is zero; NMOS Transistor 106 is turned off but NMOS Transistor 104 turns on, pulling the value of PWDNZ1 to the lower rail, i.e., a value of zero. PWDNZ1 will turn off NMOS Transistor 110 and will turn on PMOS Transistor 108, so that PKEEP2 has a value equal to NSUB. Because  $V_{PAD}$  is less than  $V_{DD}$ , both NSUB and PKEEP2 have a value of  $V_{DD}$ .

**[0028]** In the fourth case,  $V_{PAD}$  is greater than  $V_{DD}$  and Circuit 300A is in power-down mode. PKEEP and NSUB are equal to  $V_{PAD}$ , PWDN is equal to one and PWDNZ1 is equal to zero. PMOS Transistor 102 will not turn on due to a positive  $V_{GS}$ , NMOS Transistor 104 is on and NMOS Transistor 106 is on, so PWDNZ1 is equal to GND. PWDNZ1 will then turn on PMOS Transistor 108 and turn off NMOS Transistor 110, so that PKEEP2 is set to equal NSUB, which is equal to  $V_{PAD}$ . The new modified fail-safe signal will thus fulfill the requirements set in Table 1.

**[0029]** The described embodiment provides a low area solution to the problem of fail-safe shared pin settling time issue between different blocks. A large switch, such as the additional switch shown in FIG. 3B, would impact the settling time of output by the parasitic capacitors, but using the described embodiment does not require a large switch and won't significantly impact output settling time of all IPs sharing the same pin.

**[0030]** Reference to an element in the singular does not mean "one and only one" unless explicitly so stated, but instead means "one or more."

**[0031]** Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

## CLAIMS

What is claimed is:

1. An integrated circuit (IC) for providing an improved fail-safe signal to a module sharing a fail-safe pin at which a voltage can be greater than a voltage of an upper rail, the IC comprising:
  - a first circuit segment that receives a first fail-safe signal and a first power-down signal and provides an intermediate signal, wherein the first fail-safe signal indicates when the voltage at the fail-safe pin is greater than the upper rail, and the first power-down signal indicates when the module is powered down; and
  - a second circuit segment connected to receive the intermediate signal and to provide the improved fail-safe signal to the module.
2. The IC as recited in claim 1 wherein the first circuit segment is coupled between a second power-down signal that is the inverse of the first power-down signal and a lower rail.
3. The IC as recited in claim 2 wherein the second circuit segment is coupled between a high signal that is the higher of the upper rail and the voltage at the fail-safe pin.
4. The IC as recited in claim 3 wherein the first circuit segment comprises:
  - a first PMOS transistor coupled in series with a first NMOS transistor;
  - a second NMOS transistor coupled in parallel with the first NMOS transistor; and
  - wherein the first fail-safe signal is coupled to drive a gate of the first PMOS transistor and a gate of the second NMOS transistor and the second power-down signal is coupled to drive a gate of the first NMOS transistor.
5. The IC as recited in claim 4, wherein the second circuit comprises a second PMOS transistor coupled in series with a third NMOS transistor, the intermediate signal being coupled to drive a gate of the second PMOS transistor and a gate of the third NMOS transistor and the improved fail-safe signal being taken from a point between the second PMOS transistor and the third NMOS transistor.
6. The IC as recited in claim 5 wherein the body of the first PMOS transistor and the body of the second PMOS transistor are coupled to the high signal.
7. The IC as recited in claim 6 wherein the first fail-safe signal is provided by a third circuit segment coupled between the fail-safe pin and the lower rail.

8. The IC as recited in claim 7 wherein the third circuit segment comprises a third and a fourth PMOS transistor coupled in series with a fourth NMOS transistor, a gate of the third PMOS transistor and a gate of the fourth NMOS transistor being controlled by the upper rail and a gate of the fourth PMOS transistor being controlled by the lower rail, and wherein the body of the third PMOS transistor and the body of the fourth PMOS transistor are coupled to the high signal.

9. The IC as recited in claim 8 wherein the high signal is provided by a fourth circuit segment coupled between the fail-safe pin and the upper rail.

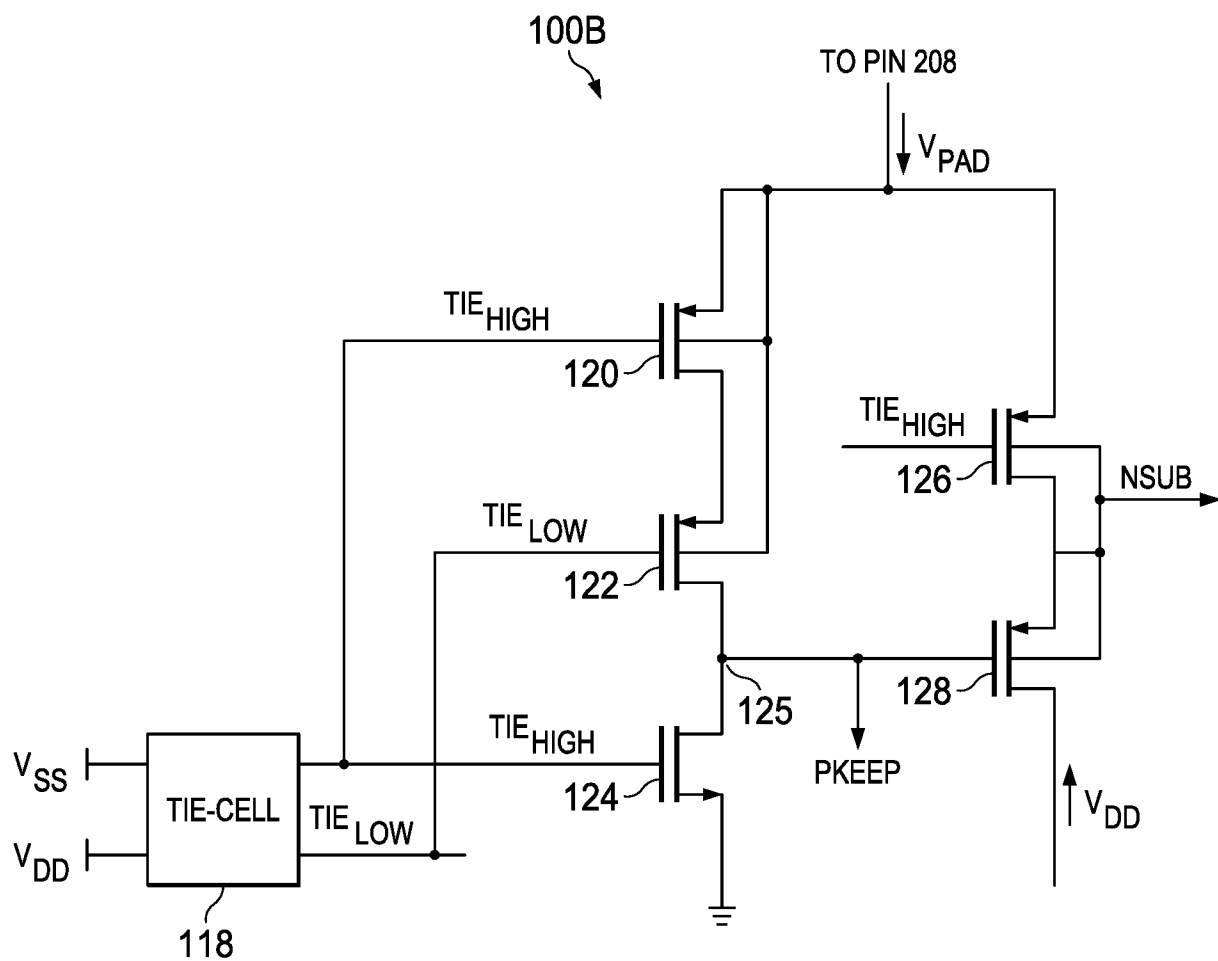
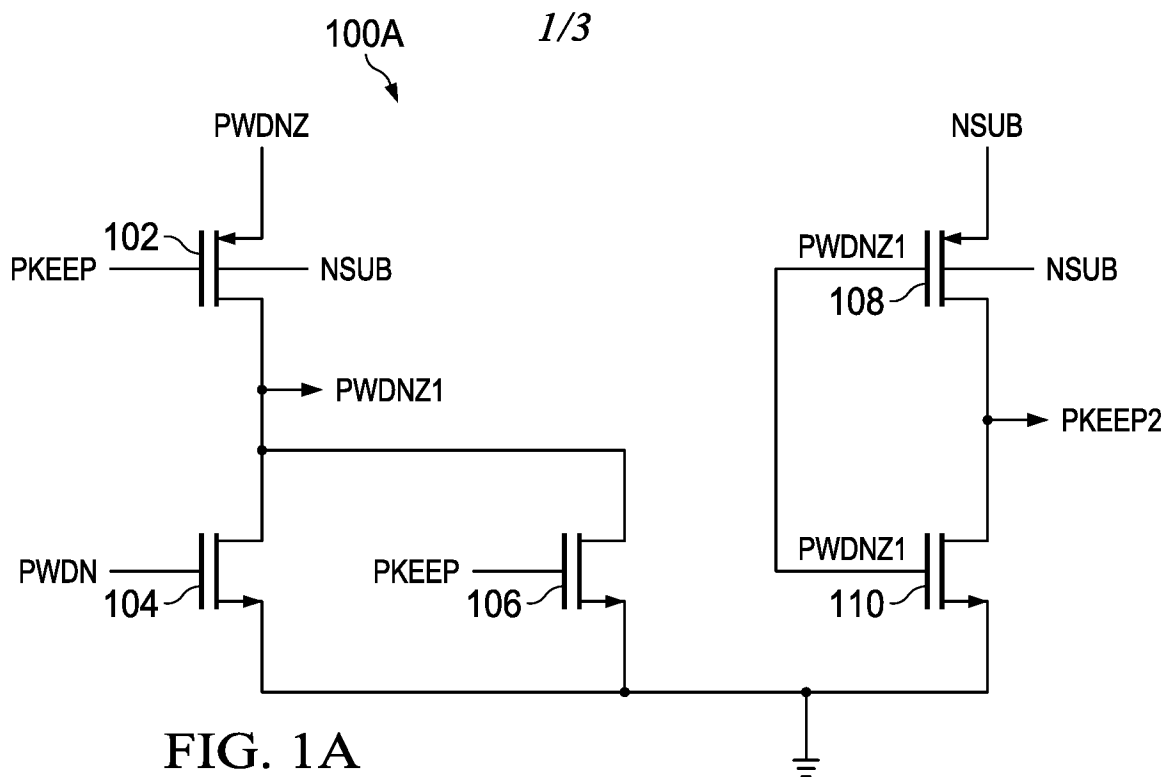
10. The IC as recited in claim 9 wherein the fourth circuit segment comprises a fifth PMOS transistor coupled in series with a fifth NMOS transistor, the gate of the fifth PMOS transistor being controlled by the upper rail and the gate of the fifth NMOS transistor being controlled by the first fail-safe signal, the high signal being taken at a point between the fifth PMOS transistor and the fifth NMOS transistor, and wherein the substrate of the fifth NMOS transistor and the fifth PMOS transistor are coupled to the high signal.

11. An integrated circuit (IC) comprising:

- a plurality of circuit blocks that share a common pin, wherein a voltage at the common pin can be greater than a voltage of an upper rail;

- a first circuit block of the plurality of circuit blocks, the first circuit block comprising a PMOS transistor coupled in series between the common pin and the upper rail; and

- a fail-safe circuit that receives the voltage at the common pin and a power-down signal for the first circuit block and provides a first fail-safe signal that turns off the PMOS transistor whenever the voltage at the common pin is greater than the upper rail and also when the first circuit block is in power-down mode.



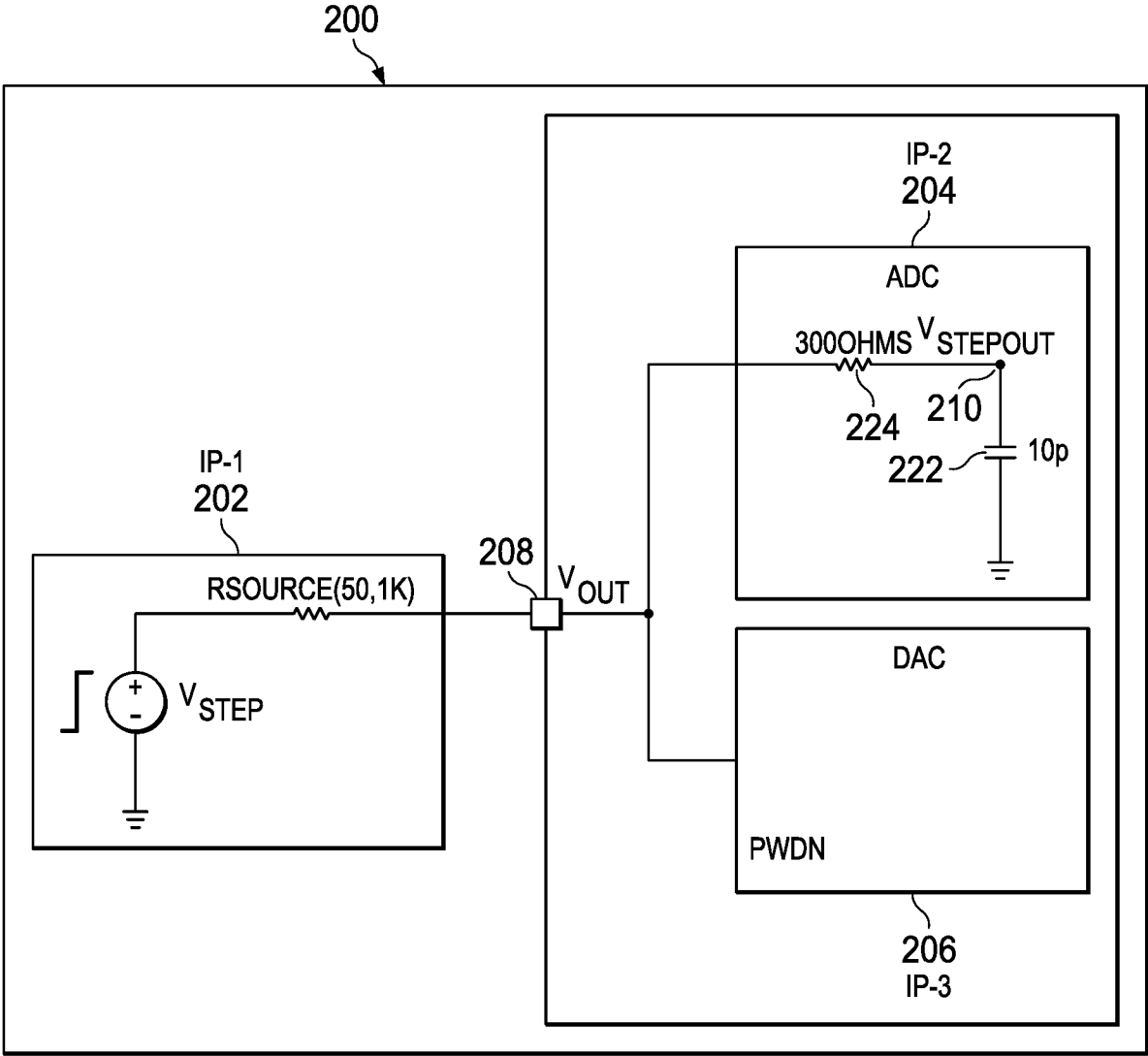


FIG. 2

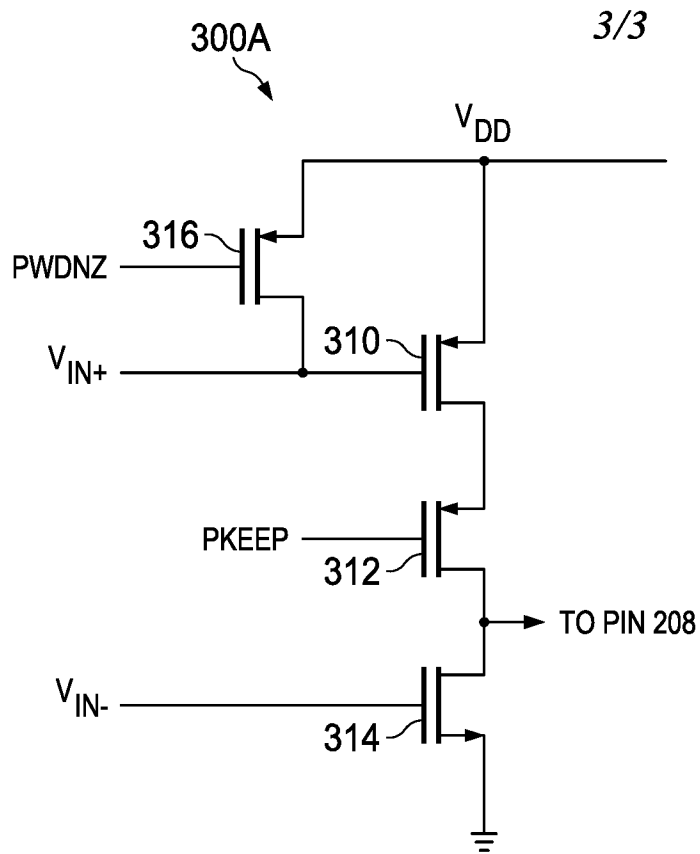


FIG. 3A

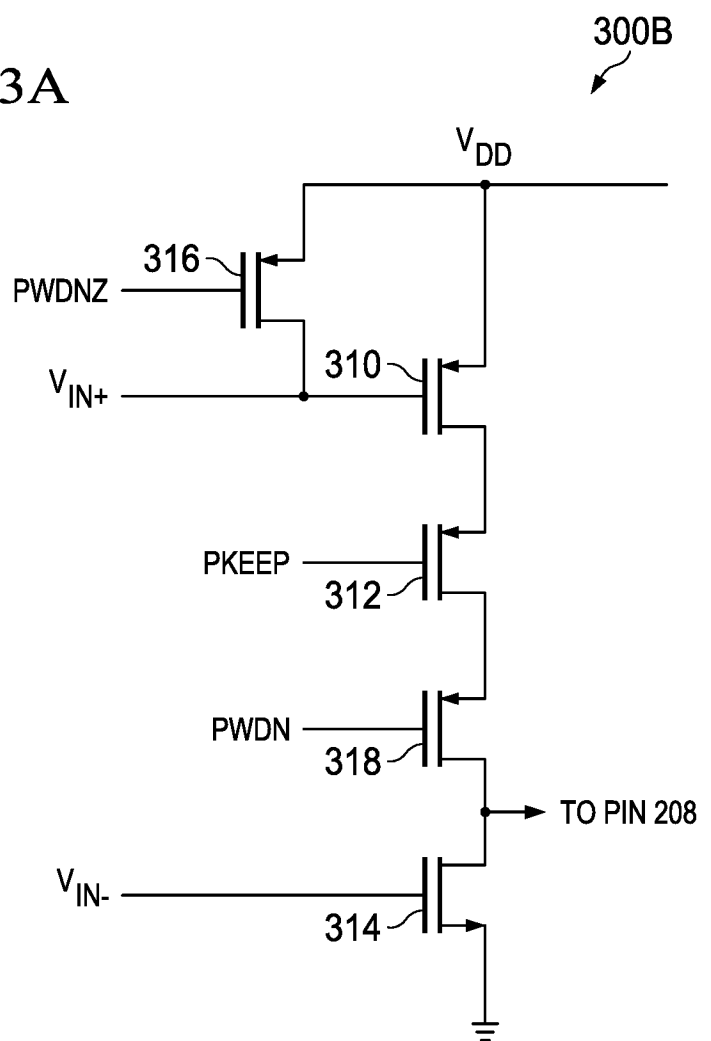


FIG. 3B

**INTERNATIONAL SEARCH REPORT**

International application No.

PCT/US 2017/025418

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|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>A. CLASSIFICATION OF SUBJECT MATTER</b><br><div style="text-align: right; font-weight: bold; margin-right: 50px;"><i>H03K 3/00 (2006.01)</i></div>                                                                                                                                                                                                |                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| According to International Patent Classification (IPC) or to both national classification and IPC                                                                                                                                                                                                                                                    |                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| <b>B. FIELDS SEARCHED</b>                                                                                                                                                                                                                                                                                                                            |                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| Minimum documentation searched (classification system followed by classification symbols)<br><div style="text-align: center; margin-top: 10px;">H03K 3/00</div>                                                                                                                                                                                      |                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched                                                                                                                                                                                                                        |                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)<br><div style="text-align: center; margin-top: 10px;">PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE</div>                                                                               |                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| <b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>                                                                                                                                                                                                                                                                                                        |                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| Category*                                                                                                                                                                                                                                                                                                                                            | Citation of document, with indication, where appropriate, of the relevant passages                                                                                  | Relevant to claim No.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| X                                                                                                                                                                                                                                                                                                                                                    | US 6304112 B1 (U.S. PHILIPS CORPORATION) 16.10.2001, abstract, claims,                                                                                              | 1, 11                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| A                                                                                                                                                                                                                                                                                                                                                    | col. 2, lines 18 –col.3, lines 35                                                                                                                                   | 2-10                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| A                                                                                                                                                                                                                                                                                                                                                    | US 7656185 B2 (SAMSUNG ELECTRONICS CO., LTD) 02.02.2010                                                                                                             | 1-11                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| A                                                                                                                                                                                                                                                                                                                                                    | US 5404359 (TANDEM COMPUTERS INCORPORATED) 04.04.1995                                                                                                               | 1-11                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| A                                                                                                                                                                                                                                                                                                                                                    | US 6320406 B1 (TEXAS INSTRUMENTS INCORPORATED) 20.11.2001                                                                                                           | 1-11                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| <div style="display: flex; justify-content: space-between; align-items: flex-start;"> <div style="width: 45%;"> <input type="checkbox"/> Further documents are listed in the continuation of Box C.                         </div> <div style="width: 45%;"> <input type="checkbox"/> See patent family annex.                         </div> </div> |                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| *                                                                                                                                                                                                                                                                                                                                                    | Special categories of cited documents:                                                                                                                              | “T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention<br>“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone<br>“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art<br>“&” document member of the same patent family |
| “A”                                                                                                                                                                                                                                                                                                                                                  | document defining the general state of the art which is not considered to be of particular relevance                                                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| “E”                                                                                                                                                                                                                                                                                                                                                  | earlier document but published on or after the international filing date                                                                                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| “L”                                                                                                                                                                                                                                                                                                                                                  | document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| “O”                                                                                                                                                                                                                                                                                                                                                  | document referring to an oral disclosure, use, exhibition or other means                                                                                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| “P”                                                                                                                                                                                                                                                                                                                                                  | document published prior to the international filing date but later than the priority date claimed                                                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| Date of the actual completion of the international search                                                                                                                                                                                                                                                                                            | Date of mailing of the international search report                                                                                                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 23 June 2017 (23.06.2017)                                                                                                                                                                                                                                                                                                                            | 14 August 2017 (14.08.2017)                                                                                                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| Name and mailing address of the ISA/RU:<br>Federal Institute of Industrial Property,<br>Berezhkovskaya nab., 30-1, Moscow, G-59,<br>GSP-3, Russia, 125993<br>Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37                                                                                                                                      | Authorized officer<br><div style="text-align: right; margin-right: 50px;">L. Afanasiev</div> Telephone No. 8 499 240 25 91                                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |