Abstract: Examples disclosed herein relate to a switch between a first power source and a second power source. Examples include a first power source electrically coupled to a load via a first transistor and a second transistor. A second power source electrically coupled to the load via a third transistor. A controller electrically coupled to drive the first transistor, the second transistor, and the third transistor to switch between the first power source and the second power source according to a determined voltage of the first power source and the second power source. The first transistor and the second transistor are back-to-back transistors, and the third transistor includes a body diode between a source terminal and a drain terminal of the third transistor to limit a voltage drop at the load in response to interruption of power from the first power source.

Title: SWITCH BETWEEN FIRST POWER SOURCE AND SECOND POWER SOURCE

FIGURE 2
SWITCH BETWEEN FIRST POWER SOURCE AND SECOND POWER SOURCE

BACKGROUND

[0001] As reliance on electronic systems continues to grow, so too does the demand for reliable power systems and backup schemes for these electronic systems. Servers, for example, may provide architectures for backing up data to flash or persistent memory as well as backup power sources for powering this backup of data after an interruption of power. Data may be backed up as part of a shutdown of a server.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] The following detailed description references the drawings, wherein:

[0003] FIG. 1 is a block diagram of an example of a system to reduce backflow current;

[0004] FIG. 2 is a block diagram of an example of a system to reduce backflow current; and

[0005] FIG. 3 is a flowchart of an example method for limiting backflow current.

DETAILED DESCRIPTION

[0008] In the following discussion and in the claims, the term "couple" or "couples" is intended to include suitable indirect and/or direct connections. Thus, if a first component is described as being coupled to a second component, that coupling may, for example, be: (1) through a direct electrical or mechanical connection, (2) through an indirect electrical or mechanical connection via other devices and connections, (3) through an optical electrical connection, (4) through a wireless electrical connection, and/or (5) another suitable coupling.

[0007] As used herein, a "device" may be a motor, desktop computer, laptop (or notebook) computer, workstation, tablet computer, mobile phone, smart device, server, blade enclosure, imaging device, or any other device or equipment operating under electrical power or including an electrical system. In the examples described herein, "backflow current" refers to a reverse flow of current in an electrical system from an intended or designed direction, in an example, the flow of current in an electrical system may be designed to be from a power source to a load and backflow current may refer to a flow of current from the load to the power source. In such example, in an electronic recharging mode, the flow of current in the electrical system may be designed to be from a charging power supply to the power source while bypassing the load, and backflow current may refer to a flow of current to the load rather than to the power source. As used herein, in an electronic system, "back-to-back transistors" refers to two transistors electrically coupled to each other by the same type of terminal. For example, two field-effect transistors (FETs) may be described as back-to-back when a source terminal of a first transistor is electrically coupled to a source terminal of a
second transistor. In another example, two FETs may be described as back-to-back when a drain terminal of a first transistor is electrically coupled to a drain terminal of a second transistor. In yet another example, two bipolar transistors may be described as back-to-back when a collector terminal of a first transistor is electrically coupled to a collector terminal of a second transistor. Similarly, two bipolar transistors may be described as back-to-back when an emitter terminal of a first transistor is connected to an emitter terminal of a second transistor.

[0008] An interruption of a power supply to a device may damage components in the device. In an example, some devices can include a load which may be damaged if power supply is interrupted. A number of loads can include storage controllers or devices associated with the device. For example, a load can include cache memory, dual inline memory modules (DIMMs), Non-Volatile Dual in-Line Memory Modules (NVDIMMs), and/or array control logic, among other storage controllers and/or devices.

[0009] An interruption of a primary power supply can be scheduled or un-scheduled. For instance, a scheduled interruption of the primary power supply can be the result of scheduled maintenance on the device and/or a number of loads. An un-scheduled primary power supply interruption can be an interruption in the primary power supply. An un-scheduled primary power supply interruption can occur when, for example, the primary power supply fails momentarily or for an extended period of time. Failure can include an unintentional loss of power to devices and/or loads from the primary power supply.

[0010] A secondary power supply can be provided to the device. For example, a micro-uninterruptible power supply (µUPS) can be an integrated secondary power supply that is used to provide emergency power to a load when a primary power supply (e.g., input power source) is interrupted. Interruption of a primary power supply can refer to a power failure, power surge, inadequate power, and/or transient faults. A pUPS can provide near-instantaneous protection from power interruptions by supplying energy stored in batteries, super capacitors, or flywheels, among others. However, there may be a delay in activation of a pUPS if there is an interruption of a primary power supply. In other examples, the near-instantaneous supply of energy provided by a pUPS may not be sufficiently instantaneous to provide adequate voltage to the load to perform certain functions.

[0011] The flow of current from the secondary power supply to the load may be near-instantaneous when the secondary power source is electrically coupled to the load via a transistor acting as a switch. The delay in current flow from the secondary power supply to the load may result from the time it takes for sufficient current to flow across the channel of the transistor to power the load. For example, in a P-channel FET, there is a time delay between when a voltage
at the gate terminal of the FET (or a base terminal in bipolar transistor) is initially applied and when there is a sufficient reduction in the resistance in a channel between the source terminal and the drain terminal such that a current may flow from the source terminal to the drain terminal and to the load. A transistor is considered "activated" or "fully saturated" when the resistance across the channel of the transistor is reduced such that sufficient current is flowing across the channel to an output terminal of the transistor (e.g., a collector of bipolar transistor, a source terminal or drain terminal of a FET) to a component coupled thereto.

[0012] In some devices, it may be desirable to move data from volatile cache memory in the device to non-volatile memory upon the removal of a primary power supply. However, moving data from cache memory to non-volatile memory can involve a secondary power supply. The secondary power supply can include an integrated secondary power supply. For example, the integrated secondary power supply can include a pUPS that is used to provide power for moving data from cache memory to non-volatile memory (i.e., data backup) when the primary power supply is interrupted.

[0013] In an example, there may be a delay between the interruption of the primary power supply and the secondary power supply providing power to the system. The interruption in the primary power supply may result in a loss of sufficient power to the load to move data from volatile cache memory to non-volatile memory. Although an electrical system may be designed to switch from the primary power supply to the secondary power supply before the loss of sufficient power (i.e., below a threshold level) to perform data backup, this switch between primary power supply and secondary power supply may not be completed fast enough to restore sufficient power to the load. For example, the power provided to the load may drop below the threshold level because of backflow current diverting power from the load. In an example, in the time between electrically coupling the secondary power source and the flow of sufficient current from the secondary power source to the load, backflow current may drain power from the load below the threshold level. In some examples, such a backflow current may flow towards the secondary power source and may damage the secondary power source. For example, if the backflow current is of a higher voltage than the secondary power source, it may damage the secondary power source. In another example, when recoupling a primary power source to an electronic system, backflow current may flow toward the primary power source from the secondary power source and damage the primary power source or the load.

[0014] To address these issues, in the examples described herein, a system that can reduce or limit the backflow of current while switching between a first power source and a second power source is provided. In an example, the system detects when a voltage supplied by the first
power source falls below a threshold level or a voltage level provided by the second power source and switches to the second power source. The first power source may be a main power supply. In such an example, the first power source may be electrically decoupled from the load in response to detection of a voltage drop from main power supply to reduce a potential backflow current when switching to the second power source. In an example, during a time delay between electrically decoupling the first power source and electrically coupling the second power source, a voltage drop at the load may be limited to a certain level to maintain power to a subcomponent of the load. For example, the system may limit the voltage drop at the load by selecting a diode to limit backflow current. In an example, the subcomponent of the load may be data backup subsystems to transfer volatile cache memory to non-volatile memory. However, the examples are not limited thereto and the power remaining in the system while switching between the first power source and the secondary source may be the entire load of the system or any other subcomponent in the load.

[0015] Referring now to the drawings, FIG. 1 is a block diagram of an example of a system 100 to reduce backflow current. System 100 includes a first power source 110, a second power source 120, a controller 130, a load 140, a first transistor 150, a second transistor 160, and a third transistor 170. In the example of FIG. 1, each of first transistor 150, second transistor 160, and third transistor 170 include a body diode between a source terminal and a drain terminal thereof. However, the examples are not limited thereto and first transistor 150, second transistor 180, and third transistor 170 may not include a body diode. In such an example, a separate diode may be coupled to at least one of first transistor 150, second transistor 160, and third transistor 170. For example, a separate diode may be coupled to third transistor 170 to reduce a voltage drop at the load 140 according to a forward voltage drop of the separate diode.

[0016] In an example, the first power source 110 may be a main power supply to the system 100. First power source 110 may be a direct current (DC) or alternating current (AC) power source, for example, a voltage from a wall outlet (mains supply) plug, a battery, super capacitors, an electrical motor, a photovoltaic cell, an inverter, flywheels, etc. In an example, the second power source 120 may be a secondary or backup power supply to the system 100. In such an example, second power source 120 may be a battery, super capacitor, electrical motor, a photovoltaic cell, an inverter, flywheels, etc. However, the examples are not limited thereto and first power source 110 may be a backup power supply to system 100 and second power source 120 may be a main power supply to system 100.

[0017] Controller 130 may be any hardware or programing in combination with hardware to compare voltages and drive a transistor. Controller 130 may determine and/or compare the voltages
provided by first power source 110 and second power source 120. Controller 130 may drive a gate terminal of each of first transistor 150, second transistor 160, and third transistor 170 according to the determined voltages of first power source 110 and second power source 120. In an example, controller 130 may be hardware, such as, a comparator, a differential amplifier, etc. in another example, controller 130 may be hardware in combination with machine readable instructions, for example, a processing resource and a machine readable storage medium including instructions executable by the processing resource to compare voltages of first power source 110 and second power source 120 and drive one or more of first transistor 150, second transistor 160, and third transistor 170 in response to the comparative voltage. However, the examples are not limited thereto, controller 130 may determine a voltage and a separate circuit element(s) may drive a gate terminal of each of first transistor 150, second transistor 160, and third transistor 170 according to the determined voltage. For example, a separate controller may drive each of first transistor 150, second transistor 160, and third transistor 170 according to a voltage determined by controller 130.

[0018] In an example, the load 140 may be any device, circuitry, or other electrically operable device which is to receive power from the first power source 110. For example, the load may be a motor, a light emitting diode (LED), a motherboard of a computer, a server, a server node, etc. The load 140 may include subcomponents. In an example, the system 100 may be designed to power load 140 via first power source 110. In such a system, when an interruption in first power source 110 is detected, the system 100 switch to provide power to load 140 from second power source 120. However, the examples are not limited thereto and switching to provide power from second power source 120 may result in providing power to certain subcomponents of load 140, such as, a subcomponents of a data backup subsystem or any other subcomponent of load 140.

[0019] First transistor 150, second transistor 160, and third transistor 170 may be a FET, such as a metal-oxide-semiconductor field-effect transistor (MOSFET), junction field-effect transistor (JFET), dual-gate MOSFET (DGMOSFET), fast-reverse or fast-recovery epitaxial diode FET (FREDFET), heterostructure insulated gate field-effect transistor (HiGFET), modulation-doped field-effect transistor (MODFET), tunnel field-effect transistor (TFET), metal-semiconductor field-effect transistor (MESFET), nanoparticle organic memory field-effect transistor (NOMFET), graphene nanoribbon field-effect transistor (GNRFET), vertical-slit field-effect transistor (VeSFET), carbon nanotube field-effect transistor (CNTFET), organic field-effect transistor (OFET), and quantum field effect transistor (QFET). Although depicted as P-channel transistors in FIG. 1, first transistor 150, second transistor 160, and third transistor 170 may be an N-channel transistor. In other examples,
one or more of first transistors 150, second transistors 160, and third transistor 170 may be a bipolar
transistor.

[0020] in the example of FIG. 1, first transistor 150 and second transistor 160 are back-to-back transistors electrically coupled to first power source 110 and load 140. Although in the example of FIG. 1 a source terminal of first transistor 150 is coupled to a source terminal of second transistor 160, the examples are not limited thereto, and first transistor 150 and second transistor 160 may be back-to-back transistors via respective drain terminals. Each of first transistor 150 and second transistor 160 may include a body diode forward biased towards each other. In other words, the body diode of first transistor 150 has a forward voltage drop in a direction towards second transistor 160 and the body diode of second transistor 160 has a forward voltage drop in a direction toward first transistor 150. However, the examples are not limited thereto, and first transistor 150 and second transistor 160 may not include a body diode.

[0021] Third transistor 170 may be electrically coupled to second power source 120 and load 140. In such an example, third transistor 170 may act as a switch to electrically couple second power source 120 and load 140. In an example, the body diode of third transistor 170 may be forward biased such that a voltage at load 140 remains within an operating parameter of load 140. For example, the body diode of the third transistor 170 may allow current to flow until the third transistor 170 is activated such that a reduction in the voltage at the load due to the interruption of first power source 110 is limited by the forward voltage drop of the body diode of third transistor 170. The body diode of the third transistor 170 may be selected to reduce or limit the voltage drop at the load to a negligible level. For example, the body diode of third transistor 170 may be selected to reduce or limit voltage drop at the load to near zero.

[0022] in an example, controller 130 is to drive the gate terminal of first transistor 150, second transistor 160, and third transistor 170 to electrically couple the load 140 to either first power source 110 or second power source 120. In other words, first transistor 150 and second transistor 160 may act as a switch to couple first power source 110 to load 140 and third transistor 170 may act as a switch to couple second power source 120 to load 140. In an example, controller 130 may decouple first power source 110 from load 140 when the voltage at first power source 110 falls below a threshold level. In other words, controller 130 may turn off the flow of current (i.e., turn off voltage supply) from first power source 110 to load 140 if the voltage at first power source drops below the threshold level, in such an example, controller 130 may drive a gate terminal of third transistor 170 to electrically couple second power source 120 to load 140 in response to decoupling first power source 110 from load 140. In other words, controller 130 may turn on the flow of current from second power source 120 to load 140 in response to turning off the flow of current from the first power source.
110. in another example, the controller 130 may decouple the first power source 110 from load 140 when the detected voltage at first power source 110 is at or below the voltage detected at second power source 120. Similarly, in such an example, the controller 130 may drive third transistor 170 to electrically couple the second power source 120 to the load 140 in response to the electric decoupling of first power source 110 from load 140. The voltage at first power source 110 may drop below the threshold value or below the voltage at second power source 120 in response to an intentional or unintentional interruption of first power source 110.

[0023] In an example, a voltage at the load 140 may be discharged or backflow towards second power source 120 while third transistor 170 is activated. In such an example, a body diode of third transistor 170 may limit or reduce backflow current from reaching second power source 120 and may also limit the voltage drop at the load 140 to approximately the voltage drop at the body diode of third transistor 170. The body diode of third transistor 170 may be selected to control the voltage drop at the load 140 to maintain sufficient power levels in the load 140 while third transistor 170 is activated to perform a certain function. For example, in a device in which volatile cache memory is to be transferred to non-volatile memory in response to an interruption in the first power source 110, the voltage drop at the load 140 may be limited by the body diode of third transistor 170 to maintain sufficient power to transfer the volatile cache memory. However, the examples are not limited thereto and other functions of the load may be maintained during the transition period between the electrically decoupling first power source 110 and electrically coupling second power source 120.

[0024] In some examples, the controller 130 may drive third transistor 170 to electrically decouple the second power source 120 from load 140 in response to detecting a higher voltage from first power source 110 relative to the voltage of second power source 120. In such an example, controller 130 may drive first transistor 150 and second transistor 160 to electrically couple first power source 110 to load 140 to reinitiate a power supply from first power source 110.

[0025] FIG. 2 is a block diagram of an example system 200 to reduce backflow. System 200 includes a first power source 210, a second power source 220, a controller 230, a load 240, a first transistor 250, a second transistor 280, a third transistor 270, and a fourth transistor 290. In the example of FIG. 2, each of first transistor 250, second transistor 260, third transistor 270, and fourth transistor 290 include a body diode. However, the examples are not limited thereto and first transistor 250, second transistor 280, third transistor 270, and fourth transistor 290 may not include a body diode. In such an example, a separate diode may be coupled to at least one of first transistor 250, second transistor 260, third transistor 270, and fourth transistor 290. For example, a separate diode may be coupled to third transistor 270 to reduce a voltage drop at the
load 240 according to the forward bias of the separate diode as described above with respect to FIG. 1.

In an example, the first power source 210 and the second power source 220 may be substantially similar to the first power source 110 and the second power source 120 described above with regards to FIG. 1. Similarly, controller 230 and load 240 may be substantially similar to controller 130 and load 140, respectively, described above with respect to FIG. 1.

As described above with respect to FIG. 1, first transistor 250, second transistor 260, third transistor 270, and fourth transistor 290 may be a FET. In an example, first transistor 250, second transistor 280, third transistor 270, and fourth transistor 290 may be any type of FET as described above with respect to FIG. 1. Although depicted as P-channel transistors in FIG. 2, first transistor 250, second transistor 260, third transistor 270, and fourth transistor 290 may be an N-channel transistor.

First transistor 250 and second transistor 260 may be substantially similar to first transistor 150 and second transistor 180 and may function in substantially the same way as described above with respect to FIG. 1. In particular, first transistor 250 and second transistor 260 may be back-to-back transistors electrically coupled to first power source 210 and load 240, such that a source terminal of first transistor 250 is coupled to a source terminal of second transistor 260. As described above with respect to FIG. 1, controller 230 may drive first transistor 250 and second transistor 260 to electrically couple first power source 210 to load 240 in response to a detected voltage of first power source 210. For example, first power source 210 may be decoupled from load 240 in response to the voltage at first power source 210 dropping below a threshold level or a voltage of the second power source 220.

Third transistor 270 and fourth transistor 290 may be electrically coupled to second power source 220 and may be arranged to be back-to-back transistors, such that, a drain from third transistor 270 is coupled to a drain from fourth transistor 290. However, the examples are not limited thereto, and third transistor 270 and fourth transistor 290 may be back-to-back transistors coupled via respective source terminals. In an example, controller 230 may drive third transistor 270 and fourth transistor 290 to electrically couple second power source 220 to load 240 in response to first power source 210 electrically decoupling from load 240.

In the example of FIG. 2, fourth transistor 290 may be electrically coupled to second power source 220 further electrically isolate or decouple second power source 220 from load 240 when the controller 230 determines first power source 210 is to be coupled to load 240 after an interruption in first power supply 210. In other words, fourth transistor 290 is to electrically isolate second power source 220 from the load 240 (i.e., turn-off second power source 220) in response
first power source 210 electrically coupling to load 240 after an interruption in first power source 210. As described above with respect to FIG. 1, controller 230 may determine the first power source 210 is to be coupled to load 240 to provide power when a voltage at first power source 210 is higher than a voltage at second power source 220 or a threshold value. In an example, first power source 210 may be a 12V main power supply and second power source 220 may be a 6V battery or super capacitor. In such an example, controller 230 may determine first power source 210 is to be electrically coupled to load 240 until a voltage at first power supply 210 drops below 6V or a threshold value. For example, the threshold value may be 5 V. Controller 230 may drive a gate terminal of first transistor 250 and second transistor 260 to electrically decouple first power source 210 in response to a drop of voltage at first power source 210. In addition, controller 230 may drive a gate terminal of third transistor 270 and fourth transistor 290 to electrically couple second power source 220 to load 240 in response to a decoupling first power source 210 from load 240. In an example, when controller 230 determine the voltage at first power source 210 exceeds a threshold level or a voltage at second power source 220, controller 230 may drive third transistor 270 to decouple second power supply 220 from load 240 and fourth transistor 290 to electrically isolate second power supply 220. In such an example, controller 230 may drive first transistor 250 and second transistor 260 to couple first power source 210 to load 240 in response to second power source 220 electrically decoupling from load 240. In an example, the load 240 may be the reinitiated in a specific sequence in response to receiving a power supply from a source with a voltage greater than the threshold level or a voltage of second power source 220.

[0031] In an example, controller 230 may drive a gate terminal of third transistor 270 to act as a switch to decouple second power supply 220 from load 240 and drive a gate terminal of fourth transistor 290 to electrically isolate (i.e., turn off) second power supply 220. In another example, a separate circuit element may drive fourth transistor 290 to electrically isolate second power supply 220 from load 240. For example, a second controller or a switch may drive fourth transistor 290.

[0032] FIG. 3 is a flowchart of an example method 300 for limiting backflow current. Although execution of method 300 is described below with reference to system 200 described above, other suitable systems (system 100) for the execution of method 300 can be utilized. Additionally, implementation of method 300 is not limited to such examples.

[0033] At 302 of method 300, system 200 may decouple first power source 210 from load 240 in response to controller 230 determining a voltage provided by first power source 210 is less than a voltage at second power source 220. In an example, first power source 210 may be a 12V main power supply and second power source 220 may be a 6V battery.
At 304, system 200 may limit a voltage drop at load 240 via a body diode of third transistor 270 while third transistor 270 and fourth transistor 290 are activated to provide current flow from second power source 220 to load 240. In other words, when third transistor 270 and fourth transistor 290 are activated, it may close a switch between second power source 220 and load 240 to allow a current to flow from second power source 220 to load 240. In the example of FIG. 3, the load may be a motherboard of a device or a component of a motherboard of a device. For example, the load may be a data backup subsystem of the motherboard.

At 306, system 200 may provide power to load 240 when third transistor 270 and fourth transistor 290 are activated by controller 230 to electrically coupled second power source 220 to allow a current to flow to load 240. In other words, when third transistor 270 and fourth transistor 290 are activated, a switch is closed between load 240 and second power source 220 to allow current to flow from the second power source 220 to load 240.

At 308, in response to controller 230 determining first power source 210 has a higher voltage than second power source 220, controller 230 may drive third transistor 270 and fourth transistor 290 to electrically decouple and isolate second power source 220 from load 240. In the example of FIG. 2, fourth transistor 290 may switch off second power source 220.

Although the flowchart of FIG. 3 shows a specific order of performance of certain functionalities, method 300 is not limited to that order. For example, the functionalities shown in succession in the flowchart may be performed in a different order, may be executed concurrently or with partial concurrence, or a combination thereof. In some examples, functionalities described herein in relation to FIG. 3 may be provided in combination with functionalities described herein in relation to any of FIGS. 1-2.
What is claimed is:

1. A system, comprising
a first power source electrically coupled to a load via a first transistor and a second transistor;
a second power source electrically coupled to the load via a third transistor;
a controller electrically coupled to drive the first transistor, the second transistor, and the third transistor to switch between the first power source and the second power source according to a determined voltage of the first power source and the second power source,
wherein the first transistor and the second transistor are back-to-back transistors, and
wherein the third transistor includes a body diode between a source terminal and a drain terminal of the third transistor to limit a voltage drop at the load in response to interruption of power from the first power source.

2. The system of claim 1, wherein the controller is to control the first transistor and the second transistor to shut off a flow of current from the first power source to the load in response to interruption of the first power source.

3. The system of claim 1, wherein the controller is to control the third transistor to turn on a flow of current from the second power source to the load in response to detection of an interruption of power from the first power source.

4. The system of claim 1, wherein the controller is to control the third transistor to turn on a flow of current from the second power source to the load in response to detection that a voltage at the first power source is lower than a voltage at the second power source.
5. The system of claim 1, wherein the controller is to control the third transistor to turn off a flow of current from the second power source to the load in response to detection that a voltage at the first power source is higher than a voltage at the second power source.

6. The system of claim 1, wherein the body diode of the third transistor limits a voltage drop at the load.

7. The system of claim 1, wherein the body diode of the third transistor limits a flow of current from the main power source to the backup power source.

8. A system, comprising:

   a first power source electrically coupled to a load via a first transistor and a second transistor;

   a second power source electrically coupled to the load via a third transistor and a fourth transistor; and

   a controller electrically coupled to drive the first transistor, the second transistor, the third transistor, and the fourth transistor to switch between the first power source and the second power source according to a relative voltage of the first power source and the second power source, wherein the first transistor and the second transistor are back-to-back transistors, wherein the third transistor and the fourth transistor are back-to-back transistors, wherein the third transistor includes a body diode between a source terminal and a drain terminal of the third transistor to limit a voltage drop at the load in response to interruption of power from the first power source.

9. The system of claim 8, wherein the controller is to control the first transistor and the second transistor to turn off voltage supply from the first power source to the load when there is a loss of power from the first power source.
10. The system of claim 9, wherein the controller is to control the third transistor and the fourth transistor to turn on a flow of current from the second power source to the load in response to detection of a lower voltage at the first power source relative to the voltage at the second power source.

11. The system of claim 9, wherein the controller is to control the third transistor and the fourth transistor to turn on a flow of current from the second power source to the load in response to detection of a higher voltage of the first power source relative to a voltage at the second power source.

12. The system of claim 11, wherein the fourth transistor is to electrically isolate the second power source from the load.

13. The system of claim 9, wherein the load is a motherboard.

14. A method for reducing backflow current, comprising:

   decoupling a first power source to a load in response to determining a voltage at the first power source is less than a voltage at a second power source;

   limiting a voltage drop at the load via a diode while a switch electrically coupling the second power source to the load is closed;

   providing the second power source to the load when the switch is closed, and

   in response to the first power source having a higher voltage relative to the second power source, electrically decoupling the second power source from the load,

   wherein the load is a motherboard.
15. The method of claim 14, wherein the second power source is to power a subcomponent of the motherboard to move data from a volatile cache memory to a non-volatile memory.
DECOUPLING FIRST POWER SOURCE TO LOAD IN RESPONSE TO DETERMINING VOLTAGE AT FIRST POWER SOURCE IS LESS THAN VOLTAGE AT SECOND POWER SOURCE

LIMITING VOLTAGE DROP AT LOAD VIA DIODE WHILE SWITCH ELECTRICALLY COUPLING SECOND POWER SOURCE TO LOAD IS CLOSED

PROVIDING SECOND POWER SOURCE TO LOAD WHEN THE SWITCH IS CLOSED

IN RESPONSE TO FIRST POWER SOURCE HAVING HIGHER VOLTAGE THAN SECOND POWER SOURCE, ELECTRICALLY DECOUPLING SECOND POWER SOURCE FROM THE LOAD

FIGURE 3
### B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G1C 5/14; H02J 1/10; H02M 7/537; H02H 3/00; H02J 7/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

- Korean utility models and applications for utility models
- Japanese utility models and applications for utility models

Electronic database consulted during the international search (name of database and, where practicable, search terms used)

eKOMPASSKIPO internal

& Keywords: first, second, third, transistor, load, controller, switch, voltage, back-to-back, body, diode, backflow, power, source

### C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Y</td>
<td>US 05654859 A (FONG SHI) 05 August 1997&lt;br&gt;See column 3, 1 lines 29-34; column 5, 1 lines 33-35, 50-53, 57-61; column 6, 1 lines 26-31; column 7, 1 lines 6-7, 17-22; and figures 3-5.</td>
<td>1-15</td>
</tr>
<tr>
<td>Y</td>
<td>US 05764032 A (BRUCE DUDLEY MOORE) 09 June 1998&lt;br&gt;See column 2, 1 lines 48-50; column 3, 1 lines 30-39; column 4, 1 lines 5-9; and figures 2b, 4.</td>
<td>1-15</td>
</tr>
<tr>
<td>A</td>
<td>US 2007-0268726 AI (HASSAN ALI KOJORI et al.) 22 November 2007&lt;br&gt;See paragraph [0043]; and figure 2.</td>
<td>1-15</td>
</tr>
<tr>
<td>A</td>
<td>US 2010-0164289 AI (CHRISTOPHER BRUCE UMMINGER et al.) 01 July 2010&lt;br&gt;See paragraph [0031]; and figure 4.</td>
<td>1-15</td>
</tr>
<tr>
<td>A</td>
<td>US 2011-0013438 AI (MICHAEL FRISCH et al.) 20 January 2011&lt;br&gt;See paragraph [0037]; and figure 3.</td>
<td>1-15</td>
</tr>
</tbody>
</table>

Further documents are listed in the continuation of Box C.

- * Special categories of cited documents:
  - "A" document defining the general state of the art which is not considered to be of particular relevance
  - "E" earlier application or patent but published on or after the international filing date
  - "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
  - "O" document referring to an oral disclosure, use, exhibition or other means
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**Name and mailing address of the ISA/KR**

International Application Division
Korean Intellectual Property Office
189 Cheongna-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea

Facsimile No. +82-42-472-7140

**Authorized officer**

BYUN, Sung Cheal

Telephone No. +82-42-481-8262

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