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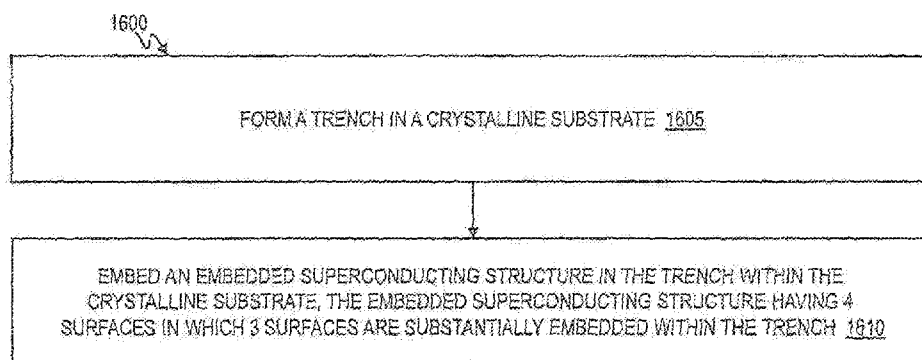
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FIG. 16



(57) Abstract: A technique relates to a superconducting electronic device. A crystalline substrate (105) has a trench (110). An embedded superconducting structure (205) is embedded in the trench (110) within the crystalline substrate (105). The embedded superconducting structure (205) has 4 surfaces in which 3 surfaces are substantially embedded within the trench (110), 3 sides are not exposed to oxygen, and 3 sides are not oxidized. A nonlinear superconducting element (350) may be formed on the embedded superconducting structure (205), and a second superconducting structure (705) may be formed on the nonlinear superconducting element (350).

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SUPERCONDUCTING ELECTRONIC INTEGRATED CIRCUIT

TECHNICAL FIELD

[0001] The present invention relates to superconducting technology, and more specifically, to superconducting electronic integrated circuits.

BACKGROUND

[0002] In one approach called circuit quantum electrodynamics, quantum computing employs active superconducting devices called qubits to manipulate and store quantum information, and resonators (e.g., as a two-dimensional (2D) planar waveguide or as a three-dimensional (3D) microwave cavity) to read out and facilitate interaction among qubits. Each superconducting qubit comprises one or more Josephson junctions shunted by capacitors in parallel with the junctions. The qubits are capacitively coupled to 2D or 3D microwave cavities. The energy associated with the qubit resides in the electromagnetic fields around the Josephson junction and especially in the vicinity of relatively larger shunt capacitance structures. To date, a major focus has been on improving lifetimes of the qubits in order to allow calculations (i.e., manipulation and readout) to take place before the information is lost to decoherence of the qubits. Currently, superconducting qubit coherence times can be as high as 100 microseconds, and efforts are being made to increase the coherence times. One area of research with respect to increasing coherence times is focused on eliminating lossy materials from areas of relatively high electromagnetic field energy density such as in the vicinity of sharp corners and edges of the thin films of which the qubits are comprised. Such materials in proximity to the qubit can include imperfections that support defects known as two-level systems (TLSs).

[0003] Therefore, there is a need in the art to address the aforementioned problem.

SUMMARY

[0004] Viewed from a first aspect the present invention provides a superconducting device comprising: a crystalline substrate; and an embedded superconducting structure embedded in a trench within the crystalline substrate, the embedded superconducting structure including a superconducting metal having 4 surfaces in which 3 surfaces are substantially embedded within the trench.

[0005] Viewed from a further aspect the present invention provides a method of forming a superconducting device, the method comprising: forming a trench in a crystalline substrate; and embedding an embedded superconducting structure in the trench within the crystalline substrate through a damascene type process, the embedded superconducting structure having 4 surfaces in which 3 surfaces are substantially embedded within the trench.

[0006] Viewed from a further aspect the present invention provides a superconducting device comprising: a first embedded superconducting structure embedded in a first trench within a crystalline substrate, the first embedded superconducting structure having 4 surfaces in which 3 surfaces are substantially embedded within the first trench; a second embedded superconducting structure embedded in a second trench within the crystalline substrate, the second embedded superconducting structure having 4 surfaces in which 3 surfaces are substantially embedded within the second trench; and a superconducting nonlinear element formed on at least a portion of the first embedded superconducting structure and at least a portion of the second embedded superconducting structure.

[0007] According to one or more embodiments, a superconducting device is provided. The superconducting device includes a crystalline substrate and an embedded superconducting structure embedded in a trench within the crystalline substrate. The embedded superconducting structure including a superconducting metal having 4 surfaces in which 3 surfaces are substantially embedded within the trench.

[0008] According to one or more embodiments, a superconducting device is provided. The superconducting device includes a bottom superconducting structure is embedded in a trench within a crystalline substrate, and the bottom superconducting structure has bottom surfaces substantially embedded within the trench. A superconducting nonlinear element is formed on top of the bottom superconducting structure. A top superconducting structure is formed on top of the superconducting nonlinear element.

[0009] According to one or more embodiments, a method of forming a superconducting device is provided. The method includes forming a trench in a crystalline substrate through a damascene type process and embedding an embedded superconducting structure in the trench within the crystalline substrate. The embedded superconducting structure has 4 surfaces in which 3 surfaces are substantially embedded within the trench.

[0010] According to one or more embodiments, a method of forming a superconducting device is provided. The method includes embedding a bottom superconducting structure in a trench within a crystalline substrate. The bottom superconducting structure has bottom surfaces substantially embedded within the trench. The method includes provides a superconducting nonlinear element formed on the bottom superconducting structure and providing a top superconducting structure formed on top of the superconducting nonlinear element.

[0011] According to one or more embodiments, a superconducting device is provided. The superconducting device includes a first embedded superconducting structure embedded in a first trench within the crystalline substrate. The first embedded superconducting structure having 4 surfaces in which 3 surfaces are substantially embedded within the first trench. The superconducting device includes a second embedded superconducting structure embedded in a second trench within the crystalline substrate. The second embedded superconducting structure has 4 surfaces in which 3 surfaces are substantially embedded within the second trench. Also, the superconducting device includes a superconducting nonlinear element formed on at least a portion of the first embedded superconducting structure and at least a portion of the second embedded superconducting structure.

[0012] According to one or more embodiments, a superconducting device is provided. The superconducting device includes a crystalline substrate having a trench, a barrier layer lining the trench, and an embedded superconducting structure embedded in the trench on the barrier layer within the crystalline substrate. The embedded superconducting structure includes a superconducting metal having 4 surfaces in which 3 surfaces are substantially embedded within the trench. Materials forming a combination of the barrier layer and the embedded superconducting structure are selected from the group consisting of (i) an AlN barrier layer and an Al embedded superconducting structure, (ii) a TaN barrier layer and a Ta embedded superconducting structure, and (iii) a Nb barrier layer and a Nb embedded superconducting structure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Embodiments of the present invention will now be described, by way of example only, with reference to the accompanying drawings in which:

FIG. 1 is a cross-sectional view of an electronic circuit depicting trench formation according to one or more embodiments.

FIG. 2 is a cross-sectional view of the electronic circuit depicting formation of an inlaid/embedded superconducting interconnect according to one or more embodiments.

FIG. 3 is a cross-sectional view of the electronic circuit depicting deposition of a trilayer structure according to one or more embodiments.

FIG. 4 is a cross-sectional view of the electronic circuit depicting patterning and etching of the stack according to one or more embodiments.

FIG. 5 is a cross-sectional view of the electronic circuit depicting deposition of a barrier layer according to one or more embodiments.

FIG. 6 is a cross-sectional view of the electronic circuit depicting exposing the top of the hardmask layer according to one or more embodiments.

FIG. 7 is a cross-sectional view of the electronic circuit depicting formation of a top superconducting contact according to one or more embodiments.

FIG. 8 is a cross-sectional view of the electronic circuit depicting etching according to one or more embodiments.

FIG. 9 is a cross-sectional view of the electronic circuit depicting an example with a barrier layer formed in the trench according to one or more embodiments.

FIG. 10 is a cross-sectional view of the electronic circuit of a qubit according to one or more embodiments.

FIG. 11 is a transmission electron microscope (TEM) image of a cross-sectional view of an example embedded superconducting interconnect according to one or more embodiments.

FIG. 12 is a top view of an embedded superconducting interconnect illustrating an example geometric shape according to one or more embodiments.

FIG. 13 is a top view of an embedded superconducting interconnect illustrating an example geometric shape according to one or more embodiments.

FIG. 14 is a schematic of a one junction superconducting quantum interference device (SQUID) that can be formed via one or more embedded superconducting interconnects according to one or more embodiments.

FIG. 15 is a schematic of a two junction superconducting quantum interference device (SQUID) that can be formed via one or more embedded superconducting interconnects according to one or more embodiments.

FIG. 16 is a method of forming a superconducting device according to one or more embodiments.

FIG. 17 is a method of forming a superconducting device according to one or more embodiments.

FIG. 18 is a method of forming a superconducting device according to one or more embodiments.

DETAILED DESCRIPTION

[0014] Various embodiments are described herein with reference to the related drawings. Alternative embodiments may be devised without departing from the scope of this document. It is noted that various connections and positional relationships (e.g., over, below, adjacent, etc.) are set forth between elements in the following description and in the drawings. These connections and/or positional relationships, unless specified otherwise, may be direct or indirect, and are not intended to be limiting in this respect. Accordingly, a coupling of entities

may refer to either a direct or an indirect coupling, and a positional relationship between entities may be a direct or indirect positional relationship. As an example of an indirect positional relationship, references to forming layer "A" over layer "B" include situations in which one or more intermediate layers (e.g., layer "C") is between layer "A" and layer "B" as long as the relevant characteristics and functionalities of layer "A" and layer "B" are not substantially changed by the intermediate layer(s).

[0015] Superconducting inlaid interconnects have been discussed in the state-of-the-art. For example, US 6482656 discusses a semiconductor device including a damascene superconducting interconnect, formed of a Ba—Cu—Ca—O superconducting material, in a dielectric. In the state-of-the-art, the superconducting structure described is located above the substrate, embedded in a deposited amorphous dielectric layer, and the superconductor is an oxide, specifically an alloy of oxygen with 3 metals.

[0016] However, according to one or more embodiments, the present superconducting structure is a metal or metal alloy without oxygen, is embedded in a trench within the crystalline substrate (not an amorphous dielectric), and is not located above the substrate in a deposited amorphous dielectric layer. Typically, the damascene process, well-known in the field of microelectronics fabrication, may be used to create such embedded superconducting structures. But unlike typical (normal conductor) applications where the conductor is embedded in a non-crystalline dielectric or insulating material, such as an amorphous glass, the present invention embeds the superconductor in a crystalline substrate. The fundamental advantages are twofold. First, a high-quality crystalline substrate may possess a significantly lower density of TLS-type defects when cooled to cryogenic temperatures, compared to a typical amorphous glass insulator or other noncrystalline insulator. Second, the damascene process enables the embedding of metals into the etched crystalline trenches in a vacuum deposition process, thereby eliminating formation of any metal native oxide on the 3 surfaces in contact with the crystalline substrate. This also substantially reduces sources of TLS losses.

[0017] Superconducting qubits have been discussed in the literature starting in about 2000. State-of-the-art qubits have exposed surfaces, and are susceptible to drift and degraded

performance due to chemical changes at the exposed interfaces. State-of-the-art qubits include a resonator and capacitors, both having 4 surfaces in which 3 of the 4 surfaces are exposed and open to chemical changes, and these chemical changes are due to processing damage, air oxidation, adsorbed contaminants, and possibly other effects. Exposed surfaces lead to qubit frequency changes and degradation of qubit performance. For resonators, exposed surfaces lead to a reduced quality factor (Q) and drift in the quality factor (Q) over time.

[0018] One or more embodiments provide for the elimination of exposed surfaces thereby rendering the qubit or resonator more stable over time. One or more embodiments provide qubits and resonant signal lines (embedded interconnects) in which only 1 of the 4 surfaces is exposed. For example, embodiments are configured to provide qubits and resonant signal lines in which the total surface area is more stable and in which 3 of the 4 surfaces are prevented from any chemical change during manufacture and use.

[0019] Electrical structures in direct contact with the resonant signal lines (waveguides) have the same requirement for stable operation. Accordingly, embodiments are configured to eliminate chemical changes due to integration/fabrication and due to air oxidation or moisture ingress at the exposed interfaces. One or more embodiments provide nonlinear electrical elements that are encapsulated (thus more stable and prevented from any chemical change during manufacture and use), as compared to state-of-the-art nonlinear elements.

[0020] Now, turning to the figures, FIGS. 1-9 illustrate fabrication processes of forming an electronic circuit according to one or more embodiments. The electronic circuits include one or more inlaid superconducting interconnects as discussed further herein.

FIG. 1 is a cross-sectional view of an electronic circuit 100 depicting trench formation according to one or more embodiments. One or more trenches 110 may be formed in a crystalline substrate 105. The trench 110 extends in the z-axis and is in part of the damascene fabrication to form inlaid superconductor interconnects.

[0021] The crystalline substrate 105 is a crystalline material. A crystalline substrate has a repeating structure, in which the distance between atoms is regular and uniform, and the crystalline substrate is free of impurity atoms; the top surface has been polished to produce a smooth surface with low roughness. The substrate 105 may be crystalline silicon (Si), sapphire (Al_2O_3), silicon carbide (SiC), boron nitride (BN), aluminum nitride (AlN), gallium arsenide (GaAs), magnesium oxide (MgO), and/or other crystalline wafer-type material which is an electrical insulator at cryogenic temperatures. All of the above properties of the crystalline substrate are readily available for the example of crystalline Si wafers. In another implementation, other crystalline materials may be utilized as the crystalline substrate 105. Again, normal damascene conductors are typically embedded in non-crystalline insulators at room temperature, such as amorphous glass or polymer materials.

[0022] FIG. 2 is a cross-sectional view of the electronic circuit 100 depicting formation of the inlaid superconducting interconnect according to one or more embodiments. A superconducting metal that forms the superconducting interconnect 205 is formed in the trench 110. The damascene method may be utilized to form the superconducting metal interconnect 205.

[0023] The superconducting interconnect 205 is embedded directly into the crystalline substrate 105. The top surface of the electronic circuit 100 is planarized to a smooth surface, for example, by chemical mechanical polishing/planarization (CMP), and this forms a superconducting metal interconnect with a top surface having root mean square (RMS) roughness of less than 1 nm (and preferably, but not a necessity, less than 0.3 nm) when measured by atomic force microscopy (AFM). The superconducting interconnect 205 may be designed to fit the desired function. In one implementation, the superconducting interconnect 205 may be a bottom contact, a connecting wire, a resonator (e.g., resonator wiring), capacitor plates, a transmission line, etc. It should be appreciated that multiple trenches 110 of different shapes and sizes can be formed in the crystalline substrate 105, such that superconducting interconnects 205 of different shapes and sizes and functions are correspondingly formed. The superconducting interconnect 205 can be utilized to connect to other embedded superconducting interconnects 205.

[0024] FIG. 3 is a cross-sectional view of the electronic circuit 100 depicting deposition of a superconducting trilayer tunnel junction structure 350 according to one or more embodiments. The trilayer tunnel junction structure 350 is formed on top of the embedded superconducting interconnect 205. The trilayer tunnel junction structure 350 includes a bottom superconducting layer 305 deposited on top of the crystalline substrate 105. The trilayer tunnel junction structure 350 includes a tunnel barrier layer 310 deposited on top of the bottom superconducting layer 305 and a top superconducting layer 315 deposited on top of the tunnel barrier layer 310. The trilayer tunnel junction structure 350 is a superconducting nonlinear element, which may be referred to as a Josephson Junction (JJ), a SQUID (superconducting quantum interference device), or, when in conjunction with additional interconnects and linear elements, a qubit (quantum binary digit).

[0025] A hardmask layer 320 is formed on top of the top superconducting layer 315 of the trilayer structure 350.

[0026] FIG. 4 is a cross-sectional view of the electronic circuit 100 depicting patterning and etching of the stack 360 according to one or more embodiments. The trilayer structure 350 and the hardmask layer 320 are etched into the stack 360 such that the stack 360 is (only) on top of the embedded superconducting interconnects 205 and no longer on top of the substrate 105.

[0027] The hardmask layer 320 is a superconducting material. Example materials of the hardmask layer 320 may include Nb, NbN, TiN, Ta, and TaN. Example materials of the tunnel barrier layer 310 may include Al_2O_3 , AlN, HfO_2 , and MgO.

[0028] Example materials of the bottom superconducting layer 305, the top superconducting layer 315, and the superconducting interconnect 205 may include tantalum (Ta), tantalum nitride (TaN), niobium (Nb), niobium-titanium (NbTi) alloys, titanium nitride (TiN), cobalt silicide (CoSi_2), niobium nitride (NbN), or aluminum (Al). The trilayer tunnel junction structure 350 is a nonlinear electronic element. The trilayer tunnel junction structure

350 may be a Josephson Junction (JJ) which enables distinct energy states when combined with capacitor elements as required for a qubit, as understood by one skilled in the art.

[0029] It is noted that the superconducting materials discussed herein operate according to superconducting principles at ultra-low temperatures, and the superconducting materials are not superconducting at room temperatures. For example, the superconducting materials discussed herein are metals or metal alloys superconducting at a predefined temperature, typically 1 – 20 Kelvin. Further, the superconducting materials discussed herein are not oxides that include barium (Ba), copper (Cu), or other metals in order to operate at temperatures above about 20 Kelvin (K).

[0030] FIG. 5 is a cross-sectional view of the electronic circuit 100 depicting deposition of an encapsulation layer according to one or more embodiments. An insulating encapsulation layer 505 is deposited over the top surface of the electronic circuit 100. The insulating encapsulation layer 505 may be referred to as a passivation layer.

[0031] The insulating encapsulation layer 505 covers the top of substrate 105, portions of the top of embedded superconducting interconnect 205, and the top of the hardmask layer 320. The insulating encapsulation layer 505 also covers the sides of the trilayer structure 350 and sides of the hardmask layer 320. The insulating encapsulation layer 505 (or passivation layer) may be an oxide or a nitride. In one implementation, the insulating encapsulation layer 505 may be silicon nitride. In other implementations, the insulating encapsulation layer 505 may be amorphous silicon or an insulating oxide, although an insulating nitride may function better.

[0032] FIG. 6 is a cross-sectional view of the electronic circuit 100 depicting exposing the top of the hardmask layer 320 according to one or more embodiments. Etching may be performed to remove the insulating encapsulation layer 505 from the top of the hardmask layer 320. The top surface of the hardmask layer 320 is exposed while sidewalls of the insulating encapsulation layer 505 remains on the sides of the trilayer structure 350 and the hardmask layer 320.

[0033] FIG. 7 is a cross-sectional view of the electronic circuit 100 depicting formation of a top superconducting contact according to one or more embodiments. A superconducting top contact 705 is formed on top of the hardmask layer 320. Also, the superconducting top contact 705 is formed on top of a portion of the insulating encapsulation layer 505. The electronic circuit 100 may form part of a qubit. FIG. 7 is one implementation of the electronic circuit 100. In FIG. 7, the insulating encapsulation layer 505 remains on the substrate 105.

[0034] FIG. 8 is a cross-sectional view of the electronic circuit 100 depicting etching according to one or more embodiments. Unlike FIG. 7, the insulating encapsulation layer 505 is etched to be aligned under the superconducting top contact 705. The electronic circuit 100 has the insulating encapsulation layer 505 removed on both sides of the superconducting top contact 705 to clear the field, such that the area is clear on the substrate 105. The structure shown in FIG. 8 may be part of a qubit or a SQUID.

[0035] FIG. 9 is a cross-sectional view of the electronic circuit 100 depicting an example with a barrier layer formed in the trench 110 according to one or more embodiments. In FIG. 9, a fabrication process has been performed such that a lining barrier layer 905 also referred to as a liner has been previously deposited in the trench 110. The lining barrier layer 905 may be an insulator or a conductor (or a superconductor). In one implementation, the lining barrier layer 905 may be the same material as the insulating encapsulation layer 505. The barrier layer 905 may be referred to as a liner, adhesion layer, or seed layer. Its function is to provide a diffusion barrier and adhesion layer between the superconducting metal 205 and the crystalline substrate 105, as well as a nucleation layer (or seed layer) for the subsequent deposition of the superconducting metal 205. While some insulating materials could provide these liner functions, they may also typically contain TLS lossy elements, and hence may not be preferable. In one implementation, a more preferable liner material 905 (but not a necessity) would be a metal conductor, and more preferably (but not a necessity) a superconductor. Due to ease of processing, a metal nitride of the same superconducting interconnect metal may be the most preferable (but not a necessity) as the liner material 905 in one implementation. The lining barrier layer 905/embedded superconductor 205 then forms a bilayer superconducting system, and examples materials are AlN/Al, TaN/Ta and NbN/Nb.

[0036] Further discussion is provided regarding passivation layers which are insulating encapsulation layer 505 and/or lining barrier layer 905. The insulating encapsulation layer 505 and/or the lining barrier layer 905 may be deposited by PVD, chemical vapor deposition (CVD), low pressure chemical vapor deposition (LPCVD), plasma-enhanced chemical vapor deposition PECVD, atomic layer deposition (ALD), plasma-enhanced atomic layer deposition (PEALD) depending on temperature limits. The silicon surface passivation of the silicon substrate 105 via the insulating encapsulation layer 505 may improve coherence of the qubit (i.e., the electronic circuit 100), or it may degrade coherence by TLS interactions. Additionally, the silicon damascene trench liner which is barrier layer 905 may improve or degrade coherence of the qubit (i.e., the electronic circuit 100), depending on its material properties.

[0037] As a trilayer encapsulant, the insulating encapsulation layer 505 wraps around the trilayer tunnel junction structure 350, such that the top of the trilayer structure 350 is covered/protected by the superconducting top contact 705 and the bottom of the trilayer structure 350 is on top of and/or protected by the embedded superconducting interconnect 205 (which may be a bottom contact and/or microwave resonator connected to the trilayer structure 350). The insulating encapsulation layer 505 is hermetic to H₂O (water), O₂ (oxygen), and possibly also, but not necessarily, H₂ (hydrogen), as well as typical aqueous and solvent-based cleaning chemicals. This last property allows the use of cleaning chemicals to remove lossy residues and oxides from the superconductor exposed surfaces, thereby improving coherence, without damaging any components of the trilayer tunnel junction structure 350.

[0038] FIG. 10 is a cross-sectional view of the electronic circuit 1000 of another qubit structure according to one or more embodiments. The electronic circuit 1000 of the qubit is made with damascene capacitor plates and a liftoff style Josephson junction (JJ). The electronic circuit 1000 in FIG. 10 includes features of the electronic circuit 100 and techniques used to fabricate the electronic circuit 100 as understood by one skilled in the art.

[0039] The electronic circuit 1000 includes the crystalline substrate 105 and embedded superconducting interconnects 205A and 205B, which were formed, for example, in two trenches 110. In FIG. 10, the superconducting interconnects are embedded superconducting

capacitor plates 205A and 205B. As discussed above, example materials of the embedded superconducting capacitor plates 205A and 205 may include tantalum (Ta), tantalum nitride (TaN), niobium (Nb), niobium-titanium (NbTi) alloys, titanium nitride (TiN), cobalt silicide (CoSi₂), niobium nitride (NbN), aluminum (Al). The embedded capacitor plates 205A and 205B are embedded in the crystalline substrate 105. The top surfaces of the embedded capacitor plates 205A and 205B and the crystalline substrate 105 form a level plane. The top surfaces of the embedded capacitor plates 205A and 205B may routinely have an RMS roughness by AFM of < 1 nm, and more particularly < 0.3 nm.

[0040] Between the two embedded superconducting capacitor plates 205A and 205B is a region 1005 of flat crystalline substrate where there is no topography, and this flat substrate region 1005 is particularly suited to locate the nonlinear junction. Accordingly, to form the trilayer structure 350, techniques known in the art are used, specifically the bottom superconducting layer 305 is deposited on top of the crystalline substrate 105 at the flat substrate region 1005 and on top of the embedded superconducting capacitor plate 205A. The tunnel barrier layer 310 is formed on top of the bottom superconducting layer 305. In an embodiment, the tunnel barrier layer 310 is formed by oxidation of a thin portion of the bottom superconducting layer 305. The top superconducting layer 315 is formed on top of the tunnel barrier layer 310, on top of part of the flat substrate region 1005, and on top of part of the embedded superconducting capacitor plate 205B.

[0041] The bottom superconducting layer 305 is connected to the first superconducting capacitor plate 205A. In one implementation, the tunnel barrier (oxide) layer 310 may be formed by oxidation of the bottom superconducting layer 305, with no exposure to the air. The top superconducting layer 315 is connected to the second superconducting capacitor plate 205B. The area of the nonlinear junction is represented by 1010, and this non-linear junction 1010 is defined by the area of overlap of the top superconducting layer 315 with the bottom superconducting layer 305. The area of the nonlinear junction 1010 and the tunnel barrier layer 310 thickness are the primary quantities that determine the resistance of the nonlinear junction 1010. The area of the nonlinear junction 1010 and the tunnel barrier layer 310 can be adjusted according to the qubit design, thus changing the resistance of the nonlinear junction 1010.

[0042] FIG. 11 is a transmission electron microscope (TEM) image 1100 of cross-sectional view of an example embedded superconducting interconnect according to one or more embodiments. The TEM image 1100 shows that the embedded superconducting interconnect is formed in a crystalline substrate. The example embedded superconducting interconnect is formed of niobium, and the example crystalline substrate is silicon.

[0043] It should be noted that while the structure in FIG. 11 shows a coplanar top surface shared by the superconducting metal and the surrounding crystalline substrate, it is also possible, by using processes which are known to those skilled in the art, to adjust the relative heights of the top surfaces of the superconductor relative to the crystalline substrate. For example, the superconductor top surface could be recessed (e.g. by selective wet or dry etching) slightly below the crystalline top surface. Conversely, the crystalline top surface could be recessed below the superconductor top surface. In this manner, the dielectric environment in which the supercurrent electric fields reside at the top corners of the superconductor can be adjusted from mainly “air” (or vacuum) to mainly that of the crystalline substrate. This adjustment may further optimize coherence by reducing losses or crosstalk to neighboring interconnects.

[0044] FIG. 12 is a top view of an embedded superconducting interconnect 1205 illustrating an example geometric shape according to one or more embodiments. The embedded superconducting interconnect 1205 is formed in the crystalline substrate 105, and they may have a coplanar top surface, or a non-coplanar top surface. The example superconducting interconnect 1205 may be an inductor and/or microwave resonator that connects to one or more other embedded superconducting interconnects, connects to one or more electronic circuits (e.g., one or more qubits), and connects to one or more wires.

[0045] FIG. 13 is a top view of an embedded superconducting interconnect 1305 illustrating an example geometric shape according to one or more embodiments. The embedded superconducting interconnect 1305 is formed in the crystalline substrate 105, and they have a coplanar top surface. The example superconducting interconnect 1305 may be an embedded wire or resonator that connects to one or more other embedded superconducting interconnects,

connects to one or more electronic circuits (e.g., one or more qubits), and connects to one or more wires.

[0046] The teachings of features and methods discussed herein can be formed into any desired circuit, and examples are illustrated below for illustration purposes and not limitation. FIG. 14 is a schematic of a one junction superconducting quantum interference device (SQUID) 1400 that can be formed via one or more embedded superconducting interconnects according to one or more embodiments. FIG. 15 is a schematic of a two junction superconducting quantum interference device (SQUID) 1500 that can be formed via one or more embedded superconducting interconnects according to one or more embodiments.

[0047] The “X” represents a Josephson junction (JJ) or nonlinear junction 1410. In one implementation, the nonlinear junction 1410 may be the trilayer structure 350 and/or formed using one of the techniques discussed in forming the trilayer structure 350. The solid lines 1420 are embedded superconducting metal interconnects, such as the embedded superconducting metal interconnects 205; examples are shown in FIGS. 12 and 13. The inductors 1405 are embedded superconducting interconnects having the desired shape, resistance, and inductance. The inductors 1405 are inlaid in the substrate, and examples are shown in FIGS. 12 and 13.

[0048] In another embodiment, the nonlinear junction may be a lift-off (shadow-mask) formed structure, as is known in the art. This type of non-linear junction was described above in reference to FIG. 10.

[0049] In FIG. 14, the one junction SQUID 1400 includes inductor 1405 connected to the nonlinear junction 1410.

[0050] In FIG. 15, the two junction SQUID 1500 includes two inductors 1405 connected in series and their opposite ends are respectively connected to nonlinear junctions 1410.

[0051] FIG. 16 is a flow chart 1600 of a method of forming a superconducting device (e.g., electronic device 100, 1000) according to one or more embodiments.

[0052] At block 1605, a trench 110 is formed in a crystalline substrate 105.

[0053] At block 1610, an embedded superconducting structure 205 is formed in the trench 110 within the crystalline substrate 105, where the embedded superconducting structure 205 includes a superconducting metal having 4 surfaces in which 3 surfaces are substantially embedded within the trench 110.

[0054] A conducting or insulating barrier layer 905 is attached to the 3 surfaces of the embedded superconducting structure 205 in the trench 110. The embedded superconducting structure 205 comprises a superconducting material/metal that is superconducting at a predefined temperature.

[0055] The 3 surfaces of the embedded superconducting structure 205 have no direct interface to air. The 3 surfaces of the embedded superconducting structure contain substantially no oxygen, meaning undetectable by standard micro-analytical methods. For example, typically less than 100 ppm of oxygen (O) would constitute “substantially no oxygen”. In a second example, “substantially no oxygen” means oxygen is not detected by the commonly used method called Energy Loss Spectroscopy (EELS) in a transmission electron microscope (TEM) image. A roughness of a top surface of the embedded superconducting structure 205 is about less than 1 nanometer. A roughness of a top surface of the embedded superconducting structure is about less than 0.5 nm. A roughness of a top surface of the embedded superconducting structure is about 0.3 nm.

[0056] The superconducting metal is selected from the group consisting of tantalum (Ta), tantalum nitride (TaN), niobium (Nb), niobium-titanium (NbTi) alloys, titanium nitride (TiN), cobalt silicide (CoSi₂), niobium nitride (NbN), aluminum (Al).

[0057] A superconducting nonlinear element 350 is electrically connected to the embedded superconducting structure 205. A top superconducting structure 320 (e.g. hard mask) is formed on a top surface of the superconducting nonlinear element 350. An insulating encapsulation layer 505 is formed on sides of the superconducting nonlinear element 350. The superconducting nonlinear element is selected from a group consisting of a liftoff Josephson junction and a trilayer Josephson junction.

[0058] The crystalline substrate is selected from a group consisting of silicon, sapphire, silicon carbide, boron nitride, aluminum nitride, gallium arsenide, and/or magnesium oxide. FIG. 17 is a flow chart 1700 of a method of forming a superconducting device (e.g., electronic devices 100, 1000) according to one or more embodiments.

[0059] At block 1705, a bottom superconducting structure 205 is embedded in a trench 110 within a crystalline substrate 105, where the bottom superconducting structure 205A has bottom surfaces substantially embedded within the trench 110.

[0060] At block 1710, a superconducting nonlinear element 350 is formed on the bottom superconducting structure 205.

[0061] At block 1715, a top superconducting structure 705 is formed on top of the superconducting nonlinear element 350.

[0062] An insulating encapsulation layer 505 is formed on sides of the superconducting nonlinear element 350. A conducting or insulating barrier layer 905 is attached to the bottom surfaces substantially embedded within the trench 110.

[0063] The bottom superconducting structure 205 includes a superconducting material that is superconducting at a predefined temperature. The bottom and top superconducting structures 205, 705 and the superconducting nonlinear element 350 together superconducting nonlinear

element form (function as) a qubit. The superconducting nonlinear element 350 may be a trilayer qubit, and the trilayer qubit includes an oxide layer 310 sandwiched between a bottom superconducting contact 305 and a top superconducting contact 315. The superconducting nonlinear element is selected from a group consisting of a liftoff Josephson junction and a trilayer Josephson junction.

[0064] A method of forming a superconducting device includes forming a trench in a crystalline substrate, and embedding an embedded superconducting structure in the trench within the crystalline substrate through a damascene type process. The embedded superconducting structure has 4 surfaces in which 3 surfaces are substantially embedded within the trench.

[0065] FIG. 18 is a flow chart 1800 of a method of forming a superconducting device (e.g., electronic device 1000) according to one or more embodiments. At block 1805, a first embedded superconducting structure 205A is embedded in a first trench 110A within the crystalline substrate 105, where the first embedded superconducting structure 205A has 4 surfaces in which 3 surfaces are substantially embedded within the first trench 110A. At block 1810, a second embedded superconducting structure 205B is embedded in a second trench 110B within the crystalline substrate 105, where the second embedded superconducting structure 205B has 4 surfaces in which 3 surfaces are substantially embedded within the second trench 110B. At block 1815, a superconducting nonlinear element 350 is formed on at least a portion of the first embedded superconducting structure 205A and at least a portion of the second embedded superconducting structure 205B.

[0066] Technical effects and benefits include improved semiconductor devices, including, for example, superconducting structures. Technical benefits provide a novel structure and method that provide for the elimination of exposed surfaces thereby rendering the qubit more stable over time. One or more embodiments provide qubits and/or resonant signal lines in which only 1 of the 4 surfaces is exposed. For example, embodiments are configured to provide qubits and resonant signal lines in which the total surface area is more stable and in which 3 of the 4 surfaces are prevented from any chemical change during manufacture and use.

[0067] It should be appreciated that the design for semiconductor devices may be included in or utilize features of an integrated circuit layout. An integrated circuit (IC) layout is also known as an IC layout, IC mask layout, or mask design. The integrated circuit layout is the representation of an integrated circuit in terms of planar geometric shapes which correspond to the patterns of metal, oxide, semiconductor layers, etc., that make up the components of the integrated circuit. Such an integrated circuit layout, including the layout of a semiconductor device, may be stored in a computer readable medium in preparation for fabrication as understood by one skilled in the art.

[0068] It will be noted that various microelectronic device fabrication methods may be utilized to fabricate the components/elements discussed herein as understood by one skilled in the art. In semiconductor device fabrication, the various processing steps fall into four general categories: deposition, removal, patterning, and modification of electrical properties. Deposition is any process that grows, coats, or otherwise transfers a material onto the wafer. Available technologies include physical vapor deposition (PVD), chemical vapor deposition (CVD), electrochemical deposition (ECD), molecular beam epitaxy (MBE) and more recently, atomic layer deposition (ALD) among others.

[0069] Removal is any process that removes material from the wafer: examples include etch processes (either wet or dry), and chemical-mechanical planarization (CMP), etc.

[0070] Patterning is the shaping or altering of deposited materials, and is generally accomplished by a combination of lithographic and etching steps. For example, in conventional lithography, the wafer is coated with a chemical called a photoresist; then, a machine called a stepper focuses, aligns, and moves a wafer to the next “step” or chip site, exposing select portions of the wafer below to short wavelength light; the exposed regions are washed away by a developer solution. After etching or other processing, the remaining photoresist is removed. Patterning may also include electron-beam lithography.

[0071] The descriptions of the various embodiments of the present invention have been presented for purposes of illustration, but are not intended to be exhaustive or limited to the embodiments disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope of the described embodiments. The terminology used herein was chosen to best explain the principles of the embodiments, the practical application or technical improvement over technologies found in the marketplace, or to enable others of ordinary skill in the art to understand the embodiments disclosed herein.

Clauses

1. A superconducting device comprising: a bottom superconducting structure embedded in a trench within a crystalline substrate, the bottom superconducting structure having bottom and sidewall surfaces substantially embedded within the trench; a superconducting nonlinear element formed on top of the bottom superconducting structure; and a top superconducting structure formed on top of the superconducting nonlinear element.
2. The superconducting device of clause 1, wherein an insulating encapsulation layer is formed on sides of the superconducting nonlinear element.
3. The superconducting device of clause 1, wherein a conducting or insulating barrier layer is attached to the bottom and sidewall surfaces substantially embedded within the trench.
4. The superconducting device of clause 1, wherein the bottom superconducting structure comprises a superconducting material that is superconducting at a predefined temperature.
5. The superconducting device of clause 1, wherein the bottom and top superconducting structures and the superconducting nonlinear element together form a qubit or a SQUID.
6. The superconducting device of clause 1, wherein the superconducting nonlinear element is selected from a group consisting of a liftoff Josephson junction and a trilayer Josephson junction.

7. The superconducting device of clause 1, wherein the bottom and top superconducting structures and the superconducting nonlinear element form a trilayer qubit or a SQUID; and wherein the trilayer qubit includes an oxide layer sandwiched between a bottom superconducting contact and a top superconducting contact.

8. A method of forming a superconducting device, the method comprising:
embedding a bottom superconducting structure in a trench within a crystalline substrate, the bottom superconducting structure having bottom surfaces substantially embedded within the trench;
providing a superconducting nonlinear element formed on the bottom superconducting structure; and
providing a top superconducting structure formed on top of the superconducting nonlinear element, wherein an encapsulation layer is formed on sides of the superconducting nonlinear element.

9. The method of clause 8, wherein a conducting or insulating barrier layer is attached to the bottom surfaces substantially embedded within the trench.

10. The method of clause 8, wherein the bottom superconducting structure comprises a superconducting material that is superconducting at a predefined temperature.

11. A superconducting device comprising:
a first embedded superconducting structure embedded in a first trench within a crystalline substrate, the first embedded superconducting structure having 4 surfaces in which 3 surfaces are substantially embedded within the first trench;
a second embedded superconducting structure embedded in a second trench within the crystalline substrate, the second embedded superconducting structure having 4 surfaces in which 3 surfaces are substantially embedded within the second trench; and
a superconducting nonlinear element formed on at least a portion of the first embedded superconducting structure and at least a portion of the second embedded superconducting structure.

12. A superconducting device comprising:
- a crystalline substrate having a trench;
 - a barrier layer lining the trench; and
 - an embedded superconducting structure embedded in the trench on the barrier layer
- within the crystalline substrate, the embedded superconducting structure including a superconducting metal having 4 surfaces in which 3 surfaces are substantially embedded within the trench;
- wherein materials forming a combination of the barrier layer and the embedded superconducting structure are selected from the group consisting of (i) an AlN barrier layer and an Al embedded superconducting structure, (ii) a TaN barrier layer and a Ta embedded superconducting structure, and (iii) a Nb barrier layer and a Nb embedded superconducting structure.

CLAIMS

1. A superconducting device comprising:
a crystalline substrate; and
an embedded superconducting structure embedded in a trench within the crystalline substrate, the embedded superconducting structure including a superconducting metal having 4 surfaces in which 3 surfaces are substantially embedded within the trench.
2. The superconducting device of claim 1, wherein an insulating or conducting barrier layer is attached to the 3 surfaces of the embedded superconducting structure in the trench; and wherein the superconducting metal is superconducting at a predefined temperature.
3. The superconducting device of either of the preceding claims, wherein the 3 surfaces of the embedded superconducting structure have no direct interface to air; and wherein the 3 surfaces of the embedded superconducting structure contain substantially no oxygen.
4. The superconducting device of any of the preceding claims, wherein a roughness of a top surface of the embedded superconducting structure is less than about 1 nanometer.
5. The superconducting device of any of the preceding claims, wherein a roughness of a top surface of the embedded superconducting structure is less than about 0.3 nm.
6. The superconducting device of any of the preceding claims, wherein the superconducting metal is selected from the group consisting of tantalum (Ta), tantalum nitride (TaN), niobium (Nb), niobium-titanium (NbTi) alloys, titanium nitride (TiN), cobalt silicide (CoSi₂), niobium nitride (NbN), aluminum (Al).
7. The superconducting device of any of the preceding claims, wherein a superconducting nonlinear element is electrically connected to the embedded superconducting structure.

8. The superconducting device of claim 7, wherein the superconducting nonlinear element is selected from a group consisting of a liftoff Josephson junction and a trilayer Josephson junction.
9. The superconducting device of either of claims 7 or 8, wherein a top superconducting structure is formed on a top surface of the superconducting nonlinear element.
10. The superconducting device of claim 9, wherein an insulating encapsulation layer is formed on sides of the superconducting nonlinear element.
11. The superconducting device of any of the preceding claims, wherein the crystalline substrate is selected from a group consisting of silicon, sapphire, silicon carbide, boron nitride, aluminum nitride, gallium arsenide, and magnesium oxide.
12. The superconducting device of any of the preceding claims, wherein the embedded superconducting structure comprises a superconducting material that is superconducting at a predefined temperature.
13. The superconducting device of any of claims 9 to 12, wherein the embedded and top superconducting structures and the superconducting nonlinear element together form a qubit or a SQUID.
14. The superconducting device of any of claims 9 to 13, wherein the embedded and top superconducting structures and the superconducting nonlinear element form a trilayer qubit or a SQUID; and
wherein the trilayer qubit includes an oxide layer sandwiched between a bottom superconducting contact and a top superconducting contact.
15. A superconducting device of any of claims 2 to 14, wherein materials forming a combination of the barrier layer and the embedded superconducting structure are selected from the group consisting of (i) an AlN barrier layer and an Al embedded superconducting structure,

(ii) a TaN barrier layer and a Ta embedded superconducting structure, and (iii) a Nb barrier layer and a Nb embedded superconducting structure.

16. A method of forming a superconducting device, the method comprising:
forming a trench in a crystalline substrate; and
embedding an embedded superconducting structure in the trench within the crystalline substrate through a damascene type process, the embedded superconducting structure having 4 surfaces in which 3 surfaces are substantially embedded within the trench.
17. The method of claim 16, wherein a conducting or insulating barrier layer is attached to the 3 surfaces of the embedded superconducting structure in the trench.
18. The method of either of claims 16 or 17, wherein the embedded superconducting structure comprises a superconducting material that is superconducting at a predefined temperature;
wherein the 3 surfaces of the embedded superconducting structure have no direct interface to air; and
wherein the 3 surfaces are not oxidized.
19. A method of any of claims 16 to 18, the method comprising:
providing a superconducting nonlinear element formed on the embedded superconducting structure; and
providing a top superconducting structure formed on top of the superconducting nonlinear element, wherein an encapsulation layer is formed on sides of the superconducting nonlinear element.
20. A superconducting device comprising:
a first embedded superconducting structure embedded in a first trench within a crystalline substrate, the first embedded superconducting structure having 4 surfaces in which 3 surfaces are substantially embedded within the first trench;

a second embedded superconducting structure embedded in a second trench within the crystalline substrate, the second embedded superconducting structure having 4 surfaces in which 3 surfaces are substantially embedded within the second trench; and

a superconducting nonlinear element formed on at least a portion of the first embedded superconducting structure and at least a portion of the second embedded superconducting structure.

FIG. 1

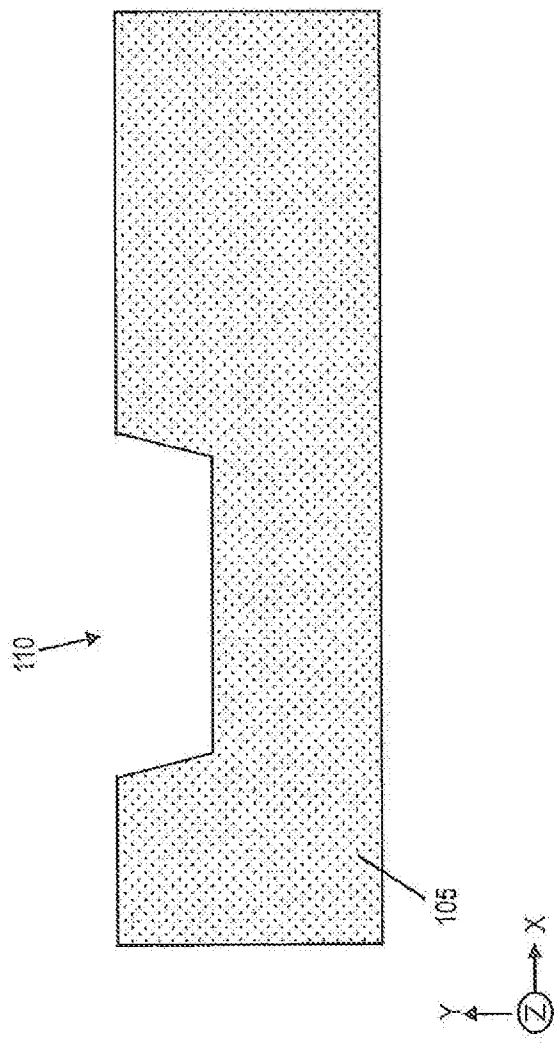


FIG. 2

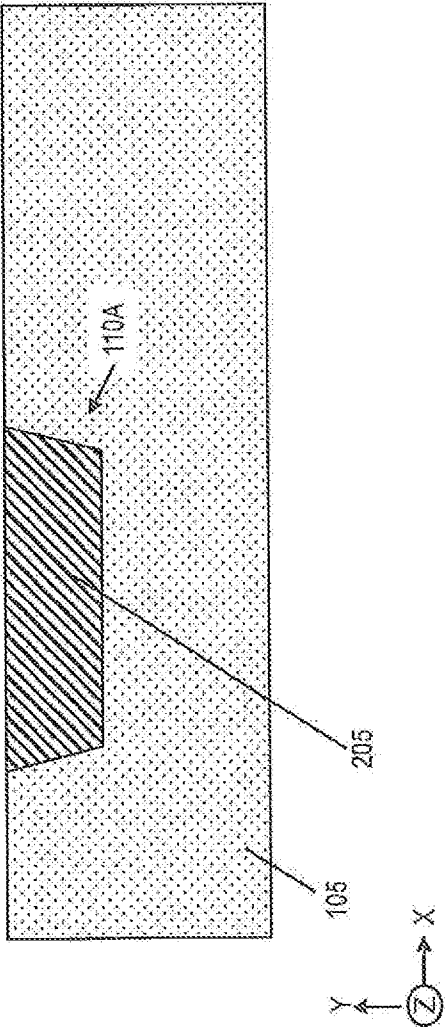


FIG. 3

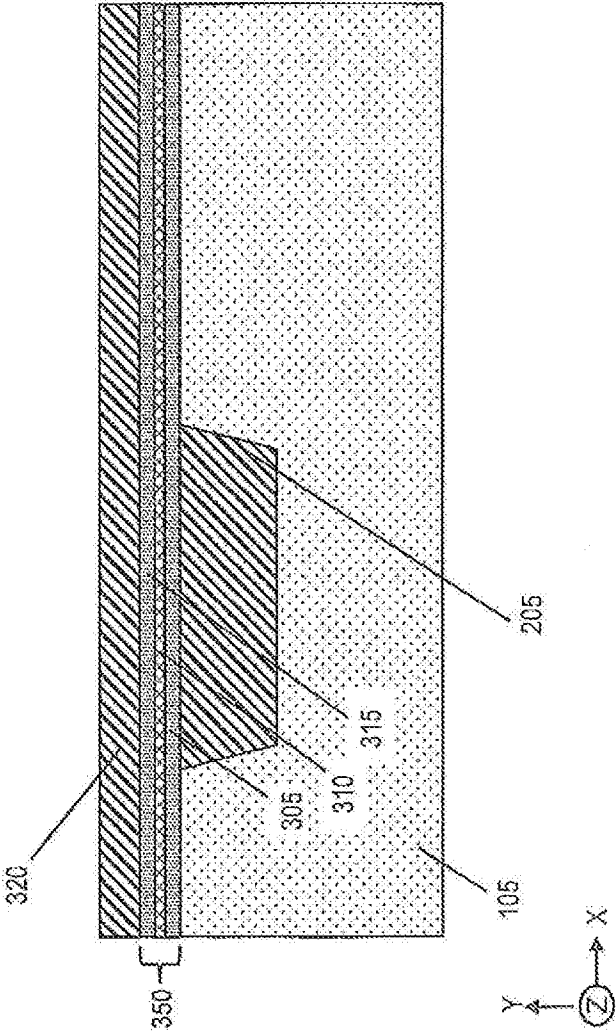


FIG. 4

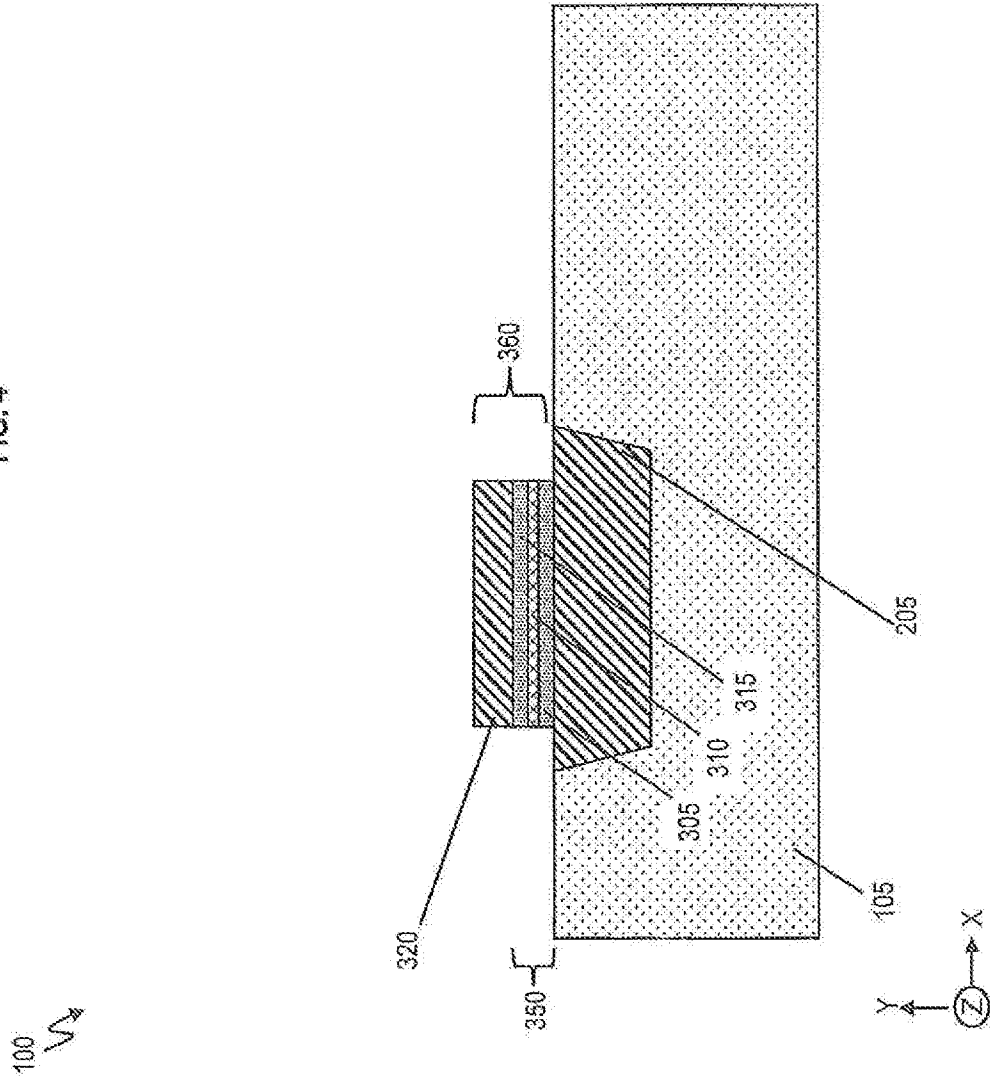


FIG. 5

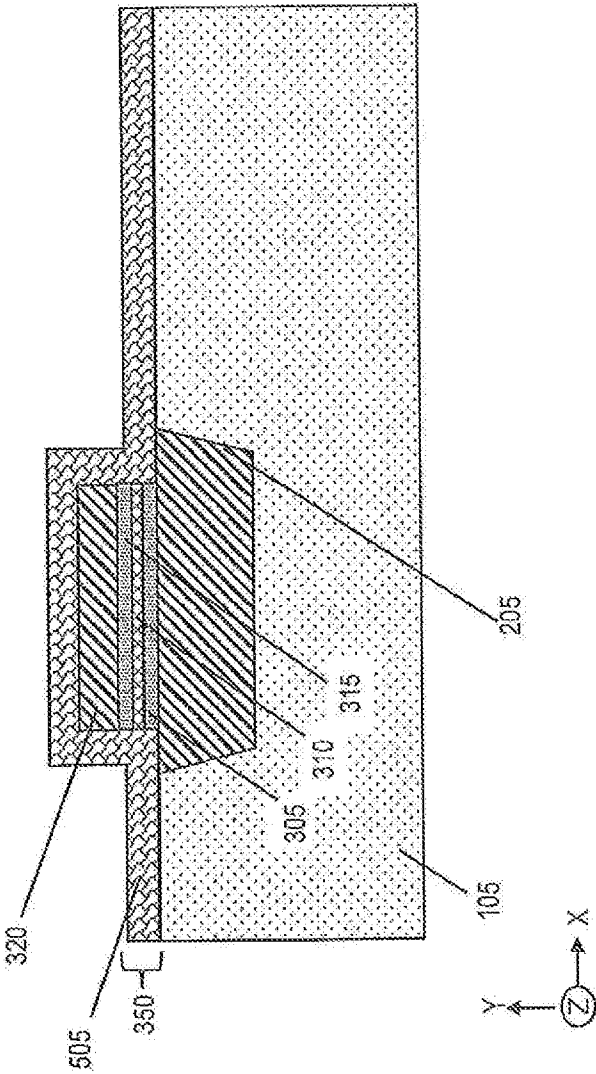


FIG. 6

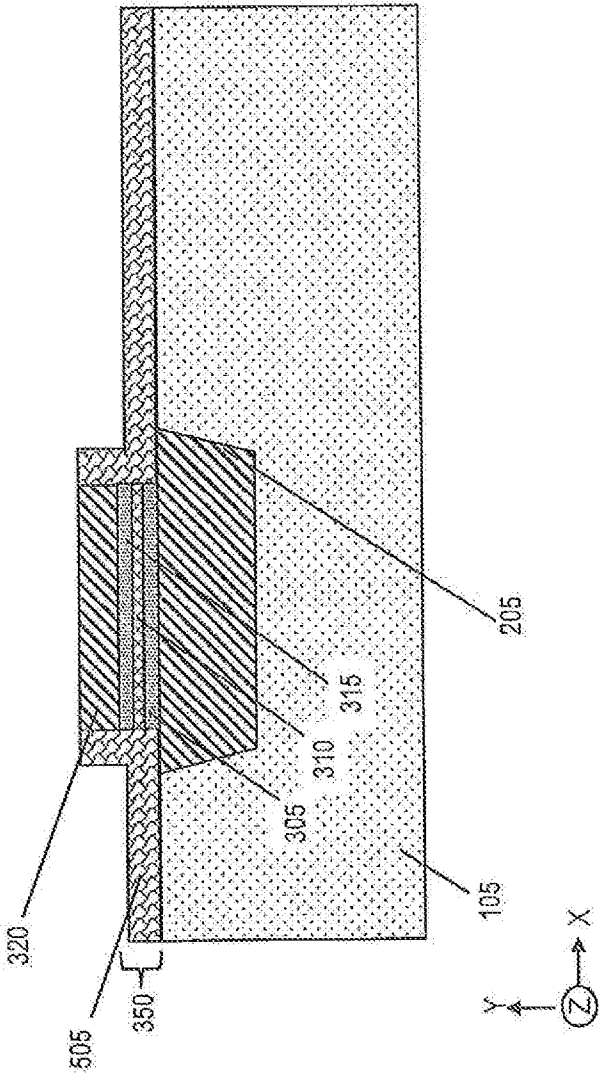


FIG. 7

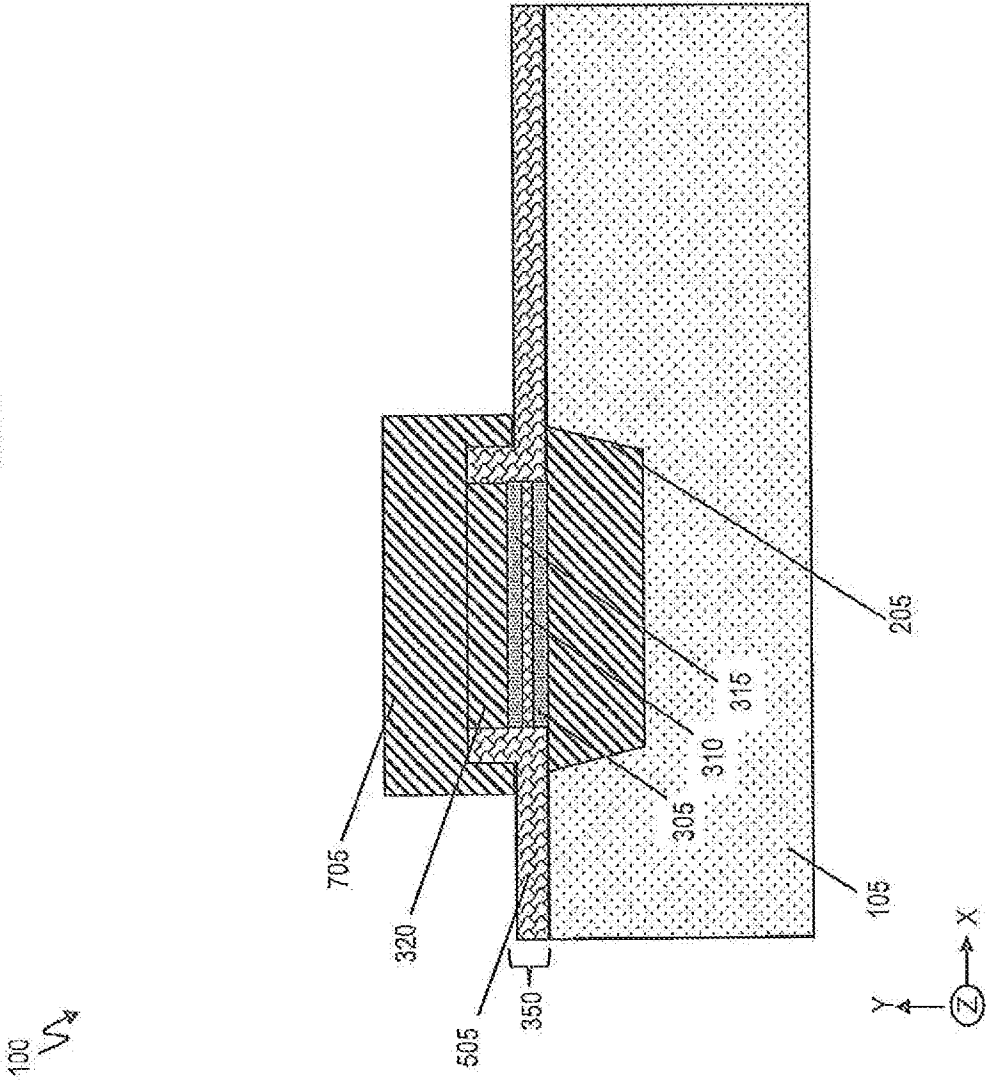


FIG. 8

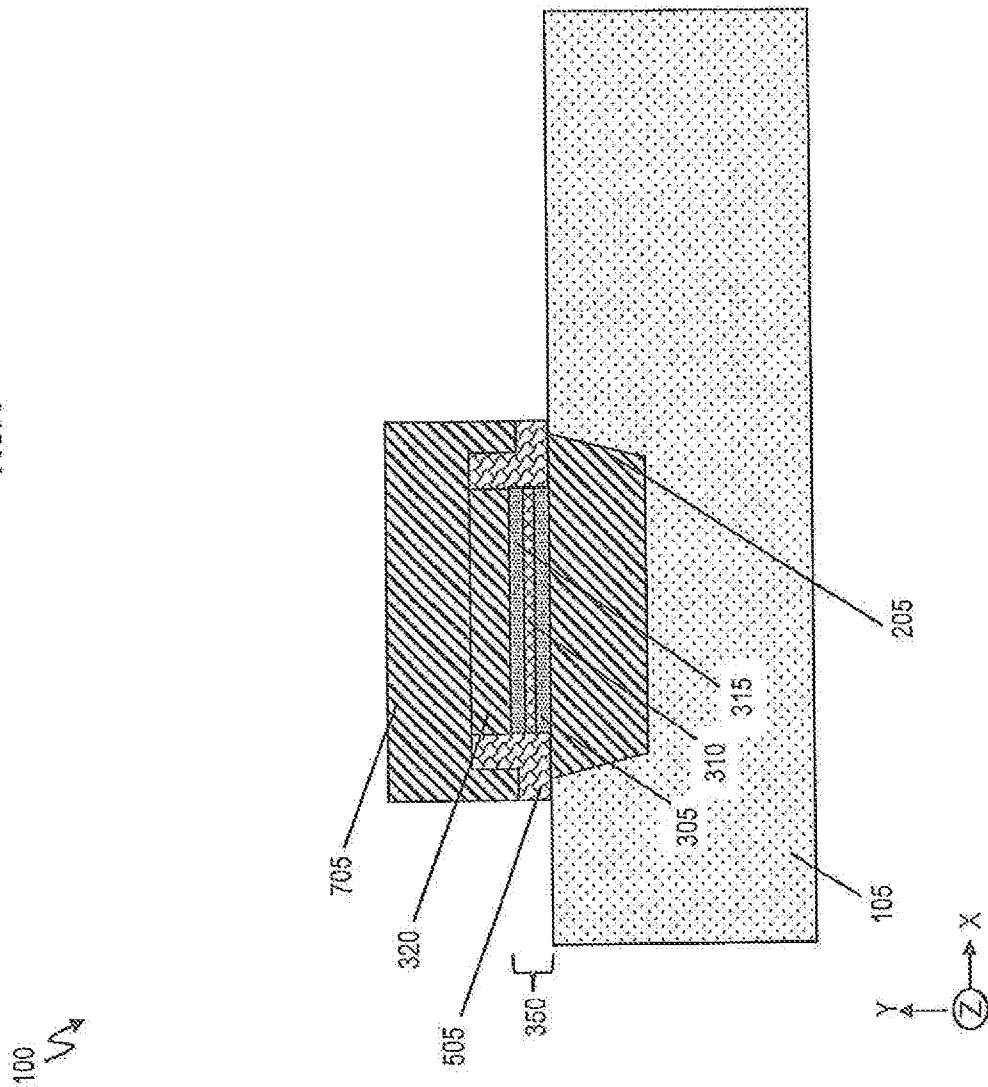
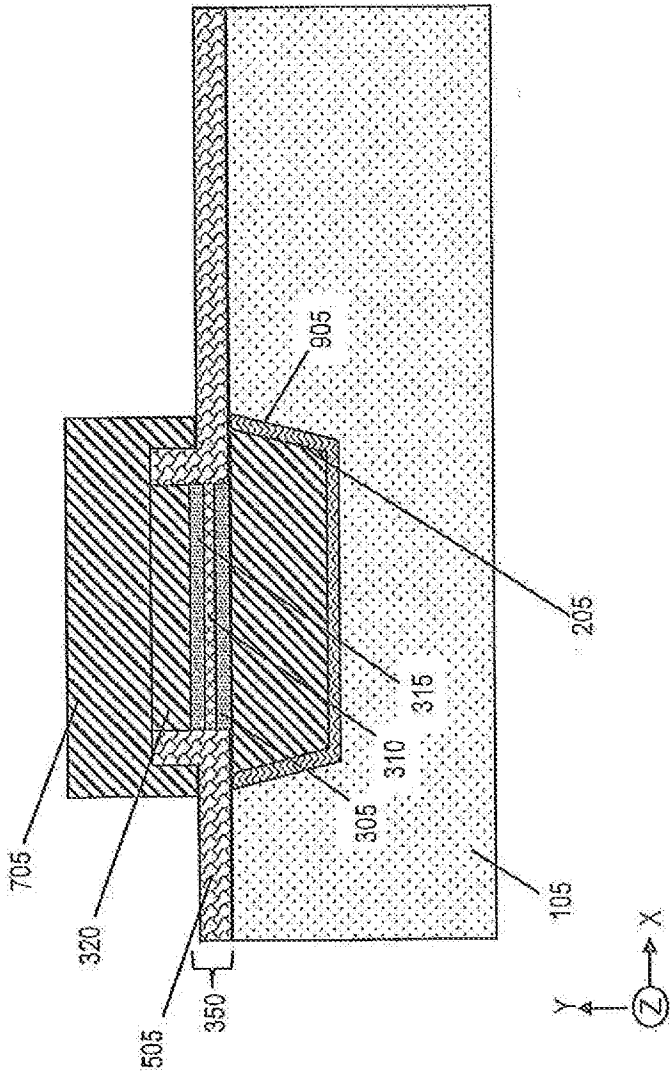


FIG. 9

100



Q. E. L.

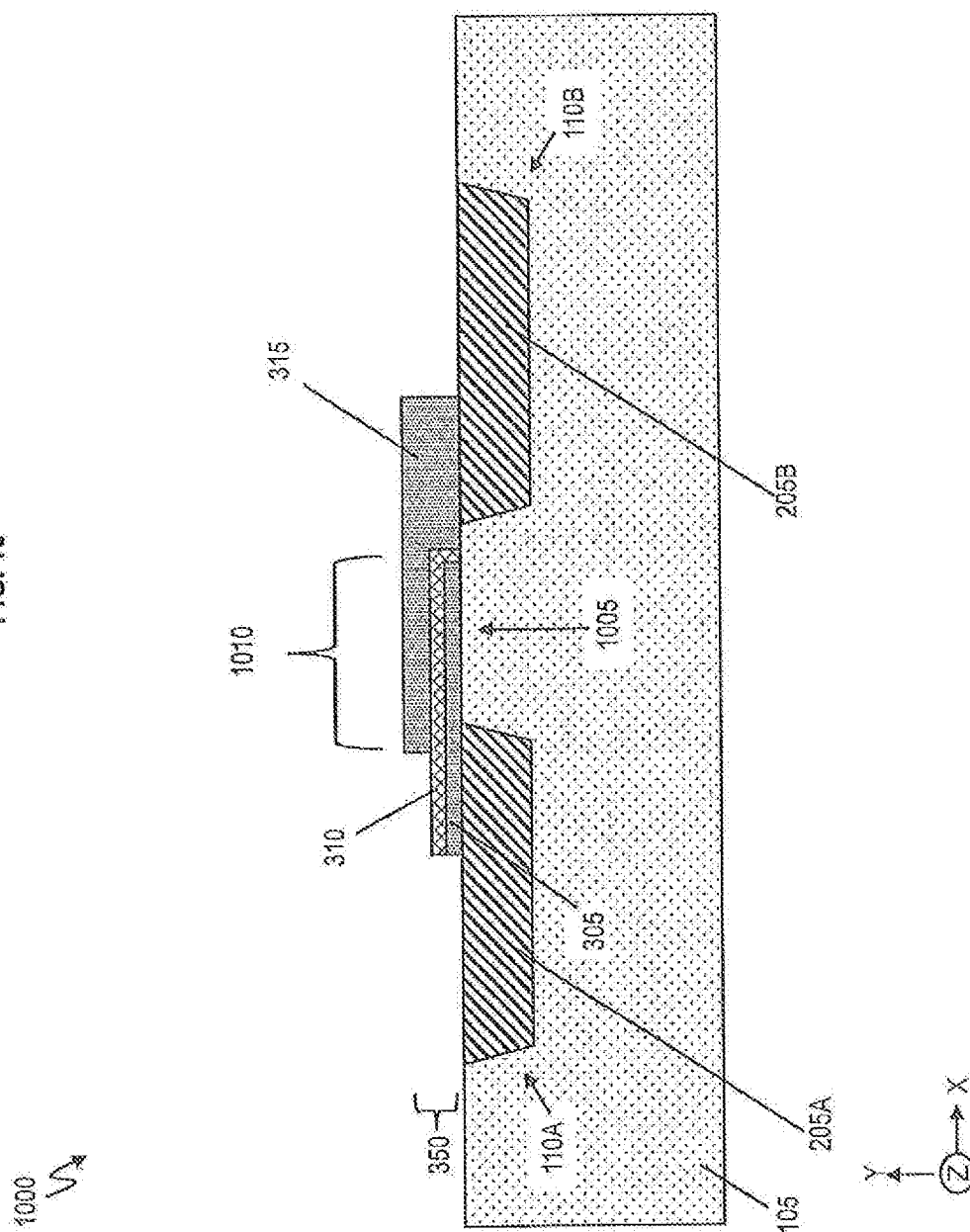


FIG. 11

1100

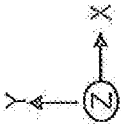
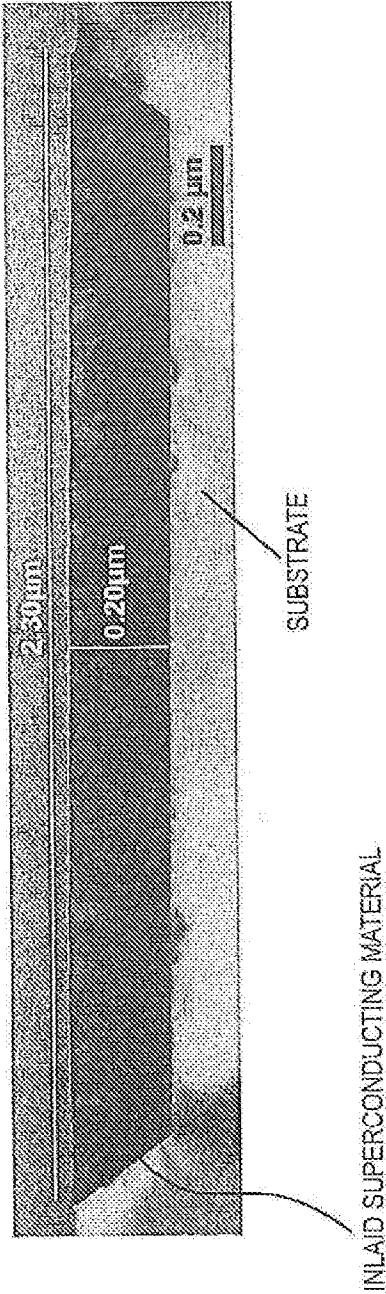


FIG. 13

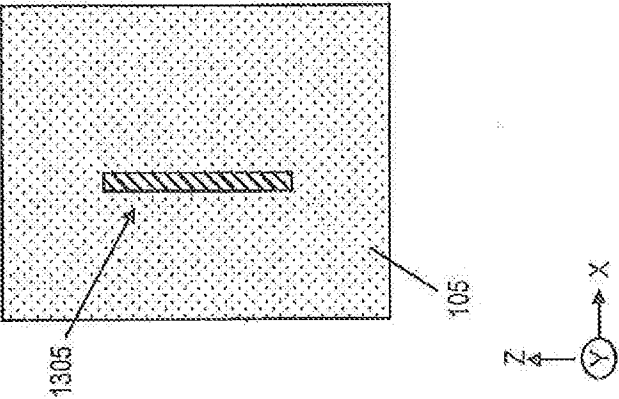
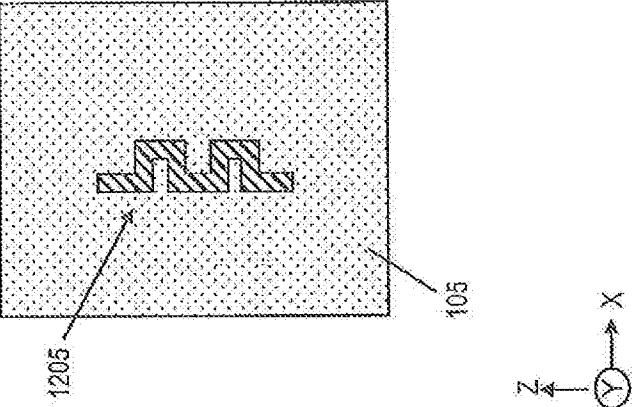


FIG. 12



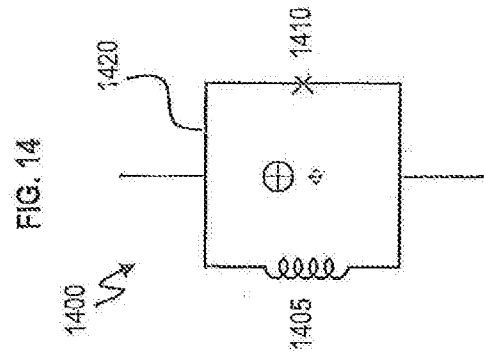
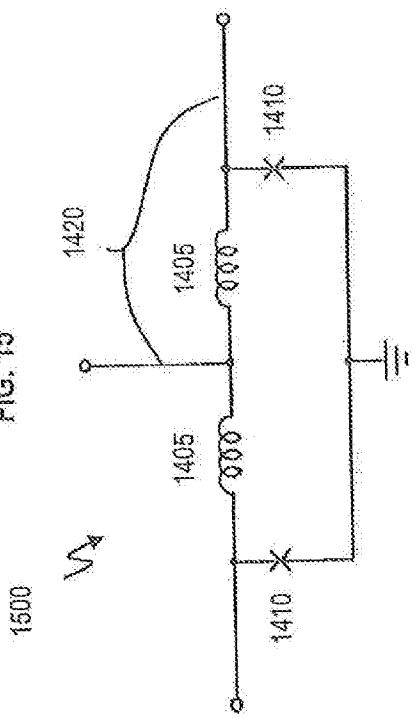
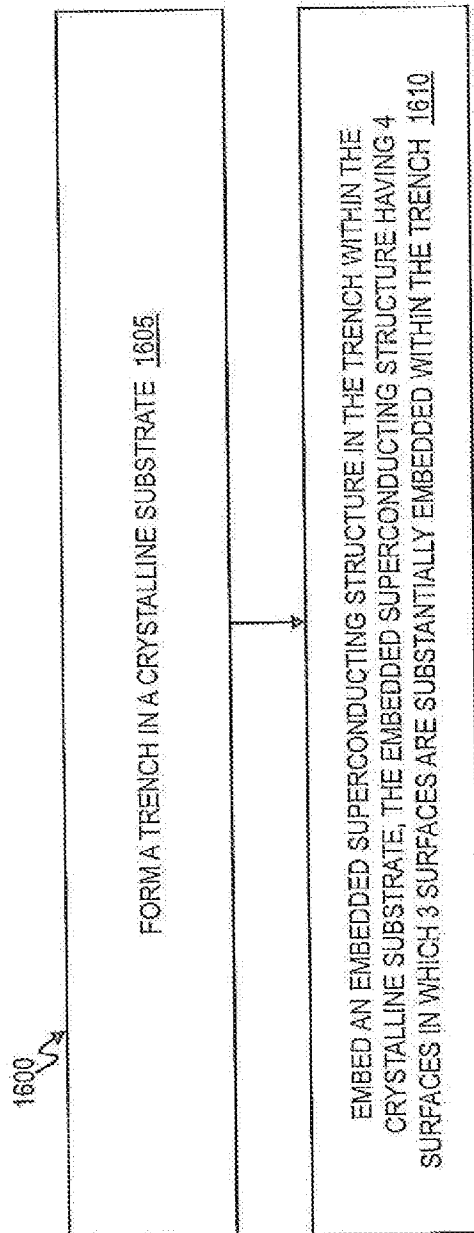


FIG. 15



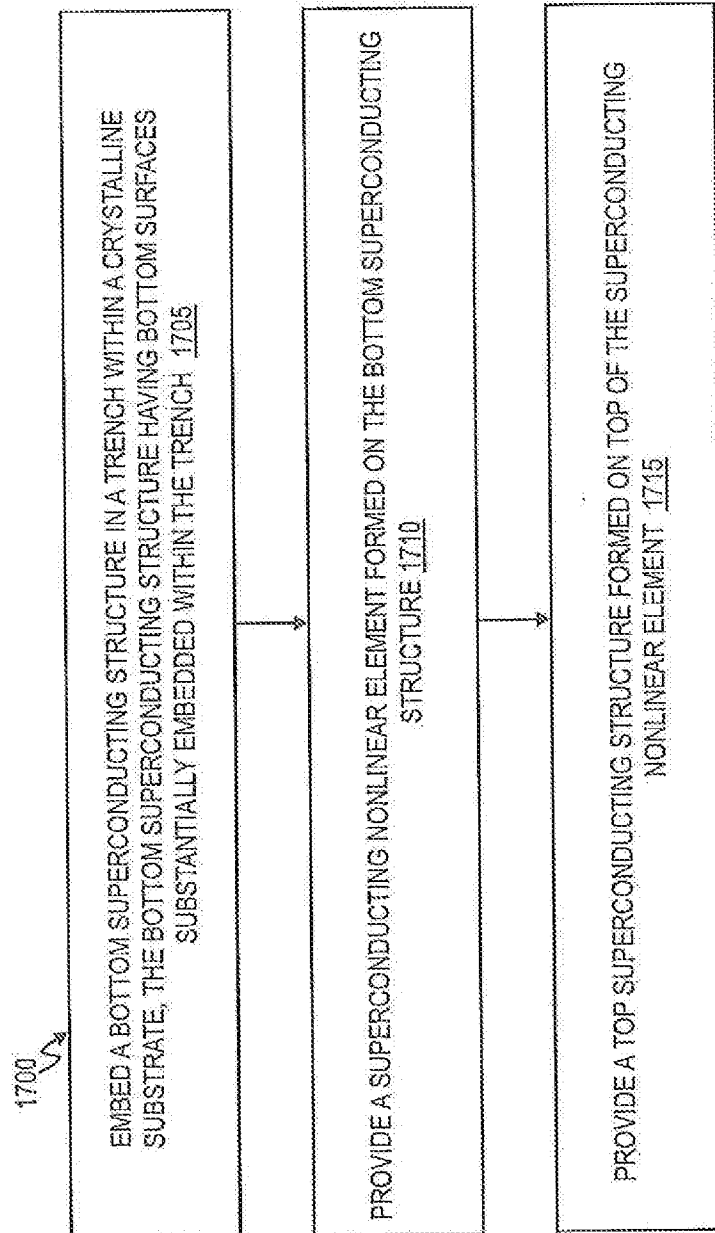
14/16

FIG. 16



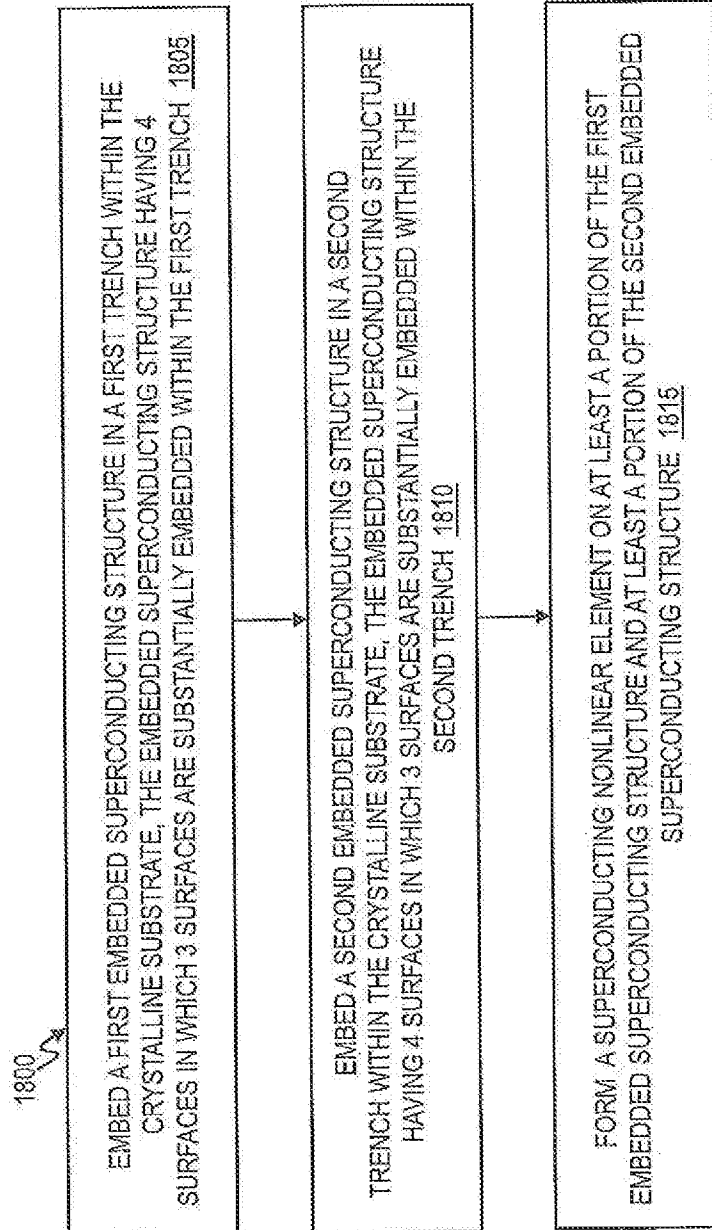
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FIG. 17



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FIG. 18



INTERNATIONAL SEARCH REPORT

International application No.

PCT/IB2017/054396

A. CLASSIFICATION OF SUBJECT MATTER

H01L 39/22(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, EPODOC, WPI, CNKI, IEEE: substrate, trench, groove, recess, concave, concavity, superconducting, embed, bury, buried, tunnel, junction, josephson, qubit, squid

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP S58125880 A (HITACHI LTD.) 27 July 1983 (1983-07-27) description, page 346, line 1 in the upper left column to line 9 in the lower right column, figure 1	1-20
A	CN 102334206 A (D-WAVE SYSTEMS INC.) 25 January 2012 (2012-01-25) the whole document	1-20
A	JP S61174782 A (AGENCY IND. SCIENCE TECHN.) 06 August 1986 (1986-08-06) the whole document	1-20
A	JP S63205975 A (AGENCY IND. SCIENCE TECHN.) 25 August 1988 (1988-08-25) the whole document	1-20

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

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“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

13 September 2017

Date of mailing of the international search report

27 September 2017

Name and mailing address of the ISA/CN

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/IB2017/054396

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				EP	3098865	A1	30 November 2016
				US	9490296	B2	08 November 2016
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