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(71) Applicant *(for all designated States except US)*: THOMSON CONSUMER ELECTRONICS S.A. [FR/FR]; 9, place des Vosges, La Défense 5, F-92400 Courbevoie (FR).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: COLLET, Eric [FR/FR]; 7, place Lamartine, F-67400 Illkirch (FR). KERDRANVAT, Michel [FR/FR]; 30, rue de la Fontaine, F-67870 Bischoffsheim (FR).

(74) Agent: WÖRDEMANN, Hermes; Deutsche Thomson-Brandt GmbH, Patent Dept., Göttinger Chaussee 76, D-30453 Hannover (DE).

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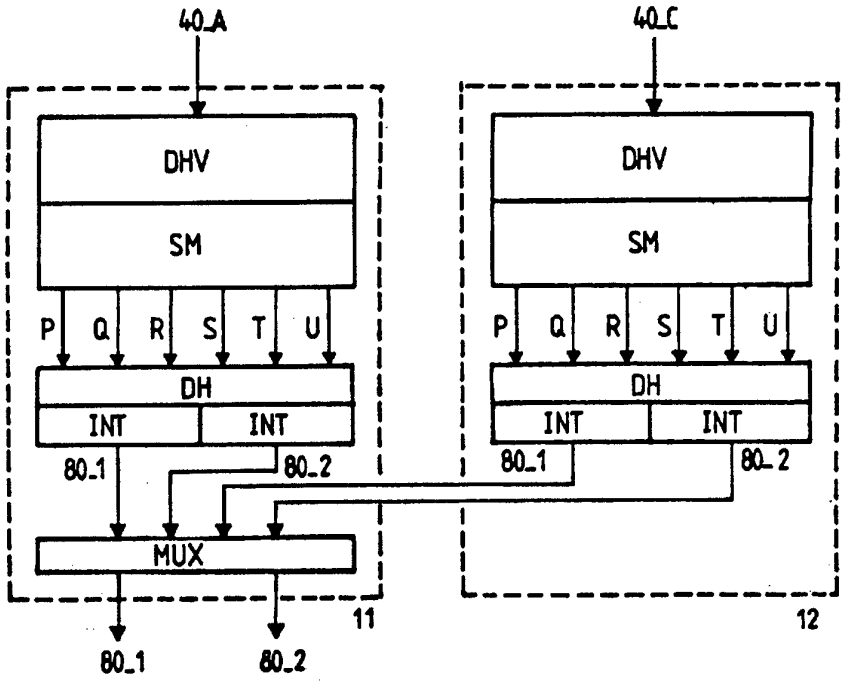
(57) Abstract

For motion compensated interpolation (MCI) with sub-pixel accuracy the missing pixels need to be generated or interpolated prior to the motion compensation. The required pixel values (P, Q, R, S) are stored using line and pixel delays (DHV). A switch matrix selects in response to a motion vector such stored pixels which are currently needed for the processing. In order to avoid sub-pixel MCI, the interpolation (INT) is carried out prior to the motion compensation. Thus, the input data rate of the motion compensation circuitry is twice then that of the interpolation circuitry. The resulting hardware complexity is high. The invention leads to a reduced amount of stored data for performing a sub-pixel MCI using a simple switch matrix (SM), only. A special arrangement of delays (DH) storing pixel values needed for the processing is used to extend the existing delay array (DHV). Because an increased number of pixels involved is used, an improved sub-pixel MCI is achieved. This is possible due to the fact that such delay extension does not affect significantly the decoded picture quality even if adjacent motion vectors do not match exactly to the current motion vector. The invention can be used in every system making use of MCI, especially in decoders of coding systems based on spatio-temporal subsampling and motion compensation. Motion compensation and interpolation are achieved simultaneously at the clock frequency of the input data stream.



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Method and Apparatus for motion compensated interpolation

The present invention relates to a method and to an apparatus for motion compensated interpolation.

Background

For motion compensated interpolation (MCI) with sub-pixel accuracy the missing pixels need to be generated or interpolated prior to the motion compensation. For the Barcelona Olympic Games THOMSON HDMAC receivers have been built. Such receivers fulfil the preliminary HDMAC specification of the BRD (bandwidth restoration decoder) chip set for the Olympic Receiver Project / Version 2.1, Philips.
The required pixel values are stored using line and pixel delays. A switch matrix selects such stored pixels which are currently needed for the processing. In order to avoid sub-pixel MCI, the interpolation is carried out prior to the motion compensation. Thus, the input data rate of the motion compensation circuitry is twice then that of the interpolation circuitry. The resulting hardware complexity is high.
Sub-pixel interpolation does mean interpolation of pixels located between available samples.

Invention

It is one object of the invention to disclose a method of combined motion compensation and interpolation having a sub-pixel precision, but using only a limited number of pixels accessed by the switch matrix. This object is reached by the method disclosed in claim 1.

It is a further object of the invention to disclose an apparatus which utilises the inventive method. This object is reached by the apparatus disclosed in claim 8.

The invention leads to a reduced amount of stored data for performing a sub-pixel MCI using a simple switch matrix, only. A special arrangement of delays storing pixel values needed for the processing is used to extend the existing delay array. Because an increased number of pixels involved is used, an improved sub-pixel MCI is achieved. This is possible due to the fact that such delay extension does not affect significantly the decoded picture quality even if adjacent motion vectors do not match exactly to the current motion vector. The invention can be used in every system making use of MCI, especially in decoders of coding systems based on spatio-temporal subsampling and motion compensation. Motion compensation and interpolation are achieved simultaneously at the clock frequency of the input data stream. Therefore, the amount of data to process and the resulting hardware complexity are lower than in the cited prior art. The switch matrix is connected to line and pixel delays storing a window of a frame (or field) at time t from which a MCI is achieved to build a frame (or field) at time (t+/-T) by random access depending on motion vectors. T is a multiple of the frame (field) period. The number of pixels extracted by the switch matrix at each clock period is limited by hardware complexity constraints.
The invention is based on the hypothesis that two consecutive sets of switch matrix outputs are juxtaposed or intersected. So, several consecutive sets of switch matrix outputs can be stored in order to carry out an interpolation using all available pixels. The hypothesis has been validated by investigating the behaviour on very critical source materials.
The invention can be used in every system using motion compensation. Especially, it is suited to coding/decoding systems based on spatio-temporal subsampling and motion compensation like HD-MAC.

In HDMAC this technique can be performed directly on sub-sampled fields. For each current pair of pixels (denoted 80-1 and 80-2) to be interpolated six samples come out of the switch matrix. In fact, only four samples are dedicated to the interpolation of one of these pixels, but two samples of the 2*4 samples are com-

mon. Therefore, only six switch matrix outputs are required. Due to the inventive delay extension at the output of the switch matrix the interpolation filter can use an input window of ten pixels for calculating an output pixel value (80_1 or 80_2). The vertical dimension of the interpolation filter is given by the number of different lines accessed by the switch matrix, e.g. three. The horizontal dimension is not limited by the switch matrix but depends only on the number of switch matrix output sets which are stored.
In the prior art the interpolation filter has a spread of pixels greater than the spread of pixels given by the switch matrix outputs. So the interpolation needs to be carried out prior to the switch matrix in order to reach the required accuracy. But this way of hardware implementation doubles the sample rate at the input of the switch matrix and requires a data de-multiplexing to maintain the input frequency of the interpolator.
The combination of interpolation and motion compensation maintains a low input frequency for the processing and optimises the required number of line delays which are very hardware consuming. This number is determined only by the range of motion compensation in vertical direction.
Advantageously, the invention can also be applied to every system which uses motion compensated interpolation for display rate upconversion.

The MPEG (motion pictures expert group) codec system uses motion compensation with motion vectors at half pixel accuracy. Consequently, sub-pixel motion compensated interpolation is required on an orthogonal grid (quincunx grid in HDMAC). As the way of achieving motion compensated interpolation is part of the MPEG standard none approximation at block border is allowed, because the encoded prediction error of a block is added to the motion compensation.

In principle, in the inventive method of motion compensated interpolation the output pixel values are interpolated from input pixel values located within a window which is related to the spatial and/or temporal location of the current output pixel,

wherein the pixel values required for said window are made available using delay means and switch matrix means, the outputs of which are currently connected in response to a motion vector to such of said delay means which currently deliver said input pixel values, and wherein each of the outputs of said switch matrix means pass through at minimum one further delay unit and said outputs of the switch matrix means and the outputs of said delay units are used to form an increased window for interpolating said output pixel values.

Advantageous additional embodiments of the inventive method are resulting from the respective dependent claims.

In principle the inventive apparatus is suited for motion compensated interpolation, wherein the output pixel values are interpolated from input pixel values located within a window which is related to the spatial and/or temporal location of the current output pixel and comprises:

- delay means which make available the pixel values required for said window;
- switch matrix means, the outputs of which are currently connected in response to a motion vector to such of said delay means which currently deliver said input pixel values;
- at minimum one delay unit at each switch matrix means output through which each of the outputs of the switch matrix means passes, wherein said outputs of the switch matrix means and the outputs of said delay units are used to form an increased window;
- interpolating means subsequent to said delay units for interpolating said output pixel values.

Advantageous additional embodiments of the inventive apparatus are resulting from the respective dependent claims.

Drawings

Preferred embodiments of the invention are described with reference to the accompanying drawings, which show in:

Fig. 1 block diagram of the inventive MCI;
Fig. 2 pixels used in the MCI;
Fig. 3 possible locations of motion vector displaced pixels within a quincunx sampling grid;
Fig. 4 horizontal and vertical delays in more detail;
Fig. 5 interpolation windows;
Fig. 6 interpolation scheme using the inventive delay arrangement;
Fig. 7 interpolation circuit;
Fig. 8 position of the interpolation windows within the sampling grid;
Fig. 9 windows at the input of the switch matrices;
Fig. 10 vertical position limitation tables for field 40_A;
Fig. 11 vertical position limitation tables for field 40_C;
Fig. 12 possible locations of motion vector displaced pixels within an orthogonal sampling grid.

Preferred embodiments

In the HDMAC HDTV system the luminance and chrominance pixels are processed on a block basis. Different processing modes are assigned to the block types depending on the amount of motion within the picture content of a block:

mode	*motion speed*
80ms	static or near static
40ms	medium
20ms	rapid

Data reduction is achieved by spatial and temporal subsampling and motion compensation. To each mode a specific subsampling pattern is assigned. In the 40ms mode for each second field motion compensation is used. Since the 40ms mode is statistically the most used in the HDMAC coding algorithm it is very important

to achieve a proper 40ms processing in the BRD. Without taking into account a compatibility improvement circuitry, the 40ms processing begins in a SSPC circuitry (Sub Sampling Pattern Conversion) which converts all the transmitted picture information (e.g. sub-sampled pixel values) into the 40ms sub sampling pattern. Due to a related reduction of the number of occupied field memories from five to three, some temporal commutations between the 40ms and the 80ms mode are not properly processed. This has a great influence on the motion compensated field because the motion compensation is symmetrical and can look into blocks which are not transmitted in the 40ms mode. Then the 40ms processing itself is carried out using interpolation in the odd fields and using motion compensation in the even fields.

An advantageous simplification concerns the output pattern of the 40ms branch. In the known BRD the hardware cost was increased significantly by circuits which did no processing except compensating delays between the mode branches. In particular, this is true for compensation delays introduced subsequent to the 40ms branch while the 80ms processing was achieved. In order to suppress these compensation delays the 40ms branch output corresponds to the 80ms pattern and allows the 40ms blocks to be processed by an 80ms interpolator.

A further simplification according to the invention is related to the motion compensation processing. In the known BRD, motion compensation was achieved after interpolating the two surrounding odd fields. The output were full definition fields.
Now, the motion compensation is performed on the 40ms quincunx grid and the output are the two 80ms mode patterns 80_1 and 80_2.
The previous 40ms branch was composed of six circuits: two interpolators and four motion compensated delays. Now there are two motion compensated interpolators, only. The hardware complexity of these circuits mainly results from the required switch matrix. This switch matrix is composed of line delays and pixel delays which permit a random access to motion vector displaced pixels.

In the known switch matrix, nine line delays were used for access to four pixels, in the new one only seven line delays are needed for access to six pixels.
In Fig. 1 two motion compensated interpolators 11 and 12 receive 40ms blocks 40_A and 40_C of the first and of the third field of each two consecutive frames. A set of horizontal and vertical delays DHV is followed by a switch matrix SM. The six output pixel values P, Q, R, S, T and U of each switch matrix SM pass through a further array of horizontal delays DH. To get all pixel values for the 80ms output grid these delays are followed by interpolators INT.
For the interpolation the four nearest pixels P, Q, R and S of a single motion vector displaced output pixel are required. The two corresponding sets of four pixels have at least two common pixels because of the spatial location of the 80_1 and 80_2 outputs. This means that by using the same window the access to six pixels P, Q, R, S, T and U is sufficient for motion compensating the 80_1 and 80_2 outputs.
The calculated output values 80_1 and 80_2 of the 40ms branch are combined in a multiplexer MUX which delivers at each 27MHz clock cycle the final output values 80_1 of the odd field in the 80ms mode pattern and 80_2 of the even field in the 80ms mode pattern.

In Fig. 3, the four possible line 30 and column 31 locations IP1, IP2, IP3 and IP4 of motion vector displaced pixels within the 80ms grid are depicted to illustrate the six required interpolation inputs P, Q, R, S, T and U. Circles O mark the spatial location of the 80_1 output values and triangles Δ the spatial location of the 80_2 output values.

As explained before, the motion compensation on the quincunx grid needs an interpolation when a motion vector displaced pixel is not on the quincunx grid. In this case it is difficult to have a correct interpolated pixel when using only the four nearest pixels P, Q, R and S. This problem is overcome by memorising in the horizontal delays DH three consecutive switch matrix outputs. As depicted in Fig. 2a, twelve pixels having ten

different spatial locations Q-1, Q0, Q1, P-1, R-1/P0, R0/P1, R1, S-1, S0 and S1 are available for the interpolation of the output pixel values 80_1 and 80_2 in the interpolators INT, if the same vector is used to access them.
As shown in Fig. 2b, at block border 20 some problems can occur when the motion vector of the adjacent block is different. In this case, seven pixels Q0, Q1, P0, R0, R1, S0 and S1 out of the ten used in the interpolators INT give correct input values.
In order to avoid complex controls at the block borders, two assumptions are made. These assumptions have been carefully investigated over picture sequences offering very busy motion areas. The investigations proofed that such assumptions can be allowed.
The first assumption is that an interpolation using seven correct pixels, especially the four nearest pixels, out of the ten contained in the interpolation window shown in Fig. 5 will not give a noticeable error, but, maybe in some particular picture content, a blurred pixel, only.
The second assumption concerns the continuity existing in every motion vector field obtained by a block based motion estimator, which would validate the use of three pixels outside the current block. When discontinuity appears in a motion vector field the HDMAC encoder usually chooses the 20ms mode. If the motion compensation does not give a good result, then the first assumption should work because a zero vector is applied to 20ms blocks

Fig. 4b shows the set of horizontal and vertical delays DHV in more detail. The input values 40_A and 40_B, respectively, pass through a chain of seven line delays LD which make available in parallel the pixels of eight lines of the current field at the outputs Pv1 to Pv8. These outputs correspond to the vertical vector positions Vy=7, Vy=5, Vy=3, ..., Vy=-7. The outputs Pv1 to Pv8 are fed to the inputs 41 of horizontal delay sections HDS having the outputs 40 (Ph1 to Ph9) and which are shown in Fig. 4a in more detail. Each block T is a pixel delay.
Four of the horizontal delay sections (HDS1, HDS2, HDS3, HDS4) are depicted in Fig. 4b indicating that a subsequent switch matrix SM connects for each current pixel position such of the

outputs 40 to the respective six switch matrix outputs which represent the pixels P, Q, R, S, T and U.

Fig. 5 shows the 80_1 interpolation window 51 for the current pixel I1 and the 80_2 interpolation window 52 for the current pixel I2.

In Fig. 6 each of the six input pixel values P, Q, R, S, T and U passes through a chain of two pixel delays PD, the inputs and outputs, respectively, of which are connected in such a way to the interpolators INT that the pixels of the interpolation windows 51 and 52 are used.

Fig. 7 represents a possible hardware implementation of an interpolator INT. The input pixel values Q-1, Q1, S-1, T0, Q0, S0, P0, R0, P-1 and R1 resulting from interpolation window 51 are combined using adders "+", multipliers "-2", "4", "7", delays T and a divider or shifter "÷16".

It is worth noting that the six switch matrix outputs of the current 40ms branch output are always used in the 80_1 window 51 because they are correct even at the right border of a block:

current set = (P0, Q0, R0, S0, T0, U0)

But for hardware simplification reasons T0 is not used in the interpolation of I1 and P0 is not used in the interpolation of I2.

Fig. 8 shows precisely the window positions in case the current line is odd (Fig. 8a) or even (Fig. 8b). PB is the picture border, 81 and 83 are 80_1 windows and 82 and 84 are 80_2 windows. The marks have the following meaning:

X transmitted pixel (40ms)

□ centre of window

O sample 80_1

Δ sample 80_2

I1 and I2 can be calculated according to the following formulas:

$$I_1 = \frac{\left[-2(Q_{-1} + Q_1 + S_{-1} + S_1) + 4(Q_0 + S_0) + 7(P_0 + R_0) + (P_{-1} + R_1)\right]}{16}$$

$$I_2 = \frac{\left[-2(R_{-1} + R_1 + U_{-1} + U_1) + 4(R_0 + U_0) + 7(S_0 + T_0) + (S_{-1} + T_1)\right]}{16}$$

Odd field processing:

No motion compensation is applied on odd fields, but the switch matrix SM works with a zero vector to allow processing through a motion compensated interpolator (MCI) in the HDMAC BRD. Only the MCI with a 40_A input is active. The spatial location of the windows in Fig. 8a and Fig. 8b depends on the output line parity within the field.

Odd line:

$$80_1 = P_0$$

$$80_2 = \frac{I_1 + S_0}{2}$$

Even line:

$$80_1 = I_1$$

$$80_2 = \frac{I_2 + R_0}{2}$$

Even field processing:

The impact point IP is the motion vector displaced pixel within the set of six pixels (see Fig. 3) which are outputs of the switch matrix SM. In fact the impact point characterises the position of a couple of points 80_1 and 80_2. The motion vector (Vx, Vy) and the current line parity determine the impact point location. The current line parity is referred to an odd field since the interlace doesn't exist anymore for an 80ms output pattern.

Odd line:

The impact point IP is known from the following formula:

$$S = |V_x| + \frac{|V_y|}{2}$$

|Vx| stands for absolute value of Vx. As Vx and Vy are integers, S can be an integer or not:

$$S \text{ integer} \begin{cases} \text{If S is even IP = IP1} \\ \text{If S is odd IP = IP3} \end{cases}$$

S not integer and V_y negative $\begin{cases}\text{If } I(S) \text{ is even } IP = IP2\\ \text{If } I(S) \text{ is odd } IP = IP4\end{cases}$

S not integer and V_y positive $\begin{cases}\text{If } I(S) \text{ is even } IP = IP4\\ \text{If } I(S) \text{ is odd } IP = IP2\end{cases}$

I(S) stands for integer part of S

Even line:

The impact point IP is known from the following formula:

$$S = |V_x| + \frac{|V_y|}{2}$$

S calculation is the same as for odd lines, but the IP assignment is different:

S integer $\begin{cases}\text{If S is even } IP = IP3\\ \text{If S is odd } IP = IP1\end{cases}$

S not integer and V_y negative $\begin{cases}\text{If } I(S) \text{ is even } IP = IP4\\ \text{If } I(S) \text{ is odd } IP = IP2\end{cases}$

S not integer and V_y positive $\begin{cases}\text{If } I(S) \text{ is even } IP = IP2\\ \text{If } I(S) \text{ is odd } IP = IP4\end{cases}$

The interpolation to be achieved depends on the impact point:

$$IP1 \begin{cases} 80_1 = P_0 \\ 80_2 = \frac{I_1 + S_0}{2}\end{cases}$$

$$IP2 \begin{cases} 80_1 = \frac{I_1 + Q_0}{2} \\ 80_2 = R_0\end{cases}$$

$$IP3 \begin{cases} 80_1 = I_1 \\ 80_2 = \frac{I_2 + R_0}{2}\end{cases}$$

$$IP4 \begin{cases} 80_1 = \frac{I_1 + S_0}{2} \\ 80_2 = I_2\end{cases}$$

For an extremely negative vertical vector component Vy=-6 and Vy=-5 pixel U is not always available as well as for an extremely positive vertical vector component Vy=+6 and Vy=+5 V. Fig. 10 and Fig. 11 define these cases .Thus, the interpolation needs to be simplified:

When U is absent, then $I_2 = \frac{(3S_0 + 3T_0 + 2R_0)}{8}$

When Q is absent, then $I_1 = \frac{(3P_0 + 3R_0 + 2S_0)}{8}$

The outputs of switch matrix SM depend on the motion vector (zero vector for odd field) and on the line parity (always referred to an odd field). The Fig. 9 illustrates the accessible pixels for an odd line (Fig. 9a, Pv=5) and an even line (Fig. 9b, Pv=5). The mark @ represents an 80_1 position and the mark O an 80_2 position. In order to reduce the necessary number of line delays, not all pixels needed for the interpolation are available in any case for extreme large vertical vector components.

Fig. 10 and Fig. 11 give the coordinates of the switch matrix outputs according to the numbering of Fig. 9 and field 40_A (t-20ms). A horizontal vector component is positive for a horizontal displacement from the left to the right of the picture. A vertical vector component is positive for a vertical displacement from the bottom to the top of the picture. To have the tables referred to field 40_C (t+20ms) the sign of the vertical components needs to be inverted.

Fig. 10a defines for odd lines the vertical position PV with respect to Vy and to the Vx parity VXP.

Fig. 10b defines for odd lines the horizontal position PH with respect to Vx and to the S parity SP.

S parity for odd line: $S = |V_x| + \frac{|V_y|}{2}$.

If S is even, then S parity is even.

If S is not even, then S parity is odd.

Fig. 11a defines for even lines the vertical position PV with respect to Vy and to the Vx parity VXP.

Fig. 11b defines for even lines the horizontal position PH with respect to Vx and to the S parity SP.

S parity for even line: $S = |V_x| + \frac{|V_y| + 2}{2}$.

If S is even, then S parity is even.
If S is not even, then S parity is odd.

In an orthogonal sampling grid system, e.g. MPEG, the motion compensated interpolation is bi-linear (i.e. linear in the two spatial directions) by using the four nearest pixels P0, Q0, P1, Q1 surrounding the possible motion vector impact point. The impact point can have four different locations O within the sampling grid as depicted in Fig. 12. Therefore, a switch matrix SM must access the four pixels P0, Q0, P1, Q1.
According to the invention, the quantity of pixels to be accessed for each output pixel location of a motion compensated block can be reduced to 2 (P and Q). Due to the delays PD (similar as depicted in Fig. 6) all four required input pixel values are available for a correct interpolation.
The block border problem can be solved by extending the processing of the motion compensation by one pixel per block line. For example, if a vector should be applied to a 16*16 block, the switch matrix SM needs to access 2 pixels (P and Q) only at each pixel position of a 17*16 block. So the four pixels used in the motion compensation everywhere in the 16*16 block are accessed with the same vector and the motion compensated block can be reconstructed perfectly even at block border.

The invention can be used e.g. in TV sets and digital VCR's.

Claims

1. Method for motion compensated interpolation, wherein the output pixel values (80_1, 80_2) are interpolated (INT) from input pixel values (P, Q, R, S) located within a window (51, 52, 81-84) which is related to the spatial and/or temporal location (IP1-IP4) of the current output pixel (80_1, 80_2, I1, I2) and wherein the pixel values required for said window are made available using delay means (DHV, LD, T) and switch matrix means (SM), the outputs of which are currently connected in response to a motion vector (Vx, Vy) to such of said delay means which currently deliver said input pixel values (P, Q, R, S), **characterised in** that each of the outputs of said switch matrix means (SM) passes through at minimum one further delay unit (PD) and that said outputs of the switch matrix means and the outputs of said delay units are used to form an increased window for interpolating (INT) said output pixel values (80_1, 80_2).

2. Method according to claim 1, **characterised in** that said output pixels (80_1, 80_2) form a sample grid compared to which said input pixels are sub-sampled pixels.

3. Method according to claim 1 or 2, **characterised in** that two or more of said output pixel values (80_1, 80_2) are interpolated (INT) in parallel, wherein for each of these output pixels (80_1; 80_2) a different set (P, Q, R, S; S, R, T, U) of input pixel values is required, but a part of these sets is composed of common (R, S) input pixel values.

4. Method according to any of claims 1 to 3, **characterised in** that said interpolation (INT) is performed on a field (40_A, 40_C) basis.

5. Method according to any of claims 1 to 4, **characterised in** that said motion compensated interpolation is used for display rate upconversion.

6. Method according to any of claims 1 to 5, **characterised in** that said motion compensated interpolation is performed in an HDMAC decoder, wherein said switch matrix (SM) works with a zero vector (Vx=0, Vy=0) in odd fields.

7. Method according to any of claims 1 to 6, **characterised in** that said motion compensated interpolation is modified in case of a high vertical vector component (Vy).

8. Apparatus for motion compensated interpolation, wherein the output pixel values (80_1, 80_2) are interpolated (INT) from input pixel values (P, Q, R, S) located within a window (51, 52, 81-84) which is related to the spatial and/or temporal location (IP1-IP4) of the current output pixel (80_1, 80_2, I1, I2), related to a method according to any of claims 1 to 7 and comprising:
- delay means (DHV, LD, T) which make available the pixel values required for said window;
- switch matrix means (SM), the outputs of which are currently connected in response to a motion vector (Vx, Vy) to such of said delay means which currently deliver said input pixel values (P, Q, R, S);
- at minimum one delay unit (PD) at each switch matrix means (SM) output (P, Q, R, S, T, U) through which each of the outputs of the switch matrix means passes, wherein said outputs of the switch matrix means and the outputs of said delay units are used to form an increased window;
- interpolating means (INT) subsequent to said delay units for interpolating said output pixel values (80_1, 80_2).

9. Apparatus according to claim 8, **characterised in** that said apparatus is part of a TV receiver - especially an HDMAC or MPEG receiver - or of an HDMAC or MPEG decoder or of a digital VCR.

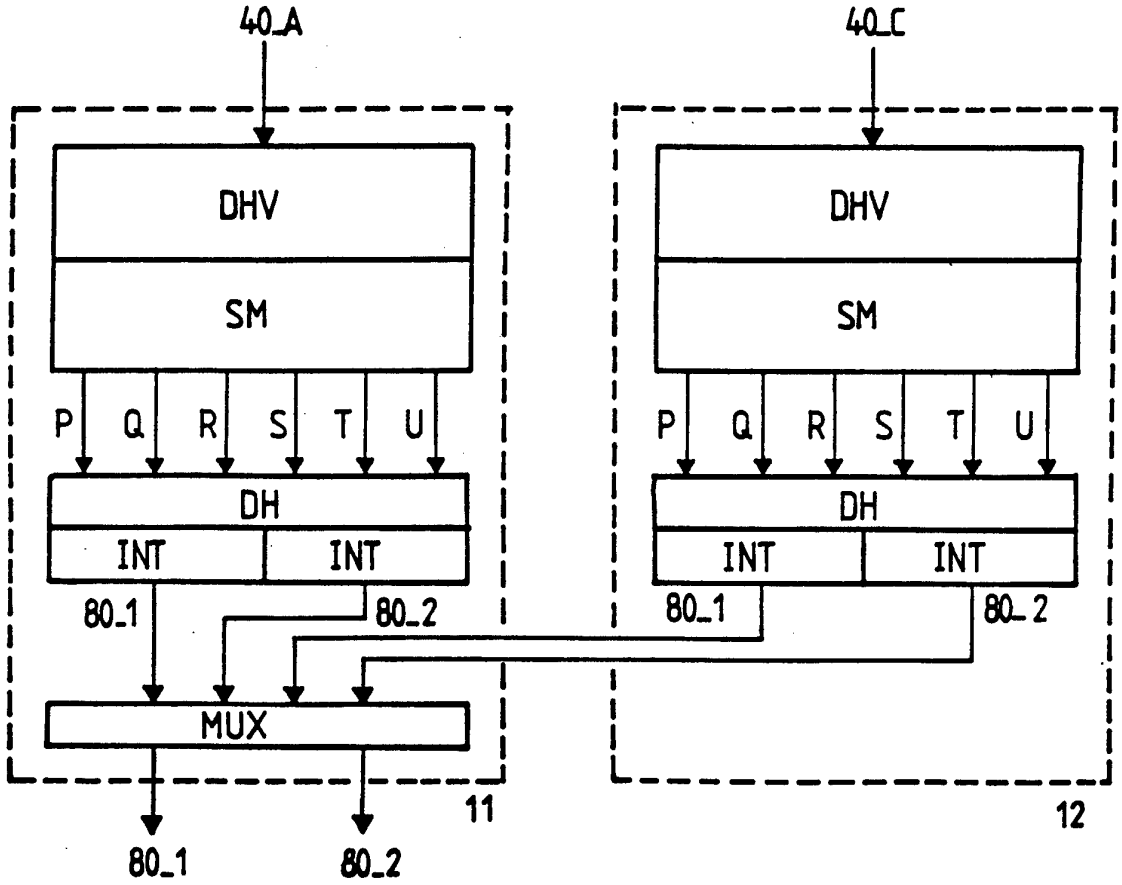


Fig.1

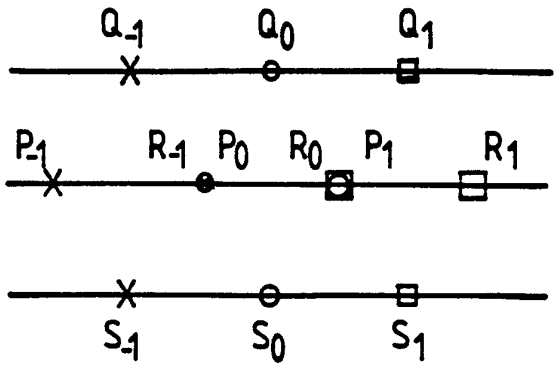


Fig.2a

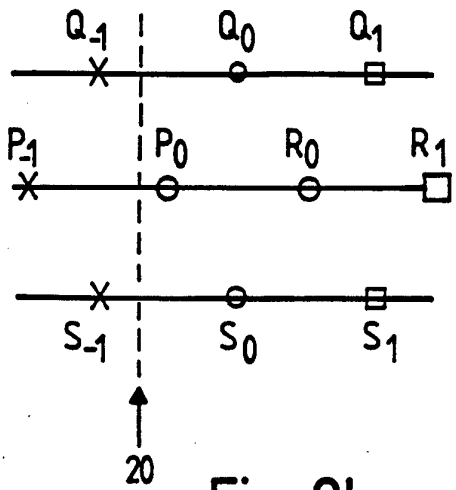


Fig. 2b

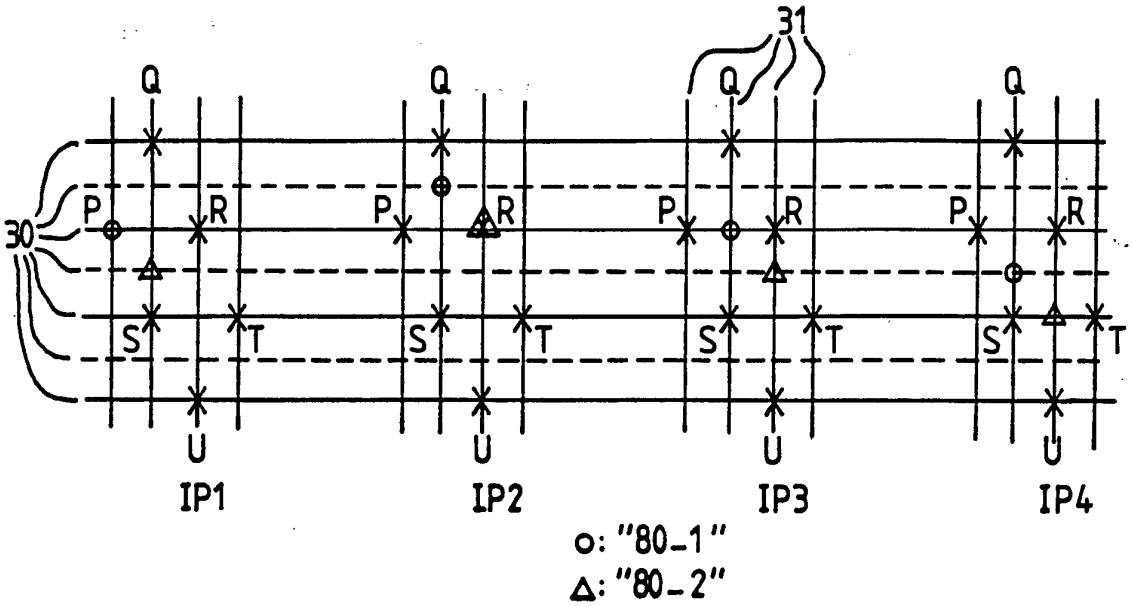


Fig.3

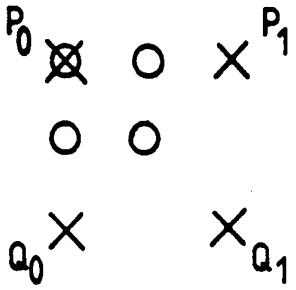


Fig.12

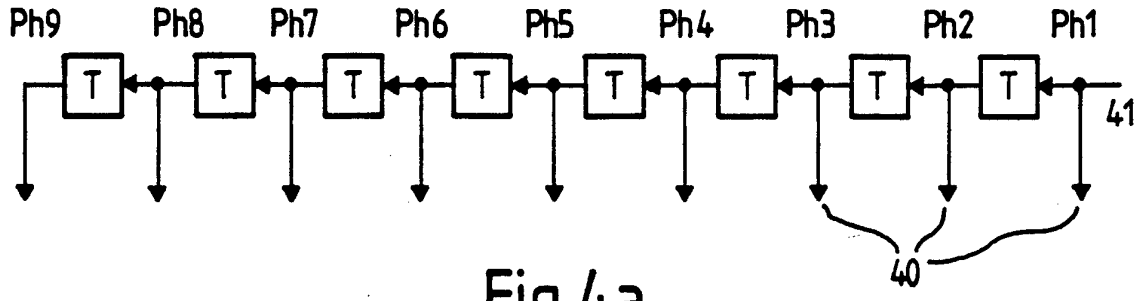
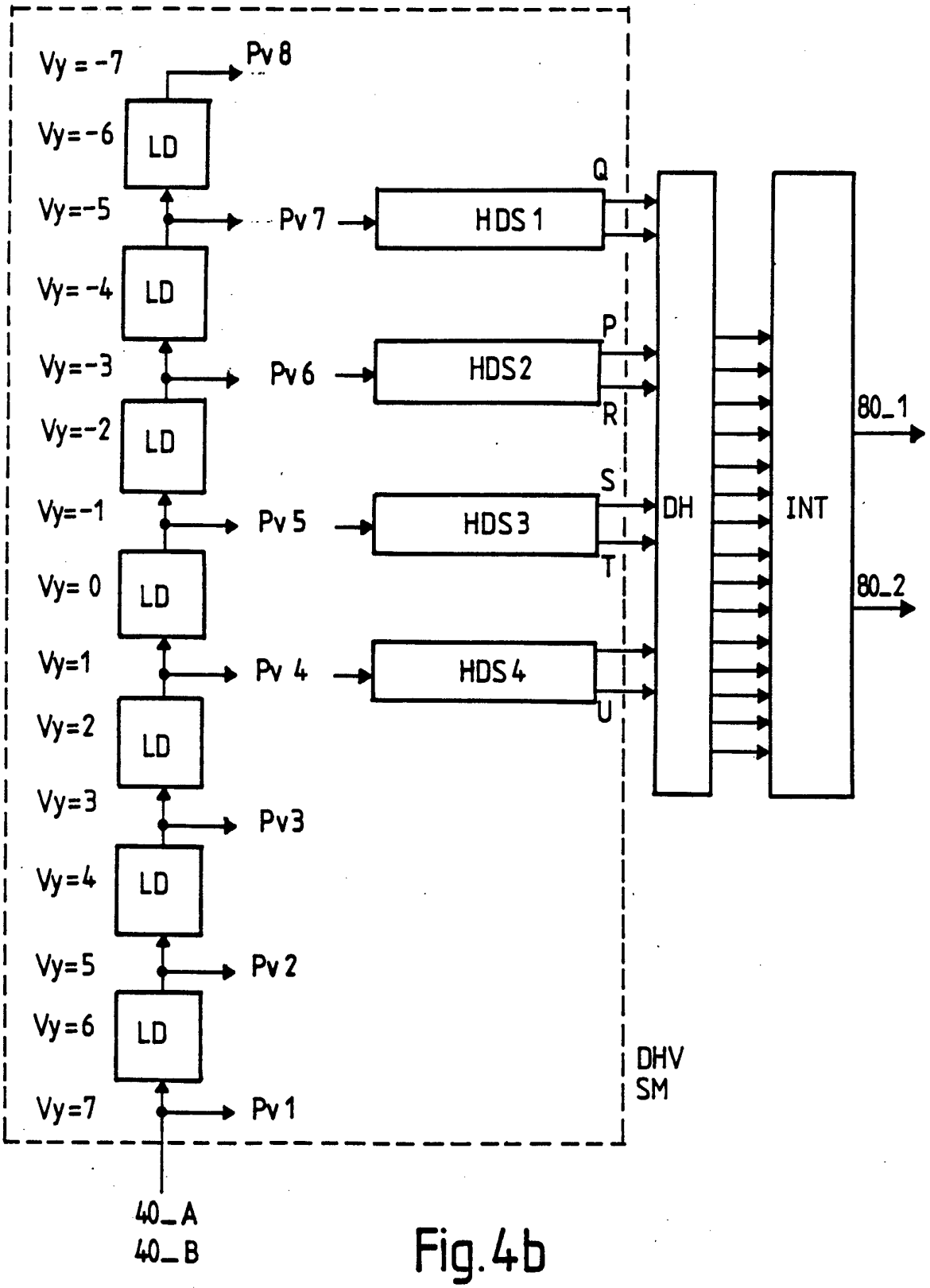


Fig.4a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Pv 8
Vy=-6
LD
Vy=-5
Pv 7
HDS 1
Q
Vy=-4
LD
Vy=-3
Pv 6
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P
R
Vy=-2
LD
Vy=-1
Pv 5
HDS3
S
T
Vy= 0
LD
Vy=1
Pv 4
HDS4
U
Vy=2
LD
Vy=3
Pv3
Vy=4
LD
Vy=5
Pv 2
Vy=6
LD
Vy=7
Pv 1
DH
INT
80_1
80_2
DHV
SM
40_A
40_B

Fig.4b

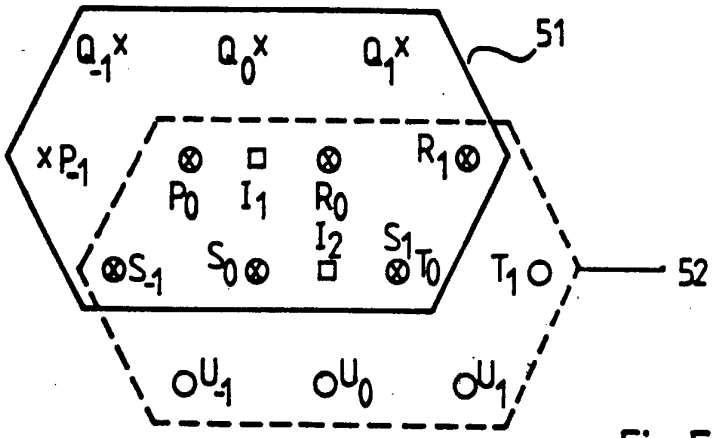
Q-1 Q0 Q1
51
P-1
P0 I1 R0 R1
I2 S1
S-1 S0 T0 T1
52
U-1 U0 U1

Fig.5

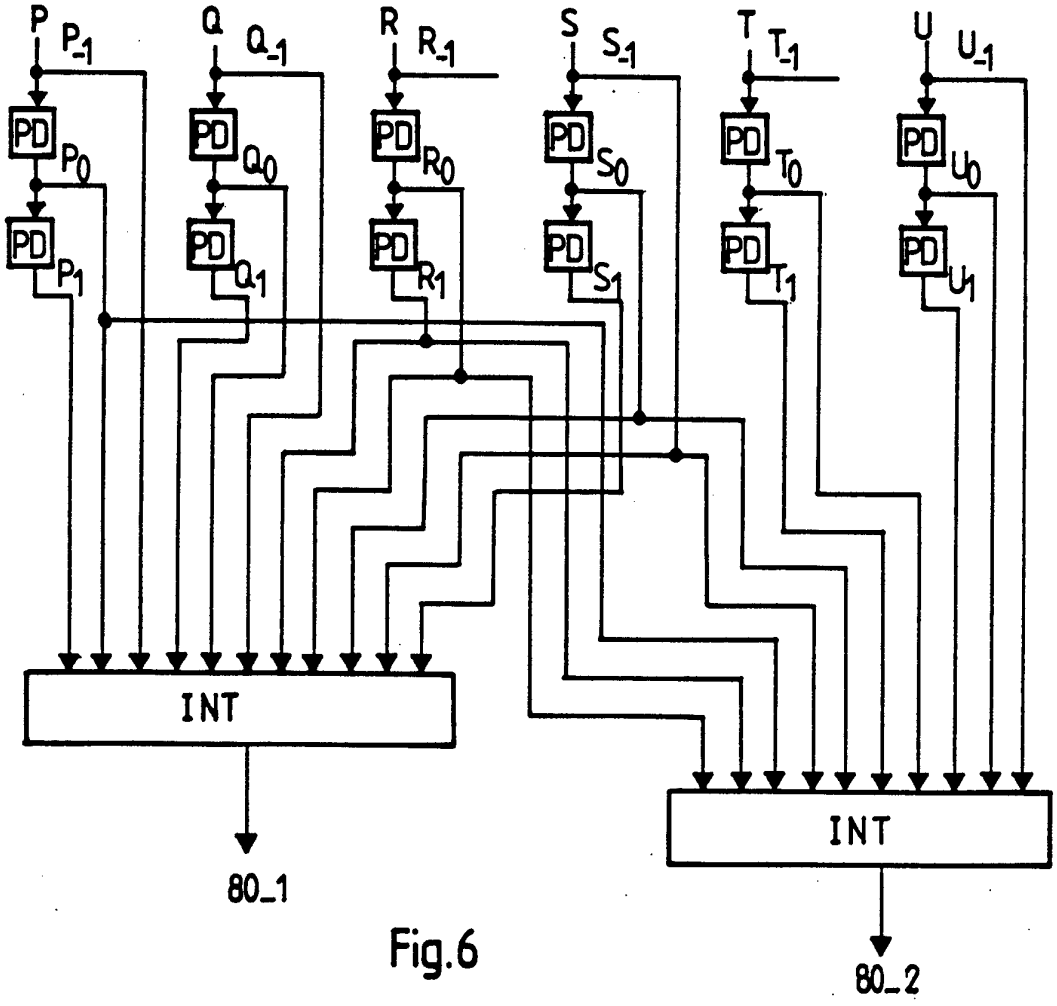
P P-1
Q Q-1
R R-1
S S-1
T T-1
U U-1
PD
P0
P1
Q0
Q1
R0
R1
S0
S1
T0
T1
U0
U1
INT
INT
80_1
80_2

Fig.6

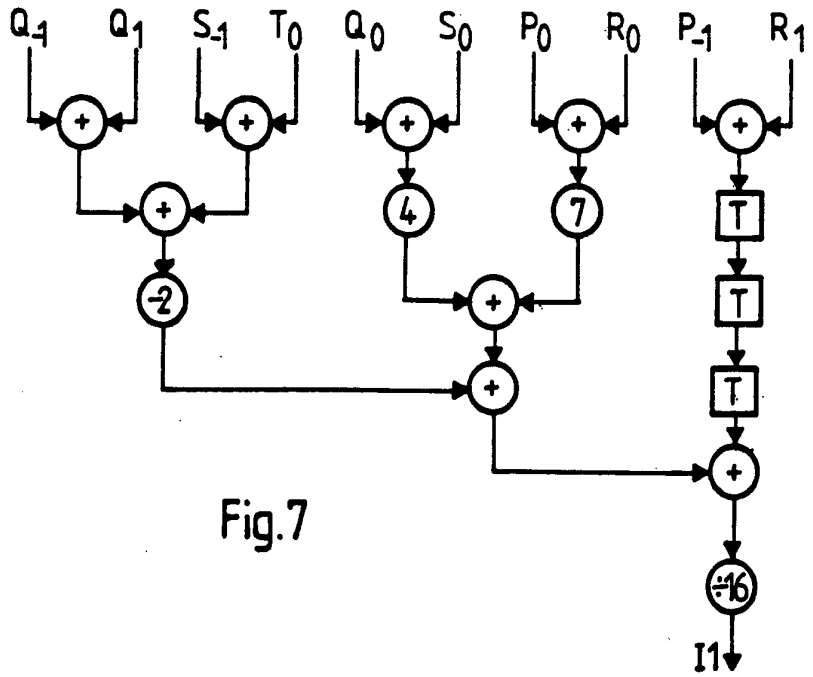

Fig.7

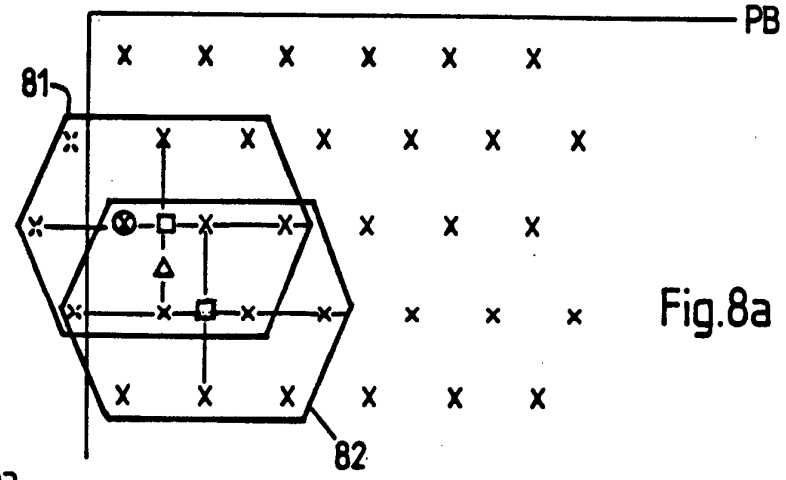

Fig.8a

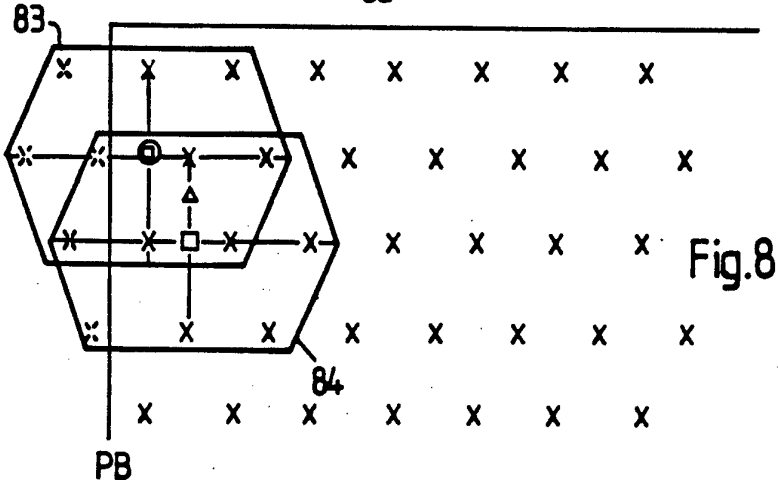

Fig.8b

Pv/Ph	9	8	7	6	5	4	3	2	1
8	X	X	X	X	X	X	X	X	X
7	X	X	X	X	X	X	X	X	X
6	X	X	X	X	X	X	X	X	X
5	X	X	X	X	@ o	X	X	X	X
4	X	X	X	X	X	X	X	X	X
3	X	X	X	X	X	X	X	X	X
2	X	X	X	X	X	X	X	X	X
1	X	X	X	X	X	X	X	X	X

Fig.9a

Pv/Ph	9	8	7	6	5	4	3	2	1
8	X	X	X	X	X	X	X	X	X
7	X	X	X	X	X	X	X	X	X
6	X	X	X	X	X	X	X	X	X
5	X	X	X	X	@ o	X	X	X	X
4	X	X	X	X	X	X	X	X	X
3	X	X	X	X	X	X	X	X	X
2	X	X	X	X	X	X	X	X	X
1	X	X	X	X	X	X	X	X	X

Fig.9b

		PV					
Vy	VXP	P	Q	R	S	T	U
6	odd	2	3	2	1	1	X
6	even	2	3	2	1	1	X
5	odd	3	4	3	2	2	1
5	even	2	3	2	1	1	X
4	odd	3	4	3	2	2	1
4	even	3	4	3	2	2	1
3	odd	3	4	3	2	2	1
3	even	4	5	4	3	3	2
2	odd	4	5	4	3	3	2
2	even	4	5	4	3	3	2
1	odd	5	6	5	4	4	3
1	even	4	5	4	3	3	2
0	odd	5	6	5	4	4	3
0	even	5	6	5	4	4	3
-1	odd	5	6	5	4	4	3
-1	even	6	7	6	5	5	4
-2	odd	6	7	6	5	5	4
-2	even	6	7	6	5	5	4
-3	odd	7	8	7	6	6	5
-3	even	6	7	6	5	5	4
-4	odd	7	8	7	6	6	5
-4	even	7	8	7	6	6	5
-5	odd	7	8	7	6	6	5
-5	even	8	X	8	7	7	6
-6	odd	8	X	8	7	7	6
-6	even	8	X	8	7	7	6

Fig.10a

		PH					
Vx	SP	P	Q	R	S	T	U
6	odd	9	8	8	8	7	8
6	even	8	8	7	8	7	7
5	odd	8	8	7	8	7	7
5	even	8	7	7	7	6	7
4	odd	8	7	7	7	6	7
4	even	7	7	6	7	6	6
3	odd	7	7	6	7	6	6
3	even	7	6	6	6	5	6
2	odd	7	6	6	6	5	6
2	even	6	6	5	6	5	5
1	odd	6	6	5	6	5	5
1	even	6	5	5	5	4	5
0	odd	6	5	5	5	4	5
0	even	5	5	4	5	4	4
-1	odd	5	5	4	5	4	4
-1	even	5	4	4	4	3	4
-2	odd	5	4	4	4	3	4
-2	even	4	4	3	4	3	3
-3	odd	4	4	3	4	3	3
-3	even	4	3	3	3	2	3
-4	odd	4	3	3	3	2	3
-4	even	3	3	2	3	2	2
-5	odd	3	3	2	3	2	2
-5	even	3	2	2	2	1	2
-6	odd	3	2	2	2	1	2
-6	even	2	2	1	2	1	1

Fig.10b

		PV					
Vy	VXP	P	Q	R	S	T	U
6	odd	2	3	2	1	1	X
6	even	2	3	2	1	1	X
5	odd	2	3	2	1	1	X
5	even	3	4	3	2	2	1
4	odd	3	4	3	2	2	1
4	even	3	4	3	2	2	1
3	odd	4	5	4	3	3	2
3	even	3	4	3	2	2	1
2	odd	4	5	4	3	3	2
2	even	4	5	4	3	3	2
1	odd	4	5	4	3	3	2
1	even	5	6	5	4	4	3
0	odd	5	6	5	4	4	3
0	even	5	6	5	4	4	3
-1	odd	6	7	6	5	5	4
-1	even	5	6	5	4	4	3
-2	odd	6	7	6	5	5	4
-2	even	6	7	6	5	5	4
-3	odd	6	7	6	5	5	4
-3	even	7	8	7	6	6	5
-4	odd	7	8	7	6	6	5
-4	even	7	8	7	6	6	5
-5	odd	8	X	8	7	7	6
-5	even	7	8	7	6	6	5
-6	odd	8	X	8	7	7	6
-6	even	8	X	8	7	7	6

Fig.11a

		PH					
Vx	SP	P	Q	R	S	T	U
6	odd	9	8	8	8	7	8
6	even	8	8	7	8	7	7
5	odd	8	8	7	8	7	7
5	even	8	7	7	7	6	7
4	odd	8	7	7	7	6	7
4	even	7	7	6	7	6	6
3	odd	7	7	6	7	6	6
3	even	7	6	6	6	5	6
2	odd	7	6	6	6	5	6
2	even	6	6	5	6	5	5
1	odd	6	6	5	6	5	5
1	even	6	5	5	5	4	5
0	odd	6	5	5	5	4	5
0	even	5	5	4	5	4	4
-1	odd	5	5	4	5	4	4
-1	even	5	4	4	4	3	4
-2	odd	5	4	4	4	3	4
-2	even	4	4	3	4	3	3
-3	odd	4	4	3	4	3	3
-3	even	4	3	3	3	2	3
-4	odd	4	3	3	3	2	3
-4	even	3	3	2	3	2	2
-5	odd	3	3	2	3	2	2
-5	even	3	2	2	2	1	2
-6	odd	3	2	2	2	1	2
-6	even	2	2	1	2	1	1

Fig.11b

INTERNATIONAL SEARCH REPORT

Internatio· ·pplication No
PCT/EP 94/01750

A. CLASSIFICATION OF SUBJECT MATTER
IPC 5 H04N7/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 5 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A,4 587 556 (COLLINS) 6 May 1986 see column 2, line 67 - column 4, line 34; figures 1-3	1,3-5,8,9
A	EP,A,0 424 269 (LABORATOIRE EUROPEEN DE RECHERCHES ELECTRONIQUES AVANCEES) 24 April 1991 see column 6, line 39 - column 8, line 45 see column 10, line 13 - column 11, line 23; figures 8,12	1,4,6,8,9
A	EP,A,0 427 576 (LABORATOIRE EUROPEEN DE RECHERCHES ELECTRONIQUES AVANCEES) 15 May 1991 see column 2, line 48 - column 18, line 45; figures 4-6	1,4,6,8,9

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"&" document member of the same patent family

1

Date of the actual completion of the international search
15 September 1994

Date of mailing of the international search report
04.10.94

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NL - 2280 HV Rijswijk
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP,A,0 347 325 (ETAT FRANCAIS) 20 December 1989 see page 3, line 50 - page 9, line 17; figures 2-8,11,11A	1,4,6,8,9
A	EP,A,0 428 216 (LABORATOIRES D'ELECTRONIQUE PHILIPS) 22 May 1991 see page 2, line 1 - page 4, line 44 see page 15, line 28 - page 20, line 48; figures 1,5,16-21	1,4,6,8,9
A	WO,A,91 12691 (N. V. PHILIPS' GLOEILAMPENFABRIEKEN) 22 August 1991 see page 5, line 13 - page 11, line 9 see page 13, line 29 - page 19, line 12; figures 1A,3-8	1,3,4,6,8,9

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Information on patent family members

Internatio application No
PCT/EP 94/01750

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