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(54) Title: THYRISTOR VOLATILE RANDOM ACCESS MEMORY AND METHODS OF MANUFACTURE

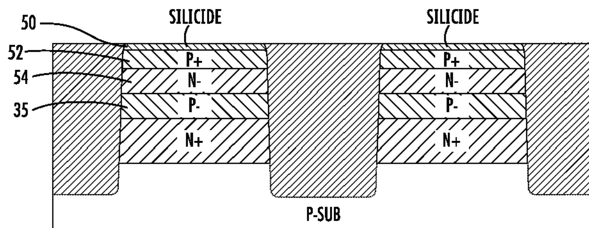

FIG. 8A (A~A')

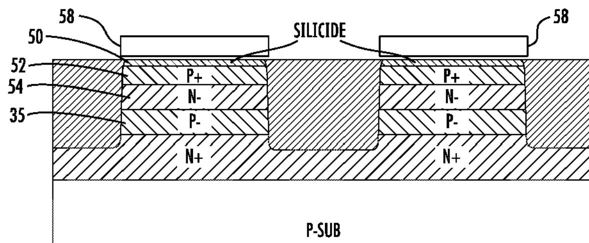

FIG. 8B (B~B')

(57) Abstract: A volatile memory array using vertical thyristors is disclosed together with methods of fabricating the array.

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Thyristor Volatile Random Access Memory and Methods of Manufacture

Description

Cross-Reference to Related Applications

[01] This patent application is related to U.S. Patent Application No. 14/841,521, filed of even date and entitled, "Methods of Reading and Writing Data in a Thyristor Random Access Memory," U.S. Patent Application No. 14/841,578, filed of even date and entitled, "Methods of Retaining and Refreshing Data in a Thyristor Random Access Memory," U.S. Patent Application No. 14/841,615, filed of even date and entitled, "Power Reduction in Thyristor Random Access;" all of which claim priority from U.S. Provisional Patent Application No. 62/186,336, filed June 29, 2015 and entitled, "High-Density Volatile RAMs, Method of Operation and Manufacture Thereof," and is a continuation-in part of U.S. Application No. 14/590,834, filed January 6, 2015 and entitled, "Cross-Coupled Thyristor SRAM Circuits and Methods of Operation," which claims priority from U.S. Provisional Patent Application No. 62/055,582, filed September 25, 3014; all of which are incorporated by reference herein for all purposes.

Background of the Invention

[02] This invention is related to integrated circuit devices and in particular to volatile random access memories, commonly known as dynamic random access memories (DRAMs).

[03] A DRAM is a type of random-access memory integrated circuit that in the most common commercial implementation stores each bit of data in a separate capacitor coupled to a transistor within the integrated circuit. The capacitor can be either charged or discharged. The states of charged or discharged are interpreted as values of a bit, i.e. '0' and '1'. The one-transistor one-capacitor cell has been the most commercially used memory cell used in DRAM devices for the last 30 years. Lithographical scaling and increasing process complexity have enabled the number of bits of storage in a DRAM to quadruple about every three years, however the individual memory cells are now so small that maintaining the capacitance of each cell, and reducing charge leakage, are significant problems inhibiting further size reductions.

[04] In response to these challenges and other problems, alternative DRAM memory cell architectures have been proposed. One such approach is known as a floating body DRAM

(FBDRAM). The FBDRAM is a single MOSFET built on either a silicon-on-insulator (SOI) (Okhonin, Int. SOI Conf., 2001) or in a triple-well with a buried N-implant (Ranica, VLSI Technology, 2004). The transistor's body forms a capacitor against the insulated substrate. The technology has yet to solve its data retention issues, particularly at scaled dimensions.

[05] Another approach to a new DRAM architecture is based on the negative differential resistance behavior of a PNPN thyristor. In these designs an active or passive gate is used. For example, a thin capacitively coupled thyristor described in US Patent 6,462,359 uses a lateral PNPN thyristor on a SOI substrate with a coupling gate for increased switching speed. Unfortunately, the lateral aspect of the design, together with the need for a gate, results in a memory cell substantially larger than a conventional one-transistor one-capacitor DRAM cell structure.

[06] Liang in US Patent 9,013,918 describes a PNPN thyristor cell constructed on top of a silicon substrate and operated in forward and reverse breakdown region for writing data into the cell. Unfortunately, the use of epitaxial or CVD semiconductor layers at the backend of the standard CMOS process, adds thermal cycles and etching steps that can degrade performance and yield of other devices earlier formed on the same substrate. In addition, PNPN devices operated in the breakdown regime pose challenges in process control and power consumption.

[07] What is needed is a DRAM memory cell smaller than the conventional one-transistor one-capacitor, that is easily scalable below 20nm design rules, is compatible with standard bulk silicon processing, and consumes less power, both statically and dynamically.

Brief Summary of the Invention

[08] This invention provides a volatile memory array suitable for implementation of dynamic random access memories in which vertical PNPN thyristors are formed in bulk silicon substrate and isolated from each other by a shallow trench of insulating material in one direction and deeper trench of insulating material in a perpendicular direction. The array of memory cells is arranged in a cross-point grid and interconnected by metal conductors and buried heavily doped layers.

[09] In one embodiment the memory array includes a row and column lines, and each thyristor has an anode connected to one of row lines and a cathode coupled to a column line. The substrate is preferably P-conductivity type with an N-conductivity type buried layer extending in a first direction to provide a column line and cathodes for the thyristors coupled to that column line. Alternating P-conductivity type and N-conductivity type layers on the

buried layer provide the bases of the thyristor, with an upper P-conductivity type layer providing the anodes of the thyristors. A conductive layer coupled to the anodes of the thyristor extending in a second direction orthogonal to the first direction provides a row line. If desired gates are formed in the insulating material to provide NMOS and PMOS transistors for improving switching speed.

[10] A method of making the array includes steps of introducing N-conductivity type dopant into a P-conductivity type semiconductor substrate to provide a buried layer to form the column lines and cathodes for the vertical thyristors. A P-conductivity type epitaxial layer is then formed on the buried layer. Etching then removes all of the epitaxial layer and the buried layer to expose portions of the substrate to form parallel deep trenches that are then filled with insulating material such as silicon dioxide. The epitaxial layer is then etched again to form shallower trenches perpendicular to the deep trenches. After filing the shallow trenches with insulating material the bases and anodes of the thyristor are doped and desired electrical contacts and connectors are formed.

[11] A method of operating the memory array to program a selected thyristor ‘on’ includes steps of applying a positive potential to the row line to which the selected thyristor is connected and applying a lower potential to the column line to which the selected thyristor is connected a lower potential where the difference between the positive potential and the lower potential is greater than that required to turn on the thyristor. All of the non-selected lines have potentials applied to them insufficient to change the state of any other thyristors. To turn the selected thyristor off a low potential is applied to the row line and a positive potential is applied to the column line sufficient to turn it off. All of the non-selected lines have potentials applied to them insufficient to change the state of any other thyristors.

[12] The selected thyristor is read a positive potential to the row line and a lower potential to the column line. The difference between the positive potential and the lower potential is sufficient to pull the column line to a higher potential if the selected thyristor was programmed on, but insufficient to cause the thyristor to pull the column line to a higher potential if the selected thyristor was programmed off. Potentials applied to the non-selected row and column lines are insufficient to change their data. Maintaining potentials on the row and column lines sufficient to keep thyristors that are on turned on, but insufficient to turn on thyristors that are off, retains the stored data in the array.

[13] A technique for reducing current in a row line to be accessed for an operation is also provided. The memory cells coupled to a row line are divided into groups and the column lines for performing operations on the memory cells are carried out by applying the necessary

potentials for that operation to only one group at a time. All other column lines are maintained at a lower potential. The operation is then performed and the next group selected.

[14] A method for refreshing the memory array consists of dividing the array into sectors and refreshing it on a sector-by-sector basis, e.g. by providing a refresh line to apply current or voltage pulses to the sector by switchably connecting only those row lines in the sector to be refreshed to the refresh line.

[15] Because the on thyristors dissipate power, power consumption in the array can be controlled by using parity bits to more closely balance numbers of on and off thyristor memory cells. For example two parity bits can define four states for a stored word that represent not changing the stored word, inverting the first four bits of the stored word, inverting the last four bits of the stored word, and inverting all of the stored word. This approach allows the stored words on average to have approximately the same number of on and off thyristors.

[16] Other objects, features, and advantages of the present invention will become apparent upon consideration of the following detailed description and the accompanying drawings, in which like reference designations represent like features throughout the figures.

Brief Description of the Drawings

[17] Figure 1A is a circuit schematic of a single thyristor memory cell.

[18] Figure 1B is an equivalent circuit schematic as used in the figures herein.

[19] Figure 2A is a circuit diagram of a 2x2 memory cell array.

[20] Figure 2B is a layout diagram showing the topology of the 2x2 memory cell array as implemented in an integrated circuit.

[21] Figures 3A-9A are cross sectional views illustrating a process for manufacturing the memory cell of Figure 1 showing the cross-sections along line A~A' from Figure 2B.

[22] Figures 3B-9B are cross sectional views illustrating a process for manufacturing the memory cell of Figure 1 showing the cross-sections along line B~B' from Figure 2B.

[23] Figure 10 is a flow chart illustrating an alternative process to the process of Figures 3-9.

[24] Figure 11A and 11B are diagrams illustrating the potentials applied to an array of memory cells when writing a '0' into a selected memory cell.

[25] Figure 12 is a diagram illustrating the potentials applied to an array of memory cells when writing a '1' into a selected memory cell.

[26] Figures 13A and 13B are diagrams illustrating the potentials applied to an array of memory cells when reading a selected memory cell.

[27] Figure 14 is a diagram illustrating the potentials applied to an array of memory cells to retain data stored in the memory cells.

[28] Figures 15A-B illustrate a thyristor memory cell with an NMOS sidewall gate in a trench adjacent the thyristor; Figure 15A shows a lateral cross-sectional view of the cell and Figure 15B shows a longitudinal cross-sectional view of the cell.

[29] Figure 16 is a circuit schematic illustrating an array of cells using the gate shown in Figures 15A-B.

[30] Figures 17A-B illustrate a thyristor memory cell PMOS sidewall gate in a trench adjacent the thyristor; Figure 17A shows a lateral cross-sectional view of the cell and Figure 17B shows a longitudinal cross-sectional view of the cell.

[31] Figure 18 is a circuit schematic illustrating an array of cells using the gate shown in Figures 17A-B.

[32] Figures 19A-B illustrate a method of rolling word line access to reduce row current; Figure 19A shows one step of the method in which a first group is selected for access and Figure 19B show the next step in which a second group is selected for access.

[33] Figure 20 is a circuit schematic illustrating a method of refreshing data stored in a sector of the memory.

[34] Figure 21 is a circuit schematic illustrating a method of sensing a memory cell using a dummy bit line.

Detailed Description of the Invention

[35] 1. An Individual Memory Cell

[36] This invention provides a thyristor-based volatile memory cell, methods of manufacturing the cell, and methods of operating an array of such cells. The memory cell has particular utility for use in dynamic random access memory (DRAM) integrated circuit, as well as circuits in which DRAM memories are embedded. Figure 1A is a circuit schematic of a thyristor coupled between an anode access line (AL) and a cathode access line (KL). The thyristor consists of two cross-coupled bipolar transistors 10 and 12. The emitter of PNP transistor 10 is coupled to the anode access line, while the emitter of NPN transistor 12 is coupled to the cathode access line. The collectors and bases of the two transistors are coupled together as shown. Figure 1B is an equivalent circuit schematic showing the thyristor 15 using conventional notation. This notation is used in subsequent figures below.

[37] Figure 2A illustrates an array of four thyristors 15a, 15b, 15c, and 15d coupled in a grid pattern to form a memory array. Thyristors 15a and 15b are connected to the same row line AL1, but to different column lines KL1 and KL2. Similarly, thyristors 15c and 15d are connected to the same row line AL2, but to different column lines KL1 and KL2.

[38] Figure 2B is a layout diagram illustrating the layout of the circuit shown in Figure 2A as an integrated circuit. The four thyristors are vertical thyristors, having anodes 20 at the corners of the layout. A deep silicon dioxide trench 22 isolates the thyristors on the left from those on the right, while a shallow trench 21 isolates the upper thyristors from the lower ones. These trenches are shown below in more detail. A conductive line 24 provides a row line for the memory array, and is coupled to the anodes of the thyristors. A similar row line (not shown) extends across the anodes of the thyristors in the row above row line 24. The figure also shows the locations of cross-sections A~A' and B~B' used in subsequent figures below.

[39] 2. The Fabrication Process

[40] Figures 3A and 3B are illustrations used to describe the beginning of the process for fabricating the structure shown in the top view of Figure 2B. In the first step of the process selected regions of the P-conductivity type silicon substrate 30 are doped with an N-conductivity type dopant, for example, arsenic, to a concentration that ranges from 1x1019 to 5x1020. The semiconductor substrate layer 30 can include single crystalline semiconductor materials such as silicon or silicon-germanium alloy. The N-conductivity type dopant 32 is introduced by well known semiconductor fabrication techniques, for example, ion implantation, and extends into the substrate 30 as illustrated to a depth of 200nm~500nm. Because the entire cell array region is open to this buried N-type doping, there is no difference between the two cross-sectional views of Figures 3A and 3B.

[41] Next, as shown in Figures 4A and 4B, an epitaxial silicon layer 35 with a thickness between about 300 nm and 500 nm is formed on top of the underlying structure, also using well-known semiconductor fabrication process technology. The epitaxial layer 35 can be either intrinsic, or in-situ doped to a P-conductivity type.

[42] Figures 5A and 5B illustrate the next steps of the process. First, a thin silicon dioxide (pad) layer 36 is grown or deposited across the upper surface of the semiconductor structure. On top of layer 36, a silicon nitride layer 38 is formed using well-known process technology. Using a mask (not shown), openings are etched through the silicon nitride layer 38 and the pad oxide layer 36 to expose the upper surface of the epitaxial layer 35 where deep trenches 39 are to be formed. Using the patterned pads as a hard mask with or without photoresist

removal, a reactive ion etch (RIE) step is then performed to etch the deep trenches 39 that extend through the memory cell area, e.g. as shown in the top view of Figure 2B. These deep trenches extend down through the overlying layers to the substrate 30. Notice that the deep trenches are parallel to each other and thus do not appear in the cross-section illustrated in Figure 5B.

[43] As next shown in Figure 6A, the deep trenches 39 are filled with insulating material such as silicon dioxide 42. This is achieved by first growing a thin liner-oxide on the exposed silicon surface of the sidewalls and bottoms of the trenches. Then using, for example, high-density plasma (HDP) enhanced chemical vapor deposition (CVD), the trenches are filled with silicon dioxide to an appropriate thickness, typically extending above the upper surface of the structure. Next, well-known chemical mechanical polishing (CMP) with high-selectivity slurry is used to planarize the surface and remove the excess trench oxide down to the pad nitride. Then, as shown in Figure 6B, another masking step is performed and shallower trenches 40 are etched. Note that the depth of the shallower trenches extends to the N-conductivity type epitaxial layer 32, and not down to the P-type substrate.

[44] Next, as shown in Figure 7B, the shallower trench is oxidized and then filled with silicon dioxide 45, in the same manner as described above. After the trench is filled with silicon dioxide and planarized by CMP, the upper layers of silicon dioxide and silicon nitride are etched away, again using conventional wet or dry etching.

[45] Figures 8A and 8B illustrate the next steps of the process. Ion implantation steps are used to introduce P-conductivity type 52 and N-conductivity type 54 impurities into the upper surface of the semiconductor creating the PNPN thyristor structure. The N-conductivity type impurity is preferably arsenic, while the P-conductivity type impurity is preferably boron, e.g. boron difluoride. After formation of region 52, a refractory metal, such as titanium, cobalt, or nickel, is deposited on to the upper surface. A rapid-thermal anneal (RTP) is then performed to create a conductive metal silicide in semiconductor regions such as region 50 to provide an ohmic contact to the anode 50 of the thyristor. The un-reacted metal is then removed by a wet etch. The buried N-type region 32 provides the cathode connection.

[46] Also shown in Figure 8B are conducting lines 58 which provide the row lines connecting the anodes of the thyristors of a row together. These conductors that can be metal, metal silicide or doped polysilicon are formed using well-known semiconductor fabrication techniques. For simplicity the row line conductors are only shown in Figure 8B, and not in subsequent figures here.

[47] Figures 9A and 9B illustrate an alternative embodiment for the anode structure 56. As shown, a raised source/drain technology can be used to form the anode by selective epitaxial growth of silicon on the upper surface of the structure. This P-type region 52 can be doped in-situ or using a masking and implantation step. As per the previous embodiment, a refractory metal and an annealing step can be used to form the anode electrode. The raised source/drain technology provides the advantage of allowing a shallower trench, yet still enabling additional space for the N- and P- regions 54 and 35 respectively.

[48] Figure 10 is a flowchart illustrating an alternative embodiment for manufacture of a vertical thyristor. One possible disadvantage of the methods described above for making the vertical thyristor is that the implanted P-type base and N-type base regions (regions 52 and 54 in Figure 8) may have peak concentration and thickness limitations resulting from higher energy implant ion scattering and channeling. Figure 10 illustrates an alternative process for achieving potentially more desirable base doping profiles while maintaining a planar silicon surface.

[49] The process begins with step 60 - the buried layer N-type implant - as described with respect to Figure 3. Then in step 61, as shown in Figure 4, epitaxial silicon of a desired thickness, e.g. 80nm – 130nm, is grown across the upper surface. Next in step 62, the peripheral region of the integrated circuit is masked with photoresist, or other material. Then in step 65 the P-type base region (region 35 in Figure 5) is implanted with appropriate dopant. The masking material is then removed from the wafer (step 66) and then another epitaxial layer of desired thickness, e.g. 120nm – 200nm, is grown across the upper surface of the wafer, and doped N-type to form the N-type base region. Finally, the alternative process returns to formation of the trench isolation regions as described in Figures 5-8 above.

[50] 3. Operation of a Memory Cell Array

[51] Figure 11A illustrates a portion of a larger array of memory cells using the thyristors described above. The illustration will allow an explanation of the methods of operating a memory array of arbitrary size to read, write, refresh and otherwise operate the memory array. Even though a 3x3 array is shown, it should be noted that this invention is not restricted to any particular number of anode and cathode access lines or memory cells. In this exemplary memory array, individual memory cells 72 are each connected to an anode line AL and a cathode line KL. For example, memory cell 72kn is connected to anode line ALk and to cathode line KLn.

[52] In Figure 11A, as well as in the next series of figures, the "selected" memory cell for a memory array operation is the central cell 72jm. The goal of the operation described with respect to Figure 11A is to write a bit of data (a logic '0') to the selected cell without disturbing the contents of the other memory cells. For illustrative purposes sample data stored in the other cells of the array is shown in the figure for each cell. For example cell 72im is 'on' storing a '0', while cell 72kn is 'off' storing a '1'.

[53] Each anode and cathode line in Figure 11 shows the voltage applied to that line to implement the desired operation – writing a logic state '0' (thyristor 'on') to cell 72jm. It should be noted that voltage ranges described here are for illustrative purposes only because the precise voltages used in a particular implementation depend upon the actual geometrical design and also the precise doping concentrations for meeting the target product specification. In addition, each of the voltage levels can be shifted up or down as long as the voltage differential between anode and cathode lines remains the same.

[54] To write a '0', the non-selected anode lines ALi and ALk are held at a potential on the order of 1.8-2.1 volts while the selected anode line ALj is raised to 2.4-3 volts. The non-selected cathode lines KLl and KLn are held at 1.2-1.5 volts, while the selected cathode line KLm is pulled down to ground potential. The effect of these potentials is to apply a potential of 2.4-3 volts across the anode and cathode of selected thyristor 72jm, which is sufficient to turn it on, representing a '0' state. All of the cells at non-selected ALs and non-selected KLs have a potential between their anodes and cathodes of about 0.6 volts, which is designed to be the standby or hold voltage, leaving the data stored by those thyristors unchanged. For cells at a selected AL/non-selected KLs or a selected KL/non-selected ALs, a potential of 1.2V~2.1V is seen between their anodes and cathodes and its upper limit is determined by the trigger voltage from a '0' state to a '1' state.

[55] One potential disadvantage of the write '0' bias scheme of Figure 11A is the sneak leakages from the '0' cells (72im and 72jl) on selected ALj or KLm because the voltage differential across their anode and cathode is higher than the standby voltage. In yet another embodiment, Figure 11B shows an alternative write '0' operation which employs a half-select scheme. In this alternative approach, all non-selected ALs and KLs are biased at half of the selected anode voltage level. As a result, cells at non-selected ALs and non-selected KLs are biased at 0 volts across their respective anode and cathode.

[56] Figure 12 is a circuit schematic of the exemplary array of memory cells using the same notation as in Figures 11A and 11B to illustrate the potentials for writing a logic '1' to the selected memory cell 72jm. The potentials on the various anode and cathode lines to

write a '1' on thyristor 72jm are shown. The non-selected cathode lines KLl and KLn are held at ground potential, while the non-selected anode lines are held at a potential of 0.5-0.7 volts. In a first embodiment, the selected cathode line is raised to 1.8-2.0 volts and the selected anode line is pulled to ground potential. Alternatively, potentials at ALs and KLs can be level shifted for the benefit of decoder and driver designs. For example, bias voltage on selected ALj and non-selected KLs can be raised from 0V to 0.6V and bias voltages on selected KLm and non-selected ALs are also increased by 0.6V.

[57] Figure 13A is a circuit schematic of an array of memory cells using the same notation as in Figure 12 to illustrate the potentials on the anode and cathode lines for reading the logic state of a memory cell. In this case the non-selected anode lines Ali and ALk are held at a potential of 0.5-0.7 volts, while all the cathode lines, both selected and non-selected, are grounded. The selected anode line is raised to 1.0-1.4 volts.

[58] If the selected thyristor 72jm was previously programmed 'on', i.e. a logic state of '0', then the applied potential between its anode and cathode will turn it on and pull cathode line KLm to a higher potential. A well-known sense amplifier coupled to cathode line KLm detects this rise in potential. The increase in potential is interpreted as indicating the thyristor was at a logic state of '0'. On the other hand, if the selected thyristor 72jm was previously programmed 'off', i.e. a logic state of '1', then the applied potential between its anode and cathode will not be sufficient to turn it on. In this case the sense amplifier will not detect any rise in potential of cathode line KLm. The absence of change in the potential of the cathode line is interpreted as indicating the thyristor was at a logic state of '1'. Alternatively, the logic state of a selected memory cell can also be sensed from the anode line because the same current flows into the anode and comes out of the cathode.

[59] Figure 13B shows another embodiment for reading the stored logic state in the memory cells. In this approach an entire column is read in one cycle. aAl non-selected cathode lines (KLs) are biased at 0.5-0.7V or their standby levels and selected anode lines are pre-charged to a pre-determined read voltage level above the standby voltage. An exemplary range is 1~1.4V which drives sufficient cell current through cells storing '0' data. Sense amplifiers coupled to selected ALs detect any potential drops for the '0' logic states. Conversely, logic state '1s' are detected if cells on selected anode lines are previously programmed 'off'. Therefore there is no potential drop due to non-conducting cells. If it is desired to read only a limited number of cells in the column, then the non-selected ALs are biased at 05-0.7v thereby reducing the leakage.

[60] Individual thyristors in an array will, over time, gradually lose their stored data due to leakage currents. While this leakage is substantially less than occurs in a conventional one-transistor one-capacitor DRAM memory cell, to overcome the leakage current, the array can be placed in a standby state so that the stored data is retained. Figure 14 illustrates the potentials applied to the anode and cathode lines to retain the stored data in an array of thyristor memory cells. In this state all anode lines are held at 0.5-0.7 volts and all cathode lines are grounded. In this condition the 'off' thyristors are not affected, while the 'on' thyristors are continuously charged to the 'on' state. Because this standby state continuously consumes power, there is a trade-off between maintaining the thyristors in standby versus allowing discharge and periodically refreshing the array. In our preferred implementation, we refresh the entire array from 1 to 10 times per second. This is far less frequent than a conventional FET based DRAM requires refreshing - a particular advantage of this invention.

[61] Figures 15A and 15B illustrate another embodiment of the thyristor memory cell of this invention. In this embodiment sidewall NMOS gates 80 are added to the deep trenches of the structure. The remaining regions of the structure are the same as described above with regard to Figures 4-8. The benefit of adding gates 80 is to increase write speed and reduce write voltage. Because addition of the gates increases process complexity, use of the gates is dependent on the particular application expected for the memory array.

[62] The gates 80 may be formed in the deep trenches by first performing the deep silicon etch as described above with regard to Figure 5. The sidewalls of the trench are then oxidized – thereby forming the gate oxide that isolates the gate electrodes from the doped regions 32, 59, and 57. The trenches are then partially filled with silicon dioxide, e.g. by a chemical vapor deposition process. Then a conformal-doped polycrystalline silicon layer is deposited across the structure. After an anisotropic etching step removes the entire conformal polycrystalline silicon layer except as shown in Figure 15A, another trench filling operation is performed to finish filling the trenches. Appropriate planarization steps are then performed, e.g. using chemical mechanical polishing or other techniques. Later in the process an electrical connection is made to couple the gates 80 to control gate lines (GLs).

[63] Figure 16 is a circuit schematic showing an array of thyristor memory cells 72 with the addition of gates 80 as described above. The gates 80, when turned on by gate line GL, short out the NPN transistor 82 connecting the base of the PNP transistor 83 to the cathode line KL. This approach has the advantages described above – reducing the write voltage and allowing faster writes of data.

[64] Figure 17 illustrates another embodiment of vertical thyristor cell with two sidewall PMOS gates 86 in the deep trenches. These are formed in the same manner as gates 80 described above. The buried gates 86 can be connected at the pick-up regions and coupled to gate lines (GLs). These gates are formed in the same manner as described above. After a deep silicon trench-etching step, the trench gate oxide is formed. The trench is then partially filled with silicon dioxide to a depth above the N-cathode/P-base junction. A conformal conductive gate layer of, e.g. doped polycrystalline silicon is then formed. The gate layer is then anisotropically etched to form a sidewall gate completely covering the N-type base. Finally the trench is filled with silicon dioxide and then planarized, using well know technology.

[65] Figure 18 is a circuit schematic of a memory array in which the PMOS gates 86 of Figure 17 are used. The gates 86, when turned on by gate line GL, short out the PNP transistor 83 connecting the base of the NPN transistor 82 to the anode line AL. This approach has the same advantages as discussed above for the NMOS gates.

[66] One potential issue with respect to using an array of thyristors as memory cells is the requirement for higher row currents during access operations to read the memory cells. (Here we use the word 'row' as synonymous with anode, and 'column' as synonymous with cathode. Word line and bit line could also be used.) To reduce the need for higher row currents we use a technique we refer to as rolling the word line. This approach is described in conjunction with Figure 19.

[67] Figure 19A shows a row of thyristor memory cells in a memory array. The row consists of N columns of memory cells that are divided into M groups of cells. One group of 4 cells is shown at the left end of the row. The use of 4 cells for a group is merely an example; in an actual integrated circuit many more than 4 cells will be in a group. To access the cells, e.g. for reading data from them or writing data to them, a voltage VSelected is applied to the column lines of all members of the group. All of the other column lines receive a potential of VHold, where VHold is higher than VSelected. The result is that the selected group will have a current of:

[68] I group selected = M *I Selected   where I Selected is the current for one cell

[69] The remaining N/M – 1 groups of cells in the row will have a current of:

[70] I group hold = (N/M-1) * M * I hold   where I Hold is the current for one cell

[71] In use of the memory array, the procedure is to apply the selected potential for the desired operation to the first group while biasing all remaining groups to 'hold.' Once the desired operation on the first group is finished, the bias on the first group is changed to 'hold'

and the bias on the next group is changed to the selected potential, such as shown by Figure 19B. By repeating these steps of holding all groups of cells on a word line at the 'hold' potential except the selected group, and repeating this group-by-group, the row current is reduced. We refer to this technique as 'rolling' the word line.

[72] For memory cells with highly non-linear current versus voltage relationships, the holding current for a cell can be orders of magnitude lower than the selected cell read current. For example, assume a row has 128 columns divided into 8 groups, each group having 16 cells. In a typical implementation the select current will be about 10uA, while the hold current will be about 10pA, that is a factor of six orders of magnitude. Therefore:

[73] Without rolling: I row = 128 * 10uA = 1.28mA

[74] With rolling: I row = 16 * 10uA + (128-16) * 10pA = 160uA

[75] Thus rolling the word line in the manner described provides an 88% reduction in word line current, and 8 rolling accesses to access the complete row.

[76] Because each thyristor cell in a memory array that is 'on' will dissipate some current, current consumption by the memory array, and the number of such 'on' cells depends on the particular data being stored in the array. This has the undesirable effect of linking power consumption to the actual data stored in the memory. Data encoding with an objective of maintaining approximately 50% of the cells as logic '1' can be used to reduce this standby current.

[77] For example, consider an 8-bit word with 2 additional parity bits.

[78] Parity = 00 no change

[79] Parity = 01 invert lower 4 bits

[80] Parity = 10 invert upper 4 bits

[81] Parity = 11 invert all bits

[82] In the following examples the parity bits are the first two bits preceding the stored word of data and are in italics.

[83] Example 1: all ones: 1111_1111 becomes 10_0000_1111, thus 8 ones become 5 ones.

[84] Example 2: 50%+1 one: 1010_1011 becomes 01_1010_0100, thus 5 ones become 4 ones.

[85] Example 3: 50% ones: 1010_1010 becomes 00_1010_1010, thus 4 ones become 4 ones.

[86] Example 4: 50%-1 ones: 0010_1010 becomes 00_0100_1010, thus 3 ones become 3 ones.

[87] Example 5: all zeros: 0000_0000 becomes 10_1111_0000 thus 0 ones become 5 ones.

[88] Example 6: 5 ones: 0011_1011 becomes 11_1100_0100 thus 5 ones become 3 ones.

[89] The above data encoding techniques, or other similar approaches, are useful where the array standby current is to be maintained at a relatively constant level, and used for a current source controlled standby operation. Conventional logic circuitry can be used to detect the number and position of the ones, perform the desired inversions (or not) and add the parity bits to the stored data.

[90] In the embodiment associated with Figure 14, data stored in the thyristor memory array are maintained in standby by supplying a hold voltage or current so that refresh is not needed. Under these standby conditions, all memory cells holding '0' data conduct a very low, but finite current. Due to the exponential relationship between hold current and hold voltage, it is advantageous to use a current source to keep cells alive in standby. One approach is described in our earlier patent applications, for example, U.S. Patent Application 14/590,834 entitled "Cross-Coupled Thyristor SRAM Circuits and Methods of Operation," filed January 6, 2015, which is incorporated herein by reference. There we described a technique of maintaining data retention at a low standby current using a constant current source to bias the array to the optimum holding voltage. While this approach was discussed in conjunction with SRAM memory, it can also be used with other thyristor-based volatile memories such as the ones described here.

[91] Under bias schemes described above, all memory cells holding '0' data conduct a very low but finite current in order to maintain the array data without the need for refresh. An alternative approach is to adjust the current provided to an even lower value that is not sufficient to maintain the data integrity indefinitely, but which is sufficient to maintain it for a minimum "retention" period – e.g. 1msec. This approach allows a significant reduction in the standby current. To maintain the integrity of the data indefinitely, however, a background refresh operation is performed on a sector by sector basis where the set holding current for a sector is increased to a higher value for a short period to re-establish the cell levels to a better value, but then reduced back to the normal standby current. This allows all the cells in the sector to be refreshed simultaneously, rather than on a row-by-row basis as is currently done with conventional DRAMs. Further, the refresh does not interfere with normal read/write operations, making the refresh operation externally invisible. This approach is shown in Figure 20.

[92] The figure illustrates how one refresh pulse can refresh an entire sector. The refresh pulse applied to line 90 when the CMOS switches 92 are on will refresh the sector of memory cells 72. This example illustrates current controlled standby/refresh, however, the same approach can be applied to voltage-controlled standby/refresh.

[93] Figure 21 is a circuit schematic illustrating one technique for reading data from the thyristor array. A sense amplifier 95 has one input connected to a column of memory cells 72 of the memory array. The other input of the sense amplifier 95 is connected to a column of dummy memory cells 94. The memory cells 72 and the dummy cells 94 have the column lines pre-charged to 0 volts. During a read operation the state of a programmed memory cell 72 will shift the potential of the column line up if the cell is a '0' or leave it near 0v if the cell is a '1'. The dummy memory cell's column line is shifted up by the current source at a rate ½ as fast as the column in selected array to generate differential data for the sense amplifier 95. If the selected cell is a '0', the selected column will rise above the dummy column. If the selected cell is a '1', the dummy column will rise above the selected column. The sense amplifier output can then be interpreted as a '1' or a '0' indicative of the stored data.

[94] This description of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form described, and many modifications and variations are possible in light of the teaching above. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications. This description will enable others skilled in the art to best utilize and practice the invention in various embodiments and with various modifications as are suited to a particular use. The scope of the invention is defined by the following claims.

Claims

The invention claimed is:

1. A volatile memory comprising:

a first plurality of row lines;

a second plurality of column lines; and

an array of vertical thyristors having anodes coupled to one of the row and column lines and having cathodes coupled to the other of the row and column lines.

2. A volatile memory as in claim 1 wherein each vertical thyristor comprises:

a substrate of first conductivity type;

a buried layer of opposite conductivity type extending in a first direction to provide a cathode of the thyristor and a first column line;

a first layer of first conductivity type disposed on the buried layer to provide a first conductivity type base of the thyristor;

a second layer of opposite conductivity type disposed on the first layer to provide an opposite conductivity type base of the thyristor;

an upper layer of first conductivity type to provide an anode of the thyristor; and

a conductive layer coupled to the anode of the thyristor and extending in a second direction orthogonal to the first direction to provide a first row line.

3. A volatile memory as in claim 2 further comprising:

a deep region of insulating material extending through the buried layer to the substrate in the first direction to separate columns of thyristors from each other; and

a shallow region of insulating material extending to the buried layer to separate rows of thyristors from each other.

4. A volatile memory as in claim 3 wherein:

the substrate comprises silicon;

each of the a first layer, the second layer, and the upper layer comprise portions of an epitaxial silicon layer; and

each of the deep region and the shallow region comprise silicon dioxide.

5. A volatile memory as in claim 4 wherein:

the first conductivity type is P; and

the opposite conductivity type is N.

6. A volatile memory as in claim 1 further comprising an NMOS transistor coupled to the thyristor.

7. A volatile memory as in claim 6 wherein:

each thyristor comprises a PNP transistor having an emitter, a base, and a collector, and an NPN transistor having an emitter, a base, and a collector;

the PNP emitter is coupled to the row line, the PNP base is coupled to the NPN collector, the PNP collector is coupled to the NPN base, and the NPN collector is coupled to the column line;

the NMOS transistor has one electrode provided by the NPN collector, another electrode provided by the NPN emitter, and a gate coupled to connect the NPN collector to the NPN emitter when the gate is on; and

the memory array includes gate lines coupled to the gates of a plurality of NMOS transistor gates.

8. A volatile memory as in claim 7 wherein the gate lines extend parallel to the column lines.

9. A volatile memory as in claim 1 further comprising an PMOS transistor coupled to the thyristor.

10. A volatile memory as in claim 9 wherein:

each thyristor comprises a PNP transistor having an emitter, a base, and a collector, and an NPN transistor having an emitter, a base, and a collector;

the PNP emitter is coupled to the row line, the PNP base is coupled to the NPN collector, the PNP collector is coupled to the NPN base, and the NPN collector is coupled to the column line;

the PMOS transistor has one electrode provided by the PNP collector, another electrode provided by the PNP emitter, and a gate coupled to connect the PNP collector to the PNP emitter when the gate is on; and

the memory array includes gate lines coupled to the gates of a plurality of PMOS transistor gates.

11. A volatile memory as in claim 7 wherein the gate lines extend parallel to the column lines.

12. A method of making a volatile memory array having row lines, column lines, and an array of vertical thyristors having anodes coupled to one of the row and column lines and having cathodes coupled to the other of the row and column lines, the method comprising:

introducing opposite conductivity type dopant into a first conductivity type semiconductor substrate to thereby provide a buried layer providing a cathode for each of the vertical thyristors;

forming a first conductivity type epitaxial layer on the buried layer;

removing all of the epitaxial layer and the buried layer to expose portions of the substrate from a first plurality of parallel regions extending in a first direction of the memory array to thereby form a first plurality of deep trenches;

filling the first plurality of deep trenches with insulating material;

removing all of the epitaxial layer to expose portions of the buried layer from a second plurality of parallel regions extending in a second direction of the memory array to thereby form a second plurality of shallow trenches;

filling the second plurality of shallow trenches with insulating material;

introducing opposite conductivity type dopant into an upper portion of the epitaxial layer to form upper opposite conductivity type regions separated from the buried layer by a lower portion of the epitaxial layer; and

introducing first conductivity type dopant into a top portion of the upper opposite conductivity type regions to form an anode for each of the vertical thyristors.

13. A method as in claim 11 further comprising a step of providing an electrical connection to the anode.

14. A method as in claim 12 wherein the step of providing an electrical connection comprises:

introducing a refractory metal into the anode; and

annealing the anode to thereby form a metal silicide layer.

15. A method as in claim 11 further comprising:

before the step of introducing first conductivity type dopant into a top portion of the upper opposite conductivity type regions, a step of forming a further epitaxial layer on an upper surface of the epitaxial layer; and

later providing electrical connections to the further epitaxial layer to provide connections to the anodes of the thyristors.

16. A method of making a volatile memory array having row lines, column lines, and an array of vertical thyristors having anodes coupled to one of the row and column lines and having cathodes coupled to the other of the row and column lines, the method comprising:

introducing opposite conductivity type dopant into a first conductivity type semiconductor substrate to thereby provide a buried layer providing a cathode for each of the vertical thyristors;

forming a first epitaxial layer of first conductivity type on the buried layer;

forming a second epitaxial layer of opposite conductivity type on the first epitaxial layer;

removing all of the first and second epitaxial layers and the buried layer to expose portions of the substrate from a first plurality of parallel regions extending in a first direction of the memory array to thereby form a first plurality of deep trenches;

filling the first plurality of deep trenches with insulating material;

removing all of the of the first and second epitaxial layers to expose portions of the buried layer from a second plurality of parallel regions extending in a second direction of the memory array to thereby form a second plurality of shallow trenches;

filling the second plurality of shallow trenches with insulating material; and

introducing first conductivity type dopant into a top portion of the second epitaxial layer to form an anode for each of the vertical thyristors.

17. A method as in claim 15 further comprising a step of providing an electrical connection to the anode.

18. A method as in claim 16 wherein the step of providing an electrical connection comprises:

introducing a refractory metal into the anode; and

annealing the anode to thereby form a metal silicide layer.

19. A method as in claim 15 further comprising:

before the step of introducing first conductivity type dopant into a top portion of the upper opposite conductivity type regions, a step of forming a further epitaxial layer on an upper surface of the second epitaxial layer; and

later providing electrical connections to the further epitaxial layer to provide connections to the anodes of the thyristors.

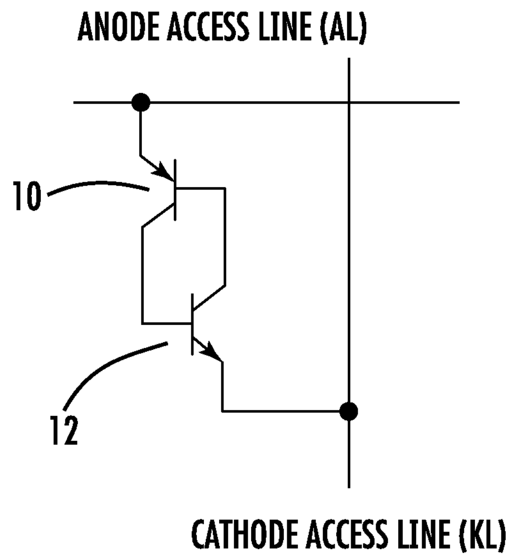

FIG. 1A

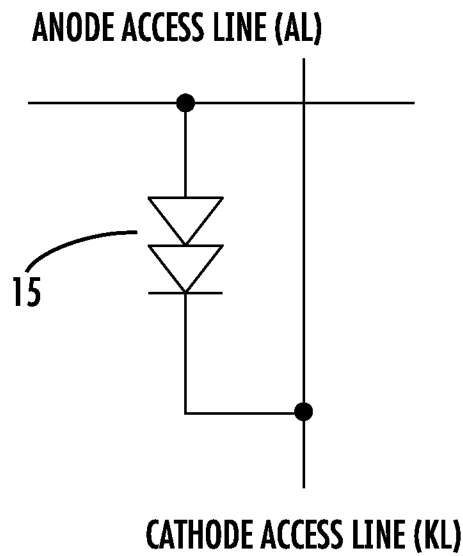

FIG. 1B

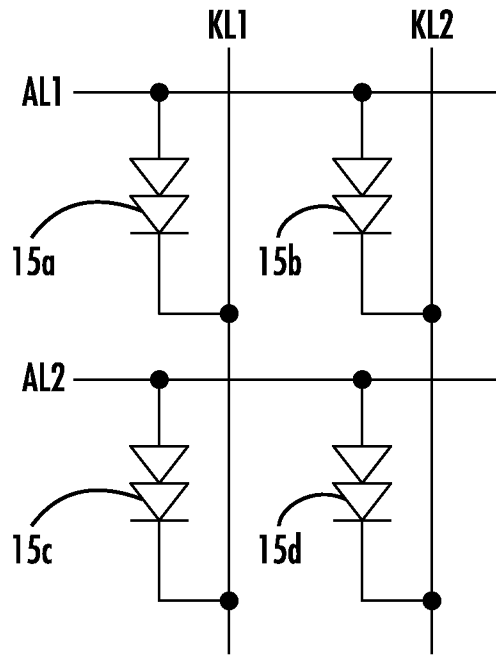

FIG. 2A

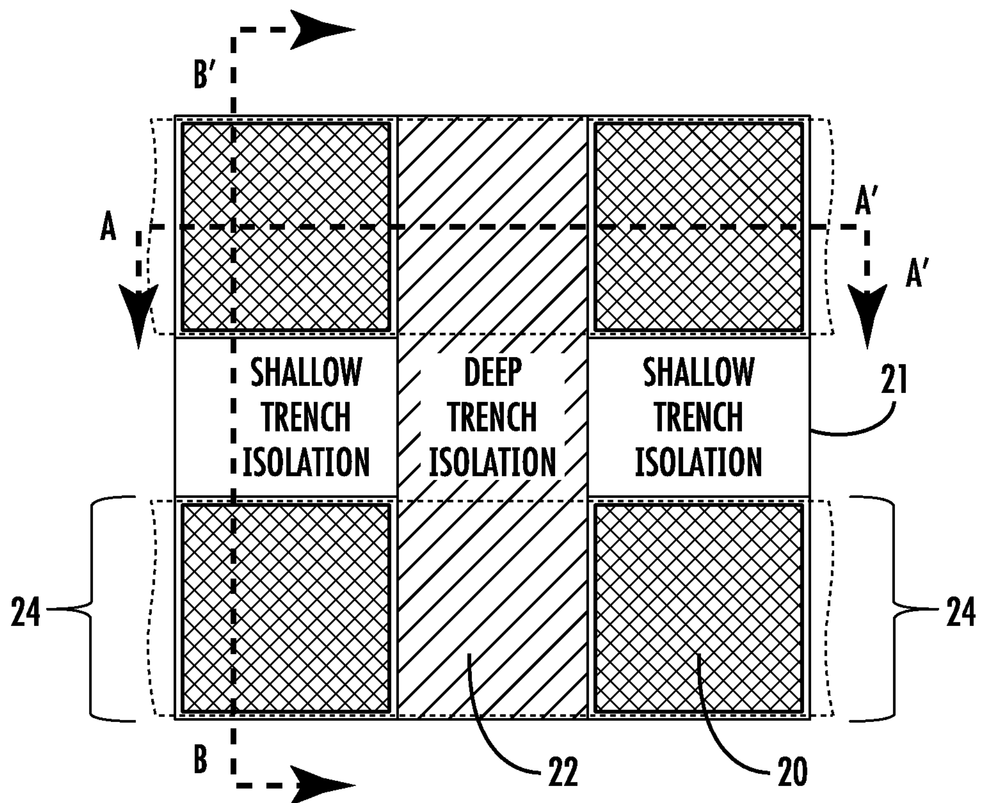

FIG. 2B

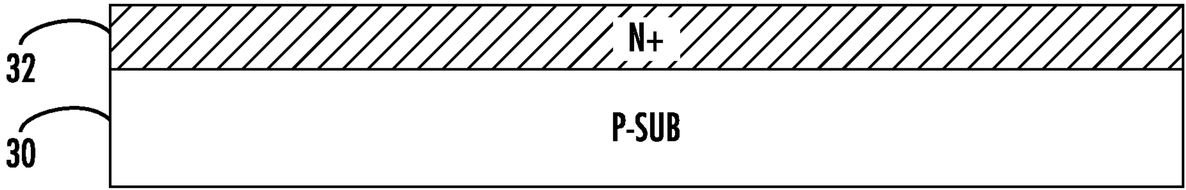

FIG. 3A (A~A′)

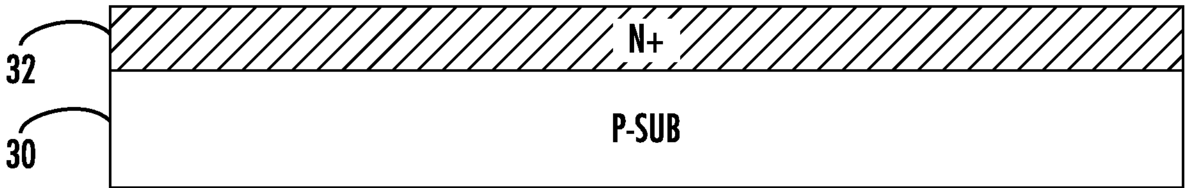

FIG. 3B (B~B′)

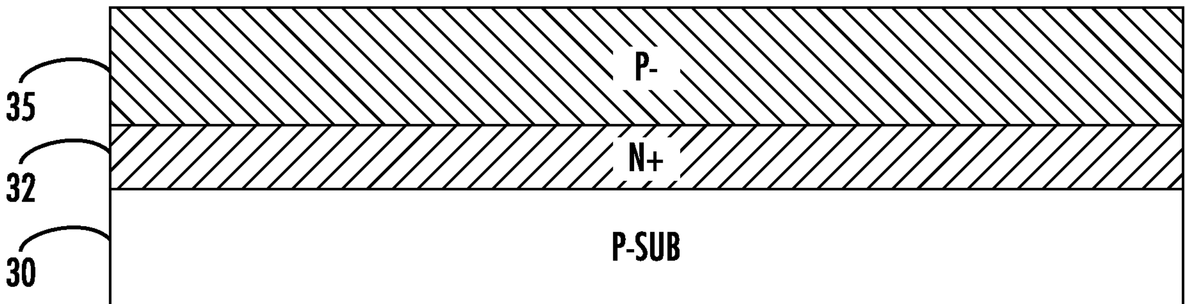

FIG. 4A (A~A′)

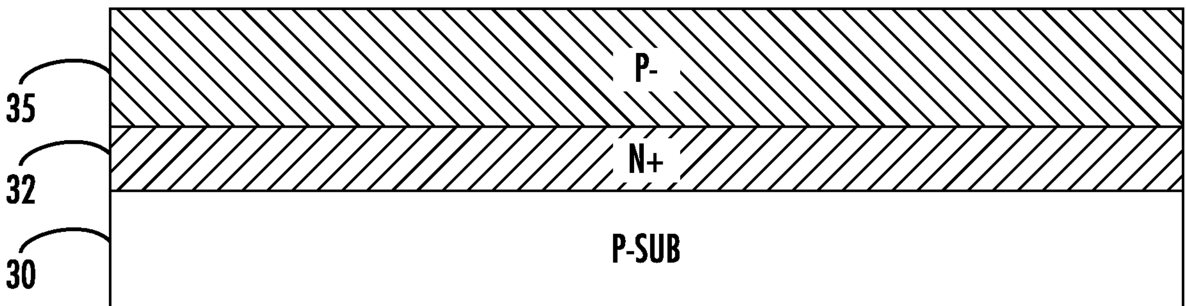

FIG. 4B (B~B′)

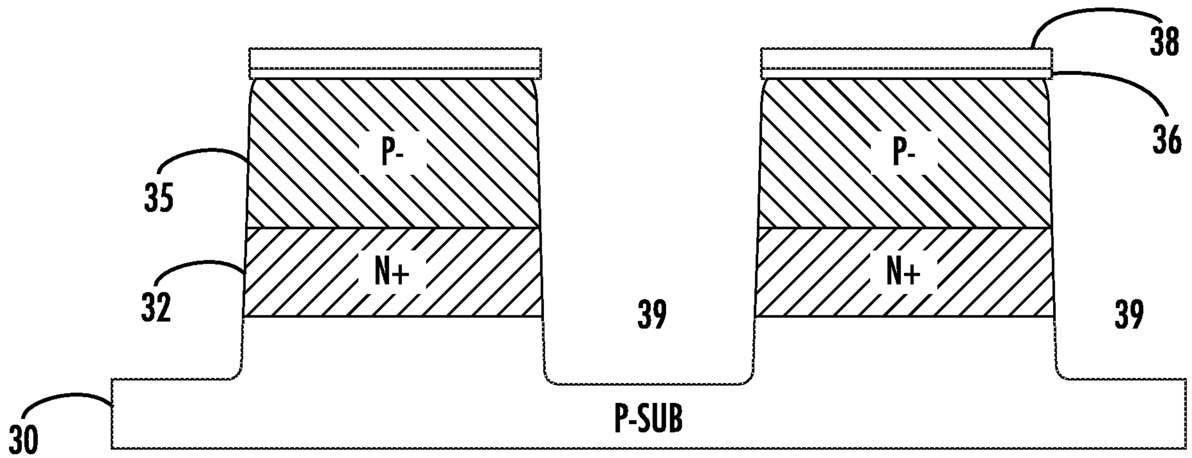

FIG. 5A (A~A')

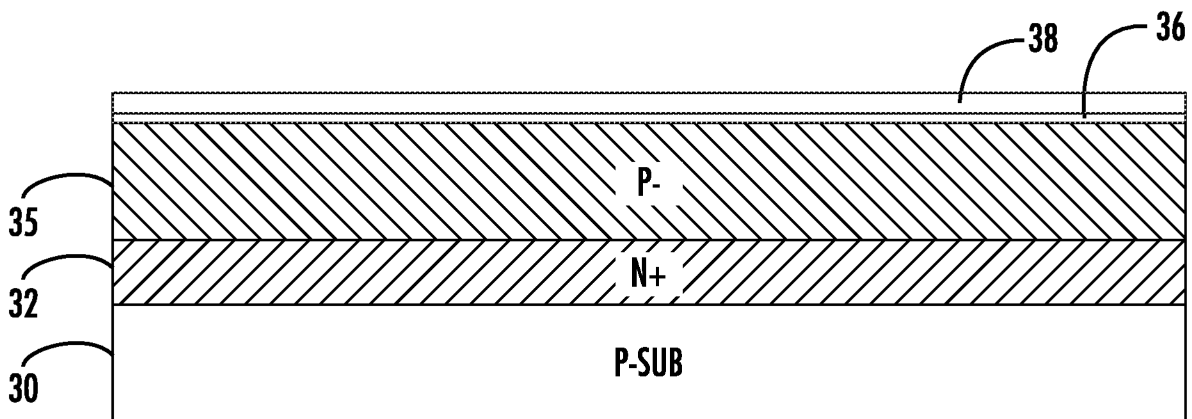

FIG. 5B (B~B')

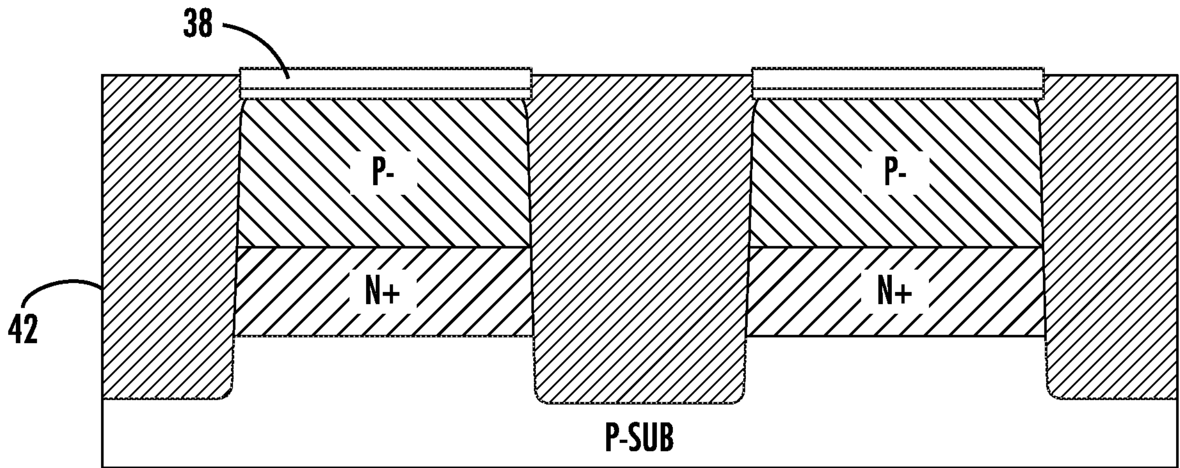

FIG. 6A (A~A')

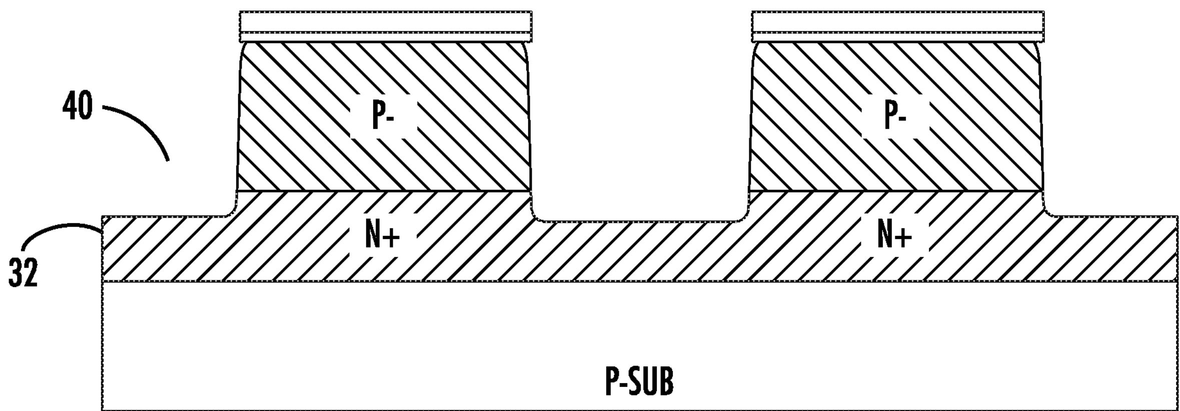

FIG. 6B (B~B')

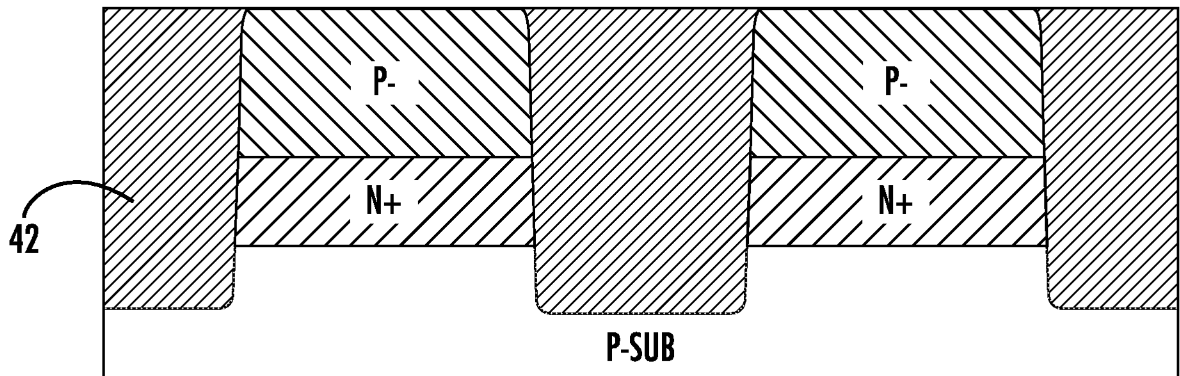

FIG. 7A (A~A')

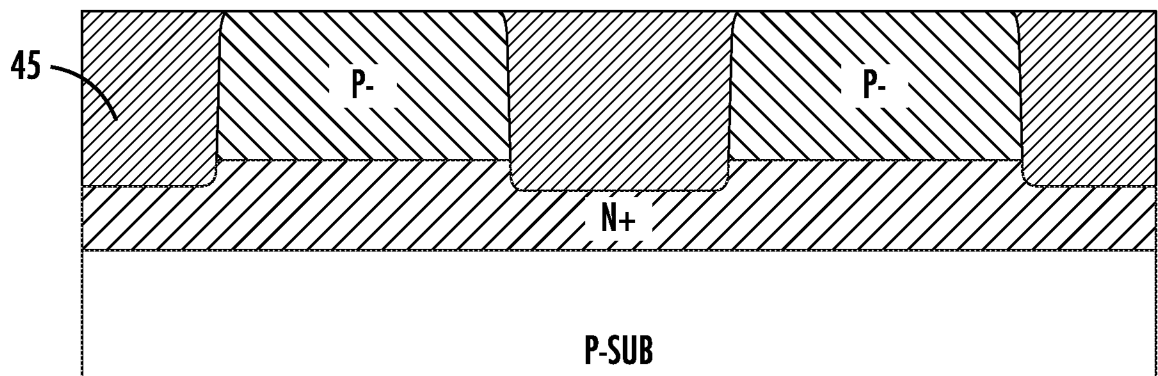

FIG. 7B (B~B')

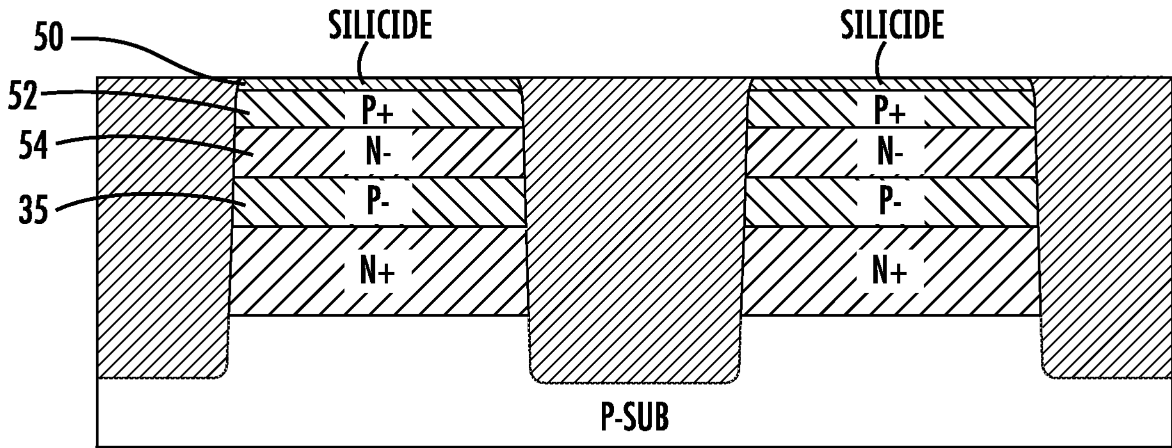

FIG. 8A (A~A')

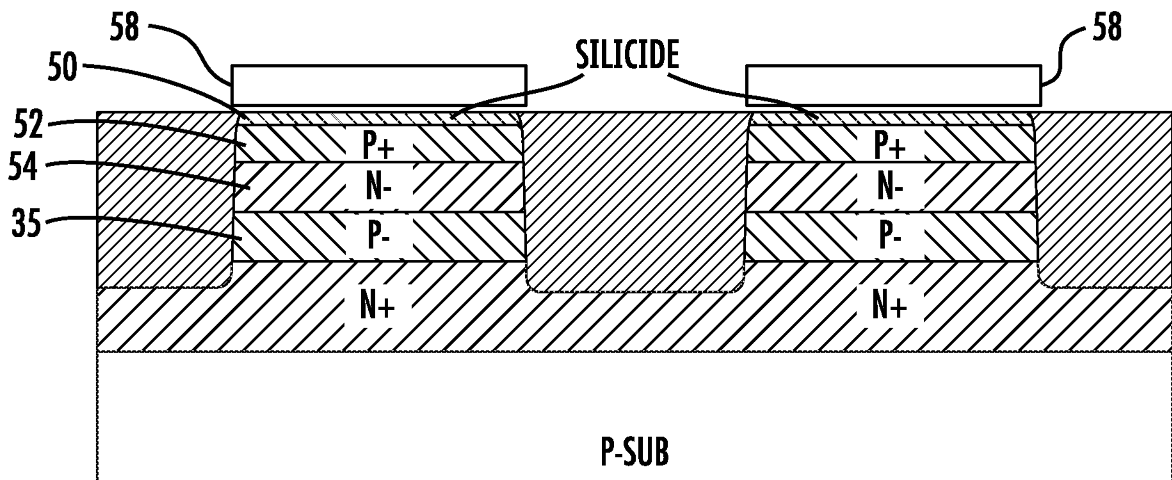

FIG. 8B (B~B')

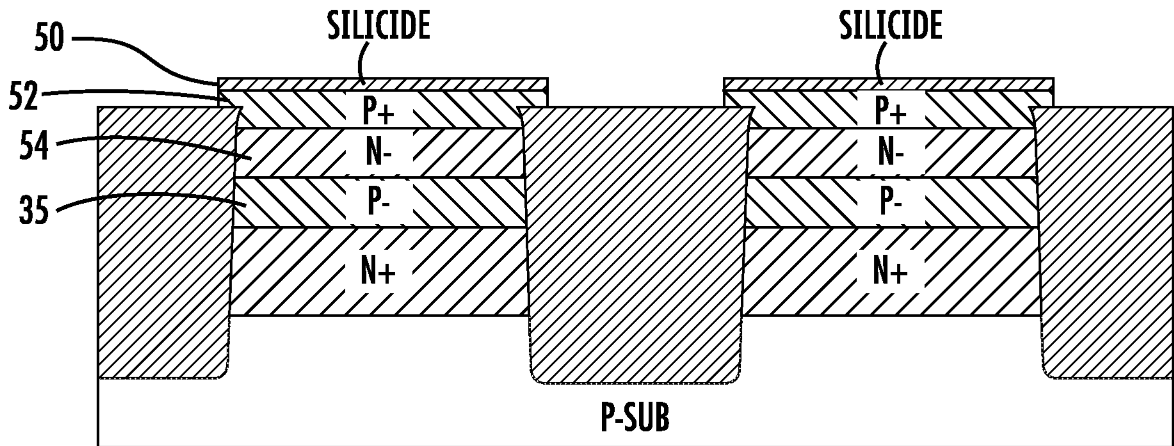

FIG. 9A (A~A')

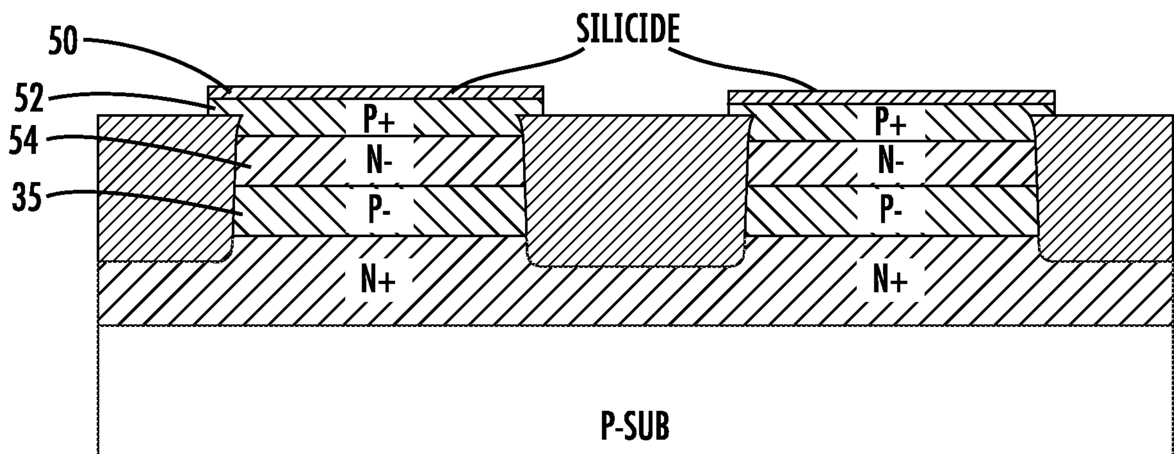

FIG. 9B (B~B')

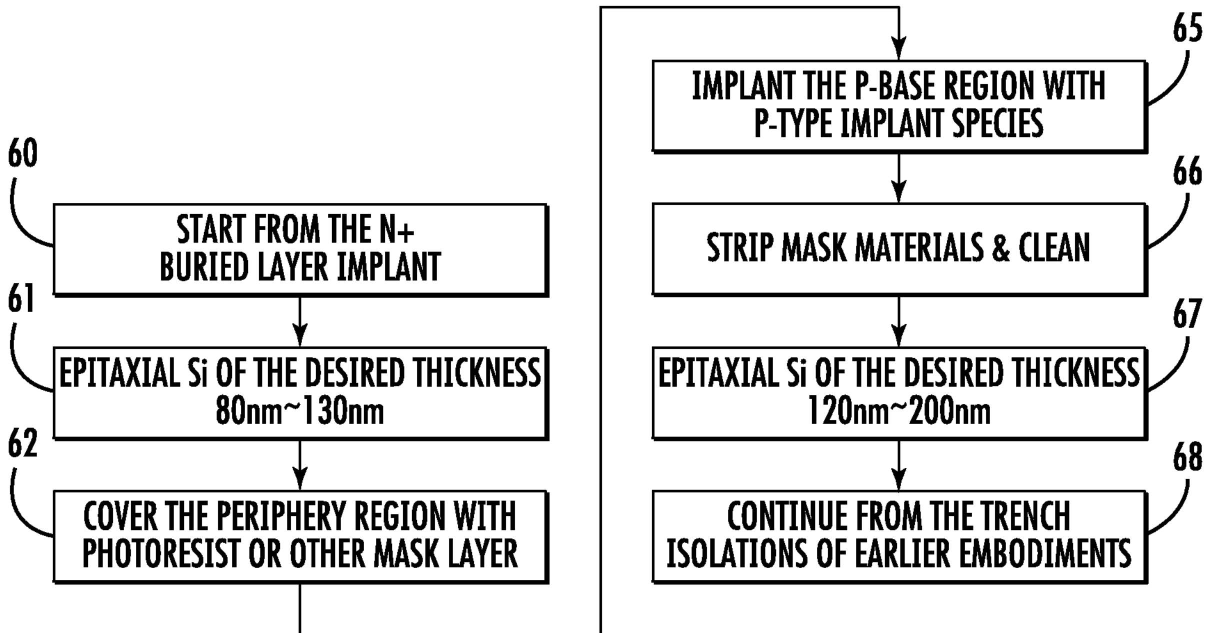

FIG. 10

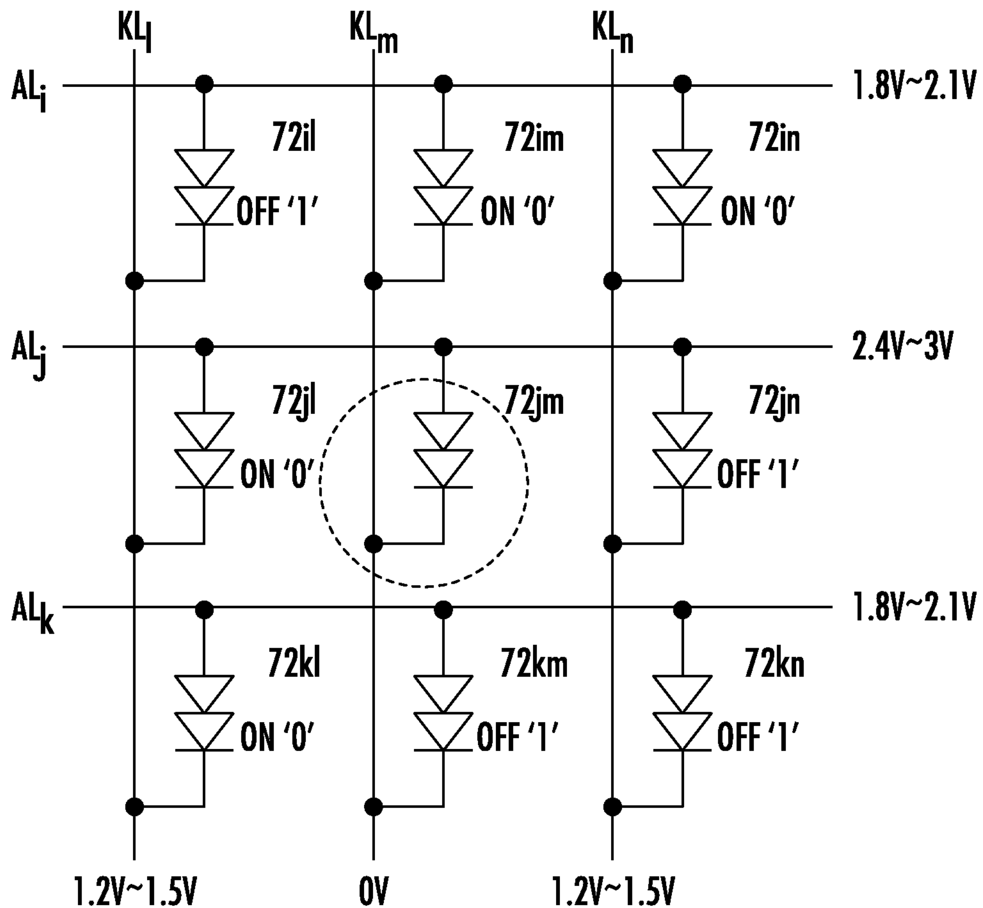

FIG. 11A

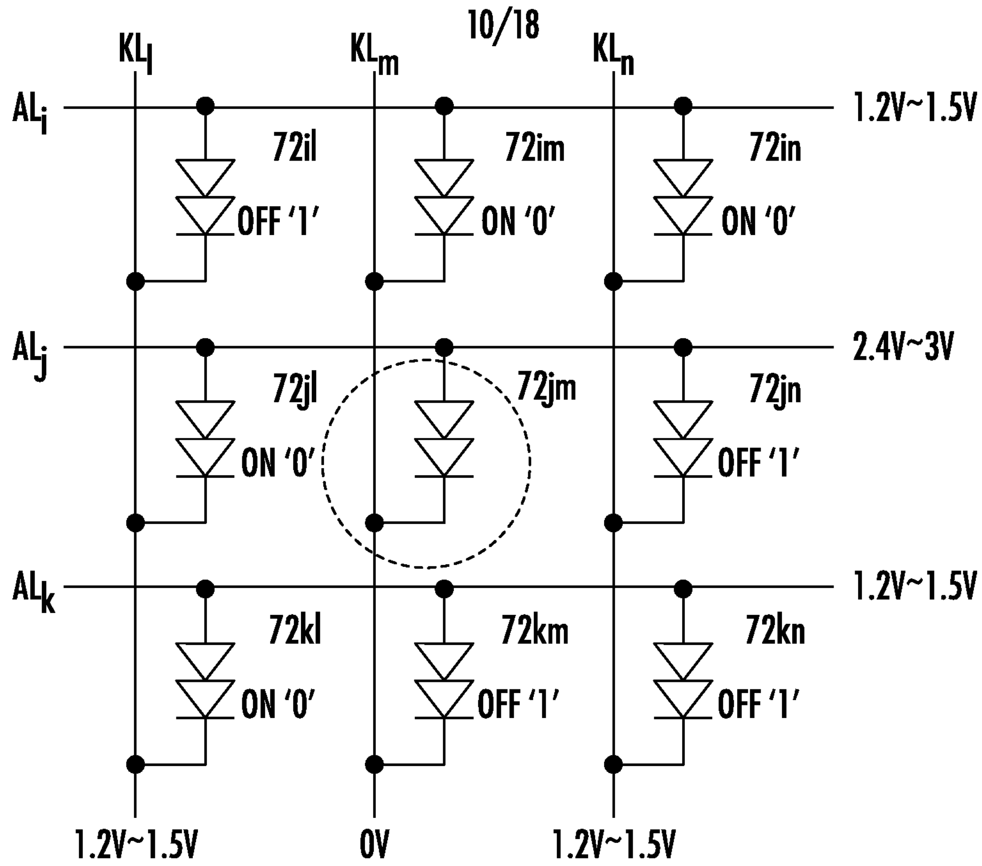

FIG. 11B

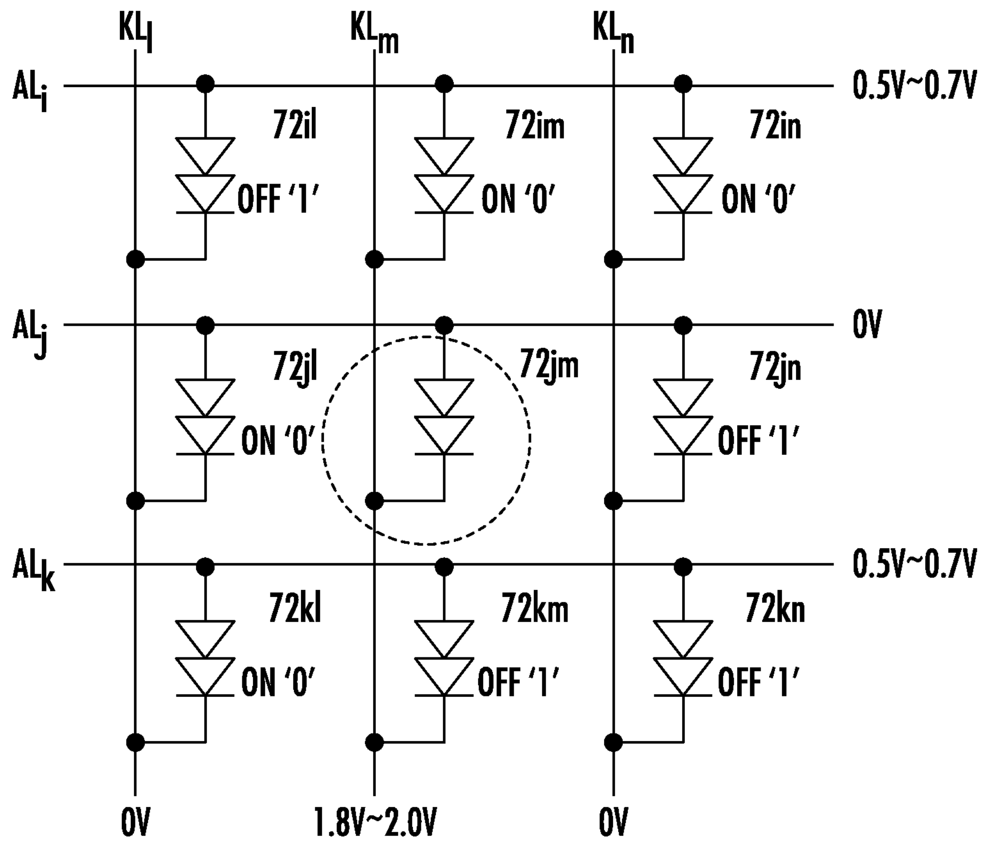

FIG. 12

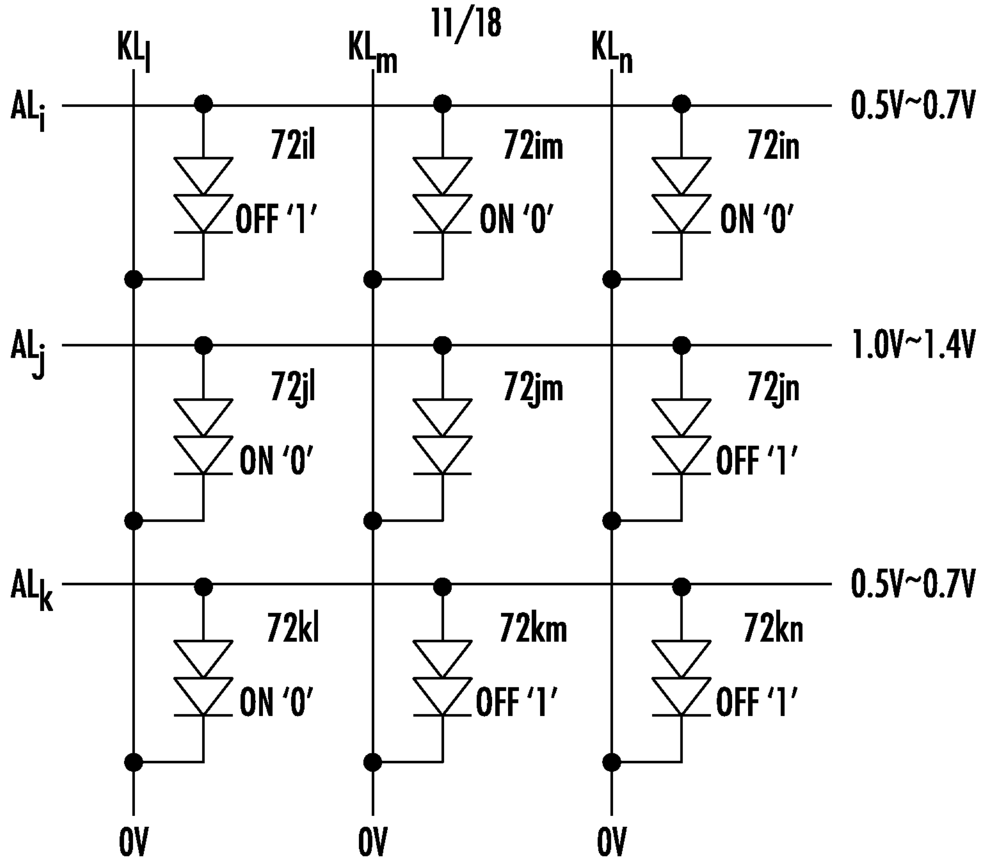

FIG. 13A

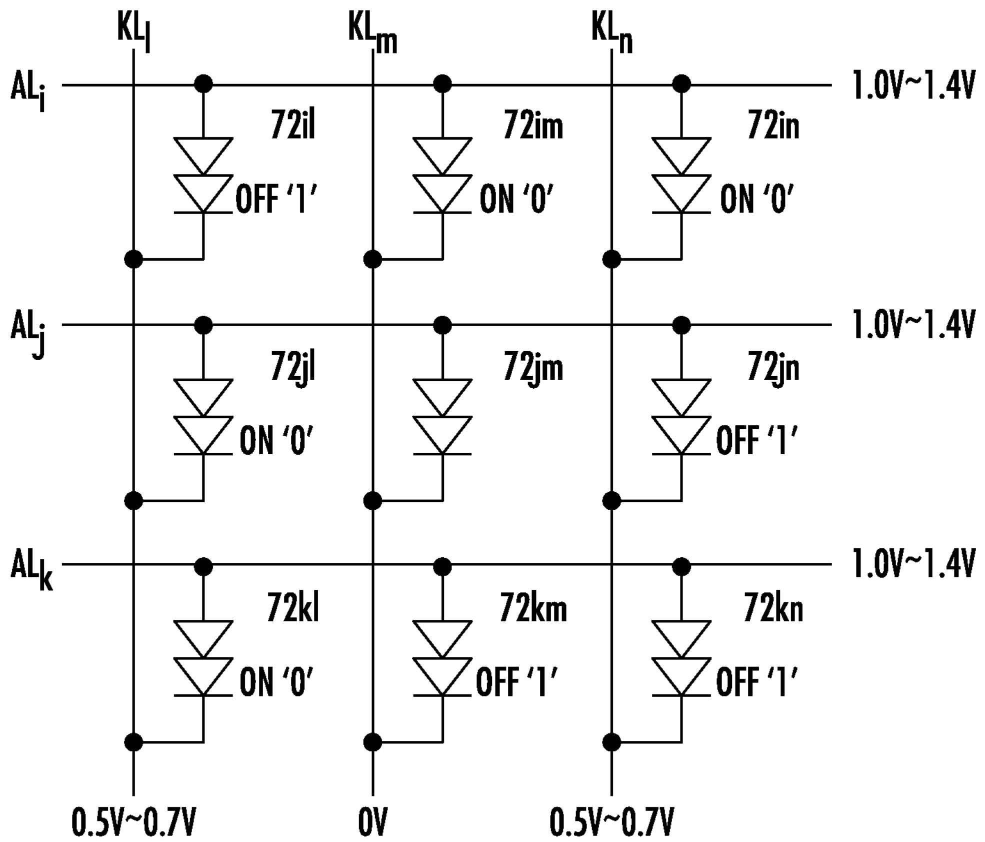

FIG. 13B

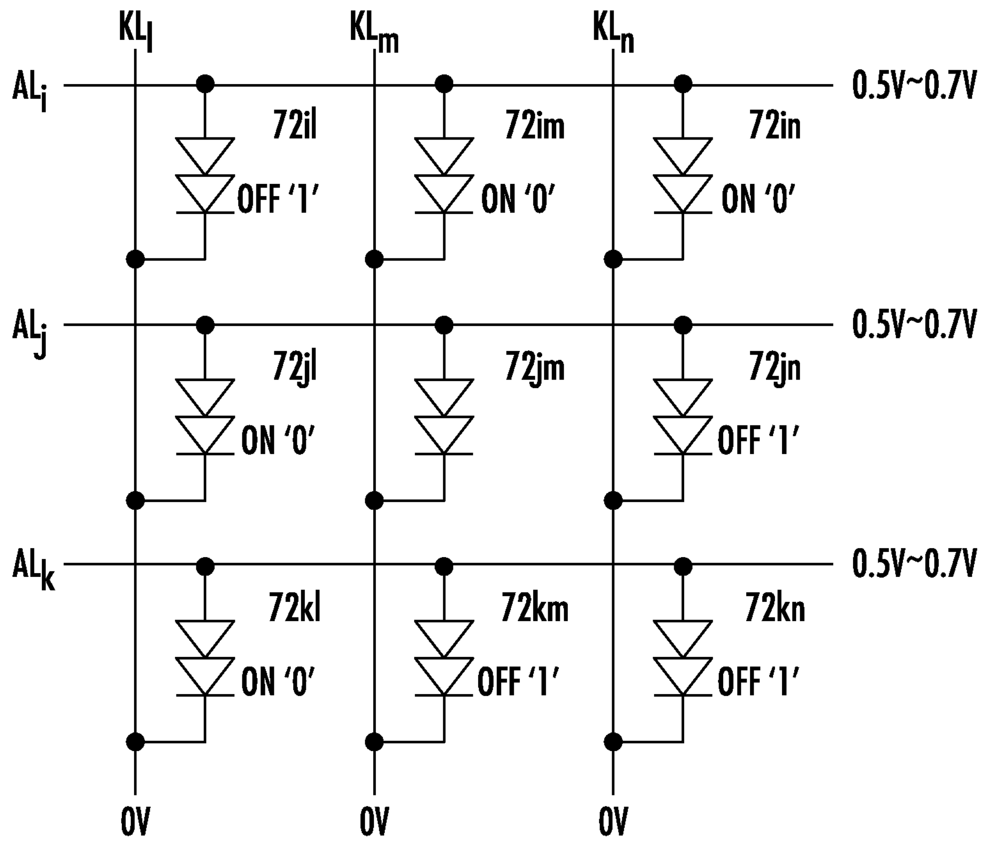

FIG. 14

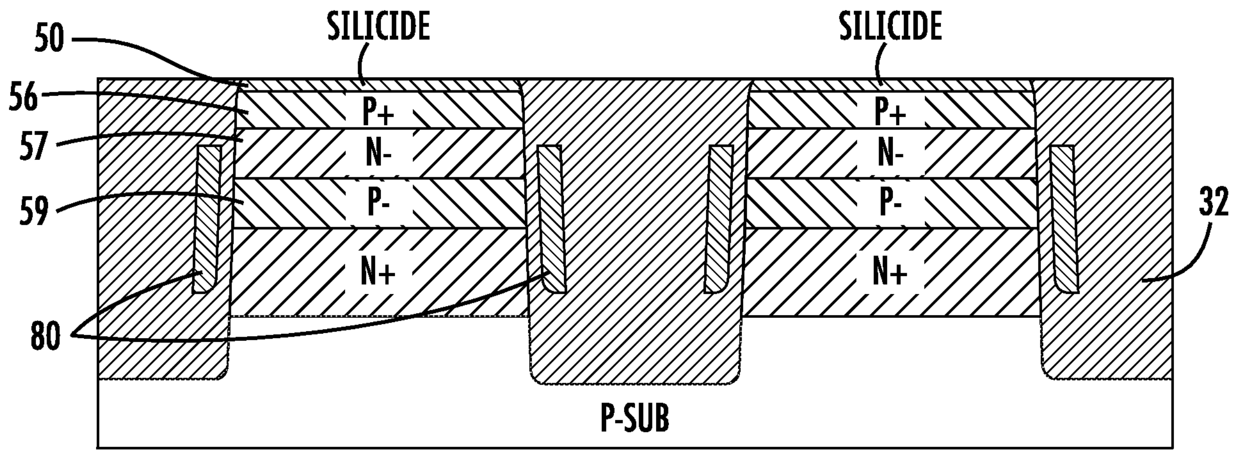

FIG. 15A (A~A')

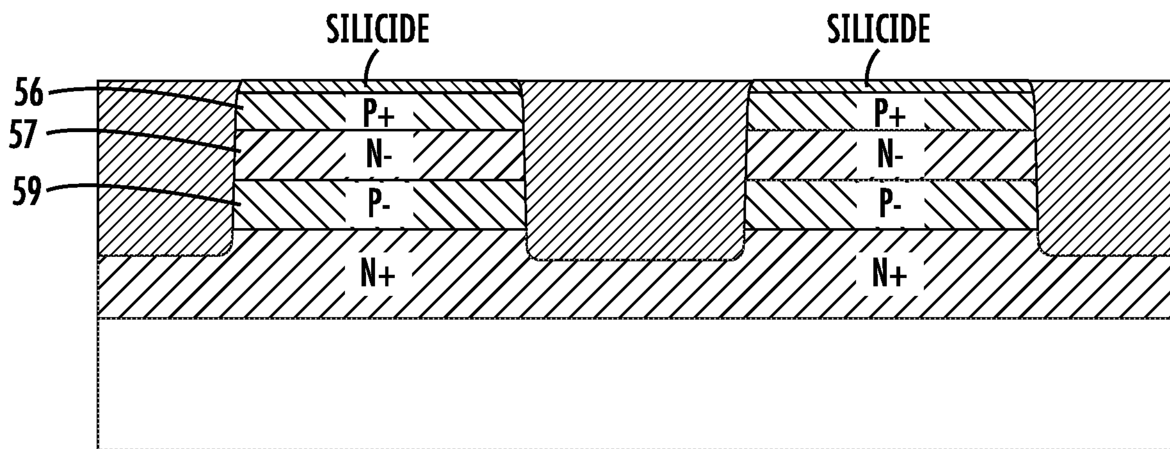

FIG. 15B (B~B')

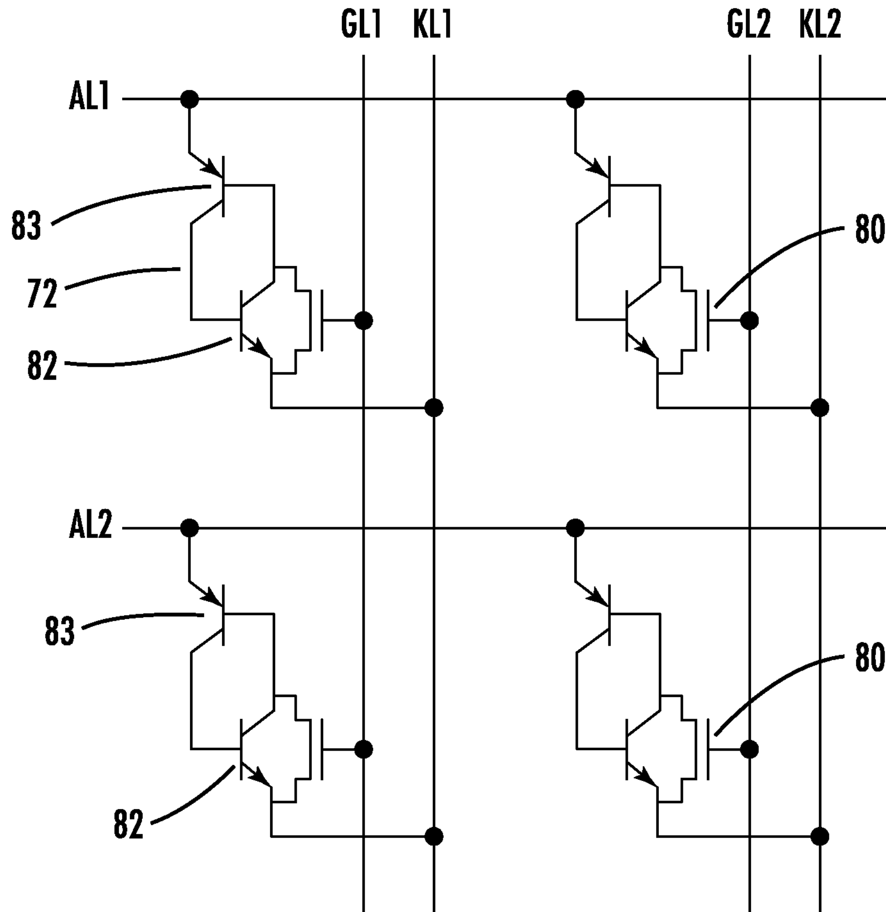

FIG. 16

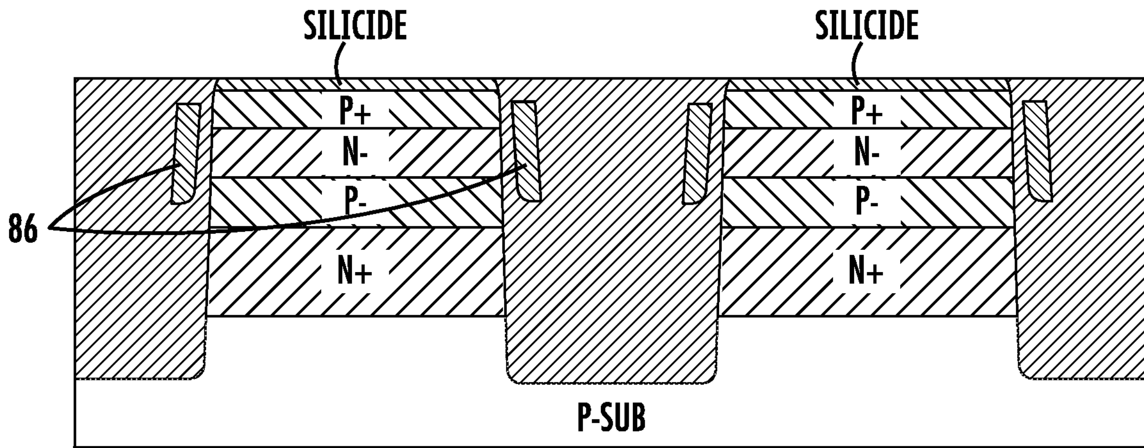

FIG. 17A (A~A')

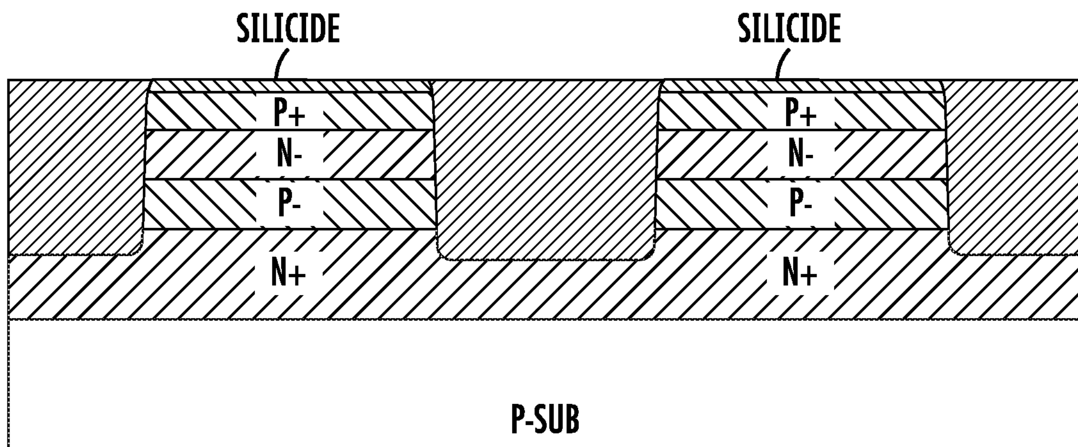

FIG. 17B (B~B')

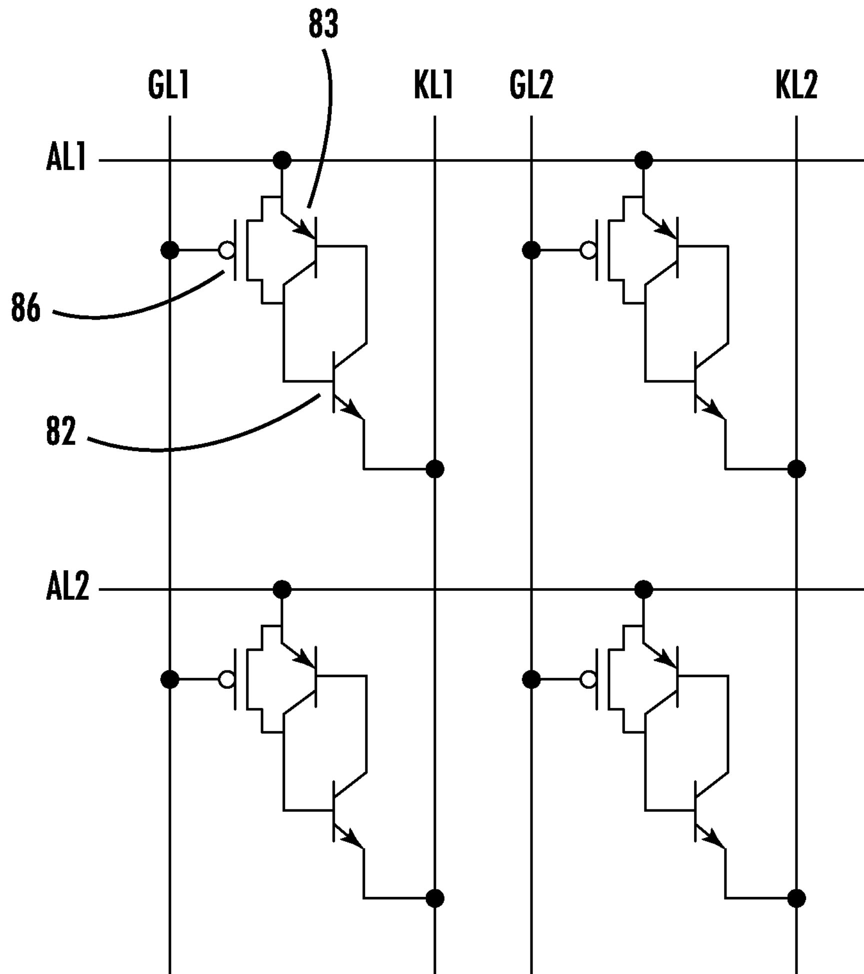

FIG. 18

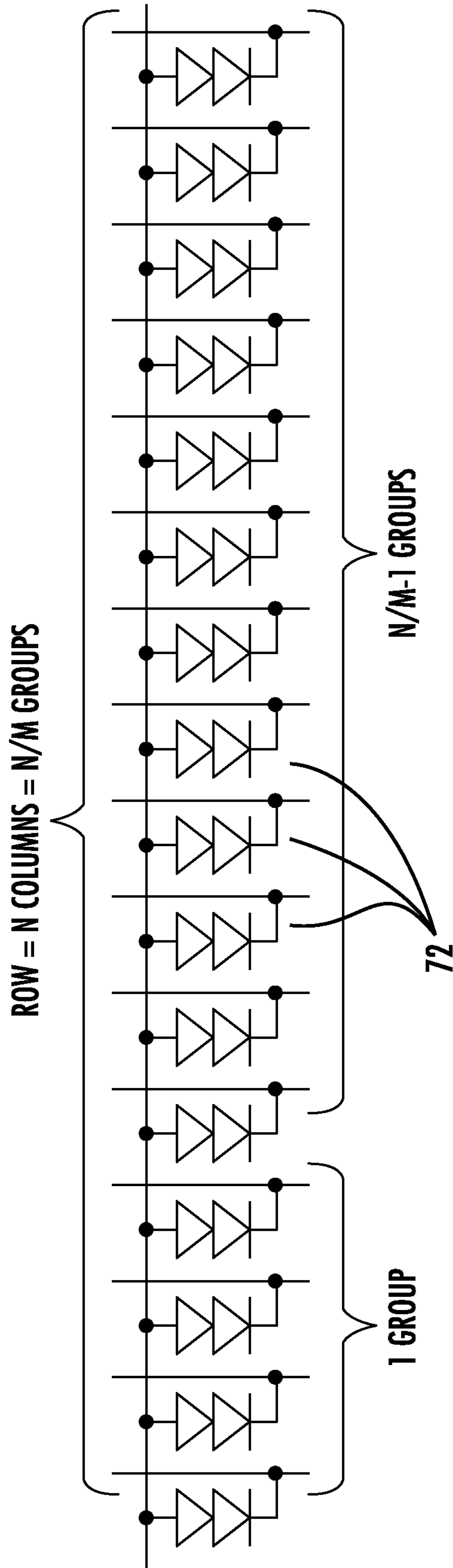

FIG. 19A

NEXT

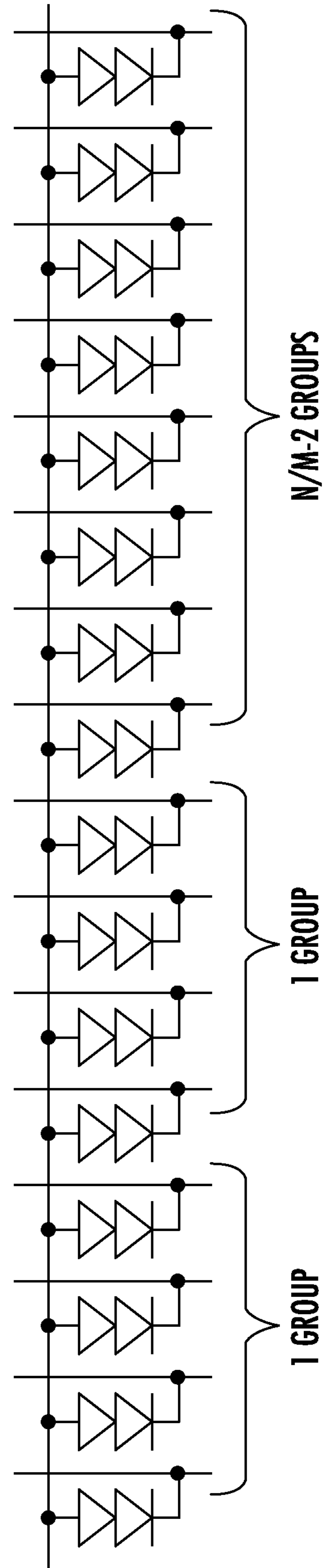

FIG. 19B

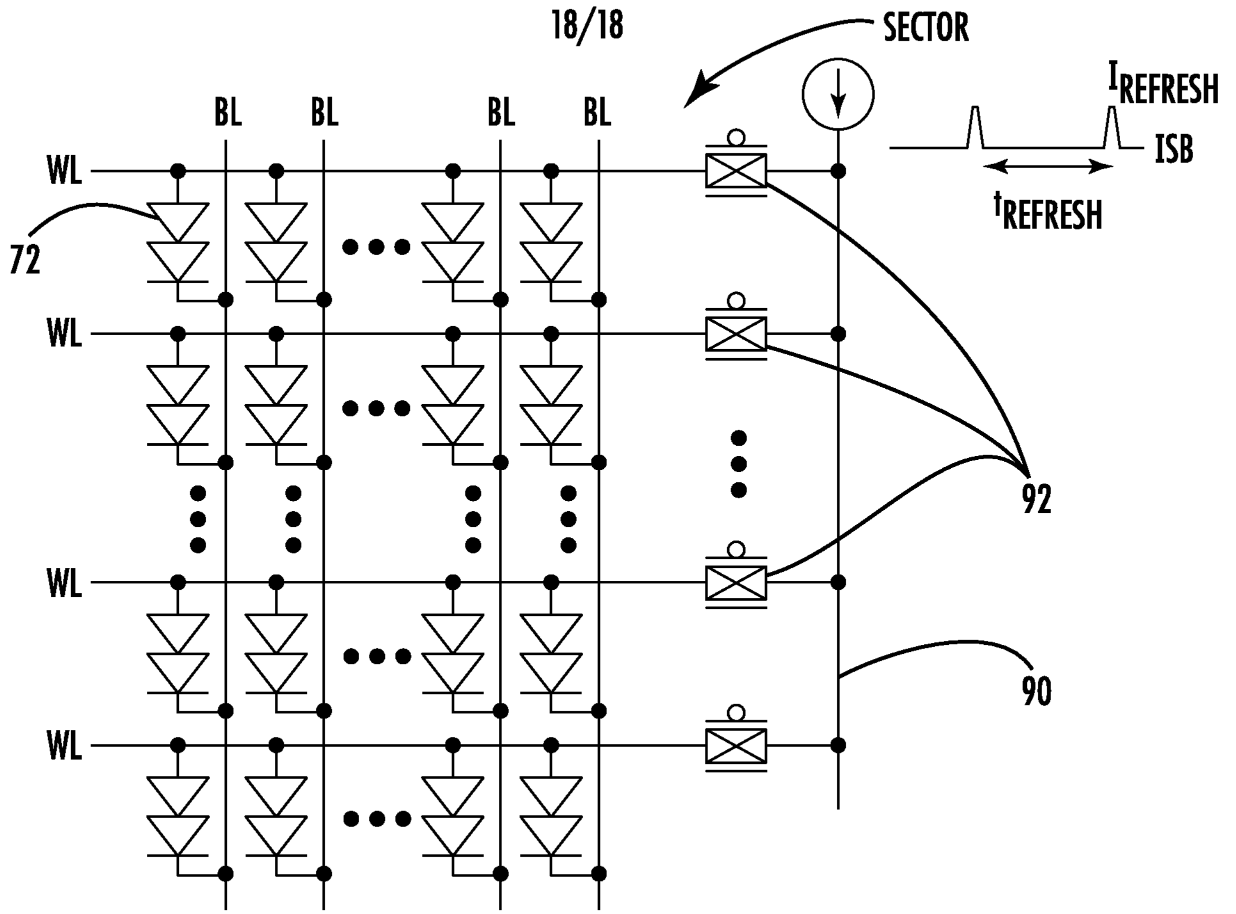

FIG. 20

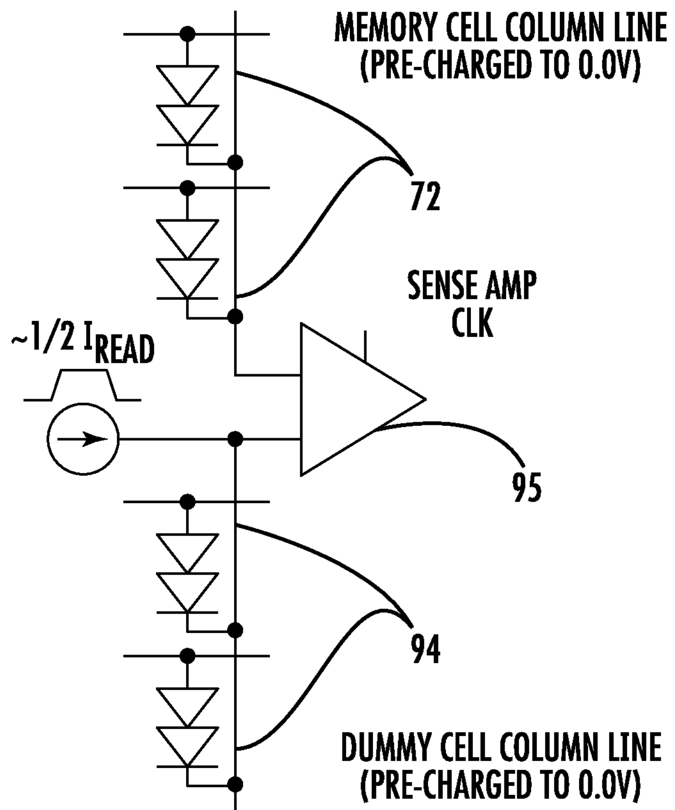

FIG. 21

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/052499

A. CLASSIFICATION OF SUBJECT MATTER
IPC (2016.01) G11C 11/00, H01L 21/76, H01L 27/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC (2016.01) G11C 11/00, H01L 27/00, H01L 21/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Databases consulted: PATENTSCOPE, Esp@cenet, Google Patents
Search terms used: thristor, thrystor, PNPN, diode, SCR, array, trench, deep, shallow,buried, orthogonal, vertical,NMOS,manufacture, fabrication

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014269046 A1 LAURIN et al. 18 Sep 2014 (2014/09/18) ¶ 0003, 0031, 0033, 0034, 0042, 0090, 0091, 0092, 0095 fig. 17, 18A, 18B	1-3,8,11,13-15, 17-19
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Y	US 2008239803 A1 CHO 02 Oct 2008 (2008/10/02) ¶ 0036	4
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A	US 2010232200 A1 SHEPARD 16 Sep 2010 (2010/09/16) Whole document	1-19

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

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