(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
13 June 2019 (13.06.2019)

WIPO | PCT

(10) International Publication Number
WO 2019/112766 A1

(51) International Patent Classification:
H01L 21/8234 (2006.01) *H01L 21/8238* (2006.01)
H01L 27/088 (2006.01) *H01L 27/092* (2006.01)

(21) International Application Number:
PCT/US2018/061221

(22) International Filing Date:
15 November 2018 (15.11.2018)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
15/835,810 08 December 2017 (08.12.2017) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:
— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:
— *with international search report (Art. 21(3))*

(54) **Title:** INTEGRATED CIRCUIT WITH METAL GATE HAVING DIELECTRIC PORTION OVER ISOLATION AREA

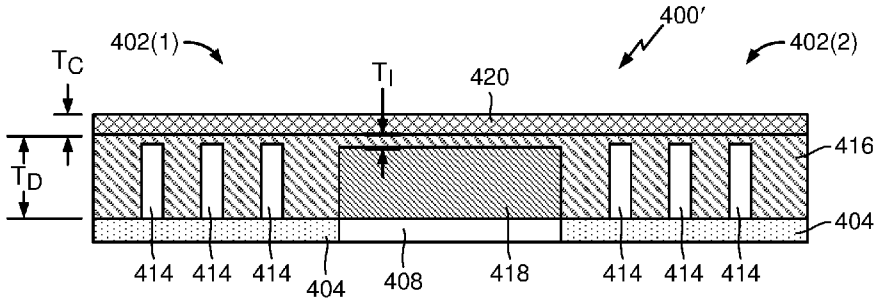

FIG. 4C

(57) **Abstract:** An integrated circuit may include a substrate, a first three- dimensional (3D) transistor (402(1)) formed on a first diffusion region (404) of the substrate, and a second 3D transistor (402(2)) formed on a second diffusion region (404) of the substrate. The first 3D transistor includes a gate that extends from between a source and a drain of the first 3D transistor, across an isolation region (408) of the substrate, to and between a source and a drain of the second 3D transistor. The gate includes a gate metal (416) that has an isolation portion extending over the isolation region of the substrate and a diffusion portion extending over the first and second diffusion regions of the substrate. The isolation portion of the gate metal has a thickness (Ti) less than a maximum thickness (Td) of the diffusion portion of the gate metal.

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INTEGRATED CIRCUIT WITH METAL GATE HAVING DIELECTRIC PORTION OVER ISOLATION AREA

BACKGROUND

[0001] This application claims the benefit of U.S. Application Serial No. 15/835,810, entitled "INTEGRATED CIRCUIT WITH METAL GATE HAVING DIELECTRIC PORTION OVER ISOLATION AREA" and filed on December 8, 2017 which is expressly incorporated by reference herein in its entirety.

Field

[0002] Aspects of the present disclosure relate to semiconductor devices, and more particularly to reducing gate to contact parasitic capacitance in integrated circuits having three-dimensional (3D) transistors.

Background

[0003] Transistors are essential components in modern electronic devices. Large numbers of transistors are employed in integrated circuits (ICs) in many modern electronic devices. For example, components such as central processing units (CPUs) and memory systems employ large quantities of transistors for logic circuits and memory devices.

[0004] As electronic devices continue to become more functionally complex, the need to include more transistors in such devices increases. This increase is achieved in part through continued efforts to miniaturize transistors in ICs (i.e., placing more transistors into the same amount of space). Part of that effort has included moving from planar transistors to 3D transistors, such as Fin Field-Effect Transistors (FinFETs). FIGURE 1 illustrates an example FinFET 100. As shown in FIGURE 1, the FinFET 100 includes a conduction channel 102 in the form of a "fin" 104. The fin 104 is formed in a substrate 106 of a semiconductor material and has two vertical side surfaces 108 and a horizontal top surface 110. Applying a voltage to a gate 112 wrapped around the two vertical side surfaces 108 and the horizontal top surface 110 generates an electric field in the fin 104 that allows current to flow from a source 114 to a drain 116.

[0005] Multiple FinFETs, like FinFET 100 in FIGURE 1, may be implemented in an integrated circuit or in a complementary metal-oxide semiconductor (MOS) (CMOS) standard cell, for example. A CMOS standard cell provides a standard layout of P-type

MOS (PMOS) and N-type (NMOS) regions and structures for fabricating transistors and interconnect structures to form circuits, including logic circuits. For example, FIGURE 2 illustrates a 10 nm node size CMOS standard cell 200. The 10 nm CMOS standard cell 200 has six (6) fins 202(1)-202(6) positioned between two (2) power supply rails 204(1), 204(2), that can form a fin in a fabricated FinFET. For example, a FinFET could be formed in each PMOS and NMOS region 206, 208 of the CMOS standard cell 200. The PMOS region 206 is separated from the NMOS region 208 of the 10 nm CMOS standard cell 200 by an isolation region 220. Each FinFET formed in the 10 nm CMOS standard cell 200 could employ two (2) outer fins 202(1), 202(2) and 202(5), 202(6) to form their respective channel structures. The fins 202(1)-202(6) of each FinFET of the CMOS standard cell could be connected to one of a source/drain line 210(1)-210(5) acting as a source and one of a source/drain line 210(1)-210(5) acting as a drain, and be controlled by a gate contact 212(1)-212(2) over one of the four (4) gate lines 214(1)-214(4) of the CMOS standard cell acting as a gate of each FinFET.

[0006] The gate lines 214(1)-214(4) include a gate metal that can extend from one FinFET in the PMOS region 206 over the isolation region 220 to a FinFET in the NMOS region 208 of the 10 nm CMOS standard cell 200. When the gate extends across the isolation region 220, the gate metal may couple to the end of the source and drain contacts of a proximate FinFETs and create three-dimensional (3D) parasitic capacitances. In advanced CMOS technologies (e.g., 7 nm and beyond), these 3D parasitic capacitances factor prominently and can adversely impact chip performance.

SUMMARY

[0007] An integrated circuit may include a substrate, a first three-dimensional (3D) transistor, and a second 3D transistor. The first 3D transistor may be formed on a first diffusion region of the substrate and may include a first source, a first drain, and a gate extending across the first diffusion region between the first source and the first drain. The second 3D transistor may be formed on a second diffusion region of the substrate and may include a second source, a second drain, and the gate extending across the second diffusion region between the second source and the second drain. The gate may extend from the first 3D transistor across an isolation region of the substrate to the second 3D transistor. The gate may include a gate metal, which may have an isolation portion that extends over the isolation region of the substrate and a diffusion portion that extends over the first diffusion region and the second diffusion region. The isolation

portion of the gate metal may have a thickness less than a maximum thickness of the diffusion portion of the gate metal.

[0008] A method of making an integrated circuit may include providing a wafer substrate having a plurality of partially formed 3D transistors thereon. The plurality of partially formed 3D transistors has completed fin formation and gate metal deposition, depositing a gate metal over a first diffusion region of the wafer substrate, across an isolation region of the wafer substrate, and over a second diffusion region of the wafer substrate to connect a first partially formed 3D transistor to a second partially formed 3D transistor. The method may further include selectively etching the gate metal to remove a portion of the gate metal in the isolation region of the wafer substrate and depositing a gate dielectric material in the isolation region of the wafer substrate to fill in the portion of the gate metal that was removed. The method may further include polishing a top surface of the gate metal on the first diffusion region and the second diffusion region to be flush with a top surface of the gate dielectric material, and depositing additional gate metal on the previously deposited gate metal and the gate dielectric material to extend from the first partially formed 3D transistor to the second partially formed 3D transistor.

[0009] A method of making an integrated circuit may include providing a wafer substrate having a plurality of partially formed 3D transistors thereon. The plurality of 3D transistors has completed fin formation and are covered by a poly silicon, the poly silicon covering a plurality of fins disposed over a first diffusion region of the wafer substrate, across an isolation region of the wafer substrate, and over a second diffusion region of the wafer substrate. The method may further include selectively etching the poly silicon to remove a portion of the poly silicon in the isolation region of the wafer substrate, and depositing a gate dielectric material in the isolation region of the wafer substrate to fill in the portion of the poly silicon that was removed. The method may further include polishing a top surface of the gate dielectric material to be flush with a top surface of the poly silicon, and removing the poly silicon from the first diffusion region and the second diffusion region of the wafer. The method may further include depositing a gate metal over the plurality of fins disposed over the first diffusion region of the wafer substrate, the gate dielectric material extending over the isolation region of the wafer substrate, and the plurality of fins disposed over the second diffusion region of the wafer substrate.

[0010] Additional features and advantages of the disclosure will be described below. It should be appreciated by those skilled in the art that this disclosure may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present disclosure. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the teachings of the disclosure as set forth in the appended claims. The novel features, which are believed to be characteristic of the disclosure, both as to its organization and method of operation, together with further objects and advantages, will be better understood from the following description when considered in connection with the accompanying figures. It is to be expressly understood, however, that each of the figures is provided for the purpose of illustration and description only and is not intended as a definition of the limits of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] For a more complete understanding of the present disclosure, reference is now made to the following description taken in conjunction with the accompanying drawings.

[0012] FIGURE 1 a perspective diagram of an exemplary Fin Field-Effect Transistor (FinFET).

[0013] FIGURE 2 illustrates a top view of an exemplary ten (10) nanometer (nm) standard cell.

[0014] FIGURE 3A is a top plan view of a portion of an integrated circuit (IC) showing parasitic capacitances that may result from gate over isolation region coupling to source and/or drain contact ends.

[0015] FIGURE 3B is a cross-sectional diagram taken generally along the line A-A of FIGURE 3A.

[0016] FIGURE 4A is a top plan view of a portion of an IC, according to aspects of the present disclosure.

[0017] FIGURE 4B is a cross-sectional diagram taken generally along the line A-A of Figure 4A.

[0018] FIGURE 4C is a cross-sectional diagram taken generally along the line A-A of Figure 4A, according to another aspect of the present disclosure.

[0019] FIGURE 5 illustrates a process flow diagram of a method for fabricating an IC device, according to aspects of the present disclosure.

[0020] FIGURES 6A-6E illustrate a fabrication process for fabricating an IC device, according to aspects of the present disclosure.

[0021] FIGURE 7 illustrates another process flow diagram of a method for fabricating an IC device, according to aspects of the present disclosure.

[0022] FIGURES 8A-8E illustrate another fabrication process for fabricating an IC device, according to aspects of the present disclosure.

[0023] FIGURE 9 is a block diagram showing an exemplary wireless communication system in which an aspect of the disclosure may be advantageously employed.

[0024] FIGURE 10 is a block diagram illustrating a design workstation used for circuit, layout, and logic design of an IC device according to one configuration.

DETAILED DESCRIPTION

[0025] The detailed description set forth below, in connection with the appended drawings, is intended as a description of various configurations and is not intended to represent the only configurations in which the concepts described herein may be practiced. The detailed description includes specific details for the purpose of providing a thorough understanding of the various concepts. It will be apparent to those skilled in the art, however, that these concepts may be practiced without these specific details. In some instances, well-known structures and components are shown in block diagram form in order to avoid obscuring such concepts.

[0026] As described herein, the use of the term "and/or" is intended to represent an "inclusive OR", and the use of the term "or" is intended to represent an "exclusive OR". As described herein, the term "exemplary" used throughout this description means "serving as an example, instance, or illustration," and should not necessarily be construed as preferred or advantageous over other exemplary configurations. As described herein, the term "coupled" used throughout this description means "connected, whether directly or indirectly through intervening connections (e.g., a switch), electrical, mechanical, or otherwise," and is not necessarily limited to physical connections. Additionally, the connections can be such that the objects are permanently connected or releasably connected. The connections can be through switches. As described herein, the term "proximate" used throughout this description means

"adjacent, very near, next to, or close to." As described herein, the term "on" used throughout this description means "directly on" in some configurations, and "indirectly on" in other configurations.

[0027] According to aspects of the present disclosure, a dielectric material may be provided to at least partially replace a gate metal over an isolation region of a substrate. The advantages of replacing a portion of the gate metal over the isolation region with a dielectric material include reducing gate to contact parasitic capacitance by approximately 70% and improving chip performance by as much as 5-10%.

[0028] FIGURES 3A and 3B illustrate a simplified view of a portion of a conventional IC 300 having a 3D transistor, such as FinFET 302 disposed on a diffusion region 304 of a substrate. The FinFET 302 includes a gate 306 that extends from the FinFET 302, across an isolation region 308 of the substrate, to another FinFET (not shown). By way of example, FinFET 302 may be a FinFET that is formed in the PMOS region 206 of the 10 nm CMOS standard cell 200 shown in FIGURE 2, with gate 306 shown as one of the gate lines 214(1)-214(4), extending to a FinFET in another region, such as NMOS region 208. The FinFET 302 includes a source 310, a drain 312, and a plurality of fins 314, that are wrapped around by the gate 306. The gate 306 includes a gate metal 316. When the gate 306 extends across the isolation region 308 of the substrate, the gate metal 316 can couple to the end of the contacts of the source 310 and the drain 312, causing a 3D coupling parasitic capacitance. In advanced CMOS technologies (e.g., 7 nm and beyond), 3D parasitic capacitance factors prominently and can adversely impact chip performance.

[0029] To reduce 3D parasitic capacitances, according to aspects of the present disclosure, an IC may be provided, in which a portion of a gate that extends over an isolation region of a substrate is replaced with a dielectric material, thereby reducing coupling between the gate and any source and/or drain contacts of proximate FinFETs. FIGURES 4A and 4B illustrate a portion of an IC 400 having 3D transistors, such as FinFETs 402(1), 402(2) disposed on a diffusion region 404 of a substrate. The FinFET 402(1) includes a gate 406 that may extend from the FinFET 402(1), across an isolation region 408 of the substrate, to the FinFET 402(2). By way of example, like FinFET 302 of FIGURES 3A and 3B, the FinFET 402(1) may be a FinFET that is formed in the

PMOS region 206 of the 10 nm CMOS standard cell 200 shown in FIGURE 2, and FinFET 402(2) may be a FinFET that is formed in the NMOS region 208 of the 10 nm CMOS standard cell 200, with gate 406 shown as one of the gate lines 214(1)-214(4) from the PMOS region 206 to the NMOS region 208. Each of the FinFETs 402(1), 402(2) includes a source 410, a drain 412, and a plurality of fins 414, that are wrapped around by the gate 406. The gate 406 includes a gate metal 416, which may be composed of a conducting metal, such as cobalt or tungsten.

[0030] The IC 400 is similar to the IC 300 shown in FIGURES 3A and 3B, except that the gate metal 416 has a reduced thickness over the isolation region 408 of the substrate, because a portion of the gate metal over the isolation region 408 has been replaced by a gate dielectric material 418. The portion of the gate metal 416 that extends over the isolation region 408 has a thickness T_I that is less than a maximum thickness T_D of the gate metal 416 over the diffusion region 404. By way of example, the gate metal 416 may have an isolation region thickness T_I in the range of 10 nm to 35 nm and over the diffusion region 404 a maximum thickness T_D in the range of 50 nm to 80 nm.

[0031] The gate dielectric material 418 may be a silicon nitride or any other suitable dielectric material, including a combination of dielectric materials. The gate dielectric material 418, which is disposed between the isolation region 408 of the substrate and the gate metal 416, may have a thickness in the range of 40 nm to 60 nm. As mentioned above, the gate dielectric material 418 replaces a portion of the gate metal 416 over the isolation region 408 of the substrate, thereby reducing the 3D parasitic coupling capacitance of the gate metal 416 over the isolation region 408 to the contacts of the source 410 and the drain 412 of neighboring FinFETs, such as FinFET 402. This reduction in 3D parasitic capacitance will improve the performance of advanced CMOS devices.

[0032] According to aspects of the present disclosure, an optional conducting layer may further be provided on the gate metal 416. FIGURE 4C illustrates an IC 400'similar to the IC 400 in FIGURE 4B, however, the IC 400' includes a conducting layer 420 disposed on the gate metal 416. All other components of IC 400' are similar to those shown in FIGURE 4B and thus are identified by the same reference numerals.

[0033] The conducting layer 420 may be composed of a material having a higher conductivity than the gate metal 416 to improve gate conductance. For example, if the gate metal 416 is made of tungsten or cobalt, the conducting layer may be composed a

carbon material, such as graphene. Other suitable materials for the conducting layer 420 that have a higher conductivity than tungsten or cobalt include silver, copper, gold, aluminum and calcium. The conducting layer 420 may have a thickness T_C in the range of 10 nm to 30 nm.

[0034] FIGURE 5 provides a process flow diagram of a method 500 for fabricating an IC device, according to aspects of the present disclosure. The process flow diagram of FIGURE 5 may be supplemented by the fabrication process illustrations of FIGURES 6A-6E. At block 502 a wafer substrate having a plurality of partially formed 3D FinFET transistors that have completed fin formation and gate metal deposition is provided. As illustrated in FIGURE 6A, a wafer substrate 600 may have partially formed 3D transistors 602(1), 602(2) formed thereon. The partially formed 3D transistors 602(1), 602(2) are each formed on a diffusion region 604 of the wafer substrate 600, and each of the partially formed 3D transistors 602(1), 602(2) includes a plurality of fins 614. The diffusion regions 604 of the wafer substrate 600 are separated from each other by an isolation region 608 of the wafer substrate 600. The wafer substrate 600 has completed gate formation, so a gate metal 616, which may be composed of tungsten or cobalt, is provided over the fins 614 of the partially formed 3D transistors 602(1), 602(2). The gate metal 616 extends from the diffusion region 604 of one partially formed 3D transistor 602(1), across the isolation region 608 of the wafer substrate, to the diffusion region 604 of another partially formed 3D transistor 602(2), thereby connecting the partially formed 3D transistor 602(1) to the partially formed 3D transistor 602(2).

[0035] At block 504 of FIGURE 5, the gate metal 616 may be selective etched to remove a portion of the gate metal in the isolation region 608 of the wafer substrate 600. At block 506 a gate dielectric material may then be deposited in the isolation region 608 of the wafer substrate 600 to fill in the portion of the gate metal 616 that was removed in block 504. As shown in FIGURE 6B, the gate metal 616 has been selectively removed from the isolation region 608 of the wafer substrate 600 and replaced with a gate dielectric material 618. The gate dielectric material 618 may have at thickness in the range of 40 nm to 60 nm. As noted earlier, the gate dielectric material 618 may be a silicon nitride or any other suitable dielectric material.

[0036] At block 508 of FIGURE 5, the gate metal 616 may be chemical mechanically polished to level out the gate metal 616, such that a top surface of the gate metal 616 is

flush with a top surface of the gate dielectric material 618. As shown in FIGURE 6C, as a result of the chemical mechanical polish, a top surface 622 of the gate metal 616 is flush, or co-planar, with a top surface 624 of the gate dielectric material 618.

[0037] At block 510 of FIGURE 5, additional gate metal may then be deposited on the top surface 622 of the previously deposited gate metal 616 and the top surface 624 of the gate dielectric material 618. As shown in FIGURE 6D, an additional layer 626 of gate metal is provided on top of the previously deposited gate metal 616 and the gated dielectric material 618. The additional layer 626 of gate metal may be preferably composed of the same material as the gate metal 616.

[0038] The thickness of the additional layer 626 of gate metal may vary, depending on whether the gate will include an optional conducting layer on top of the gate metal. If no conducting layer will be added to the gate, the additional layer 626 of gate metal may, for example, have a thickness in the range of 10 nm to 35 nm. If a conducting layer will be added to the gate, then the additional layer 626 of gate material may, for example, be a thin layer having a thickness in the range of 1 nm to 5 nm.

[0039] At block 512 of FIGURE 5, an optional conducting layer may be deposited on the additional gate metal. The conducting material may be either deposited or grown on the top of the gate material in both the diffusion and isolation regions to form a conducting path of the gate. The conducting layer is preferably composed of material having a higher conductivity than that the gate metal. For example, if the gate metal is composed of tungsten or cobalt, the conducting layer may be composed of a carbon material, such as graphene. Other suitable materials for the conducting layer that have a higher conductivity than tungsten or cobalt include silver, copper, gold, aluminum and calcium. The conducting layer may have a thickness in the range of 10 nm and 30 nm. As shown in FIGURE 6E, a conducting layer 620 is provided on the additional layer 626 of gate metal. The conducting layer 620 may help to reduce gate resistance and improve performance of the resulting IC device.

[0040] FIGURE 7 provides a process flow diagram of another method 700 for fabricating an IC device, according to aspects of the present disclosure. The process flow diagram of FIGURE 7 may be supplemented by the fabrication process illustrations of FIGURES 8A-8E. At block 702 a wafer substrate having a plurality of partially formed 3D FinFET transistors that have completed fin formation and are covered by a dummy poly silicon gate is provided. At block 704, the dummy poly

silicon gate may be etched to remove a portion of the dummy poly silicon gate in an isolation region of the wafer substrate. As illustrated in FIGURE 8A, a wafer substrate 800 may have partially formed 3D transistors 802(1), 802(2) formed thereon. The partially formed 3D transistors 802(1), 802(2) are each formed on a diffusion region 804 of the wafer substrate 800, and each of the partially formed 3D transistors 802(1), 802(2) includes a plurality of fins 814. The diffusion regions 804 of the wafer substrate 800 are separated from each other by an isolation region 808 of the wafer substrate 800. The wafer substrate 800 has completed fin formation and the fins 814 are covered by a dummy poly silicon gate 821. A portion of the dummy poly silicon gate 821 has been removed from the isolation region 808 of the wafer substrate 800.

[0041] At block 706 of FIGURE 7, a gate dielectric material may be deposited in the isolation region of the wafer substrate to fill in the portion of the dummy poly silicon gate that was removed. At block 708 the gate dielectric material is chemical mechanically polished so that a top surface of the gate dielectric material is flush with a top surface of the dummy poly silicon gate. As shown in FIGURE 8B, a gate dielectric material 818 is provided in the isolation region 808 of the wafer substrate 800, where the dummy poly silicon gate 821 was removed. The gate dielectric material 818 has been polished, such that a top surface 824 of the gate dielectric material 818 is flush with a top surface 822 of the dummy poly silicon gate 821. The gate dielectric material 818 may have at thickness in the range of 40 nm to 60 nm. As noted earlier, the gate dielectric material 818 may be a silicon nitride or any other suitable dielectric material.

[0042] At block 710 of FIGURE 7, the dummy poly silicon gate may be removed using a lithography mask to pattern and etch out the dummy poly silicon gate. FIGURE 8C shows the wafer substrate 800 with the dummy poly silicon gate removed and the plurality of fins 814 exposed.

[0043] At block 712 of FIGURE 7, a gate metal may be deposited over the plurality of fins in the diffusion region and over the gate dielectric material in the isolation region. The gate metal may also be polished to smooth its surface. FIGURE 8D illustrates a gate metal 816 covering the fins 814 in the diffusion regions 804 of the wafer substrate 800 as well as covering the gate dielectric material 818 in the isolation region 808. After the gate metal 816 has been polished, a thickness of the gate metal 816 in the isolation region 808 is less than a maximum thickness of the gate metal 816 in the diffusion region 804. The maximum thickness T_D of the gate metal 816 in the diffusion

region may be in the range of 50 nm to 80 nm, while the thickness of the gate metal 816 in the isolation region 808 may vary, depending on whether or not the gate will include an optional conducting layer on top of the gate metal 816. If no conducting layer will be added to the gate, then, in the isolation region 808, the gate metal 816 may have a thickness T_I in the range of 10 nm to 35 nm. If a conducting layer will be added to the gate, the thickness T_I may be in the range of 1 nm to 5 nm.

[0044] At block 714 of FIGURE 7, an optional conducting layer may be deposited on the gate metal. The conducting material may be either deposited or grown on the top of the gate material in both the diffusion and isolation regions to form a conducting path of the gate. The conducting layer is preferably composed of material having a higher conductivity than that the gate metal. For example, if the gate metal is composed of tungsten or cobalt, the conducting layer may be composed of a carbon material, such as graphene. Other suitable materials for the conducting layer that have a higher conductivity than tungsten or cobalt include silver, copper, gold, aluminum and calcium. The conducting layer may have a thickness T_C in the range of 10 nm to 30 nm. As shown in FIGURE 8E, a conducting layer 820 is provided on the gate metal 816. The conducting layer 820 may help to reduce gate resistance and improve performance of the resulting IC device.

[0045] FIGURE 9 is a block diagram showing an exemplary wireless communication system 900 in which an aspect of the disclosure may be advantageously employed. For purposes of illustration, FIGURE 9 shows three remote units 920, 930, and 950 and two base stations 940. It will be recognized that wireless communication systems may have many more remote units and base stations. Remote units 920, 930, and 950 include IC devices 925A, 925C, and 925B that include the disclosed IC devices. It will be recognized that other devices may also include the disclosed IC devices, such as the base stations, switching devices, and network equipment. FIGURE 9 shows forward link signals 980 from the base station 940 to the remote units 920, 930, and 950 and reverse link signals 990 from the remote units 920, 930, and 950 to base stations 940.

[0046] In FIGURE 9, remote unit 920 is shown as a mobile telephone, remote unit 930 is shown as a portable computer, and remote unit 950 is shown as a fixed location remote unit in a wireless local loop system. For example, the remote units may be a mobile phone, a hand-held personal communication systems (PCS) unit, a portable data

unit such as a personal data assistant, a GPS enabled device, a navigation device, a set top box, a music player, a video player, an entertainment unit, a fixed location data unit such as a meter reading equipment, or other devices that store or retrieve data or computer instructions, or combinations thereof. Although FIGURE 9 illustrates remote units according to the aspects of the disclosure, the disclosure is not limited to these exemplary illustrated units. Aspects of the disclosure may be suitably employed in many devices, which include the disclosed IC devices.

[0047] FIGURE 10 is a block diagram illustrating a design workstation used for circuit, layout, and logic design of the IC devices disclosed above. A design workstation 1000 includes a hard disk 1001 containing operating system software, support files, and design software such as Cadence or OrCAD. The design workstation 1000 also includes a display 1002 to facilitate design of a circuit 1010 or a IC device 1012. A storage medium 1004 is provided for tangibly storing the design of the circuit 1010 or the IC device 1012. The design of the circuit 1010 or the IC device 1012 may be stored on the storage medium 1004 in a file format such as GDSII or GERBER. The storage medium 1004 may be a CD-ROM, DVD, hard disk, flash memory, or other appropriate device. Furthermore, the design workstation 1000 includes a drive apparatus 1003 for accepting input from or writing output to the storage medium 1004.

[0048] Data recorded on the storage medium 1004 may specify logic circuit configurations, pattern data for photolithography masks, or mask pattern data for serial write tools such as electron beam lithography. The data may further include logic verification data such as timing diagrams or net circuits associated with logic simulations. Providing data on the storage medium 1004 facilitates the design of the circuit 1010 or the IC device 1012 by decreasing the number of processes for designing semiconductor wafers.

[0049] For a firmware and/or software implementation, the methodologies may be implemented with modules (e.g., procedures, functions, and so on) that perform the functions described herein. A machine-readable medium tangibly embodying instructions may be used in implementing the methodologies described herein. For example, software codes may be stored in a memory and executed by a processor unit. Memory may be implemented within the processor unit or external to the processor unit. As used herein, the term “memory” refers to types of long term, short term, volatile,

nonvolatile, or other memory and is not to be limited to a particular type of memory or number of memories, or type of media upon which memory is stored.

[0050] If implemented in firmware and/or software, the functions may be stored as one or more instructions or code on a computer-readable medium. Examples include computer-readable media encoded with a data structure and computer-readable media encoded with a computer program. Computer-readable media includes physical computer storage media. A storage medium may be an available medium that can be accessed by a computer. By way of example, and not limitation, such computer-readable media can include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or other medium that can be used to store desired program code in the form of instructions or data structures and that can be accessed by a computer; disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above should also be included within the scope of computer-readable media.

[0051] In addition to storage on computer readable medium, instructions and/or data may be provided as signals on transmission media included in a communication apparatus. For example, a communication apparatus may include a transceiver having signals indicative of instructions and data. The instructions and data are configured to cause one or more processors to implement the functions outlined in the claims.

[0052] Although the present disclosure and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the technology of the disclosure as defined by the appended claims. For example, relational terms, such as “above” and “below” are used with respect to a substrate or electronic device. Of course, if the substrate or electronic device is inverted, above becomes below, and vice versa. Additionally, if oriented sideways, above and below may refer to sides of a substrate or electronic device. Moreover, the scope of the present application is not intended to be limited to the particular configurations of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be

developed that perform substantially the same function or achieve substantially the same result as the corresponding configurations described herein may be utilized according to the present disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

[0053] Those of skill would further appreciate that the various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the disclosure herein may be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the present disclosure.

[0054] The various illustrative logical blocks, modules, and circuits described in connection with the disclosure herein may be implemented or performed with a general-purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general-purpose processor may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices (e.g., a combination of a DSP and a microprocessor, multiple microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration).

[0055] The steps of a method or algorithm described in connection with the disclosure may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module may reside in RAM, flash memory, ROM, EPROM, EEPROM, registers, hard disk, a removable disk, a CD-ROM, or any other form of storage medium known in the art. An exemplary storage medium is

coupled to the processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor. The processor and the storage medium may reside in an ASIC. The ASIC may reside in a user terminal. In the alternative, the processor and the storage medium may reside as discrete components in a user terminal.

[0056] In one or more exemplary designs, the functions described may be implemented in hardware, software, firmware, or any combination thereof. If implemented in software, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. Computer-readable media includes both computer storage media and communication media including any medium that facilitates transfer of a computer program from one place to another. A storage media may be any available media that can be accessed by a general purpose or special purpose computer. By way of example, and not limitation, such computer-readable media can include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that can be used to carry or store specified program code means in the form of instructions or data structures and that can be accessed by a general-purpose or special-purpose computer, or a general-purpose or special-purpose processor. Also, any connection is properly termed a computer-readable medium. For example, if the software is transmitted from a website, server, or other remote source using a coaxial cable, fiber optic cable, twisted pair, digital subscriber line (DSL), or wireless technologies such as infrared, radio, and microwave, then the coaxial cable, fiber optic cable, twisted pair, DSL, or wireless technologies such as infrared, radio, and microwave are included in the definition of medium. Disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above should also be included within the scope of computer-readable media.

[0057] The previous description of the disclosure is provided to enable any person skilled in the art to make or use the disclosure. Various modifications to the disclosure will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other variations without departing from the spirit or scope of the disclosure. Thus, the disclosure is not intended to be limited to the examples and

designs described herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

CLAIMS

WHAT IS CLAIMED IS:

1. An integrated circuit, comprising:

a substrate;

a first three-dimensional (3D) transistor formed on a first diffusion region of the substrate, the first 3D transistor including a first source, a first drain, and a gate extending across the first diffusion region between the first source and the first drain;

a second 3D transistor formed on a second diffusion region of the substrate, the second 3D transistor including a second source, a second drain, and the gate extending across the second diffusion region between the second source and the second drain;

wherein the gate extends from the first 3D transistor across an isolation region of the substrate to the second 3D transistor, the gate including a gate metal,

wherein the gate metal has an isolation portion extending over the isolation region of the substrate and a diffusion portion extending over the first diffusion region and the second diffusion region, the isolation portion of the gate metal having a thickness less than a maximum thickness of the diffusion portion of the gate metal.

2. The integrated circuit of claim 1, wherein the gate further includes a gate dielectric material between the isolation region of the substrate and the gate metal, the gate dielectric material having a thickness in the range of 40 nm to 60 nm.

3. The integrated circuit of claim 1, wherein the thickness of the isolation portion of the gate metal is in the range of 10 nm to 35 nm.

4. The integrated circuit of claim 1, wherein the gate metal is composed of a material selected from the group consisting of cobalt and tungsten.

5. The integrated circuit of claim 1, wherein the gate further includes a conducting layer disposed on the gate metal.

6. The integrated circuit of claim 5, wherein the conducting layer has a thickness in the range of 10 nm to 30 nm.

7. The integrated circuit of claim 5, wherein the conducting layer is composed of a material selected from the group consisting of graphene, copper, aluminum, and gold.

8. The integrated circuit of claim 1, integrated into a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a

computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and/or a fixed location data unit.

9. A method of making an integrated circuit, comprising:

providing a wafer substrate having a plurality of partially formed three-dimensional (3D) transistors thereon, the plurality of partially formed 3D transistors having completed fin formation and gate metal deposition, the gate metal deposition extending over a first diffusion region of the wafer substrate, across an isolation region of the wafer substrate, and over a second diffusion region of the wafer substrate to connect a first partially formed 3D transistor of the plurality of partially formed 3D transistors to a second partially formed 3D transistor of the plurality of partially formed 3D transistors;

selectively etching the gate metal to remove a portion of the gate metal in the isolation region of the wafer substrate;

depositing a gate dielectric material in the isolation region of the wafer substrate to fill in the portion of the gate metal that was removed;

polishing a top surface of the gate metal to be flush with a top surface of the gate dielectric material; and

depositing additional gate metal on the previously deposited gate metal and the gate dielectric material to extend from the first partially formed 3D transistor to the second partially formed 3D transistor.

10. The method of claim 9, wherein the gate dielectric material has a thickness in the range of 40 nm to 60 nm.

11. The method of claim 9, wherein depositing additional gate metal includes depositing a thin layer of gate metal having a thickness in the range of 1 nm to 5 nm.

12. The method of claim 11, further comprising forming a conducting layer on the gate metal.

13. The method of claim 12, wherein the conducting layer has a thickness in the range of 10 nm to 30 nm.

14. The method of claim 12, where in the conducting layer is composed of a material selected from the group consisting of graphene, copper, aluminum, and gold.

15. The method of claim 9, wherein the gate metal is composed of a material selected from the group consisting of cobalt and tungsten.

16. A method of making an integrated circuit, comprising:

providing a wafer substrate having a plurality of partially formed three-dimensional (3D) transistors thereon, the plurality of partially formed 3D transistors having completed fin formation and covered by a poly silicon, the poly silicon covering a plurality of fins disposed over a first diffusion region of the wafer substrate, across an isolation region of the wafer substrate, and over a second diffusion region of the wafer substrate;

selectively etching the poly silicon to remove a portion of the poly silicon in the isolation region of the wafer substrate;

depositing a gate dielectric material in the isolation region of the wafer substrate to fill in the portion of the poly silicon that was removed;

polishing a top surface of the gate dielectric material to be flush with a top surface of the poly silicon;

removing the poly silicon from the first diffusion region and the second diffusion region of the wafer substrate; and

depositing a gate metal over the plurality of fins disposed over the first diffusion region of the wafer substrate, the gate dielectric material extending over the isolation region of the wafer substrate, and the plurality of fins disposed over the second diffusion region of the wafer substrate.

17. The method of claim 16, wherein the gate dielectric material has a thickness in the range of 40 nm to 60 nm.

18. The method of claim 16, further comprising depositing a conducting layer on the gate metal.

19. The method of claim 18, wherein the conducting layer has a thickness in the range of 10 nm to 30 nm.

20. The method of claim 18, wherein depositing the conducting layer includes depositing a material selected from the group consisting of graphene, copper, aluminum, and gold.

21. The method of claim 16, wherein depositing the gate metal includes depositing a material selected from the group consisting of cobalt and tungsten.

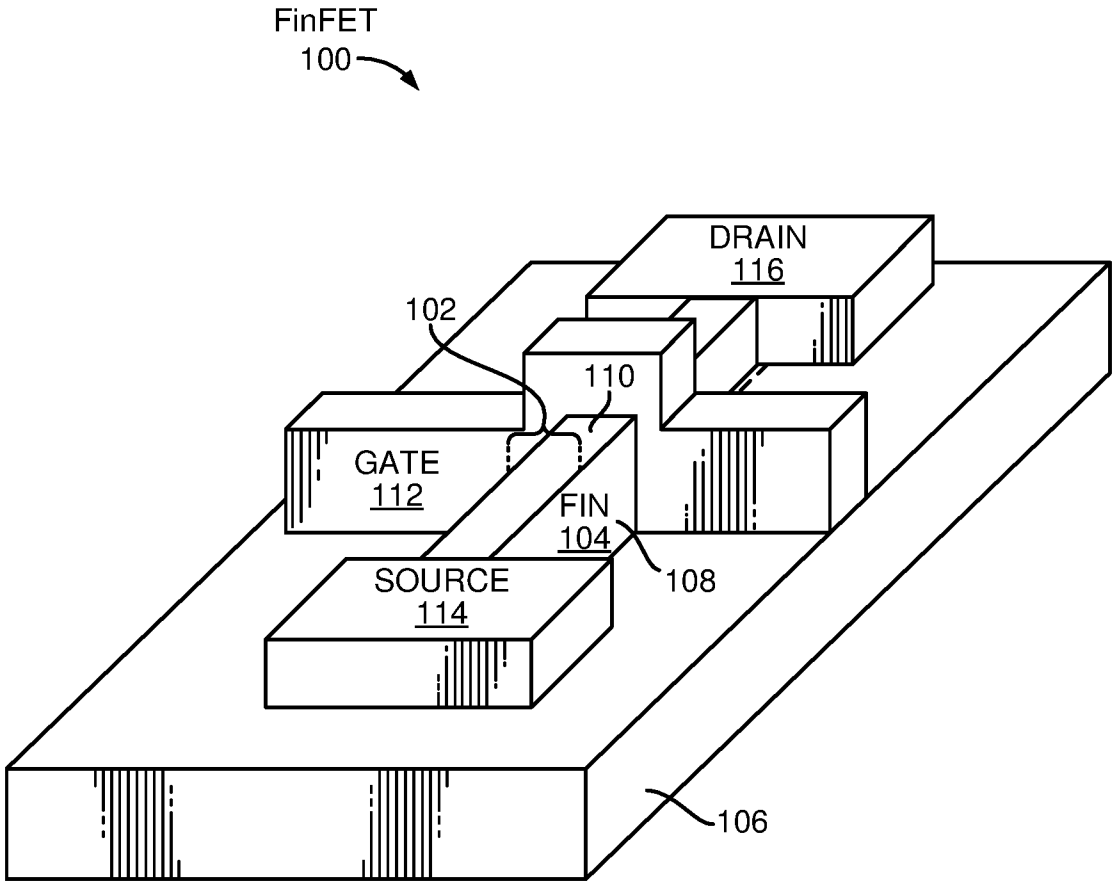
FinFET
100
DRAIN
116
102
110
GATE
112
FIN
104
108
SOURCE
114
106

FIG. 1

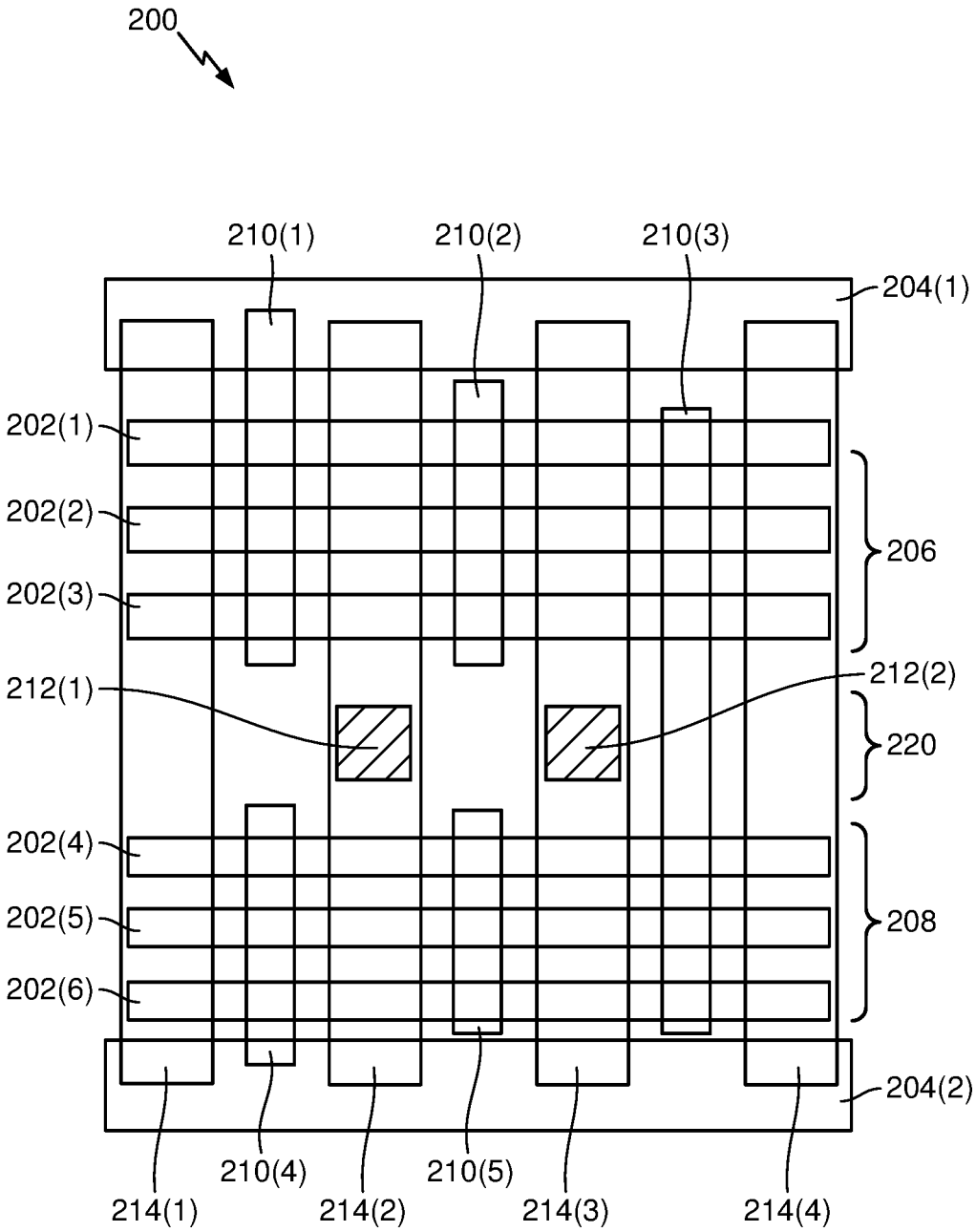
200
210(1)
210(2)
210(3)
204(1)
202(1)
202(2)
202(3)
206
212(1)
212(2)
220
202(4)
202(5)
202(6)
208
204(2)
210(4)
210(5)
214(1)
214(2)
214(3)
214(4)

FIG. 2

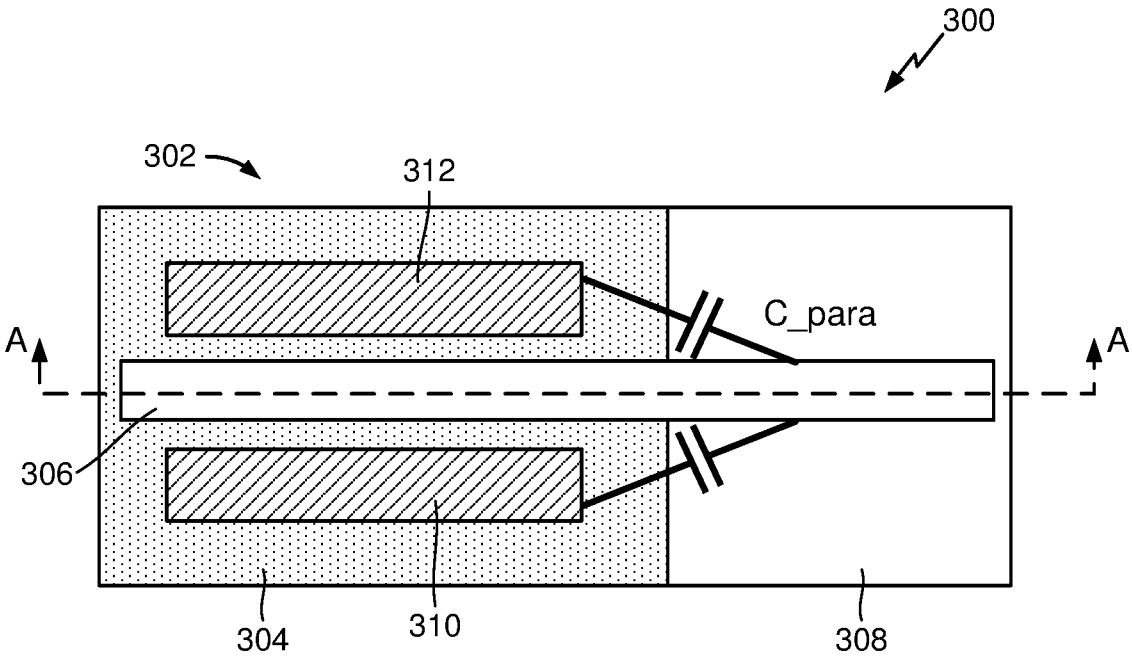
300
302
312
C_para
A
A
306
304
310
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FIG. 3A

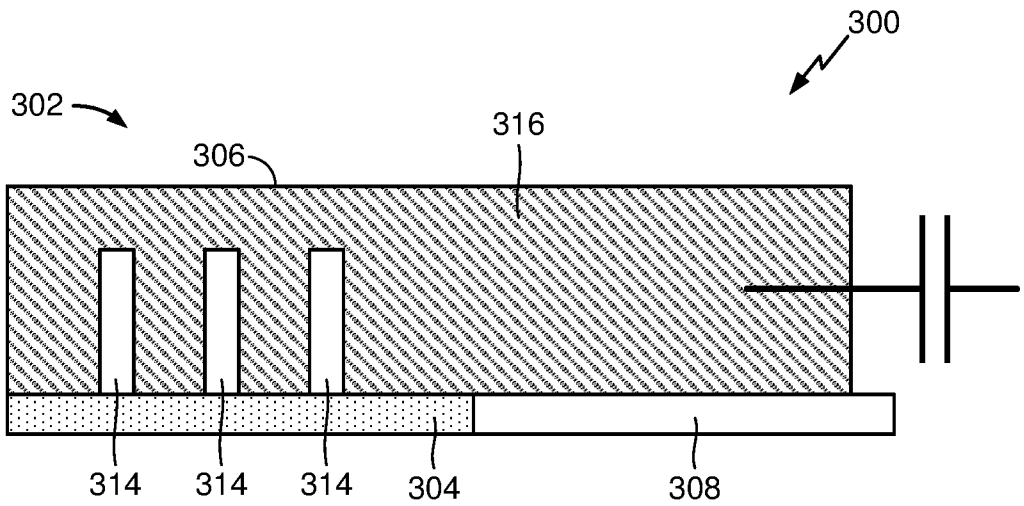

300
302
316
306
314
314
314
304
308

FIG. 3B

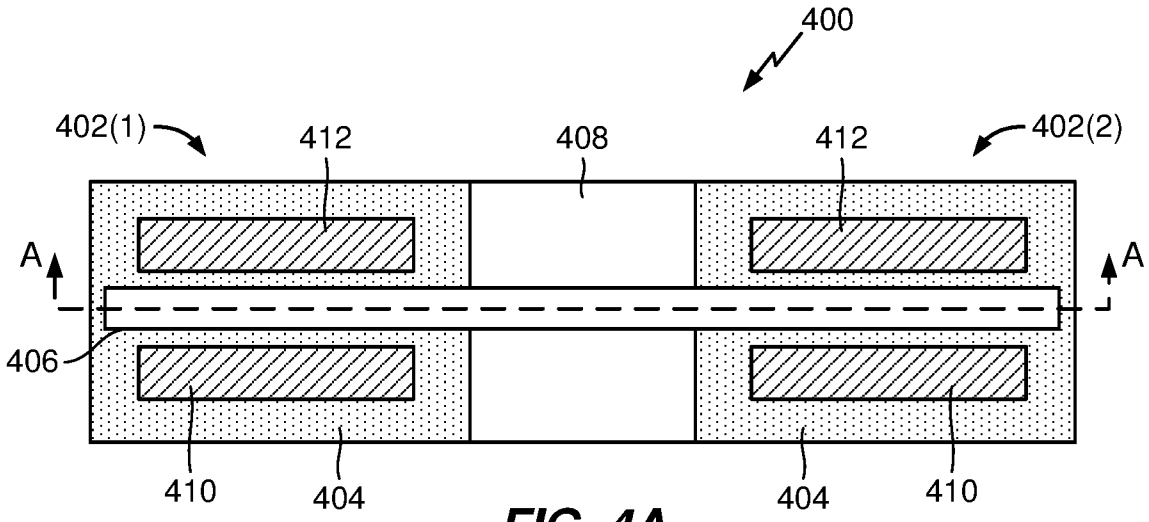


FIG. 4A

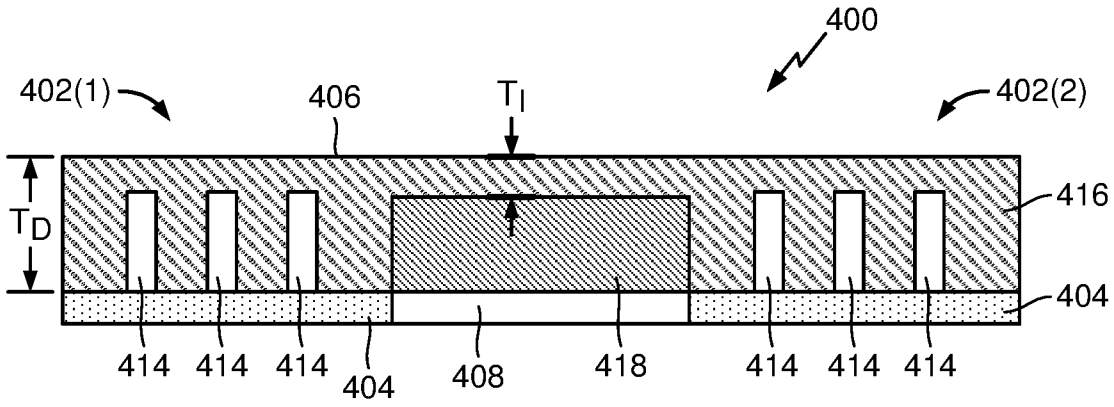


FIG. 4B

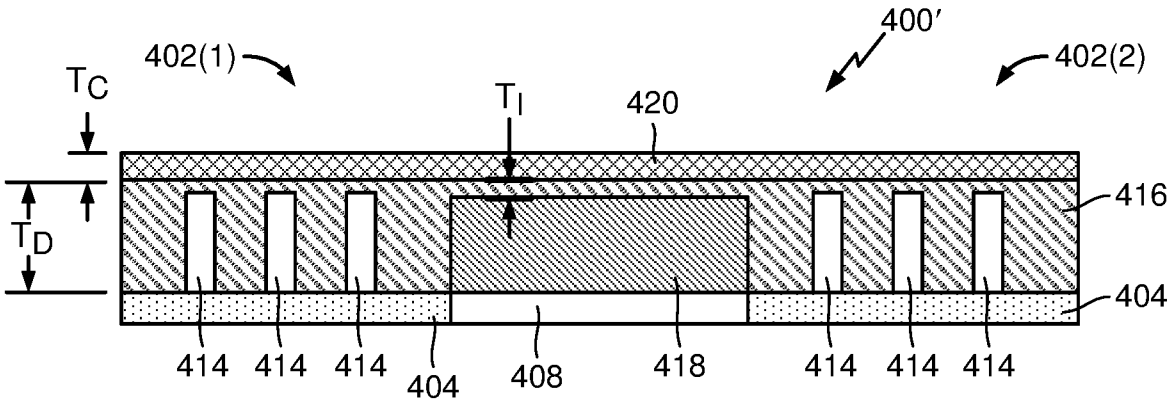


FIG. 4C

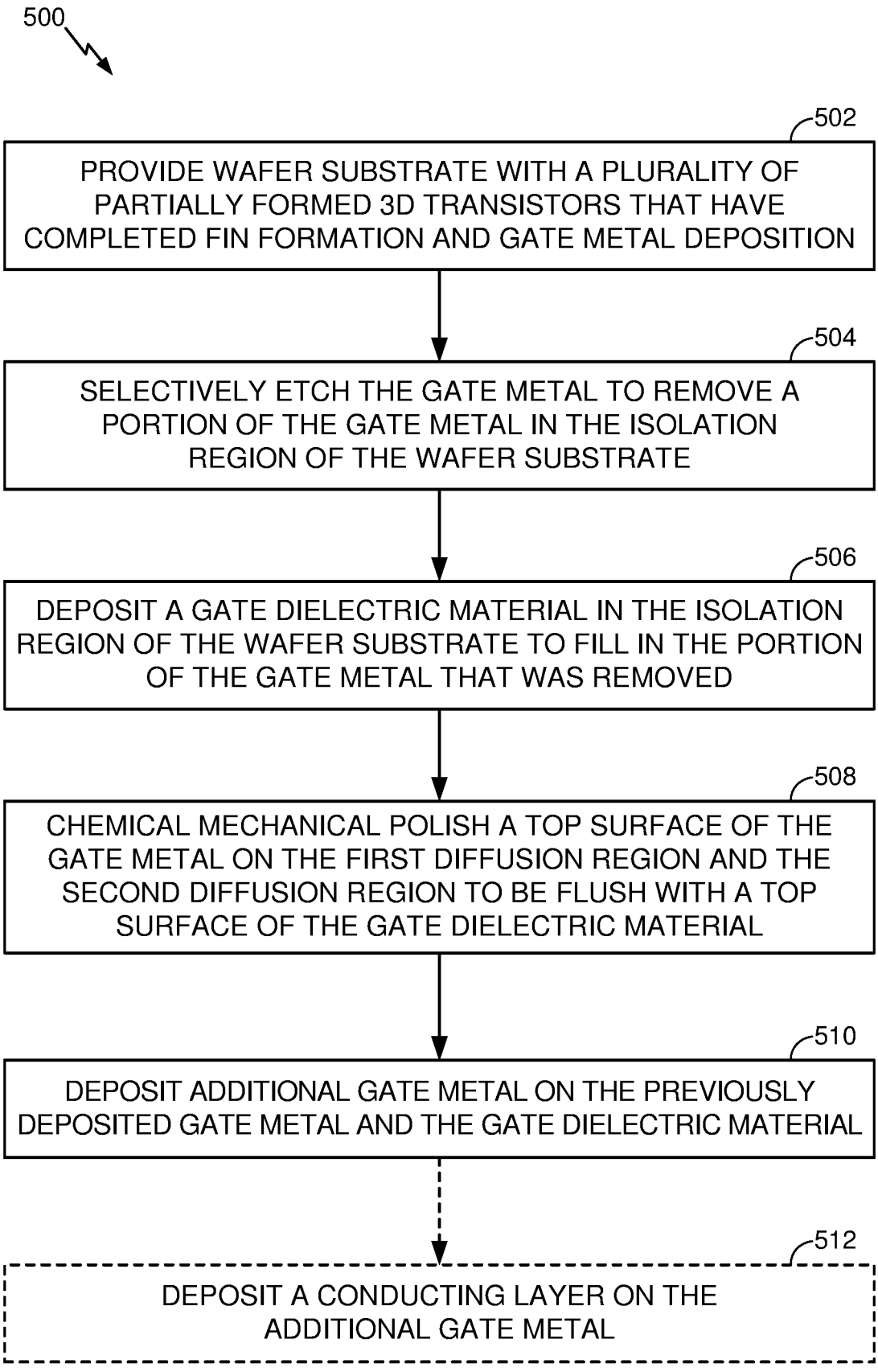

500
502
PROVIDE WAFER SUBSTRATE WITH A PLURALITY OF PARTIALLY FORMED 3D TRANSISTORS THAT HAVE COMPLETED FIN FORMATION AND GATE METAL DEPOSITION
504
SELECTIVELY ETCH THE GATE METAL TO REMOVE A PORTION OF THE GATE METAL IN THE ISOLATION REGION OF THE WAFER SUBSTRATE
506
DEPOSIT A GATE DIELECTRIC MATERIAL IN THE ISOLATION REGION OF THE WAFER SUBSTRATE TO FILL IN THE PORTION OF THE GATE METAL THAT WAS REMOVED
508
CHEMICAL MECHANICAL POLISH A TOP SURFACE OF THE GATE METAL ON THE FIRST DIFFUSION REGION AND THE SECOND DIFFUSION REGION TO BE FLUSH WITH A TOP SURFACE OF THE GATE DIELECTRIC MATERIAL
510
DEPOSIT ADDITIONAL GATE METAL ON THE PREVIOUSLY DEPOSITED GATE METAL AND THE GATE DIELECTRIC MATERIAL
512
DEPOSIT A CONDUCTING LAYER ON THE ADDITIONAL GATE METAL

FIG. 5

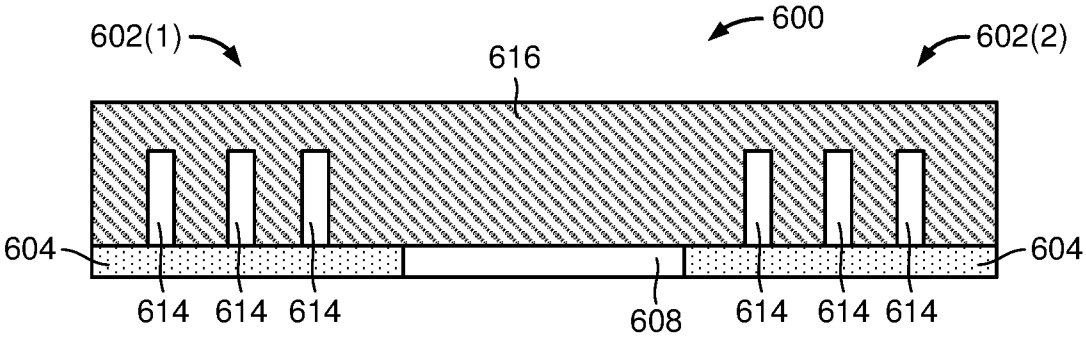


FIG. 6A

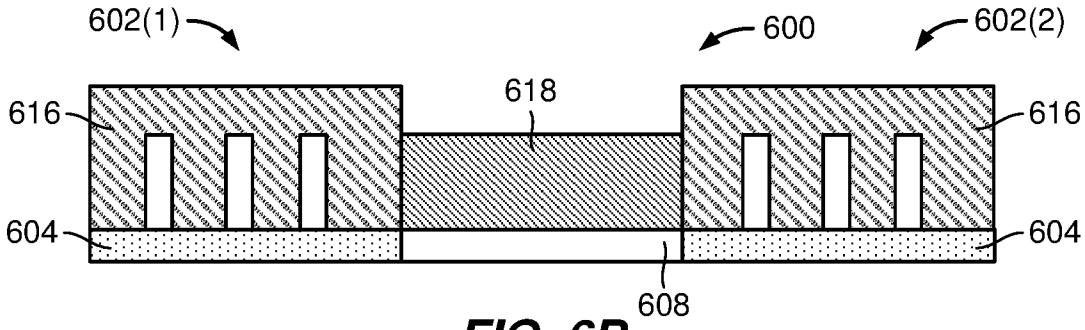


FIG. 6B

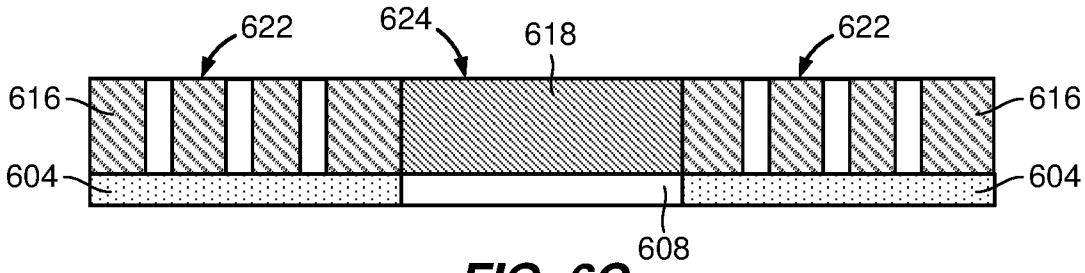


FIG. 6C

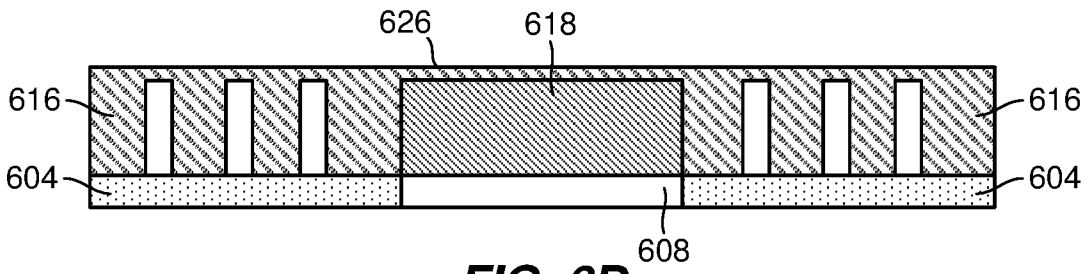


FIG. 6D

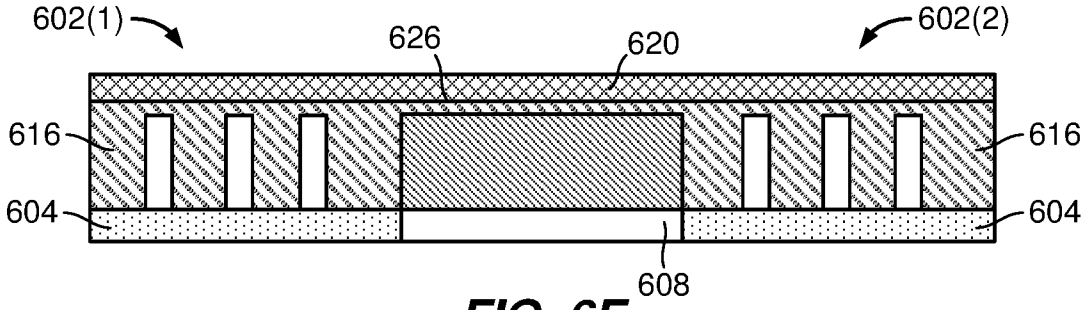


FIG. 6E

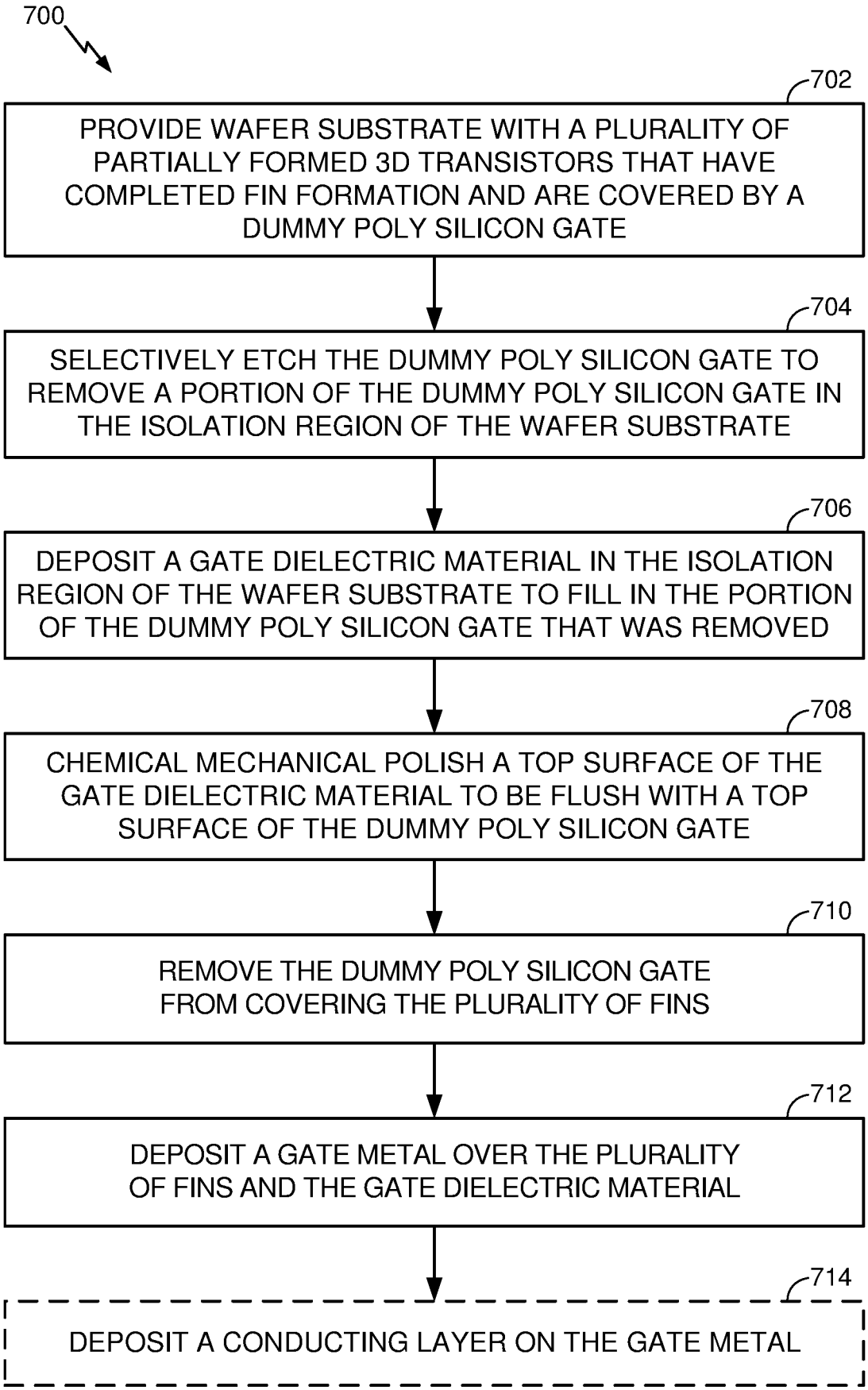

700
702
PROVIDE WAFER SUBSTRATE WITH A PLURALITY OF PARTIALLY FORMED 3D TRANSISTORS THAT HAVE COMPLETED FIN FORMATION AND ARE COVERED BY A DUMMY POLY SILICON GATE
704
SELECTIVELY ETCH THE DUMMY POLY SILICON GATE TO REMOVE A PORTION OF THE DUMMY POLY SILICON GATE IN THE ISOLATION REGION OF THE WAFER SUBSTRATE
706
DEPOSIT A GATE DIELECTRIC MATERIAL IN THE ISOLATION REGION OF THE WAFER SUBSTRATE TO FILL IN THE PORTION OF THE DUMMY POLY SILICON GATE THAT WAS REMOVED
708
CHEMICAL MECHANICAL POLISH A TOP SURFACE OF THE GATE DIELECTRIC MATERIAL TO BE FLUSH WITH A TOP SURFACE OF THE DUMMY POLY SILICON GATE
710
REMOVE THE DUMMY POLY SILICON GATE FROM COVERING THE PLURALITY OF FINS
712
DEPOSIT A GATE METAL OVER THE PLURALITY OF FINS AND THE GATE DIELECTRIC MATERIAL
714
DEPOSIT A CONDUCTING LAYER ON THE GATE METAL

FIG. 7

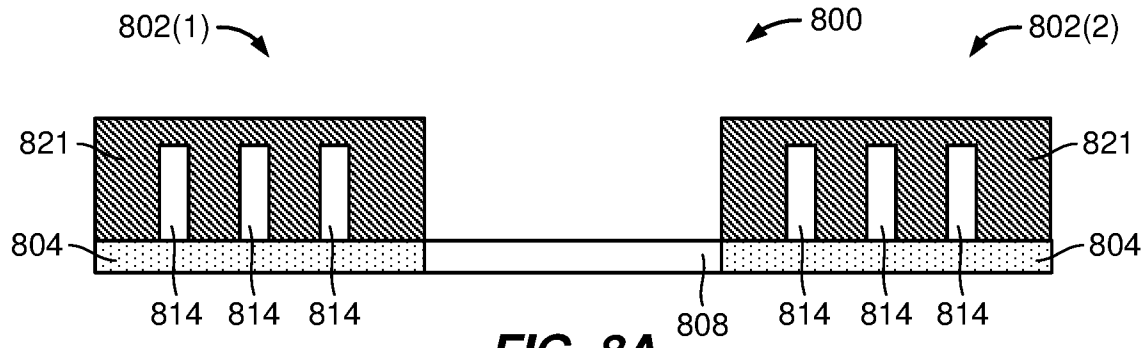


FIG. 8A

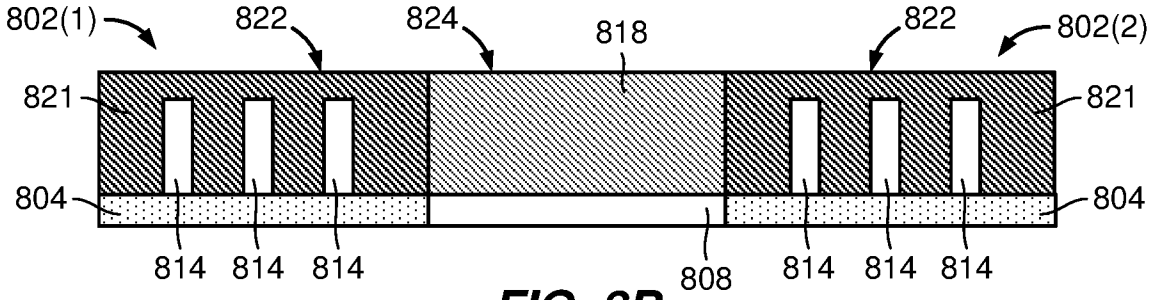


FIG. 8B

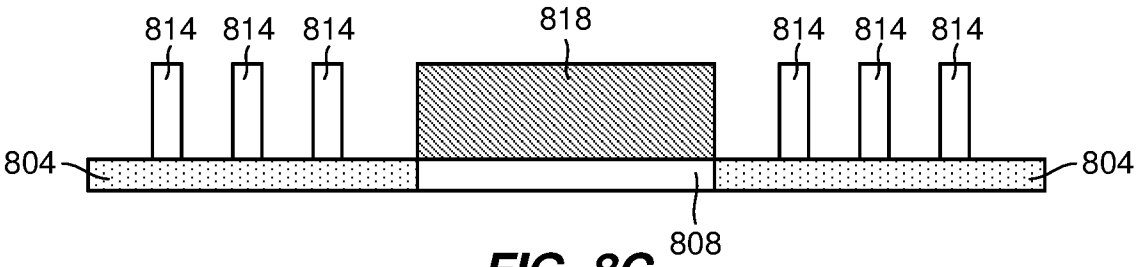


FIG. 8C

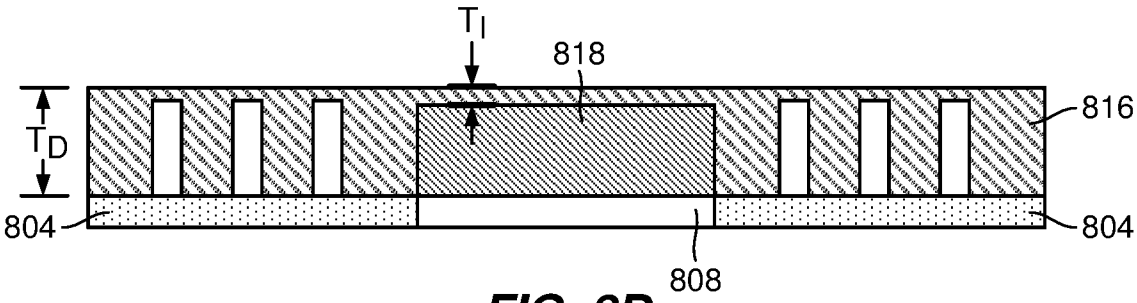


FIG. 8D

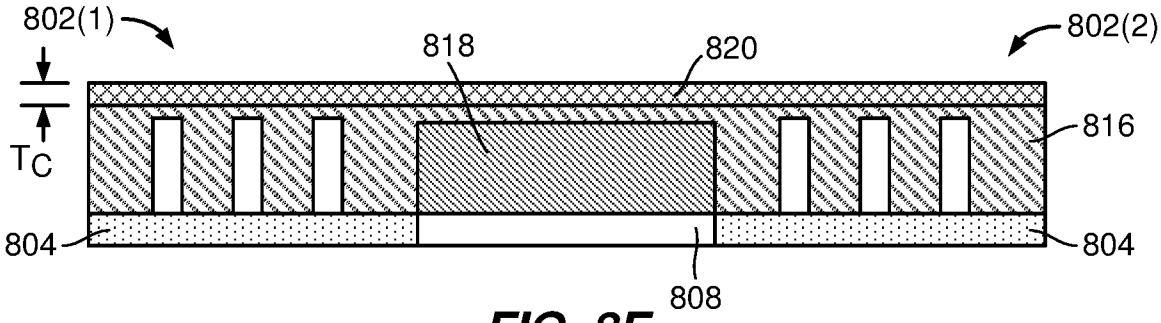
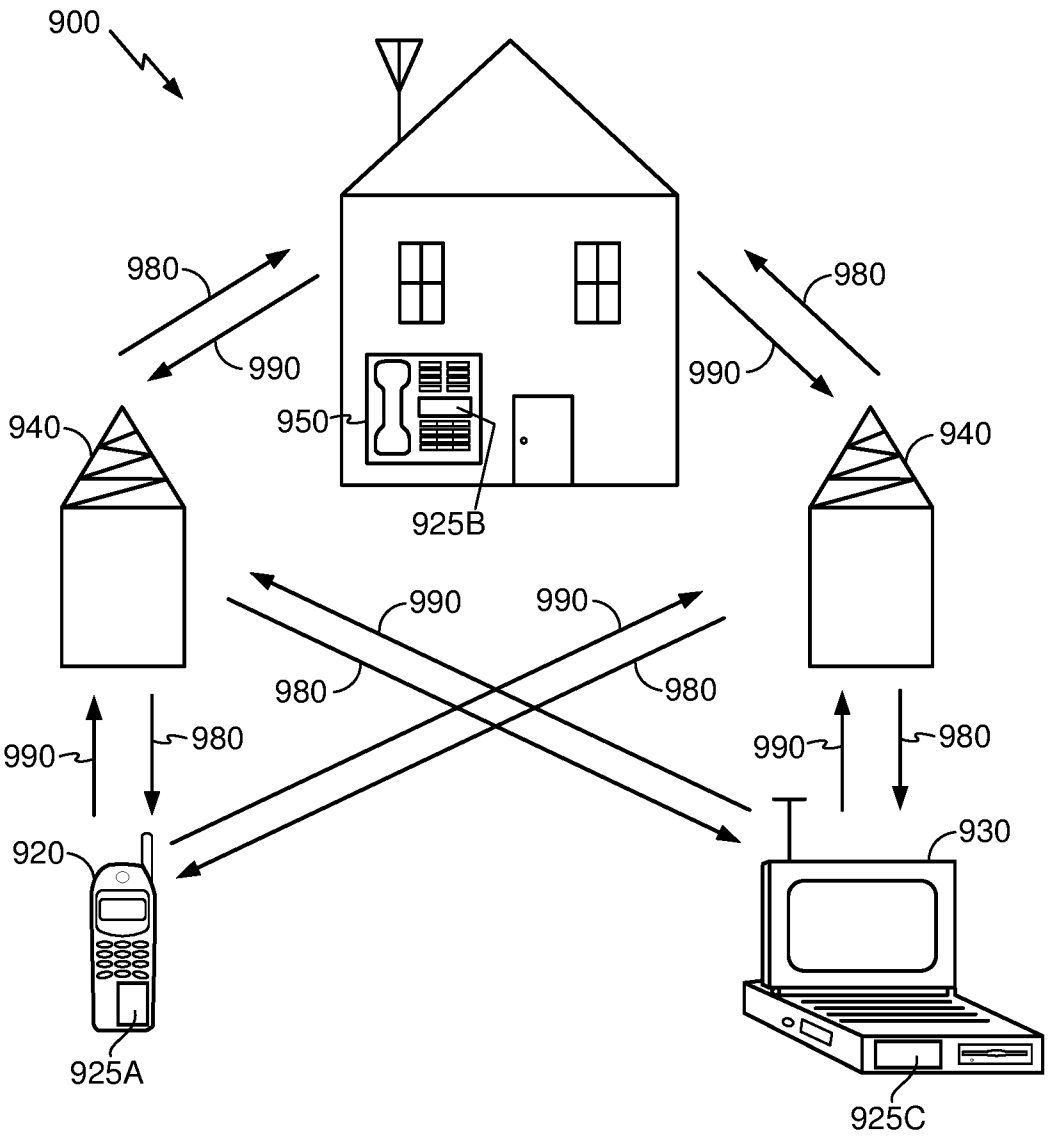


FIG. 8E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925B
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925A
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FIG. 9

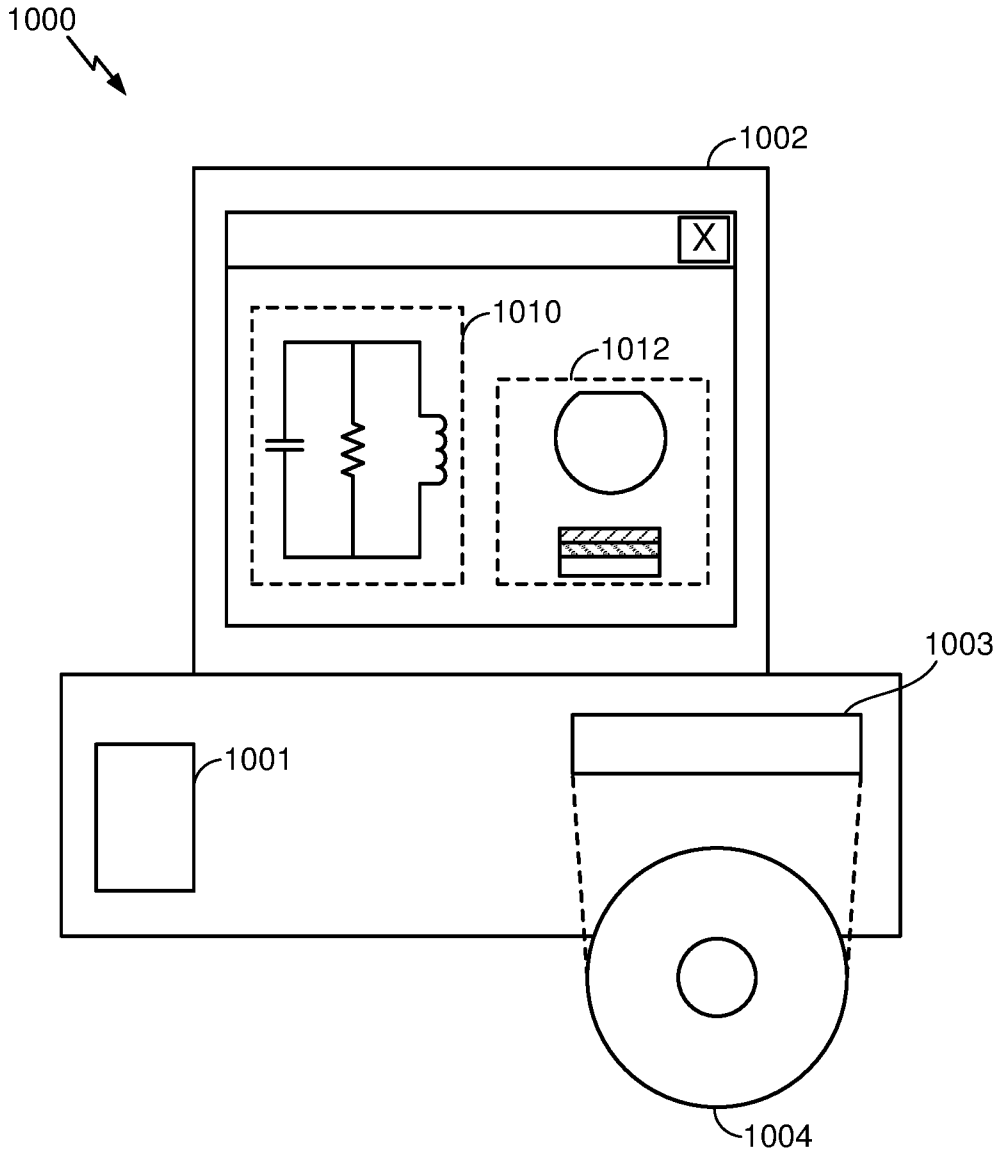

FIG. 10

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2018/061221

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/8234 H01L27/088
ADD. H01L21/8238 H01L27/092

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2016/365453 A1 (KIM JU-HYUN [KR] ET AL) 15 December 2016 (2016-12-15) paragraphs [0118], [0146], [0196] - [0220], [0250]; figures 4, 6, 8, 10, 16-18	1-8
X Y A	EP 3 244 447 A1 (IMEC VZW [BE]) 15 November 2017 (2017-11-15) paragraphs [0023], [0067] - [0108]; figure 1	1-7, 16-21 11-14 10
X Y	US 2017/018620 A1 (LIU YANXIANG [US] ET AL) 19 January 2017 (2017-01-19) paragraphs [0019], [0027], [0033] - [0040], [0058]; figures 2, 3	1-5, 8-10,15 11-14

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 January 2019	31/01/2019

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Seck, Martin

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Form PCT/ISA/210 (second sheet) (April 2005)

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2008/157365 A1 (OTT ANDREW [US] ET AL) 3 July 2008 (2008-07-03) paragraphs [0070] - [0072]; figure 5A -----	5-7, 12-14, 18-20
A	EP 0 991 114 A2 (CHARTERED SEMICONDUCTOR MFG [SG]) 5 April 2000 (2000-04-05) paragraphs [0016], [0033]; figure 6 -----	5-7, 12-14, 18-20

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2018/061221

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		US 2016365453 A1	15-12-2016
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