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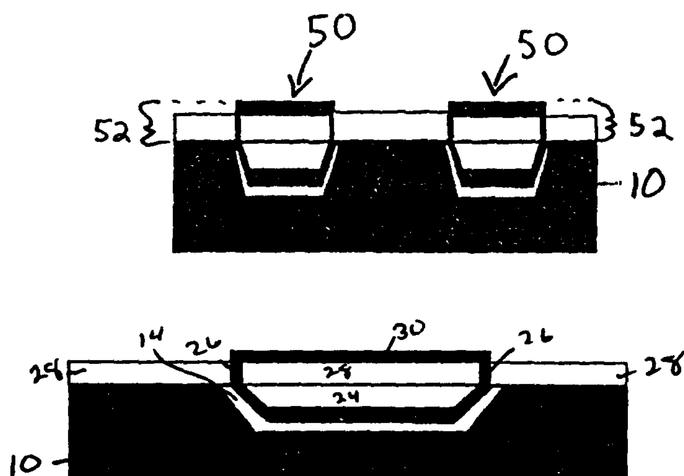
(54) Title: INTEGRATED TOROIDAL COIL INDUCTORS FOR IC DEVICES



(57) Abstract: A means for fabrication of solenoidal inductors interated in a semiconductor chip is provided. A solenoidal coil (50) is partially embedded in a deep well etched into the chip substrate (10). The non-embedded part (30) of the coil is fabricated as part of BEOL metallization layers (52). This allows for large cross-sectional area of the solenoid turns, tus reducing the turn-to-turn capacitive coupling. Because the solenoidal coils of this invention have a large diameter cross-section, the coil can be made with a large inductance value and yet occupy a small area of the chip. The farbication process includes etching of a deep cavity in the substrate after all the FEOL steps are completed; lining said cavity with a dielectric (14) followed by fabrication of the part of the coil (22) that will be embedded by deposition of a conductive material metal through a mask; deposition of dielectric (24 and 28) and planarization of the same by CMP. After planarization the fabrication of the remaining part (30) of the solenoidal coil is fabricated as part of the metallization in the BEOL (i.e. as line/vias of the BEOL). To further increase the cross section of the solenoidal coil, part of it may be built by electrodeposition through a mask on top of the BEOL layers.

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INTEGRATED TOROIDAL COIL INDUCTORS FOR IC DEVICES

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DESCRIPTION

10 The present invention relates to semiconductor devices, and more particularly to a multiturn solenoidal inductor integrated in a semiconductor chip, such as those used for radio frequency (RF) communications. The present invention also relates to a method of fabricating the inventive multiturn solenoidal inductor.

15 Inductors integrated in semiconductor chips are normally fabricated in the shape of spirals in one BEOL (back-end-of-the-line) metallization level (plus vias to connect to and from the return arm). Because of the limited thickness of BEOL metallization layers (on the order of about 2 to about 4 microns), spiral inductors have a relatively high resistance (on the order of about 1-5 ohms or greater) for a given inductance 20 value. Dual metal layers, with interconnecting vias, are sometimes utilized to reduce the spiral resistance. Because the inductance value is directly related to the length of the inductor trace, spiral inductors are limited to fairly small inductance values (on the order of about 20 nHenries or less), and occupy a fairly large area of the chip. Because the electromagnetic field of a spiral inductor is not confined, active devices 25 are typically not allowed under the inductor, and thus spiral inductors occupy a lot of chip real estate.

Integrated solenoidal inductors can also be fabricated in the BEOL layers of a semiconductor chip. These devices have limitations arising from the high capacitive 30 coupling between the solenoidal turns, which arises from the fact that the total thickness of the BEOL layers is very small, on the order of about 8 to about 10 microns, so the solenoidal turns are necessarily in close vertical proximity to each other. This close proximity also limits the cross-sectional area of the solenoid which

directly limits the achievable inductance, since solenoidal inductance is directly related to cross-sectional area.

In view of the above drawbacks in the prior art, there is a continued need for developing a multiturn solenoidal inductor integrated in a semiconductor chip which overcomes the foregoing prior art problems.

The present invention provides a multiturn solenoidal inductor integrated in a semiconductor chip. The present invention further provides a multiturn solenoidal inductor integrated in a semiconductor chip wherein the solenoid turns are sufficiently separate from each other, thereby reducing capacitive coupling between the solenoid turns.

Still further, the present invention is directed to an integrated structure which contains solenoidal coils having large diameter cross-sections associated therewith. Even further, the present invention provides an integrated structure which has solenoidal coils having a large inductance value, yet occupy a small area of the chip.

The present invention, and its advantages, are obtained by providing solenoidal inductors integrated in a semiconductor chip wherein the solenoidal coil is partially embedded in a deep well (i.e., cavity) etched into the semiconductor chip. The term "deep well" as used herein denotes a cavity whose depth from an upper surface of the semiconductor chip is from about 10 to about 50 microns, preferably from about 20 to about 25 microns. This allows for large separation of solenoid turns, and thus reduces the capacitive coupling between the turns. Because the solenoidal coils of the present invention have a large diameter cross-section (on the order of about 25 to about 35 microns), the inventive coils can be made with a large inductance value and yet occupy a small area of the chip.

One aspect of the present invention thus relates to a semiconductor structure which comprises a solenoidal coil integrated with an integrated circuit (IC) chip, wherein

said solenoidal coil is partially embedded inside a cavity formed in a substrate of said IC chip and partially in back-end-of-the-line layers of said IC chip.

In one embodiment of the present inventor, the solenoidal coil includes a magnetic
5 core. In another embodiment of the present inventor, the solenoidal coil is in the shape of a toroid.

Another aspect of the present invention relates to an electrical transformer which comprises two solenoidal coils having a common magnetic core.

10

A still further aspect of the present invention relates to a method of fabricating the above-mentioned semiconductor structure. Specifically, the inventive semiconductor structure is fabricated by the following processing steps that include:

15 (a) forming one or more cavities in a substrate of an integrated circuit (IC) chip;

(b) forming a first dielectric material over said substrate including in said one or more cavities;

20 (c) removing said first dielectric material abutting said one or more cavities, while leaving said first dielectric material in said one or more cavities as a liner;

(d) forming a bottom coil element of a solenoidal coil in said one or more dielectric lined cavities;

25

(e) forming a second dielectric material over said substrate including said bottom coil element of said solenoidal coil;

(f) removing said second dielectric material over said substrate not containing said one
30 or more cavities; and

(g) forming side coil elements and a top coil element of said solenoidal coil, wherein said top coil element is in electrical contact with said bottom coil element through said side coil elements.

5 In one embodiment of the inventive method, side coil elements are formed in step (d), and step (g) only includes formation of a top coil element.

FIG 1A shows a cross-section (not to scale) of an integrated circuit (IC) wafer with a toroidal coil partially embedded in the substrate; whereas FIG 1B shows a top-view of
10 the solenoidal coil shown in FIG 1A. A toroidal coil is a special case of the more general solenoidal shape in which a solenoid is bent back upon itself. This configuration ideally confines all of the magnetic field in the cross-sectional area of the toroid.

15 FIGS 2A-J show cross-sections of an IC wafer at different stages of fabrication of the solenoidal coil of the present invention.

FIG 3 shows a cross-section of a solenoidal coil with a magnetic core fabricated inside it.

20

The present invention, which provides a multiturn solenoidal inductor integrated in a semiconductor chip and a method of fabricating the same, will now be described in more detail by referring to the drawings that accompany the present application. It should be noted that in the accompanying drawings, like and/or corresponding
25 elements are referred to by like reference numerals.

Reference is first made to FIGS 1A (cross-sectional view) and 1B (top view) which illustrate the inventive semiconductor structure. Specifically, FIG 1A comprises a structure that includes substrate 10 having one or more solenoidal coils 50 formed
30 inside cavities that are formed in the substrate and partially in BEOL wiring levels 52. A top view of solenoidal coils 50 of FIG 1A is shown, for example, in FIG 1B.

In accordance with the present invention, each solenoidal coil 50 includes bottom coil element 22 and top coil element 30 that are in electrical contact with each through side coil elements 26. First dielectric layer 12 is formed between bottom coil element 22
5 and substrate 10 and second dielectric layer 24 is formed in between the top and bottom coil elements. The elements mentioned above that are not included in FIGS 1A-1B will be described in more detail in FIGS 2A-J.

As is shown, the coil is fabricated partially inside a cavity formed in the IC substrate
10 and partially within BEOL wiring levels. In this way, a truly three-dimensional structure can be fabricated, which is nevertheless contained with the thickness boundary of an otherwise standard IC chip. It is also noted that the coils of the present invention have a large diameter cross-section (on the order of about 25 to 35 microns); therefore the coils can be made with a large inductance value and yet occupy a small
15 area of the chip.

The processing steps used in the present invention in fabricating the structure shown in FIGS 1A and 1B will now be described in more detail by referring to FIGS 2A-J as well as the description that follows hereinbelow.

20

Specifically, FIG 2A shows an initial structure that is employed in the present invention in forming the inventive structure illustrated in FIGS 1A-B. The initial structure includes substrate 10 of an integrated circuit chip having cavities 12 (only one of which is shown in these drawings) formed partially therein. Note the cavities
25 are formed after all the front-end-of-the-line (FEOL) processing of the IC chip is completed, and a passivating layer (not shown in the drawings) of oxide or boron phosphorous-doped silicate glass (BPSG) is deposited on the wafer. This passivating layer is not shown herein since it is locally removed in the region illustrated.

30 The structure shown in FIG 2A includes conventional materials well known to those skilled in the art, and conventional processes are employed in fabricating the same.

For example, substrate 10 comprises any semiconducting material including, but not limited to: Si, Ge, SiGe, GaAs, InP, InAs and other-like III/V compound semiconductors. Substrate 10 may also be a layered semiconductor such as Si/SiGe or Si/Si as well as a silicon-on-insulator (SOI). The substrate may contain various active device regions either formed therein or formed on a surface of the substrate opposite to that of cavities 12.

Cavities 12 are formed utilizing conventional lithography (including applying a photoresist to a surface of the substrate, exposing the photoresist to a pattern of radiation and developing the pattern) and etching. The etching step includes a dry etching process such as reactive-ion etching (RIE), ion beam etching or plasma etching or a chemical wet etch process that includes a chemical etchant that is highly selective towards the substrate material. In accordance with the present invention, cavities 12 are deep cavities whose depth from the upper surface is from about 10 to about 50 microns, with a depth of from about 20 to about 25 microns being more highly preferred.

Next, first dielectric material 14 is deposited over the structure shown in FIG 2A including the top surface of substrate 10 and in cavities 12 so as to provide the structure illustrated in FIG 2B. The first dielectric material, which may be composed of an oxide such as SiO_2; nitride such as Si_3N_4; or polyimide, is formed utilizing any conventional blanket deposition process which is capable of forming a conformal layer of first dielectric material 14 on the structure. For example, first dielectric material 14 may be deposited by chemical vapor deposition (CVD), plasma-assisted CVD, sputtering and other like blanket deposition processes. The thickness of the first dielectric material may vary depending upon the type of blanket deposition process and dielectric material employed. Typically, however, the first dielectric material has a thickness of from about 1 to about 10 microns, with a thickness of from about 4 to about 5 microns being more highly preferred.

Next, any first dielectric material that is outside cavity 12 is removed from the structure providing the structure shown in FIG 2C. Note, that after this removal step the cavity in the substrate is lined with first dielectric material 14. The removal step of the present invention, which results in formation of cavities that are lined with first
5 dielectric material 14, is performed utilizing conventional planarization processes such as chemical-mechanical polishing (CMP) or grinding.

A blanket liner (e.g., TaN/Ta, TiN, WN or other like diffusion barrier material) and seed layer (e.g., Cu, Al, W, or other like conductive material) to be used for deposition
10 of the coil material is deposited, followed by a very thick photoresist. It is noted that in FIG 2D reference numeral 16 refers to both the blanket liner and seed layer, whereas reference numeral 18 refers to the photoresist.

FIG 2E shows the structure after photoresist 18 is patterned by l-line, x-ray, and etc.
15 irradiation with a large depth of focus. Note that in FIG 2E, reference numeral 20 denotes the areas of the photoresist that will be developed using a conventional photoresist developer providing the area for subsequent formation of the coil elements. In the case of a wet etched cavity, this pattern consists of the bottom elements of the coil, as well as the part of the side (rising) segments, up to, or slightly above, the level
20 of the wafer surface (i.e., the top of the cavity). For cavities with vertical sides, such as obtained by RIE, the pattern on this mask consists only of the bottom elements of the coil; fabrication of the rising elements of coil, up to the wafer surface, requires a second lithography step (using another mask consisting only of "vias"). Note the remaining drawings show this second lithography step, which may be omitted in some
25 embodiments.

After appropriate cleaning of the developed areas, coil element 22 are formed using standard techniques including, but not limited to: electrodeposition, sputtering and plating. The bottom coil elements are composed of a conventional conductive
30 material such as Cu, Al, W and other like conductors. The resultant structure

containing bottom coil elements 22 is shown, for example, in FIG 2F. Note that in this figure bottom coil elements 22 includes portions of liner/seed layer 16.

The remaining photoresist 18 is then stripped from structure shown in FIG 2F utilizing
5 conventional processes well known in the art, and any liner/seed layer 16 not containing bottom coil elements 22 is removed from the structure utilizing a conventional etching process such as RIE. These two processing steps are illustrated in FIG 2G.

10 Second dielectric material 24 is then formed over the structure utilizing one of the above-mentioned deposition processes that is employed in forming first dielectric material 14. Second dielectric material 24 may be composed of the same or different dielectric as first dielectric material 14. In a preferred embodiment of the present invention, the first and second dielectric materials are composed of the same
15 dielectric. Following deposition of second dielectric material 24, the structure is subjected to a conventional planarization process such as CMP providing the structure shown in FIG 2H. Note that during the planarization process some of bottom coil element 22 that is above the top surface of cavity 12 may also be removed.

20 Completion of the missing part of the rising elements (i.e., side coil elements 26) is accomplished as part of the BEOL fabrication of the chip by standard processes such as damascene or dual damascene, FIG 2I. This includes deposition of dielectric 28, patterning dielectric 28 by conventional lithography and etching so as to form openings in dielectric 28 which exposed bottom coil element 22, and deposition of a
25 conductive metal in the openings. Note that the side coil elements are preferably composed of the same conductive material as the bottom coil element. It is again emphasized that the formation of side coil elements may have been performed earlier; therefore the lithography and etching of the openings and subsequent filling the openings with a conductive material may be omitted.

30

The horizontal elements (i.e., top coil element 30) that complete the coil loops are fabricated either as part of the BEOL layers, or on top of the BEOL by electrodeposition, sputtering or plating a conductive material (same or different as the bottom and side coil elements, preferably the same conductive material as both the bottom and side coil elements) through a mask (not shown). The resultant structure is shown, for example, in FIG 2J.

In one embodiment of the present invention, the solenoidal coil is in the shape of a toroid. In another embodiment of the present invention, a core of magnetic material 32 such as Permalloy and AlNiCo may be incorporated at a suitable position in the middle of the coil, See FIG 3. Specifically, magnetic material 32 is formed in the structure utilizing a conventional deposition process such as CVD, plasma-assisted CVD, sputtering, plating or chemical solution deposition.

While the present invention has been particularly shown and described with respect to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and detail may be made without departing from the spirit and scope of the present invention. It is therefore intended that the present invention not be limited to the exact forms and details described and illustrated, but fall within the scope of the appended claims.

CLAIMS

1 1. A semiconductor structure comprising a solenoidal coil integrated with an
2 integrated circuit (IC) chip, wherein said solenoidal coil is partially embedded inside a
3 cavity formed in a substrate of said IC chip and partially in back-end-of-the-line layers
4 of said IC chip.

1 2. The semiconductor structure of Claim 1 wherein the solenoidal coil includes a
2 magnetic core formed between coil elements.

1 3. The semiconductor structure of Claims 1 or 2 wherein the solenoidal coil has a
2 toroid shape.

1 4. The semiconductor structure of any one of Claims 1-3 wherein said solenoidal coil
2 comprises a bottom coil element and a top coil element that are in electrical contact
3 with each other through side coil elements.

1 5. The semiconductor structure of any one of Claims 1-4 wherein said solenoidal coil
2 is composed a conductive material selected from the group consisting of Cu, Al and
3 W.

1 6. The semiconductor structure of Claim 4 wherein each of said coil elements are
2 composed of the same or different conductive material.

1 7. The semiconductor structure of any one of Claims 1-6 wherein said cavity has a
2 depth of from about 10 to about 50 microns from a top surface of said substrate.

1 8. The semiconductor structure of Claim 7 wherein said depth is from about 20 to
2 about 25 microns.

1 9. The semiconductor structure of any one of Claims 1-8 wherein said cavity is lined
2 with a first dielectric material.

1 10. The semiconductor structure of Claim 9 wherein said first dielectric material is
2 composed of a dielectric selected from the group consisting of an oxide, a nitride and
3 polyimide.

1 11. The semiconductor structure of any one of Claims 1-10 wherein said cavity
2 includes a second dielectric material that separates top coil elements from bottom coil
3 elements.

1 12. The semiconductor structure of Claim 11 wherein said second dielectric material
2 is composed of a dielectric selected from the group consisting of an oxide, a nitride
3 and a polyimide.

1 13. The semiconductor structure of any one of Claims 1-12 wherein said back-end-of-
2 the-line layers include at least a dielectric material.

1 14. The semiconductor structure of Claim 2 wherein said magnetic core includes a
2 magnetic material selected from the group consisting of Permalloy and AlNiCo.

1 15. An electrical transformer which comprises two solenoidal coils of Claim 1 having
2 a common magnetic core.

1 16. A method of fabricating a semiconductor structure comprising the steps of:
2
3 (a) forming one or more cavities in a substrate of an integrated circuit (IC) chip;
4
5 (b) forming a first dielectric material over said substrate including in said one or more
6 cavities;
7

8 (c) removing said first dielectric material abutting said one or more cavities, while
9 leaving said first dielectric material in said one or more cavities as a liner;
10
11 (d) forming a bottom coil element of a solenoidal coil in said one or more dielectric
12 lined cavities;
13
14 (e) forming a second dielectric material over said substrate including said bottom coil
15 element of said solenoidal coil;
16
17 (f) removing said second dielectric material over said substrate not containing said one
18 or more cavities; and
19
20 (g) forming side coil elements and a top coil element of said solenoidal coil, wherein
21 said top coil element is in electrical contact with said bottom coil element through said
22 side coil elements.

1 17. The method of Claim 16 wherein said one or more cavities are formed by
2 lithography and etching.

1 18. The method of Claim 16 or 17 wherein said substrate includes a passivating layer
2 formed thereon.

1 19. The method of any one of Claims 16-18 wherein said first dielectric has a
2 thickness of from about 1 to about 10 microns.

1 20. The method of Claim 19 wherein said first dielectric has a thickness of from about
2 4 to about 5 microns.

1 21. The method of any one of Claims 16-20 wherein said first dielectric material is
2 formed by a blanket deposition process.

1 22. The method of any one of Claims 16-21 wherein step (c) is carried out by a
2 planarization process.

1 23. The method of Claim 22 wherein said planarization process is chemical-
2 mechanical polishing.

1 24. The method of any one of Claims 16-23 wherein said bottom coil element is
2 formed by the steps of: forming a liner/seed layer on said first dielectric material;
3 forming a patterned photoresist on said substrate wherein said patterned photoresist
4 does not cover portions of said liner/seed layer in said cavity; and depositing a
5 conductive material onto said liner/seed layer.

1 25. The method of Claim 24 wherein said conductive material is deposited by an
2 electrodeposition process.

1 26. The method of any one of Claims 16-25 wherein said second dielectric material is
2 formed by deposition.

1 27. The method of any one of Claims 16-26 wherein step (f) includes a planarization
2 process.

1 28. The method of Claim 27 wherein said planarization process is chemical-
2 mechanical polishing.

1 29. The method of any one of Claims 16-28 wherein said side coil elements are
2 formed by damascene or dual damascene processes.

1 30. The method of any one of Claims 16-29 wherein said side coil elements are
2 formed by the steps of: forming a dielectric over said substrate including said second
3 dielectric material; providing openings in said dielectric exposing portions of said
4 bottom coil element; and filling said openings with a conductive material.

1 31. The method of any one of Claims 16-30 wherein said top coil element is formed
2 by deposition of a conductive material through a patterned mask.

1 32. The method of Claim 31 wherein said deposition comprises electrodeposition.

1 33. The method of any one of Claims 16-32 wherein side coil elements are also
2 formed in step (d) and step (g) only includes formation of said top coil element.

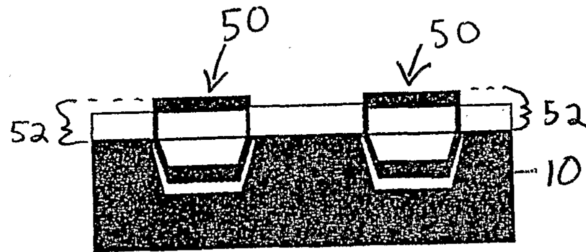

FIG 1A

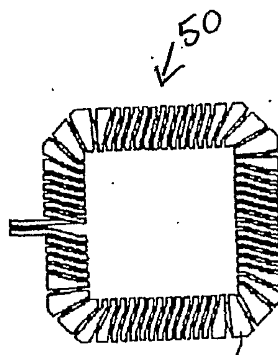

FIG 1B

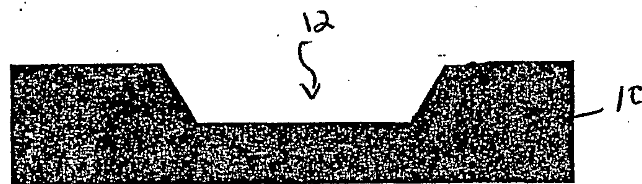

FIG 2A

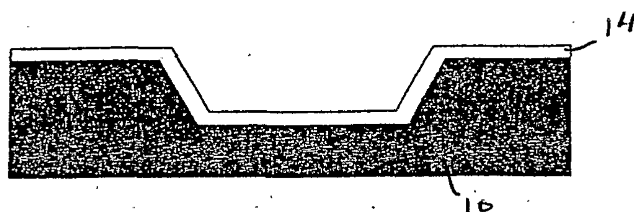

FIG 2B

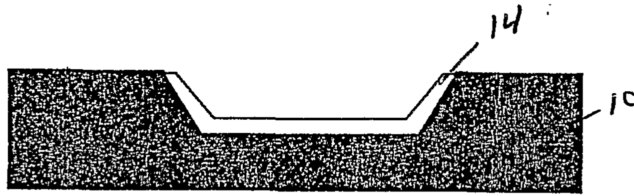

FIG 2C

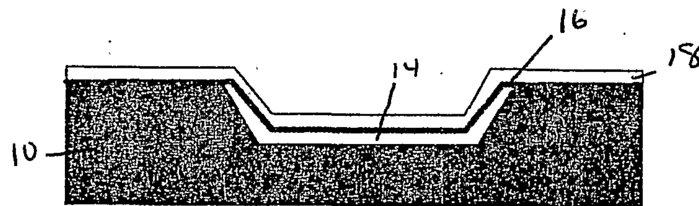

FIG 2D

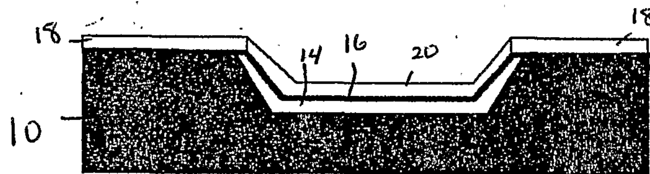

FIG 2E

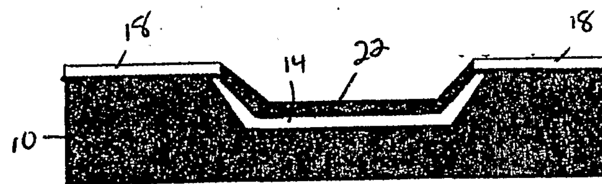

FIG 2F

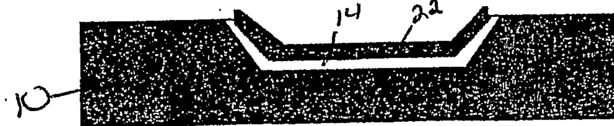

FIG 2G

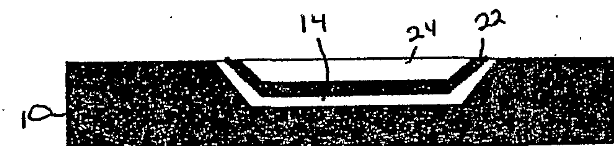

FIG 2H

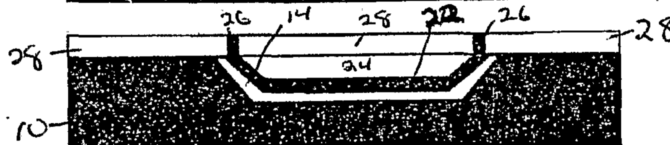

FIG 2I

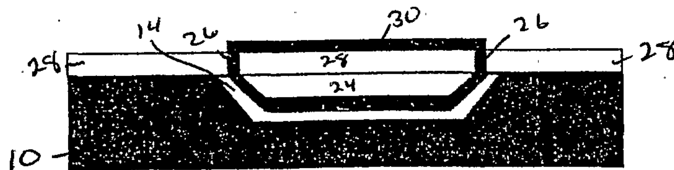

FIG 2J

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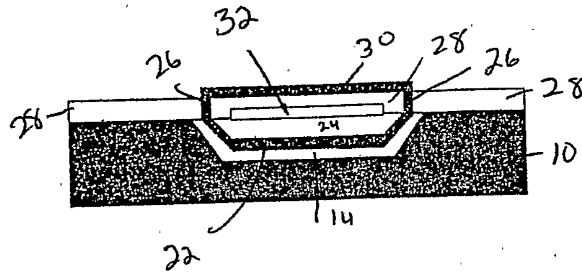

FIG 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/07992

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) :H01L 29/82, 43/00, 29/00
US CL :257/421, 422, 531, 534; 438/48, 255, 358
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
U.S. : 257/421, 422, 531, 534; 438/48, 255, 358

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y	US 5,793,272 A (BURGHARTZ et al.) 11 August 1998 (11.08.1998), figs. 9-12.	7, 8, 14, 15

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

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