(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
09 February 2023 (09.02.2023)

WIPO | PCT

(10) International Publication Number
WO 2023/014355 A1

(51) International Patent Classification:
H03F 1/02 (2006.01) *H03F 3/24* (2006.01)
H03F 3/189 (2006.01)

(21) International Application Number:
PCT/US2021/044596

(22) International Filing Date:
05 August 2021 (05.08.2021)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant: **QORVO US, INC.** [US/US]; 7628 Thorndike Road, Greensboro, North Carolina 27409 (US).

(72) Inventors: **KHLAT, Nadim**; ZAC des Ramassiers, Numero 1, Allee Maurice MAGRE, 31770 Colomiers (FR).

POTTS, Jeffrey D.; 7628 Thorndike Road, Greensboro, North Carolina 27409 (US).

(74) Agent: **WANG, Huaiyuan**; Withrow & Terranova, P.L.L.C, 106 Pinedale Springs Way, Cary, North Carolina 27511 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, IT, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(54) **Title:** POWER MANAGEMENT CIRCUIT SUPPORTING FAST VOLTAGE SWITCHING WITH REDUCED RUSH CURRENT

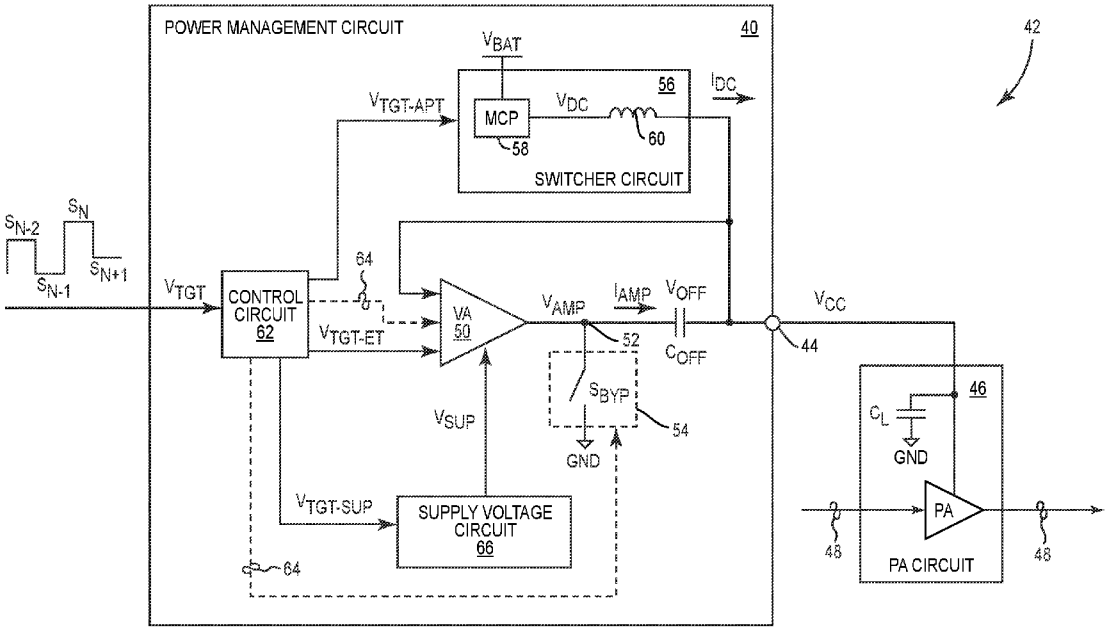

FIG. 3

(57) **Abstract:** A power management circuit supporting fast voltage switching with reduced rush current is provided. The power management circuit is configured to provide an average power tracking (APT) voltage to a power amplifier circuit for amplifying an analog signal. Moreover, the power management circuit must be able to adapt the APT voltage frequently and rapidly to enable such application as dynamic power control. In embodiments disclosed herein, the power management circuit can be configured to opportunistically activate a voltage amplifier, which is typically used to generate an envelope tracking (ET) voltage, at an appropriate time to help support fast switching of the APT voltage. As a result, the power management circuit is able to adapt the APT voltage frequently and rapidly. Furthermore, by utilizing the voltage amplifier to support fast switching of the APT voltage, it is also possible to reduce rush current in the power management circuit.

WO 2023/014355 A1

[Continued on next page]

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

POWER MANAGEMENT CIRCUIT SUPPORTING FAST VOLTAGE SWITCHING WITH REDUCED RUSH CURRENT

Field of the Disclosure

[0001] The technology of the disclosure relates generally to an envelope tracking (ET) and/or average power tracking (APT) power management circuit.

Background

[0002] Fifth-generation (5G) new radio (NR) (5G-NR) has been widely regarded as the next generation of wireless communication technology beyond the current third-generation (3G) and fourth-generation (4G) technologies. In this regard, a wireless communication device capable of supporting the 5G-NR wireless communication technology is expected to achieve higher data rates, improved coverage range, enhanced signaling efficiency, and reduced latency across a wide range of radio frequency (RF) bands, which include a low-band (below 1 GHz), a mid-band (1 GHz to 6 GHz), and a high-band (above 24 GHz).

[0003] Downlink and uplink transmissions in a 5G-NR system are widely based on orthogonal frequency division multiplexing (OFDM). In this regard, Figure 1 is a schematic diagram of an exemplary OFDM time-frequency grid 10 illustrating at least one reserve block (RB 12) for physical resource allocation in the 5G-NR system. The OFDM time-frequency grid 10 includes a frequency axis 14 representing a frequency domain and a time axis 16 representing a time domain. Along the frequency axis 14, there are a number of subcarriers 18(1)-18(M). The subcarriers 18(1)-18(M) are orthogonally separated from each other by a subcarrier spacing (SCS) of 15 KHz, for example. Along the time axis 16, there are a number of OFDM symbols 20(1)-20(N). Each of the OFDM symbols 20(1)-20(N) is separated by a cyclic prefix (CP) (not shown) configured to act as a guard band to help overcome inter-symbol interference (ISI) between the OFDM symbols 20(1)-20(N). In the OFDM time-frequency grid 10, each intersection of the subcarriers 18(1)-18M) and the OFDM symbols 20(1)-20(N) defines a resource element (RE) 22.

[0004] In a 5G-NR communication system, an RF signal 24 can be modulated into multiple subcarriers among the subcarriers 18(1)-18(N) in the frequency domain (along the frequency axis 14) and multiple OFDM symbols among the OFDM symbols 20(1)-20(N) in the time domain (along the time axis 16). The table (Table 1) below summarizes OFDM configurations supported by the 5G-NR communication system.

Table 1

SCS (KHz)	Slot Length (μs)	# of Slots per Subframe	CP (μs)	OFDM Symbol Duration (μs)	Modulation Bandwidth (MHz)
15	1000	1	4.69	71.43	50
30	500	2	2.34	35.71	100
60	250	4	1.17	17.86	200
120	125	8	0.59	8.93	400

[0005] In the 5G-NR communication system, the RF signal 24 is typically modulated with a high modulation bandwidth in excess of 200 MHz. In this regard, according to Table 1, the SCS will be 120 KHz and a transition settling time between two consecutive OFDM symbols among the OFDM symbols 20(1)-20(N) (e.g., amplitude change of the RF signal) needs to be less than or equal to the CP duration of 0.59 μs.

[0006] In addition, the wireless communication device may also need to support such internet-of-things (IoT) applications as keyless car entry, remote garage door opening, contactless payment, mobile boarding pass, and so on. Needless to say, the wireless communication device must also always make 911/E911 service accessible under emergency situations. As such, it is critical that the wireless communication device remains operable whenever needed.

[0007] Notably, the wireless communication device relies on a battery cell (e.g., Li-Ion battery) to power its operations and services. Despite recent advancement in battery technologies, the wireless communication device can run into a low battery situation from time to time. In this regard, it is desirable to

prolong battery life concurrent to enabling fast voltage changes between the OFDM symbols 20(1)-20(N).

Summary

[0008] Embodiments of the disclosure relate to a power management circuit supporting fast voltage switching with reduced rush current. The power management circuit is configured to provide an average power tracking (APT) voltage to a power amplifier circuit for amplifying an analog signal. Moreover, the power management circuit must be able to adapt the APT voltage frequently and rapidly to enable such application as dynamic power control. In embodiments disclosed herein, the power management circuit can be configured to opportunistically activate a voltage amplifier, which is typically used to generate an envelope tracking (ET) voltage, at an appropriate time to help support fast switching of the APT voltage. As a result, the power management circuit is able to adapt the APT voltage frequently and rapidly. Furthermore, by utilizing the voltage amplifier to support fast switching of the APT voltage, it is also possible to reduce rush current in the power management circuit to help prolong battery life.

[0009] In one aspect, a power management circuit is provided. The power management circuit includes a voltage output that outputs an APT voltage to a power amplifier circuit for amplifying an analog signal. The power management circuit also includes a voltage amplifier coupled to the voltage output and configured to generate an ET voltage based on an ET target voltage and a supply voltage. The power management circuit also includes a control circuit. The control circuit is configured to receive a target voltage indicating that the APT voltage will change from a present voltage level in a present time interval to a future voltage level in an upcoming time interval. The control circuit is also configured to activate the voltage amplifier prior to a start of the upcoming time interval to thereby cause the APT voltage to change to the target voltage within a defined temporal limit from the start of the upcoming time interval.

[0010] In another aspect, a power management apparatus is provided. The power management apparatus includes a power amplifier circuit configured to amplify an analog signal based on an APT voltage. The power management apparatus also includes a power management circuit. The power management circuit includes a voltage output that outputs the APT voltage to the power amplifier circuit. The power management circuit also includes a voltage amplifier coupled to the voltage output and configured to generate an ET voltage based on an ET target voltage and a supply voltage. The power management circuit also includes a control circuit. The control circuit is configured to receive a target voltage indicating that the APT voltage will change from a present voltage level in a present time interval to a future voltage level in an upcoming time interval. The control circuit is also configured to activate the voltage amplifier prior to a start of the upcoming time interval to thereby cause the APT voltage to change to the target voltage within a defined temporal limit from the start of the upcoming time interval.

[0011] Those skilled in the art will appreciate the scope of the present disclosure and realize additional aspects thereof after reading the following detailed description of the preferred embodiments in association with the accompanying drawing figures.

Brief Description of the Drawing Figures

[0012] The accompanying drawing figures incorporated in and forming a part of this specification illustrate several aspects of the disclosure, and together with the description serve to explain the principles of the disclosure.

[0013] Figure 1 is a schematic diagram of an exemplary orthogonal frequency division multiplexing (OFDM) time-frequency grid illustrating at least one reserve block (RB) for physical resource allocation;

[0014] Figure 2 is a schematic diagram of an exemplary conventional power management circuit that can draw a large rush current during voltage switching;

[0015] Figure 3 is a schematic diagram of an exemplary power management circuit configured according to an embodiment of the present disclosure to

support fast voltage switching in a power management apparatus with reduced rush current;

[0016] Figure 4 is a timing diagram providing an exemplary illustration of the power management circuit of Figure 3 configured to increase an average power tracking (APT) voltage from a present voltage level in a present OFDM symbol to a future voltage level in an upcoming OFDM symbol; and

[0017] Figure 5 is a timing diagram providing an exemplary illustration of the power management circuit of Figure 3 configured to decrease an APT voltage from a present voltage level in a present OFDM symbol to a future voltage level in an upcoming OFDM symbol.

Detailed Description

[0018] The embodiments set forth below represent the necessary information to enable those skilled in the art to practice the embodiments and illustrate the best mode of practicing the embodiments. Upon reading the following description in light of the accompanying drawing figures, those skilled in the art will understand the concepts of the disclosure and will recognize applications of these concepts not particularly addressed herein. It should be understood that these concepts and applications fall within the scope of the disclosure and the accompanying claims.

[0019] It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the present disclosure. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0020] It will be understood that when an element such as a layer, region, or substrate is referred to as being "on" or extending "onto" another element, it can be directly on or extend directly onto the other element or intervening elements may also be present. In contrast, when an element is referred to as being

"directly on" or extending "directly onto" another element, there are no intervening elements present. Likewise, it will be understood that when an element such as a layer, region, or substrate is referred to as being "over" or extending "over" another element, it can be directly over or extend directly over the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly over" or extending "directly over" another element, there are no intervening elements present. It will also be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present.

[0021] Relative terms such as "below" or "above" or "upper" or "lower" or "horizontal" or "vertical" may be used herein to describe a relationship of one element, layer, or region to another element, layer, or region as illustrated in the Figures. It will be understood that these terms and those discussed above are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures.

[0022] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the disclosure. As used herein, the singular forms "a," "an," and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises," "comprising," "includes," and/or "including" when used herein specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0023] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure belongs. It will be further understood that terms used herein should be interpreted as having a meaning

that is consistent with their meaning in the context of this specification and the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0024] Embodiments of the disclosure relate to a power management circuit supporting fast voltage switching with reduced rush current. The power management circuit is configured to provide an average power tracking (APT) voltage to a power amplifier circuit for amplifying an analog signal. Moreover, the power management circuit must be able to adapt the APT voltage frequently and rapidly to enable such application as dynamic power control. In embodiments disclosed herein, the power management circuit can be configured to opportunistically activate a voltage amplifier, which is typically used to generate an envelope tracking (ET) voltage, at an appropriate time to help support fast switching of the APT voltage. As a result, the power management circuit is able to adapt the APT voltage frequently and rapidly. Furthermore, by utilizing the voltage amplifier to support fast switching of the APT voltage, it is also possible to reduce rush current in the power management circuit to help prolong battery life.

[0025] Before discussing the power management circuit according to the present disclosure, starting at Figure 3, an overview of a conventional power management circuit that can draw a lager rush current during voltage switching is first provided with reference to Figure 2.

[0026] Figure 2 is a schematic diagram of an exemplary conventional power management circuit 26 that can draw a large rush current I_{RUSH} during voltage switching. The conventional power management circuit 26 includes a voltage source 28 and a power management integrated circuit (PMIC) 30. The voltage source 28 includes a battery 32 (e.g., a Li-Ion battery) that supplies a battery voltage V_{BAT} at a coupling node 34, which may be coupled to a ground (GND) via a capacitor C_{BYP} and a resistor R_{BYP}. The PMIC 30 is coupled to the coupling node 34 to receive the battery voltage V_{BAT} and draw a battery current I_{BAT}. Accordingly, the PMIC 30 is configured to generate an APT voltage V_{CC} based on

the battery voltage V_{BAT} and provide the APT voltage V_{CC} to a power amplifier circuit 36 for amplifying an analog signal 38.

[0027] The analog signal 38 may be modulated across a wide modulation bandwidth, which can cause a large variation of RF current at the power amplifier circuit 36. As such, it is necessary to present a low impedance to the power amplifier circuit 36 to help reduce ripple in the APT voltage V_{CC} caused by the RF current. In this regard, the conventional power management circuit 26 typically includes an offset capacitor C_{OFF} to help reduce the impedance seen by the power amplifier circuit 36.

[0028] In addition to impedance matching, the offset capacitor C_{OFF} is also used to maintain the APT voltage V_{CC} at a desired voltage level. In this regard, the offset capacitor C_{OFF} needs to be charged whenever the APT voltage V_{CC} increases and discharged whenever the APT voltage V_{CC} decreases. As such, as shown in the equation (Eq. 1) below, a change rate (dV_{CC}/dt) of the APT voltage V_{CC} is dependent on how fast the offset capacitor C_{OFF} can be charged or discharged.

$$dV_{CC}/dt = I_{RUSH} / C_{OFF} \qquad \text{(Eq. 1)}$$

[0029] In the equation (Eq. 1) above, I_{RUSH} represents a rush current associated with charging/discharging of the offset capacitor C_{OFF} and C_{OFF} represents a capacitance of the offset capacitor C_{OFF}. Particularly, when the offset capacitor C_{OFF} is charged in response to an increase of the APT voltage V_{CC}, the offset capacitor C_{OFF} draws the rush current I_{RUSH} from the battery 32. Given that the capacitance C_{OFF} is typically fixed and relatively large (e.g., 2.2 μF), the only way to reduce switching time of the APT voltage V_{CC} is to increase the rush current I_{RUSH}. For example, when the APT voltage V_{CC} changes from 1 V to 5.5 V within 0.59 μs, the rush current I_{RUSH} can be as high as 17 Amps (A), which can significantly reduce operating time of the battery 32.

[0030] To avoid amplitude clipping to the analog signal 38 at the power amplifier circuit 36, the PMIC 30 is configured to generate the APT voltage V_{CC} in

accordance with an APT target voltage V_{TGT} that corresponds to average power of the analog signal 38. As such, the APT voltage V_{CC} can swing from low to high, or vice versa, from time to time. When the conventional power management circuit 26 is provided in a legacy second generation (2G), third generation (3G), or even fourth generation (4G) wireless communication device, the APT voltage V_{CC} may change at a relatively slower rate. As such, the rush current I_{RUSH} may have a lesser impact on the battery 32. However, in a fifth generation (5G) new radio (5G-NR) wireless communication device, the APT voltage V_{CC} may need to change very frequently (e.g., between each of the OFDM symbols 20(1)-20(N) in Figure 1) and rapidly (e.g., within the CP duration of 0.59 µs). As a result, the rush current I_{RUSH} can have a tremendous impact on battery life. As such, it is desirable to reduce the rush current I_{RUSH} concurrent to supporting fast and frequent switching of the APT voltage V_{CC}.

[0031] In this regard, Figure 3 is a schematic diagram of an exemplary power management circuit 40 configured according to an embodiment of the present disclosure to support fast voltage switching in a power management apparatus 42 with reduced rush current. Herein, voltage switching refers to a voltage change (increase or decrease) from one voltage level to a different voltage level.

[0032] The power management circuit 40 includes a voltage output 44 that outputs an APT voltage V_{CC} to a power amplifier circuit 46 for amplifying an analog signal 48. The power management circuit 40 also includes a voltage amplifier 50 (denoted as "VA"). The voltage amplifier 50 is typically activated to generate an ET voltage V_{AMP} in accordance with an ET target voltage $V_{TGT\text{-}ET}$ and based on a supply voltage V_{SUP}.

[0033] The power management circuit 40 also includes an offset capacitor C_{OFF} that is coupled between an output 52 of the voltage amplifier 50 and the voltage output 44. The power management circuit 40 also includes a switch circuit 54, which includes a bypass switch S_{BYP} coupled between the output 52 of the voltage amplifier 50 and the GND. When the bypass switch S_{BYP} is opened, the offset capacitor C_{OFF} will raise the ET voltage V_{AMP} by an offset voltage V_{OFF} to generate the APT voltage V_{CC} at the voltage output 44 ($V_{CC} = V_{AMP} + V_{OFF}$). In

contrast, when the bypass switch S_{BYP} is closed, the offset capacitor C_{OFF} will be charged by a low-frequency current I_{DC} to thereby maintain the APT voltage V_{CC} at a desired voltage level. Further, when the bypass switch S_{BYP} is closed, the offset capacitor C_{OFF} also helps to reduce the impedance seen by the power amplifier circuit 46. In this regard, when the bypass switch S_{BYP} is closed, the offset capacitor C_{OFF} is functionally equivalent to the offset capacitor C_{OFF} in the conventional power management circuit 26 of Figure 2. Accordingly, the low-frequency current I_{DC} drawn by the offset capacitor C_{OFF} can be equated with the rush current I_{RUSH} in Figure 2.

[0034] As discussed in detail below, the power management circuit 40 can be configured to opportunistically activate and deactivate the voltage amplifier 50 at appropriate times to help enable fast switching of the APT voltage V_{CC} while concurrently reducing the rush current I_{DC} drawn by the offset capacitor C_{OFF}. As a result, the power management circuit 40 is able to adapt the APT voltage V_{CC} frequently and rapidly to support such applications as dynamic power control. Furthermore, by utilizing the voltage amplifier 50 to support fast switching of the APT voltage V_{CC}, it is also possible to reduce the rush current I_{DC} to help prolong battery life.

[0035] In embodiments disclosed herein, the power management circuit 40 is configured to adapt the APT voltage V_{CC} in between a pair of consecutive OFDM symbols S_{N-1} and S_N, which can be any pair of consecutive OFDM symbols among the OFDM symbols 20(1)-20(N) in Figure 1. The OFDM symbol S_{N-1} is referred to as a preceding one of the pair of consecutive OFDM symbols S_{N-1} and S_N, and the OFDM symbol S_N is referred to as a succeeding one of the pair of consecutive OFDM symbols S_{N-1} and S_N. Understandably from Figure 1, each of the OFDM symbols S_{N-1} and S_N includes a CP duration as configured according to Table 1.

[0036] In this regard, the power management circuit 40 is configured according to embodiments of the present disclosure to increase or decrease the APT voltage V_{CC} within the CP duration in each of the OFDM symbols S_{N-1} and S_N. However, it should be appreciated that the power management circuit 40

can also support fast switching of the APT voltage V_{CC} in other usage scenarios, such as adapting the APT voltage V_{CC} within an inter-frame spacing (IFS) in between two consecutive Wi-Fi frames.

[0037] The power management circuit 40 includes a switcher circuit 56. In a non-limiting example, the switcher circuit 56 includes a multi-level charge pump (MCP) 58 and a power inductor 60. The MCP 58 is configured to generate a low-frequency voltage V_{DC} based on a battery voltage V_{BAT} and in accordance with an APT target voltage $V_{TGT-APT}$. Depending on the APT target voltage $V_{TGT-APT}$, the MCP 58 may alternate the low-frequency voltage V_{DC} between different levels (e.g., 0V, V_{BAT}, or $2*V_{BAT}$) based on an appropriate duty cycle. The power inductor 60, which is coupled between the MCP 58 and the voltage output 44, is configured to induce the low-frequency current I_{DC} for charging the offset capacitor C_{OFF}.

[0038] The power management circuit also includes a control circuit 62, which can be a field-programmable gate array (FPGA), as an example. The control circuit 62 is configured to receive a target voltage V_{TGT}, for example from a transceiver circuit (not shown). The target voltage V_{TGT} provides an early indication of the APT voltage V_{CC} in any of the OFDM symbols S_{N-1} and S_N. For example, the target voltage V_{TGT} received during OFDM symbol S_{N-1} may provide an indication of the APT voltage V_{CC} in the OFDM symbol S_N. As such, the control circuit 62 can determine, based on the target voltage V_{TGT}, that the APT voltage V_{CC} will change from one voltage level to another in the OFDM symbol S_N prior to a start of the OFDM symbol S_N. Accordingly, the control circuit 62 can generate the ET target voltage V_{TGT-ET} and the APT target voltage $V_{TGT-APT}$ based on the target voltage V_{TGT} prior to the start of the OFDM symbol S_N to cause the power management circuit 40 to adapt the APT voltage V_{CC} within a defined temporal limit (e.g., the CP duration) from the start of the OFDM symbol S_N.

[0039] In one embodiment, the control circuit 62 determines (e.g., during OFDM symbol S_{N-1}) that the APT voltage V_{CC} is set to increase in the OFDM symbol S_N. In this regard, Figure 4 is a timing diagram providing an exemplary illustration of the power management circuit 40 of Figure 3 configured to increase

the APT voltage V_{CC} from a present voltage level VL_P in OFDM symbol S_{N-1} (also referred to as "a present OFDM symbol" or "present time interval") to a future voltage level VL_F in OFDM symbol S_N (also referred to as "an upcoming OFDM symbol" or "upcoming time interval"). Common elements between Figures 3 and 4 are shown therein with common element numbers and will not be re-described herein.

[0040] With reference to Figure 4, the control circuit 62 receives the target voltage V_{TGT} during the OFDM symbol S_{N-1} and prior to a start time T_1 of the OFDM symbol S_N. The target voltage V_{TGT} indicates that the APT voltage V_{CC} is set to increase from the present voltage level VL_P (e.g., 1 V) in the OFDM symbol S_{N-1} to the future voltage level VL_F (e.g., 5.5 V) in the OFDM symbol S_N. Accordingly, the control circuit 62 generates the ET target voltage V_{TGT-ET} and the APT target voltage $V_{TGT-APT}$ that are similar or identical to the target voltage V_{TGT}. Notably, during the OFDM symbol S_{N-1}, the bypass switch S_{BYP} is closed and the offset capacitor C_{OFF} is charged to maintain the APT voltage V_{CC} at the present voltage level VL_P.

[0041] Prior to the start time T_1 of the OFDM symbol S_N (e.g., at time T_2), the control circuit 62 activates the voltage amplifier 50 to generate the ET voltage V_{AMT} and source the high-frequency current I_{AMP} based on the ET target voltage V_{TGT-ET}. In a non-limiting example, the time T_2 can be so determined to account for ramping up and settling time of the voltage amplifier 50. In addition, the time T_2 can be further determined to ensure that the voltage amplifier 50 can ramp up the ET voltage V_{AMP} to a level substantially equal (VL_F - V_{OFF}) within the CP duration of the OFDM symbol S_N.

[0042] Concurrent to generating the ET voltage V_{AMP} to quickly raise the APT voltage V_{CC} to the level of (VL_F - V_{OFF}), the high-frequency current I_{AMP} will charge up a load capacitor C_L to help maintain the APT voltage V_{CC} at the level of (VL_F - V_{OFF}). The load capacitor C_L, which may be provided inside or outside the power amplifier circuit 46, has a smaller capacitance (e.g., 500 pF) compared to the offset capacitor C_{OFF}. As a result, according to equation (Eq. 1), it is

possible to charge up the load capacitor C_L quickly with a reduced amount of rush current.

[0043] At the start time T_1 of the OFDM symbol S_N, the control circuit 62 opens the bypass switch S_{BYP} such that the offset capacitor C_{OFF} can be charged by the low-frequency current I_{DC} to raise the offset voltage V_{OFF} from the present voltage level VL_P to the future voltage level VL_F. Given that the APT voltage V_{CC} has already been raised by the voltage amplifier 50 and maintained by the load capacitor C_L, it is thus possible to charge the offset capacitor C_{OFF} at a slower rate to help further reduce demand for the low-frequency current I_{DC} (a.k.a., rush current). As the offset voltage V_{OFF} gradually increases, the voltage amplifier 50 can gradually reduce the ET voltage V_{AMP} such that a sum of the ET voltage V_{AMP} and the offset voltage V_{OFF} would equal the future voltage level VL_F.

[0044] At time T_3, the offset voltage V_{OFF} is raised to the future voltage value VL_F. In this regard, the ET voltage V_{AMP} is no longer needed. Accordingly, the control circuit 62 can close the bypass switch S_{BYP} and deactivate the voltage amplifier 50. In one embodiment, the control circuit 62 may close the bypass switch S_{BYP} and deactivate the voltage amplifier 50 concurrently at time T_3. Alternatively, the control circuit 62 may deactivate the voltage amplifier 50 with a timing delay T_{DLY} from closing the bypass switch S_{BYP}.

[0045] Figure 5 is a timing diagram providing an exemplary illustration of the power management circuit 40 of Figure 3 configured to decrease the APT voltage V_{CC} from a present voltage level VL_P in OFDM symbol S_{N-1} (also referred to as "a present OFDM symbol") to a future voltage level VL_F in OFDM symbol S_N (also referred to as "an upcoming OFDM symbol"). Common elements between Figures 3 and 5 are shown therein with common element numbers and will not be re-described herein.

[0046] With reference to Figure 5, the control circuit 62 receives the target voltage V_{TGT} during the OFDM symbol S_{N-1} and prior to a start time T_1 of the OFDM symbol S_N. The target voltage V_{TGT} indicates that the APT voltage V_{CC} is set to decrease from the present voltage level VL_P (e.g., 5.5 V) in the OFDM symbol S_{N-1} to the future voltage level VL_F (e.g., 1 V) in the OFDM symbol S_N.

Accordingly, the control circuit 62 generates the ET target voltage $V_{TGT\text{-}ET}$ and the APT target voltage $V_{TGT\text{-}APT}$ that are similar or identical to the target voltage V_{TGT}. Notably, during the OFDM symbol S_{N-1}, the bypass switch S_{BYP} is closed and the offset capacitor C_{OFF} is charged to maintain the APT voltage V_{CC} at the present voltage level VL_P.

[0047] Prior to the start time T_1 of the OFDM symbol S_N (e.g., at time T_2), the control circuit 62 opens the bypass switch S_{BYP} to discharge the offset capacitor C_{OFF} to reduce the offset voltage V_{OFF} from the present voltage level VL_P to the future voltage level VL_F. The time T_2 may be so determined to ensure that the offset voltage V_{OFF} can be reduced to the future voltage level VL_F within the CP duration of the OFDM symbol S_N.

[0048] Notably, the power management circuit 40 still needs to maintain the APT voltage V_{CC} at the present voltage level VL_P during the OFDM symbol S_{N-1} while the offset capacitor C_{OFF} is discharged to reduce the offset voltage V_{OFF}. In this regard, the control circuit 62 is further configured to activate the voltage amplifier 50 to help maintain the APT voltage V_{CC} at the present voltage level VL_P before discharging the offset capacitor C_{OFF}. In addition, the voltage amplifier 50 also serves as a current sink to absorb discharge current associated with discharging the offset capacitor C_{OFF}. The control circuit 62 may activate the voltage amplifier 50 with a timing advance T_{ADV} before opening the bypass switch S_{BYP} to start discharging the offset capacitor C_{OFF}. The timing advance T_{ADV} may be so determined to ensure that the voltage amplifier 50 can be ramped up and settled to maintain the APT voltage V_{CC} at the present voltage level VL_P by the time T_2.

[0049] At time T_3, the offset voltage V_{OFF} is reduced to the future voltage value VL_F. In this regard, the ET voltage V_{AMP} is no longer needed. Accordingly, the control circuit 62 can close the bypass switch S_{BYP} and deactivate the voltage amplifier 50. In one embodiment, the control circuit 62 may close the bypass switch S_{BYP} and deactivate the voltage amplifier 50 concurrently at time T_3. Alternatively, the control circuit 62 may deactivate the voltage amplifier 50 with a timing delay T_{DLY} from closing the bypass switch S_{BYP}.

[0050] With reference back to Figure 3, the control circuit 62 may activate/deactivate the voltage amplifier 50 and open/close the bypass switch S_{BYP} based on a control signal 64. The power management circuit 40 also includes a supply voltage circuit 66 configured to generate the supply voltage V_{SUP} for the voltage amplifier 50 based on a supply target voltage $V_{TGT\text{-}SUP}$. The control circuit 62 may further generate the supply target voltage $V_{TGT\text{-}SUP}$ based on the target voltage V_{TGT}.

[0051] Those skilled in the art will recognize improvements and modifications to the preferred embodiments of the present disclosure. All such improvements and modifications are considered within the scope of the concepts disclosed herein and the claims that follow.

Claims

What is claimed is:

1. A power management circuit comprising:

a voltage output that outputs an average power tracking (APT) voltage to a power amplifier circuit for amplifying an analog signal;

a voltage amplifier coupled to the voltage output and configured to generate an envelope tracking (ET) voltage based on an ET target voltage and a supply voltage; and

a control circuit configured to:

receive a target voltage indicating that the APT voltage with change from a present voltage level in a present time interval to a future voltage level in an upcoming time interval; and

activate the voltage amplifier prior to a start of the upcoming time interval to thereby cause the APT voltage to change to the target voltage within a defined temporal limit from the start of the upcoming time interval.

2. The power management circuit of claim 1, wherein:

the present time interval corresponds to a preceding one of a pair of consecutive orthogonal frequency division multiplexing (OFDM) symbols;

the upcoming time interval corresponds to a succeeding one of the pair of consecutive OFDM symbols; and

the defined temporal limit corresponds to a cyclic prefix (CP) in each of the pair of consecutive OFDM symbols.

3. The power management circuit of claim 1, wherein the control circuit is further configured to generate the ET target voltage based on the target voltage.

4. The power management circuit of claim 1, further comprising:

a switcher circuit coupled to the voltage output and configured to generate a low-frequency current based on an APT target voltage;

an offset capacitor coupled between an output of the voltage amplifier and the voltage output and configured to raise the ET voltage by an offset voltage to generate the APT voltage at the voltage output; and

a bypass switch coupled between the output of the voltage amplifier and a ground.

5. The power management circuit of claim 4, wherein the control circuit is further configured to:

receive the target voltage indicating that the APT voltage will increase from the present voltage level to the future voltage level; and

activate the voltage amplifier prior to the start of the upcoming time interval to thereby raise the APT voltage from the present voltage level to the future voltage level within the defined temporal limit.

6. The power management circuit of claim 5, wherein the control circuit is further configured to:

generate the APT target voltage based on the target voltage; and

control the switcher circuit to generate the low-frequency current based on the APT target voltage.

7. The power management circuit of claim 6, wherein the control circuit is further configured to open the bypass switch after activating the voltage amplifier to thereby charge the offset capacitor from the present voltage level to the future voltage level based on the low-frequency current.

8. The power management circuit of claim 7, wherein the control circuit is further configured to close the bypass switch in response to the offset voltage being charged up to the future voltage level.

9. The power management circuit of claim 8, wherein the control circuit is further configured to deactivate the voltage amplifier after closing the bypass switch.

10. The power management circuit of claim 8, wherein the control circuit is further configured to deactivate the voltage amplifier and close the bypass switch concurrently.

11. The power management circuit of claim 4, wherein the control circuit is further configured to:

receive the target voltage indicating that the APT voltage will decrease from the present voltage level to the future voltage level; and

activate the voltage amplifier prior to the start of the upcoming time interval to thereby maintain the APT voltage at the present voltage level.

12. The power management circuit of claim 11, wherein the control is further configured to open the bypass switch after activating the voltage amplifier and prior to the start of the upcoming time interval to thereby discharge the offset capacitor from the present voltage level to the future voltage level within the defined temporal limit.

13. The power management circuit of claim 12, wherein the control circuit is further configured to close the bypass switch in response to the offset capacitor being discharged to the future voltage level.

14. The power management circuit of claim 13, wherein the control circuit is further configured to deactivate the voltage amplifier after closing the bypass switch.

15. The power management circuit of claim 13, wherein the control circuit is further configured to deactivate the voltage amplifier and close the bypass switch concurrently.

16. The power management circuit of claim 1, further comprising a supply voltage circuit configured to generate the supply voltage based on a supply target voltage.

17. The power management circuit of claim 16, wherein the control circuit is further configured to generate the supply target voltage based on the target voltage.

18. A power management apparatus comprising:

a power amplifier circuit configured to amplify an analog signal based on an average power tracking (APT) voltage; and

a power management circuit comprising:

a voltage output that outputs the APT voltage to the power amplifier circuit;

a voltage amplifier coupled to the voltage output and configured to generate an envelope tracking (ET) voltage based on an ET target voltage and a supply voltage; and

a control circuit configured to:

receive a target voltage indicating that the APT voltage will change from a present voltage level in a present time interval to a future voltage level in an upcoming time interval; and

activate the voltage amplifier prior to a start of the upcoming time interval to thereby cause the APT voltage to change to the target voltage within a defined temporal limit from the start of the upcoming time interval.

19. The power management apparatus of claim 18, wherein the power management circuit further comprises:

a switcher circuit coupled to the voltage output and configured to generate a low-frequency current based on an APT target voltage;

an offset capacitor coupled between an output of the voltage amplifier and the voltage output and configured to raise the ET voltage by an offset voltage to generate the APT voltage at the voltage output; and

a bypass switch coupled between the output of the voltage amplifier and a ground.

20. The power management apparatus of claim 19, wherein the power amplifier circuit comprises a load capacitor having a smaller capacitance than the offset capacitor.

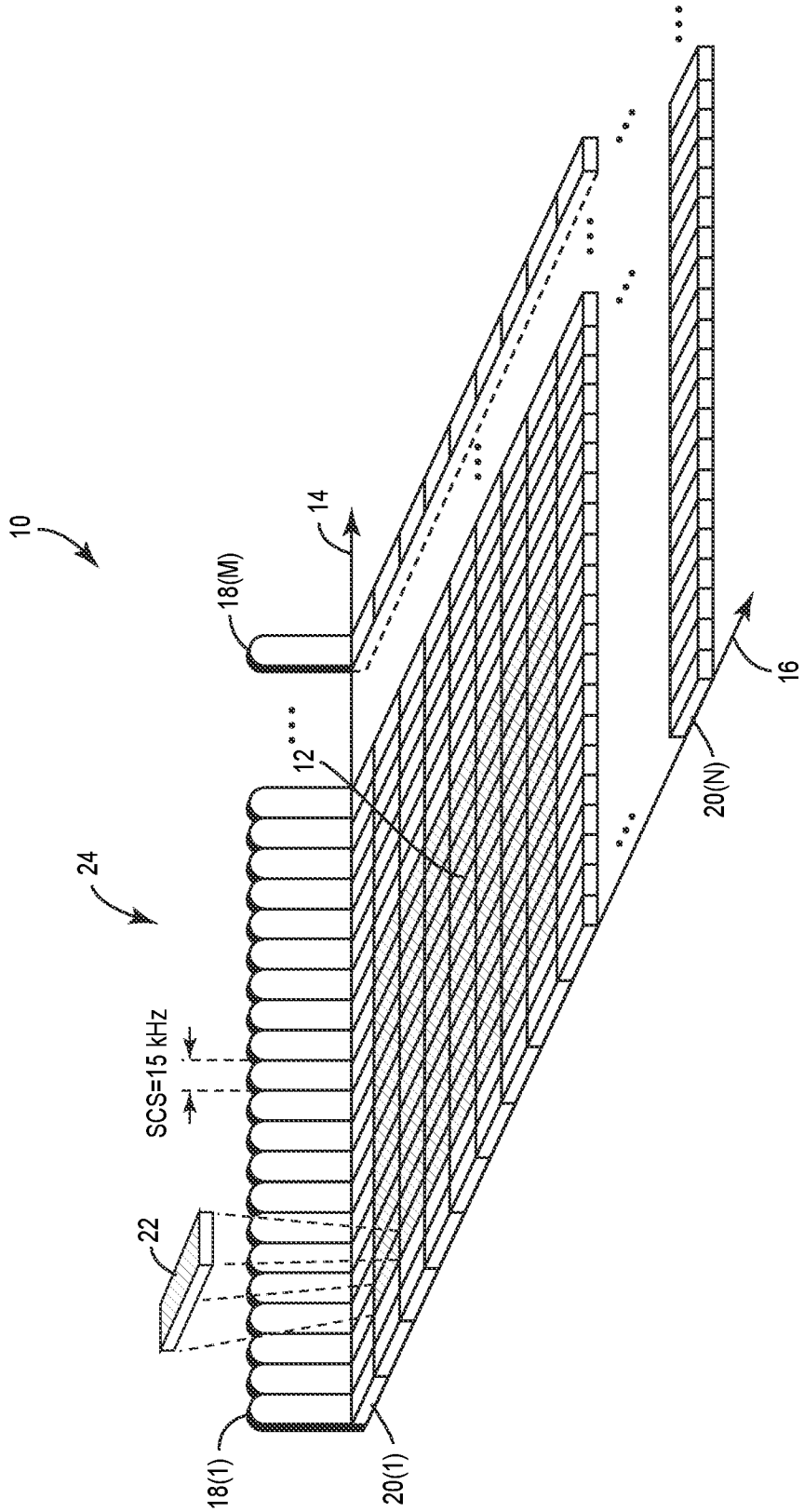

FIG. 1
(PRIOR ART)

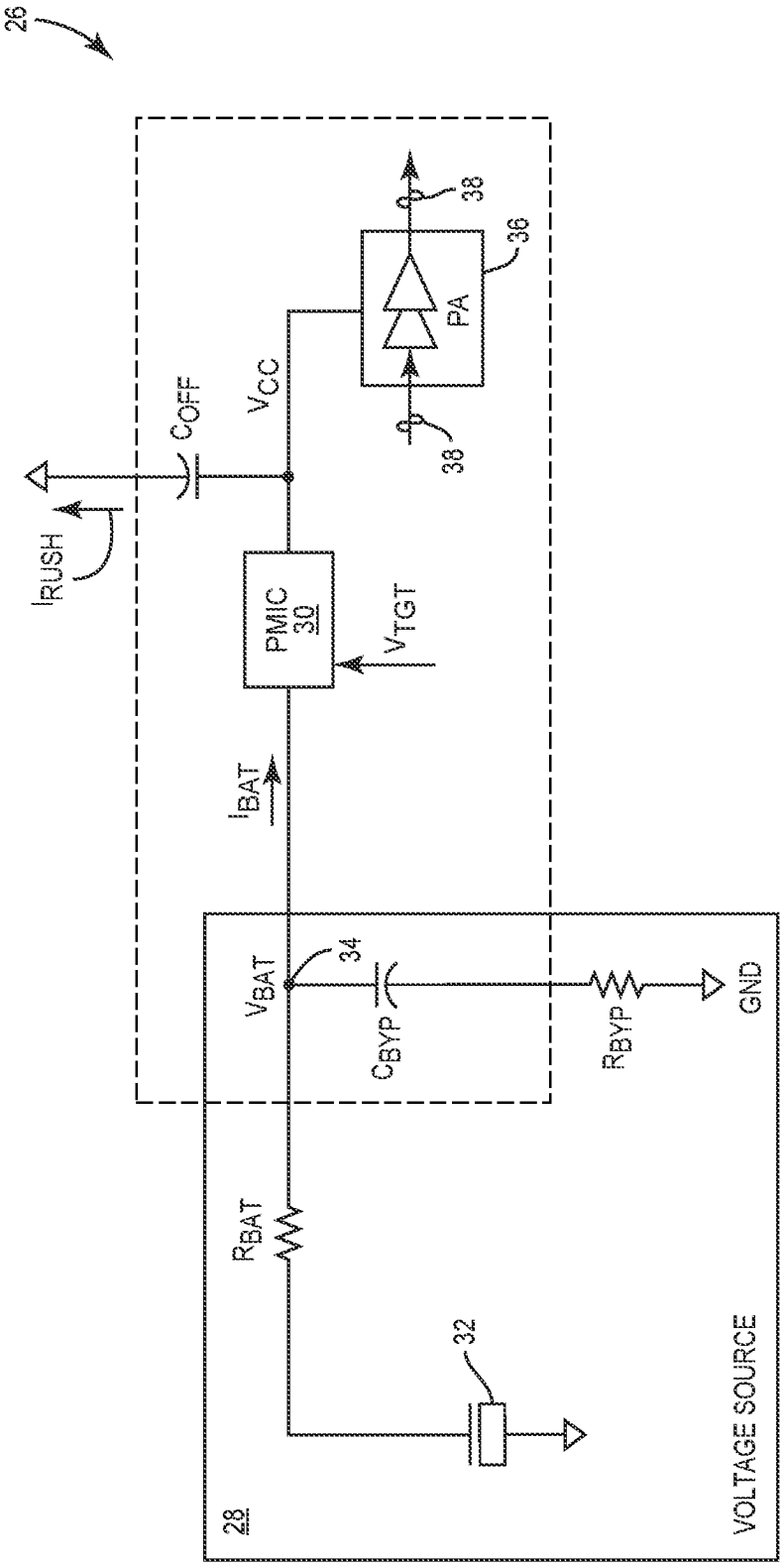
26
28
VOLTAGE SOURCE
32
RBAT
34
VBAT
CBYP
RBYP
GND
IBAT
PMIC
30
VTGT
IRUSH
COFF
VCC
PA
36
38
38

FIG. 2

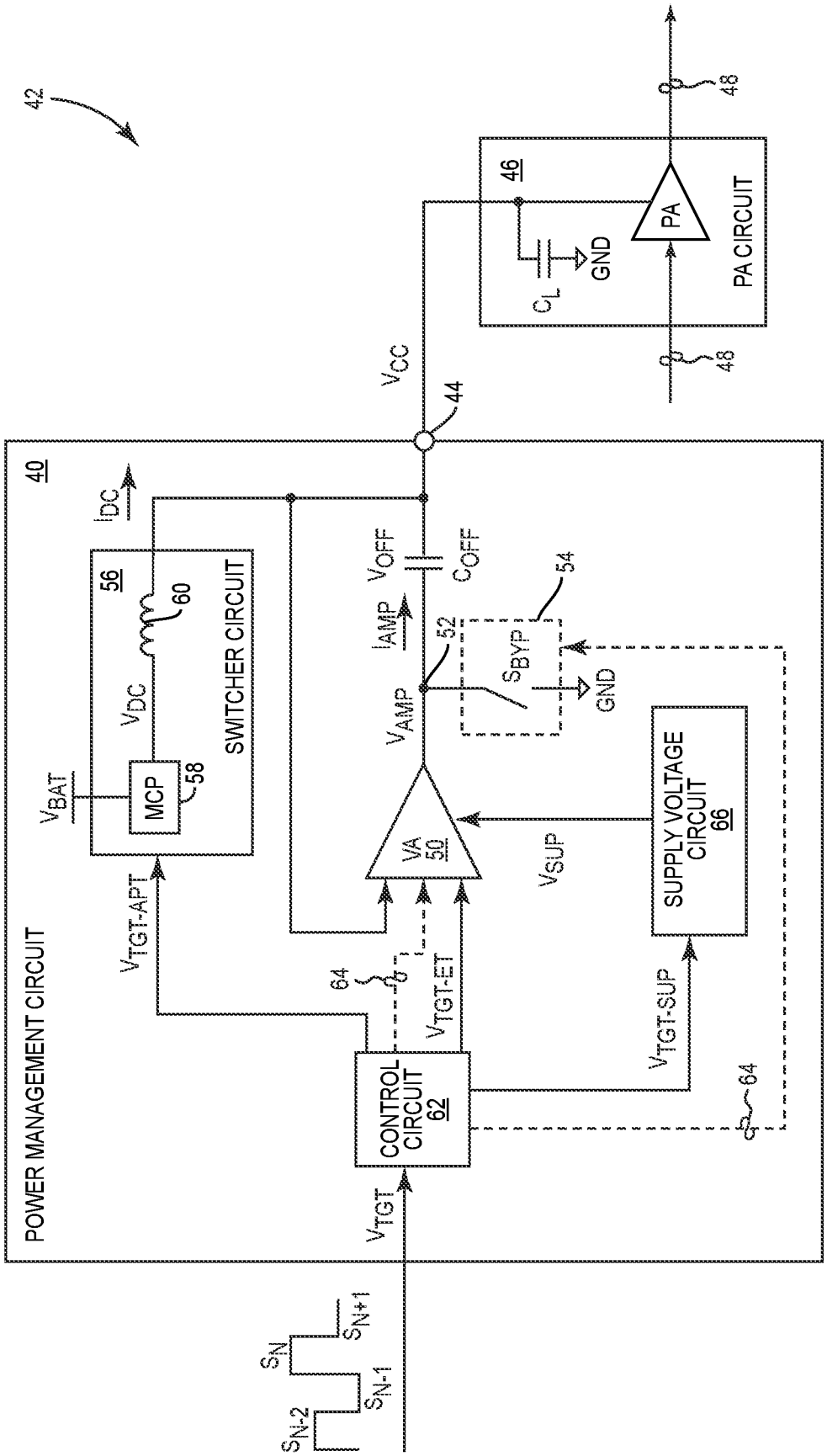
42
40
POWER MANAGEMENT CIRCUIT
V_{BAT}
I_{DC}
56
60
V_{DC}
MCP
58
SWITCHER CIRCUIT
$V_{TGT-APT}$
64
V_{TGT-ET}
V_{TGT}
CONTROL CIRCUIT 62
S_N
S_{N+1}
S_{N-1}
S_{N-2}
V_{CC}
44
V_{OFF}
C_{OFF}
I_{AMP}
52
V_{AMP}
S_{BYP}
54
GND
VA 50
V_{SUP}
SUPPLY VOLTAGE CIRCUIT 66
$V_{TGT-SUP}$
64
46
C_L
GND
PA
PA CIRCUIT
48
48

FIG. 3

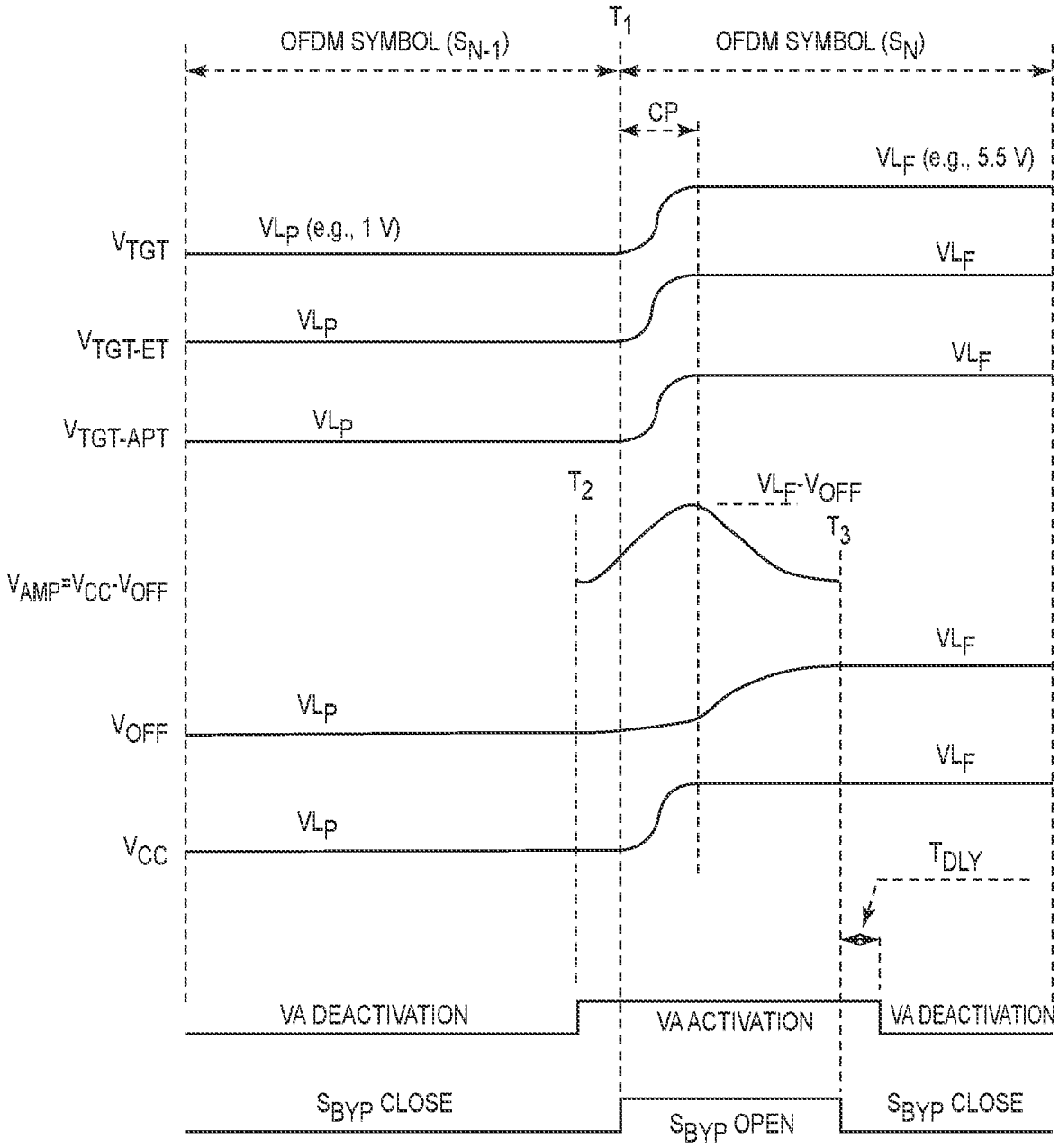
T1
OFDM SYMBOL (SN-1)
OFDM SYMBOL (SN)
CP
VLF (e.g., 5.5 V)
VTGT
VLP (e.g., 1 V)
VLF
VTGT-ET
VLP
VLF
VTGT-APT
VLP
T2
VLF-VOFF
T3
VAMP=VCC-VOFF
VLF
VOFF
VLP
VLF
VCC
VLP
TDLY
VA DEACTIVATION
VA ACTIVATION
VA DEACTIVATION
SBYP CLOSE
SBYP OPEN
SBYP CLOSE

FIG. 4

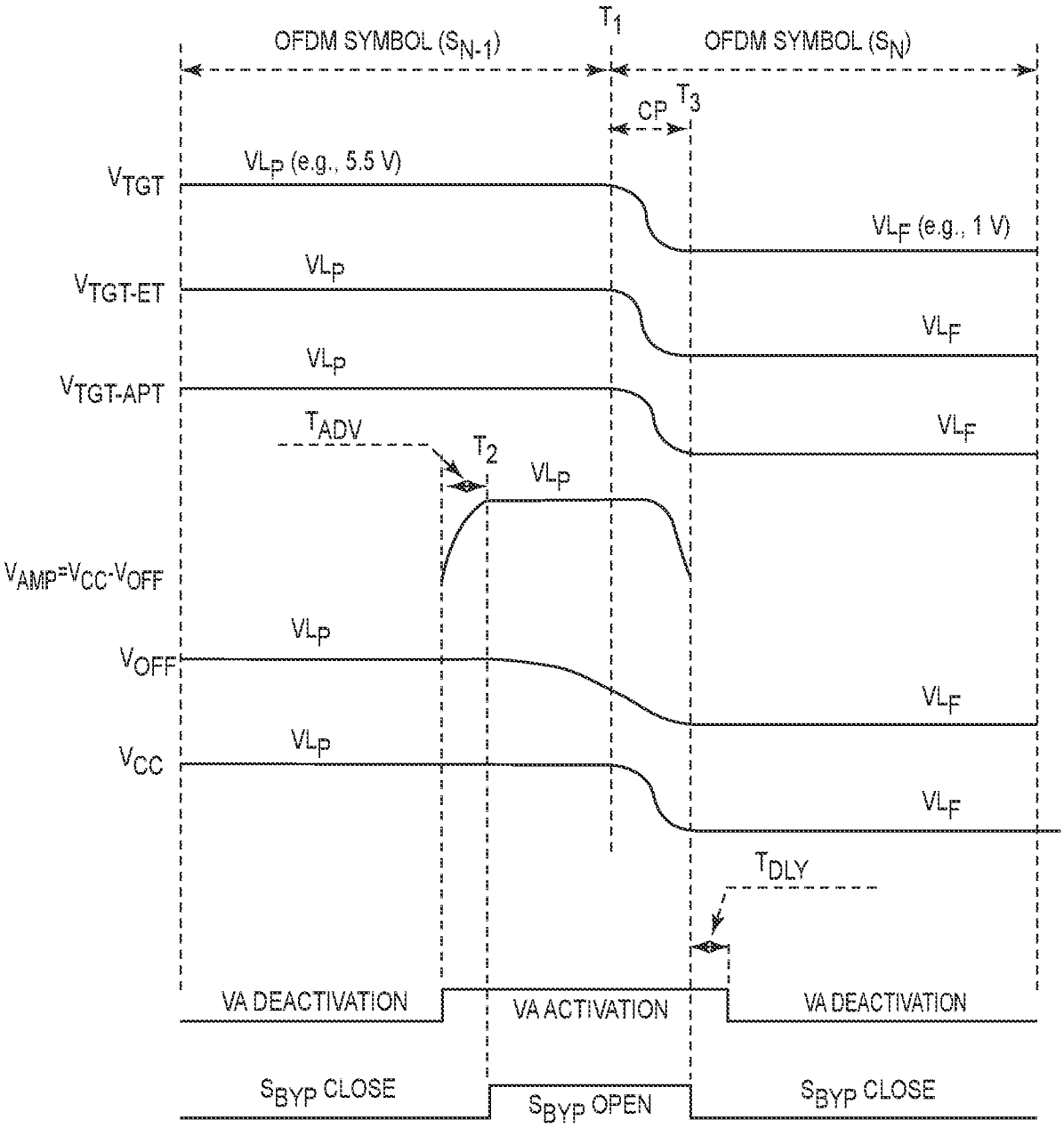
T1
OFDM SYMBOL (SN-1)
OFDM SYMBOL (SN)
CP
T3
VTGT
VLP (e.g., 5.5 V)
VLF (e.g., 1 V)
VTGT-ET
VLP
VLF
VTGT-APT
VLP
VLF
TADV
T2
VLP
VAMP=VCC-VOFF
VOFF
VLP
VLF
VCC
VLP
VLF
TDLY
VA DEACTIVATION
VA ACTIVATION
VA DEACTIVATION
SBYP CLOSE
SBYP OPEN
SBYP CLOSE

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2021/044596

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F1/02 H03F3/189 H03F3/24
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2016/094192 A1 (KHESBAK SABAH [US] ET AL) 31 March 2016 (2016-03-31) abstract; figure 2	1-20
A	US 2020/336111 A1 (KHLAT NADIM [FR]) 22 October 2020 (2020-10-22) paragraph [0054]; figure 2	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 April 2022	21/04/2022

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Zakharian, Andre

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2021/044596

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		US 2020127619 A1	23-04-2020
US 2020336111 A1	22-10-2020	NONE	