(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
30 March 2017 (30.03.2017)

WIPO | PCT

(10) International Publication Number
WO 2017/052530 Al

(51) International Patent Classification:
H01F 17/00 (2006.01) *H01F 27/29* (2006.01)

(21) International Application Number:
PCT/US2015/051658

(22) International Filing Date:
23 September 2015 (23.09.2015)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Blvd., Santa Clara, California 95054 (US).

(72) Inventors: **O'BRIEN, Kevin P.;** 1846 SE 36th Avenue, Portland, Oregon 97214 (US). **SCHROM, Gerhard;** 12010 NW Gales Creek Rd., Gales Creek, Oregon 97117 (US). **STAINES, David W.;** 640 Calvin Street, Columbia City, Oregon 97018 (US). **FISCHER, Paul B.;** 1558 NW 129th Place, Portland, Oregon 97229 (US).

(74) Agent: **GREEN, Blayne D.;** Green, Howard & Mughal, LLP, c/o CPA Global, P.O. Box 52050, Minneapolis, Minnesota 55402 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available):* AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available):* ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17 :

— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

WO 2017/052530 A1

(54) Title: HIGH CURRENT MAGNETIC THIN FILM INDUCTORS

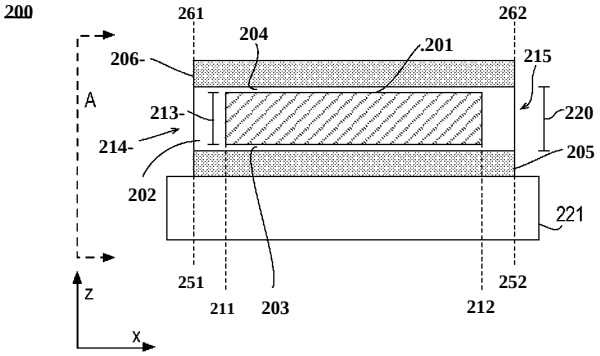

FIG. 2A

(57) Abstract: Embodiments related to high current magnetic thin film inductors having a metal trace between magnetic layers such that the magnetic layers are separated to provide edge gaps along lateral edges of the metal trace, integrated circuits having such high current magnetic thin film inductors, systems incorporating such high current magnetic thin film inductors, and methods for forming them are discussed.

HIGH CURRENT MAGNETIC THIN FILM INDUCTORS

TECHNICAL FIELD

Embodiments of the invention generally relate to inductors that may exhibit high performance when scaled to small sizes, and more particularly relate to high current magnetic thin film inductors having a metal trace between magnetic layers such that the magnetic layers are separated to provide edge gaps along lateral edges of the metal trace and related devices and manufacturing techniques.

BACKGROUND

Miniaturization of voltage regulation circuits requires scaling of inductors to very small sizes. Current solutions do not offer scaling to small sizes, simple integration, and high performance. For example, fully integrated voltage regulator (FIVR) solutions such as air core inductors provide local inductance but suffer from a loss of inductance and Q factor when scaled below a certain volume. Thin film closed magnetic inductors may scale to smaller form factors but they require complicated manufacturing and integration processes and additional circuitry to deal with nonlinear effects at high current. Strip-line inductors having closed magnetic vias at the edges of the inductor may have high coupling (e.g., 0.8 and higher), require complicated manufacturing and integration process, and exhibit highly non-linear behavior.

For example, FIG. 1A illustrates a cross-sectional view of an idealized inductor 100 having a circular conductor 101 such as copper, surrounded by a concentric circular dielectric 102 such as silicon dioxide, which is surrounded by a concentric circular magnetic material 103. FIG. IB illustrates a cross-sectional view of a prior art inductor 110 that may attempt to provide an approximation of idealized inductor 100. As shown, inductor 110 includes a conductor 111 such as copper, surrounded by a dielectric 112 such as silicon dioxide, which is surrounded by magnetic material 113 and magnetic material 114. However, inductor 110 may suffer from drawbacks as discussed above such as requiring complicated manufacturing and integration processes and additional circuitry to deal with nonlinear effects at high current. Furthermore, such inductors may exhibit inductance that decreases rapidly with increasing current.

As such, existing techniques do not provide for scalable inductor structures with a relatively simple integration process that exhibit high performance with respect to inductance, Q

factor, and coupling, particularly at increasing currents. Such problems may become critical as the miniaturization of inductors becomes desirable in various applications.

BRIEF DESCRIPTION OF THE DRAWINGS

The material described herein is illustrated by way of example and not by way of limitation in the accompanying figures. For simplicity and clarity of illustration, elements illustrated in the figures are not necessarily drawn to scale. For example, the dimensions of some elements may be exaggerated relative to other elements for clarity. Further, where considered appropriate, reference labels have been repeated among the figures to indicate corresponding or analogous elements. In the figures:

FIG. 1A illustrates a cross-sectional view of an idealized inductor;

FIG. 1B illustrates a cross-sectional view of a prior art inductor;

FIG. 2A is a cross-sectional view of an example structure of a magnetic thin film inductor;

FIG. 2B is a plan view of the example structure of FIG. 2A;

FIG. 3 is a cross-sectional view of another example structure of the magnetic thin film inductor;

FIG. 4 is a cross-sectional view of another example structure of the magnetic thin film inductor;

FIG. 5 is a cross-sectional view of another example structure of the magnetic thin film inductor and a second magnetic thin film inductor inductively coupled to the magnetic thin film inductor;

FIG. 6 is a flow diagram illustrating an example process for fabricating magnetic thin film inductors;

FIGS. 7A, 7B, 7C, 7D, 7E, and 7F are cross-sectional views of example inductor structures as particular fabrication operations are performed and FIG. 7F is another example structure of the magnetic thin film inductor;

FIG. 8 illustrates a system in which a mobile computing platform and/or a data server machine employs a magnetic thin film inductor; and

FIG. 9 is a functional block diagram of a computing device, all arranged in accordance with at least some implementations of the present disclosure.

DETAILED DESCRIPTION

One or more embodiments or implementations are now described with reference to the enclosed figures. While specific configurations and arrangements are discussed, it should be understood that this is done for illustrative purposes only. Persons skilled in the relevant art will recognize that other configurations and arrangements may be employed without departing from the spirit and scope of the description. It will be apparent to those skilled in the relevant art that techniques and/or arrangements described herein may also be employed in a variety of other systems and applications other than what is described herein.

Reference is made in the following detailed description to the accompanying drawings, which form a part hereof, wherein like numerals may designate like parts throughout to indicate corresponding or analogous elements. It will be appreciated that for simplicity and/or clarity of illustration, elements illustrated in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements for clarity. Further, it is to be understood that other embodiments may be utilized and structural and/or logical changes may be made without departing from the scope of claimed subject matter. It should also be noted that directions and references, for example, up, down, top, bottom, over, under, and so on, may be used to facilitate the discussion of the drawings and embodiments and are not intended to restrict the application of claimed subject matter. Therefore, the following detailed description is not to be taken in a limiting sense and the scope of claimed subject matter defined by the appended claims and their equivalents.

In the following description, numerous details are set forth, however, it will be apparent to one skilled in the art, that the present invention may be practiced without these specific details. In some instances, well-known methods and devices are shown in block diagram form, rather than in detail, to avoid obscuring the present invention. Reference throughout this specification to "an embodiment" or "in one embodiment" means that a particular feature, structure, function, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. Thus, the appearances of the phrase "in an embodiment" in various places throughout this specification are not necessarily referring to the same embodiment of the invention. Furthermore, the particular features, structures, functions, or characteristics may be combined in any suitable manner in one or more embodiments. For example, a first embodiment

may be combined with a second embodiment anywhere the two embodiments are not specified to be mutually exclusive.

The terms "coupled" and "connected," along with their derivatives, may be used herein to describe structural relationships between components. It should be understood that these terms are not intended as synonyms for each other. Rather, in particular embodiments, "connected" may be used to indicate that two or more elements are in direct physical or electrical contact with each other. "Coupled" my be used to indicated that two or more elements are in either direct or indirect (with other intervening elements between them) physical or electrical contact with each other, and/or that the two or more elements co-operate or interact with each other (e.g., as in a cause an effect relationship).

The terms "over," "under," "between," "on", and/or the like, as used herein refer to a relative position of one material layer or component with respect to other layers or components. For example, one layer disposed over or under another layer may be directly in contact with the other layer or may have one or more intervening layers. Moreover, one layer disposed between two layers may be directly in contact with the two layers or may have one or more intervening layers. In contrast, a first layer "on" a second layer is in direct contact with that second layer. Similarly, unless explicitly stated otherwise, one feature disposed between two features may be in direct contact with the adjacent features or may have one or more intervening features.

Inductors, integrated circuits, devices, apparatuses, computing platforms, and methods are described below related to high current thin film magnetic inductors.

As described above, it may be advantageous to miniaturize inductors such that the miniaturized inductors may be manufactured and integrated into products relatively simply and such that they exhibit high performance with respect to inductance, Q factor, and coupling, particularly at increasing currents. Such inductors may be used for various applications such as power management integrated circuits, radio frequency integrated circuits, and so on. In some embodiments discussed herein, a high current thin film magnetic inductor may include a metal trace disposed within one or more dielectric materials and first and second magnetic layers adjacent to the dielectric material(s) such that the metal trace is between at least portions of the first and second magnetic layers and such that the first and second magnetic layers are separated to provide edge gaps along lateral edges of the metal trace having a gap size not less than one-fourth of a thickness of the metal trace. In some embodiments the first magnetic layer, second

magnetic layer or both may be slotted or segmented to increase the operating frequency of the inductor.

In some embodiments discussed herein, a magnetic thin film inductor may include a first magnetic layer over a substrate, a first dielectric layer over the first magnetic layer, a metal trace over the first dielectric layer, a second dielectric layer over the metal trace, and a second magnetic layer over the second dielectric layer such that the first magnetic layer and the second magnetic layer are separated to provide edge gaps along lateral edges of the metal trace having a gap size not less than one-fourth of a thickness of the metal trace. In some embodiments, the edge gaps extend along the entire lateral edges of the metal trace. In other embodiments, the edge gaps extend along a portion or portions of the lateral edges of the metal trace.

In some embodiments, the first and second magnetic layers may extend laterally beyond the lateral edges of the metal trace. In an embodiment, the bottom surface of the first magnetic layer may be above the top layer of the metal trace and the top surface of the second magnetic layer may be below the bottom layer of the metal trace. In such an embodiment, the first and second magnetic layers may be separated by a gap size not less than the thickness of the metal trace. In another embodiment, the bottom surface of the first magnetic layer may be below the top layer of the metal trace and the top surface of the second magnetic layer may be below the bottom layer of the metal trace such that a portion of the first magnetic layer is laterally aligned with a portion of the metal trace. In such an embodiment, the first and second magnetic layers may be separated by a gap size less than the thickness of the metal trace but not less than one-fourth of the thickness of the metal trace.

In an embodiment, the first magnetic layer may extend laterally beyond the metal trace and the second layer may be laterally within the metal trace. In another embodiment, the edges of the first and second magnetics layer may aligned with the edges of the metal trace and the second layer may be laterally within the metal trace. In such embodiments, the first and second magnetic layers may be separated by a gap size not less than the thickness of the metal trace. In some embodiments, two or more inductors may be provided adjacent to one another such that inductors are inductively coupled. The two or more inductors may have the same topology or structure or they may be different.

In another embodiment, a system may include a processor, a memory coupled to the processor and a power management integrated circuit and/or a radio frequency integrated circuit

including a magnetic thin film inductor. The inductor structures discussed herein may be scalable to small sizes and may provide high performance with respect to inductance, Q factor, and coupling, particularly at increasing currents as is discussed further herein. This and additional embodiments are discussed further herein with respect to the figures.

FIG. 2A is a cross-sectional view of an example structure of a magnetic thin film inductor 200 and FIG. 2B is a plan view of the example structure of FIG. 2A, arranged in accordance with at least some implementations of the present disclosure. FIG. 2A provides a cross-sectional view taken along plane A as shown in the plan view of FIG. 2B. As shown, inductor 200 may include a metal trace 201 between magnetic layers 205, 206. In FIG. 2B, obscured metal trace 201 is illustrated via hatched lines. As shown in FIG. 2B, in an embodiment, inductor 200 may be a linear inductor. However, inductor 200 may have any suitable shape. In an embodiment, inductor 200 may be a curved inductor (e.g., inductor 200 may have a curved shape in the plan view of FIG. 2B). Also as shown, inductor 200 may include a portion of and/or be provided on a substrate 221. In some embodiments, inductor 200 may be provided adjacent to one or more additional inductors having the same or different topologies as discussed further herein with respect to FIG. 5. Inductor 200 may be characterized as a magnetic thin film inductor, a high current magnetic thin film inductor, a sandwich inductor, a low coupling inductor, or the like.

As shown, inductor 200 may include metal trace 201 disposed within at least one dielectric material 202 such that a dielectric layer 203 of dielectric material 202 separates metal trace 201 from magnetic layer 205 adjacent to dielectric material 202 and another dielectric layer 204 of dielectric material 202 separates metal trace 201 from magnetic layer 206 adjacent to dielectric material 202. For example, dielectric material 202 may include a single material or layer or multiple materials or layers to electrical separation of metal trace 201 from magnetic layers 205, 206. Furthermore, as shown, at least a portion of metal trace 201 is between at least portions of magnetic layers 205, 206 and magnetic layers 205, 206 may be separated by a gap size 220 that is not less than a thickness 213 of metal trace 201. In the embodiment of FIGS. 2A and 2B, the entirety of metal trace 201 is between at least portions of magnetic layers 205, 206.

As shown, inductor 200 may include metal trace 201 with magnetic layers 205, 206 below and above metal trace 201 and arranged such that a magnetic flux at the edges of inductor 200 (e.g., as associated with lateral edges, 211, 212, 251, 252, 261, 262 and edge gaps 214, 215) is not completely closed. Such a topology may be provided via inductor 200 for enhanced performance with respect to inductance, Q factor, and coupling as is discussed further herein and,

in particular such characteristics are discussed further after the discussion of FIG. 5. For example, the inventors have found that such a topology may provide for scalable inductors that maintain high performance as they are miniaturized.

As discussed, inductor 200 may include magnetic layer 205 over substrate 221. Substrate 221 may include any suitable material, materials, and/or integrated devices. For example, substrate 221 may include a semiconductor material such as monocrystalline silicon (Si), germanium (Ge), silicon germanium (SiGe), a III-V materials based material (e.g., gallium arsenide (GaAs)), a silicon carbide (SiC), a sapphire (AI_2O_3), a printed circuit board, or any combination thereof or the like. In some embodiments, substrate 221 may include an insulator material on a semiconductor material such as monocrystalline silicon. In some embodiments, substrate 221 may include metallization interconnect layers and/or electronic devices for integrated circuits such as transistors, memories, capacitors, resistors, optoelectronic devices, switches, or any other active or passive electronic devices separated by an electrically insulating layer, for example, an interlayer dielectric, a trench insulation layer, or the like. In some embodiments, inductor 200 and substrate 221 may form a system on a chip device.

Magnetic layer 205 may have any suitable size and shape and may include any suitable magnetic material or materials. For example, magnetic layer 205 and other magnetic layers discussed herein may include any suitable magnetic material or lamination of materials to provide a composite magnetic material with a reasonably high permeability and high resistivity. In some embodiments, magnetic layer 205 may have a width (e.g., along the x-axis) in the range of 80 to 350 microns, a thickness (e.g., along the z-axis) in the range of 0.5 to 6 microns, and a length (e.g., along the y-axis) in the range of 200 microns to 1600 microns or more. In some embodiments, magnetic layer 205 may be cobalt zirconium tantalum (CoZrTa, CZT), iron aluminum oxide (FeAlOxide), cobalt iron hafnium oxide (CoFeHfOxide), or a combination thereof. In some embodiments, magnetic layer 205 may be a lamination of materials such as a lamination of CoZrTa/FeAlOxide, a lamination of CoZrTa/Aluminum Nitride (AIN), or the like. Such laminations may include any number of alternating layers of such materials having any suitable thicknesses. In some embodiments, magnetic layer 205 may include slots (not shown) running along the x-axis (please refer to FIG. 2B). For example, such slots may separate magnetic layer 205 into segments. For example, such slots may be about one to five microns in width and may have a pitch of about 100 microns to 200 microns. Such slots may, for example, reduce undesirable eddy currents during the operation of inductor 200.

As shown, inductor 200 may include dielectric layer 203 over magnetic layer 205. Dielectric layer 203 may include any suitable material or stack of materials having any suitable size and shape that may provide electrical insulation between magnetic layer 205 and metal trace 201. In some embodiments, dielectric layer 203 may include an oxide and/or a nitride. In some embodiments, dielectric layer 203 may have a thickness in the range of 0.1 to 3 microns. As shown, in some embodiments, dielectric layer 203 may be a portion of dielectric material 202.

Also as shown, inductor 200 may include metal trace 201 over dielectric layer 203. Metal trace 201 may have any suitable size and shape and may include any suitable metal material such as copper or aluminum or the like. In some embodiments, metal trace 201 may have a width in the range of 80 to 350 microns, thickness 213 in the range of 4 to 25 microns, and a length in the range of 200 microns to 1600 microns. In the illustrated embodiment, metal trace 201 has a rectangular cuboid shape; however metal trace 201 may have any suitable shape including rounded edges, a rounded top surface, or the like.

Continuing with the embodiment of FIGS. 2A and 2B, inductor 200 may include dielectric layer 204 over metal trace 201. Dielectric layer 204 may include any suitable material or stack of materials having any suitable size and shape that may provide electrical insulation between metal trace 201 and magnetic layer 206. In some embodiments, dielectric layer 203 may include an oxide and/or a nitride. In some embodiments, dielectric layer 203 may have a thickness in the range of 0.1 to 3 microns. As shown, in some embodiments, dielectric layer 203 may be a portion of dielectric material 202. In some embodiments dielectric layers 203, 204 may include the same material or materials and, in other embodiments, they may be or may include different materials.

Furthermore, inductor 200 may include magnetic layer 206 over dielectric layer 204. Magnetic layer 206 may have any suitable size and shape and may include any suitable magnetic material or materials. In some embodiments, magnetic layer 205 may have a width (e.g., along the x-axis) in the range of 80 to 350 microns, a thickness (e.g., along the z-axis) in the range of 0.5 to 6 microns, and a length (e.g., along the y-axis) in the range of 200 microns to 1600 microns or more. In some embodiments, magnetic layer 206 may be cobalt zirconium tantalum, iron aluminum oxide, cobalt iron hafnium oxide, or a combination thereof. In some embodiments, magnetic layer 106 may be a lamination of materials such as a lamination of CoZrTa/FeAlOxide, a lamination of CoZrTa/Aluminum Nitride (AlN), or the like. Such laminations may include any number of alternating layers of such materials having any suitable

thicknesses. In some embodiments magnetic layers 205, 206 may include the same material or materials and, in other embodiments, they may be or may include different materials. In some embodiments, magnetic layer 206 may include slots (not shown) running along the x-axis (please refer to FIG. 2B) to separate magnetic layer 206 into segments. For example, such slots may be about one to five microns in width and may have a pitch of about 100 microns to 200 microns.

In the embodiment of FIGS. 2A and 2B, in the vertical direction (e.g., along the z-axis), the entirety of metal trace 201 is between portions of magnetic layers 205, 206. For example, lateral edges 211, 212 of metal trace 201 may be within lateral edges 251, 252 of magnetic layer 205 and lateral edges 261, 262 of magnetic layer 106 and lateral edges 251, 252 of magnetic layer 205 and lateral edges 261, 262 of magnetic layer 106 may extend laterally beyond lateral edges 211, 212 of metal trace 201. For example, magnetic layers 205, 206 each extend laterally beyond lateral edges 211, 212 of metal trace 201. Furthermore, in the illustrated embodiment, metal trace 201 and magnetic layers 205, 206 are vertically aligned or substantially vertically aligned. In other embodiments, the entirety of metal trace may not be vertically between magnetic layers 205, 206 and/or metal trace 201 and magnetic layers 205, 206 may not be vertically aligned.

In some embodiments, metal trace 201 and one or both of magnetic layers 205, 206 may have the same or substantially the same widths and their lateral edges may be vertically aligned or substantially vertically aligned. In an embodiment, lateral edges 211, 251, 261 may be laterally aligned or substantially laterally aligned and/or lateral edges 212, 252, 262 may be laterally aligned or substantially laterally aligned. As discussed further herein with respect to FIG. 3, in some embodiments, one or both of magnetic layers 205, 206 may have a width less than the width of metal trace 201 and one or both of be magnetic layers 205, 206 may be laterally within lateral edges 211, 212 of metal trace 201.

Furthermore, as discussed, magnetic layers 205, 206 may be separated by a gap size 220 that is not less than a thickness 213 of metal trace 201 to provide edge gaps 214, 215. Edge gaps 214, 215 may extend along the entire length of metal trace 201 (e.g., in the direction of the y-axis) or they may extend along a portion or portions of the length of metal trace 201. In the illustrated embodiment, a top surface of magnetic layer 205 is entirely below a bottom surface of metal trace 201 and a bottom surface of magnetic layer 206 is entirely above a top surface of metal trace 201 such that metal trace 201and neither magnetic layer 205 nor 206 are overlap

horizontally (e.g., along the x-axis). In other embodiments one or both of magnetic layers 205, 206 may have portions that overlap horizontally with metal trace 201.

The example structure of FIGS. 2A and 2B may provide the discussed topology of inductor 200 such that a magnetic flux at the edges of inductor 200 is not completely closed. Furthermore, the example structure of FIGS. 2A and 2B may be relatively planar and may provide ease of manufacture and integration as is discussed further herein.

FIG. 3 is a cross-sectional view of another example structure of magnetic thin film inductor 200, arranged in accordance with at least some implementations of the present disclosure. As shown in FIG. 3, inductor 200 may include substrate 221, magnetic layer 205 over substrate 221, a dielectric layer 303 over magnetic layer 205, metal trace 201 over dielectric layer 303, a dielectric layer 304 over metal trace 201 and portions of dielectric layer 303, and a magnetic layer 306 over dielectric layer 303.

As shown, inductor 200 may include metal trace 201 disposed between dielectric layer 303, which separates metal trace 201 from magnetic layer 205, and another dielectric layer 304, which separates metal trace 201 from magnetic layer 306. In the illustrated embodiment, dielectric layers 303, 304 include two distinct layers or stacks of materials or the like. In another embodiment, dielectric layers 303, 304 may comprises a single dielectric material. Furthermore, as shown, at least a portion of metal trace 201 is between at least portions of magnetic layers 205, 306 and magnetic layers 205, 306, and magnetic layers 205, 306 may be separated by a gap size 320 that is not less than a thickness 213 of metal trace 201. For example, edge gaps 214, 215 may be provided along an entire length or a portion or portions of the length of metal trace 201. As discussed with respect to FIGS. 2A and 2B, inductor 200 may include metal trace 201 with magnetic layers 205, 306 below and above metal trace 201 and arranged such that a magnetic flux at the edges of inductor 200 (e.g., as associated with lateral edges, 211, 212, 251, 252, 361, 362 and edge gaps 214, 215) is not completely closed.

As discussed, inductor 200 may include magnetic layer 205 over substrate 221. Substrate 221 and magnetic layer 205 may include any characteristics as discussed with respect to FIGS. 2A and 2B. As shown, inductor 200 may include dielectric layer 303 over magnetic layer 205. Dielectric layer 303 may include any suitable material or stack of materials having any suitable size and shape that may provide electrical insulation between magnetic layer 205 and metal trace 201. In some embodiments, dielectric layer 303 may include an oxide and/or a nitride. In some

embodiments, dielectric layer 303 may have a thickness in the range of 0.1 to 3 microns. In some embodiments, dielectric layer 303 may be a conformal dielectric layer. In some embodiments, a portion of dielectric layer 303 may extend over substrate 221 as illustrated with respect to FIG. 5.

Also as shown, inductor 200 may include metal trace 201 over dielectric layer 303. Metal trace 201 may include any characteristics as discussed with respect to FIGS. 2A and 2B. For example, metal trace may have a width in the range of 80 to 350 microns, thickness 213 in the range of 4 to 25 microns, and a length in the range of 200 microns to 1600 microns. Continuing with the embodiment of FIG. 3, inductor 200 may include dielectric layer 304 over metal trace 201. Dielectric layer 304 may include any suitable material or stack of materials having any suitable size and shape that may provide electrical insulation between metal trace 201 and magnetic layer 306. In some embodiments, dielectric layer 304 may include an oxide and/or a nitride. In some embodiments, dielectric layer 304 may have a thickness in the range of 0.1 to 10 microns. As shown, in some embodiments, dielectric layer 304 may be a conformal dielectric layer. In some embodiments dielectric layers 303, 304 may include the same material or materials and, in other embodiments, they may be or may include different materials.

Furthermore, inductor 200 may include magnetic layer 306 over dielectric layer 304. Magnetic layer 306 may have any suitable size and shape and may include any suitable magnetic material or materials. In some embodiments, magnetic layer 205 may have a width (e.g., along the x-axis) in the range of 80 to 350 microns, a thickness (e.g., along the z-axis) in the range of 0.5 to 6 microns, and a length (e.g., along the y-axis) in the range of 200 microns to 1600 microns or more. In some embodiments, magnetic layer 306 may be cobalt zirconium tantalum, iron aluminum oxide, cobalt iron hafnium oxide, or a combination thereof. In some embodiments, magnetic layer 306 may be a lamination of materials such as a lamination of CoZrTa/FeAlOxide, a lamination of CoZrTa/Aluminum Nitride (AlN), or the like. Such laminations may include any number of alternating layers of such materials having any suitable thicknesses. In some embodiments magnetic layers 205, 306 may include the same material or materials and, in other embodiments, they may be or may include different materials. In some embodiments, relative to metal trace 201, magnetic layer 306 may have a width of about 50% to about 75% of the width of metal trace 201. In an embodiment, magnetic layer 306 may have a width equal to the width of metal trace 201.

In the embodiment of FIG. 3, in a lateral direction (e.g., along the x-axis), a portion of metal trace 201 extends laterally beyond the edges of magnetic layer 306. For example, lateral

edges 211, 212 of metal trace 201 may be within lateral edges 251, 252 of magnetic layer 205 but may not bet within lateral edges 361, 362 of magnetic layer 306. For example, lateral edges 361, 362 of magnetic layer 306 may be within lateral edges 211, 212 of metal trace 201. Furthermore, in the illustrated embodiment, metal trace 201 and magnetic layers 205, 306 are vertically aligned or substantially vertically aligned. In other embodiments, lateral edges 251, 261 of magnetic layer 205 may also be within lateral edges 211, 212 of metal trace 201 and/or magnetic layer 205, magnetic layer 306, and metal trace 201 may not be vertically aligned.

Furthermore, as discussed, magnetic layers 205, 306 may be separated by a gap size 320 that is not less than a thickness 213 of metal trace 201 such that edge gaps 214, 215 are provided along an entire length or portion or portions of a length of metal trace 201. In the illustrated embodiment, a top surface of magnetic layer 205 is entirely below a bottom surface of metal trace 201 and a bottom surface of magnetic layer 306 is entirely above a top surface of metal trace 201.

The example structure of FIG. 3 may provide the discussed topology such that a magnetic flux at the edges of inductor 200 is not completely closed and the example structure of FIG. 3 may advantageously provide for the use of conformal dielectrics (e.g., without the need for using self-leveling dielectrics and/or providing planarization operations).

FIG. 4 is a cross-sectional view of another example structure of magnetic thin film inductor 200, arranged in accordance with at least some implementations of the present disclosure. As shown in FIG. 4, inductor 200 may include substrate 221, magnetic layer 205 over substrate 221a dielectric layer 303 over magnetic layer 205, metal trace 201 over dielectric layer 303, a dielectric layer 404 over metal trace 201, and a magnetic layer 406 over dielectric layer 303.

As shown, inductor 200 may include metal trace 201 disposed between dielectric layer 303, which separates metal trace 201 from magnetic layer 205, and another dielectric layer 404, which separates metal trace 201 from magnetic layer 406. Dielectric layers 303, 304 may include two distinct layers or stacks of materials or they may comprise a single dielectric material. Furthermore, as shown, at least a portion of metal trace 201 is between at least portions of magnetic layers 205, 406, and magnetic layers 205, 406 may be separated by a gap size 420 that is not less than one-fourth of a thickness 213 of metal trace 201. For example, if thickness 313 is about 8 microns, gap size 420 may be not less than about 2 microns, if thickness 213 is about 6

microns, gap size 420 may be not less than about 1.5 microns, if thickness 213 is about 4 microns, gap size 420 may be not less than about 1 micron and so on. As shown, inductor 200 may include metal trace 201 with magnetic layers 205, 406 below and above metal trace 201 and arranged such that a magnetic flux at the edges of inductor 200 (e.g., as associated with lateral edges, 211, 212, 251, 252, 461, 462 and edge gaps 214, 215) is not completely closed. As discussed above, the inventors have found that such a topology may provide for scalable inductors that maintain high performance as they are miniaturized. For example, fully sealing the edges of inductor 200 or substantially sealing the edges of inductors may hinder their performance as they are miniaturized.

As discussed, inductor 200 may include magnetic layer 205 over substrate 221 and dielectric layer 303 over magnetic layer 205. Substrate 221, magnetic layer 205, and dielectric layer may 303 include any characteristics as discussed herein. Also as shown, inductor 200 may include metal trace 201 over dielectric layer 303. Metal trace 201 include any characteristics as discussed herein such as, for example, a width in the range of 80 to 350 microns, thickness 213 in the range of 4 to 25 microns, and a length in the range of 200 microns to 1600 microns.

Continuing with the embodiment of FIG. 4, inductor 200 may include dielectric layer 404 over metal trace 201. Dielectric layer 404 may include any suitable material or stack of materials having any suitable size and shape that may provide electrical insulation between metal trace 201 and magnetic layer 406. In some embodiments, dielectric layer 304 may include an oxide and/or a nitride. In some embodiments, dielectric layer 404 may have a thickness in the range of 0.1 to 10 microns. As shown, in some embodiments, dielectric layer 404 may be a conformal dielectric layer. In some embodiments dielectric layers 303, 404 may include the same material or materials and, in other embodiments, they may include different materials. In comparison to dielectric layer 304 (please refer to FIG. 3), dielectric layer 404 is illustrated as thicker for the sake of clarity of presentation. However, as discussed, dielectric layer 404 may have any suitable thickness.

Furthermore, inductor 200 may include magnetic layer 406 over dielectric layer 404. Magnetic layer 406 may have any suitable size and shape and may include any suitable magnetic material or materials. In some embodiments, magnetic layer 406 may have a width (e.g., along the x-axis) in the range of 80 to 350 microns, a thickness (e.g., along the z-axis) in the range of 0.5 to 6 microns, and a length (e.g., along the y-axis) in the range of 200 microns to 1600 microns or more. In some embodiments, magnetic layer 205 may be cobalt zirconium tantalum,

iron aluminum oxide, cobalt iron hafnium oxide, or a combination thereof. In some embodiments, magnetic layer 406 may be a lamination of materials such as a lamination of CoZrTa/FeAlOxide, a lamination of CoZrTa/Aluminum Nitride (AlN), or the like. Such laminations may include any number of alternating layers of such materials having any suitable thicknesses. In some embodiments magnetic layers 205, 406 may include the same material or materials and, in other embodiments, they may be or may include different materials. In some embodiments, magnetic layer 406 may include slots (not shown) running along the x-axis to separate magnetic layer 406 into segments. For example, such slots may be about one to five microns in width and may have a pitch of about 100 microns to 200 microns.

In the embodiment of FIG. 4, in the vertical direction (e.g., along the z-axis), the entirety of metal trace 201 is between portions of magnetic layers 205, 406. For example, lateral edges 211, 212 of metal trace 201 may be within lateral edges 251, 252 of magnetic layer 205 and lateral edges 461, 462 of magnetic layer 406 and lateral edges 251, 252 of magnetic layer 205 and lateral edges 461, 462 of magnetic layer 406 may extend laterally beyond lateral edges 211, 212 of metal trace 201. Furthermore, in the illustrated embodiment, metal trace 201 and magnetic layers 205, 406 are vertically aligned or substantially vertically aligned.

Furthermore, as discussed, magnetic layers 205, 406 may be separated by a gap size 420 that is not less than one-fourth of thickness 213 of metal trace 201 such that edge gaps 214, 215 are provided along an entire length or portion or portions of a length of metal trace 201. In the illustrated embodiment, a top surface of magnetic layer 205 is entirely below a bottom surface of metal trace 201 and portions 411, 412 of a bottom surface of magnetic layer 406 are below a top surface of metal trace 201.

The example structure of FIG. 4 may provide the discussed topology such that a magnetic flux at the edges of inductor 200 is not completely closed and the example structure of FIG. 4 may advantageously provide for the use of conformal dielectrics (e.g., without the need for using self-leveling dielectrics and/or providing planarization operations) and a larger (e.g., wider) top magnetic layer.

FIG. 5 is a cross-sectional view of another example structure of magnetic thin film inductor 200 and a second magnetic thin film inductor 500 inductively coupled to magnetic thin film inductor 200, arranged in accordance with at least some implementations of the present disclosure. As shown in FIG. 5, inductor 200 may include substrate 221, magnetic layer 205 over

substrate 221, a dielectric layer 303 over magnetic layer 205, metal trace 201 over dielectric layer 303, a dielectric layer 504 over metal trace 201, and a magnetic layer 306 over dielectric layer 303. Furthermore, FIG. 5 illustrates an inductor 500 coupled to inductor 200. As shown, inductor 500 may include substrate 221, magnetic layer 505 over substrate 221, dielectric layer 303 over magnetic layer 505, metal trace 501 over dielectric layer 503, dielectric layer 504 over metal trace 501, and a magnetic layer 506 over dielectric layer 503.

As shown, inductor 200 may include metal trace 201 disposed between dielectric layer 303, which separates metal trace 201 from magnetic layer 205, and a portion of another dielectric layer 504, which separates metal trace 201 from magnetic layer 306. Dielectric layers 303, 504 may include two distinct layers or stacks of materials or they may comprise a single dielectric material. Furthermore, as shown, at least a portion of metal trace 201 is between at least portions of magnetic layers 205, 306, and magnetic layers 205, 306 may be separated by a gap size that is not less than a thickness of metal trace 201. As shown, inductor 200 may include metal trace 201 with magnetic layers 205, 306 below and above metal trace 201 and arranged such that a magnetic flux at the edges of inductor. Similarly, inductor 500 may include metal trace 501 disposed between dielectric layer 303, which separates metal trace 501 from magnetic layer 505, and a portion of dielectric layer 504, which separates metal trace 501 from magnetic layer 506. At least a portion of metal trace 501 is between at least portions of magnetic layers 505, 506, and magnetic layers 505, 506 may be separated by a gap size that is not less than a thickness of metal trace 501.

As discussed, inductor 200 may include magnetic layer 205 over substrate 221 and dielectric layer 303 over magnetic layer 205. Substrate 221, magnetic layer 205, and dielectric layer may 303 may include any characteristics as discussed herein. Inductor 500 may include magnetic layer 505 over substrate 221 and dielectric layer 303 over magnetic layer 205. Magnetic layer 505 may include any characteristics as discussed herein with respect to magnetic layer 205. In some embodiments magnetic layers 205, 505 may include the same material or materials and, in other embodiments, they may be or may include different materials. In an embodiment, magnetic layers 205, 505 may be a continuous magnetic layer extending between and under metal traces 201, 501.

Also as shown, inductor 200 may include metal trace 201 over dielectric layer 303 and inductor 200 may include metal trace 501 over dielectric layer 303. Metal trace 201 and metal trace 501 include any characteristics as discussed herein with respect to metal trace 201 such as,

for example, widths in the range of 80 to 350 microns, thicknesses 213 in the range of 4 to 25 microns, and lengths in the range of 200 microns to 1600 microns. Inductor 500 may include metal trace 501 over dielectric layer 303. In some embodiments metal traces 201, 501 may have the same lengths, widths, thicknesses, and material or materials and, in other embodiments, any of such characteristics may be different.

Furthermore, inductors 200, 500 may include dielectric layer 504 having at least a portion of dielectric layer 504 over metal trace 201 and at least a portion of dielectric layer 504 over metal trace 501. Dielectric layer 504 may include any suitable material or stack of materials having any suitable size and shape that may provide electrical insulation between metal traces 201, 501 and magnetic layers 306, 506, respectively. In some embodiments, dielectric layer 504 may include a self-leveling dielectric layer (e.g., a spin on glass or the like). In some embodiments, dielectric layer 504 may be formed by providing a bulk dielectric deposition and planarization techniques. In some embodiments, dielectric layer 504 may include a conformal dielectric or an additional conformal dielectric layer may be formed between metal traces 201, 501 (please refer to FIG. 7F).

Furthermore, inductor 200 may include magnetic layer 306 over dielectric layer 504 and inductor 500 may include magnetic layer 506 over dielectric layer 504. Magnetic layers 306, 506 may have any suitable size and shape and may include any suitable magnetic material or materials. In some embodiments, magnetic layers 306, 506 may have widths (e.g., along the x-axis) in the range of 80 to 350 microns, thicknesses (e.g., along the z-axis) in the range of 0.5 to 6 microns, and lengths (e.g., along the y-axis extending into and out of the page) in the range of 200 microns to 1600 microns or more. In some embodiments, magnetic layers 306, 506 may be cobalt zirconium tantalum, iron aluminum oxide, cobalt iron hafnium oxide, or a combination thereof. In some embodiments, magnetic layers 306, 506 may be laminations of materials such as laminations of CoZrTa/FeAlOxide, laminations of CoZrTa/Aluminum Nitride (AlN), or the like. Such laminations may include any number of alternating layers of such materials having any suitable thicknesses. In some embodiments, magnetic layers 306, 506 may include slots (not shown) running along the x-axis to separate magnetic layers 306, 506 into segments. For example, such slots may be about one to five microns in width and may have a pitch of about 100 microns to 200 microns. In some embodiments magnetic layers 306, 506 may have the same widths, lengths, thicknesses, slots, and materials, and, in other embodiments one or more of such characteristics may be different. As shown, metal traces 201, 501 may have edge gaps extending

along an entire length or a portion or portions of the length of metal traces 201, 501 as discussed with respect to FIGS. 2A, 2B, 3, and 4.

In the embodiment of FIG. 5, inductors 200, 500 have metal traces 201, 501 that extend laterally beyond the edges of magnetic layers 306, 506 and that are laterally within the edges of magnetic layers 305, 505 as discussed with respect to FIG. 3. However, any example inductor structure as discussed herein may be provided for inductors 200, 500 such as those illustrated and discussed with respect to FIGS. 2A and 2B, FIG. 4, and FIG. 7F. Furthermore, in some embodiments the structures of inductors 200, 500 may be the same and, in other embodiments, the structures of inductors 200, 500 may be different.

Inductors 200, 500 may provide for structures that may be miniaturized to small sizes and may provide exhibit high performance with respect to inductance, Q factor, and coupling, particularly at increasing currents. As discussed further herein, inductors 200, 500 may be employed in a variety of integrated circuits such as power management integrated circuits (e.g., via buck circuits), radio frequency integrated circuits (e.g., via resonant circuits), and so on.

As discussed, inductor 200 may be straight line or curved and, in some embodiments, inductor 200 may provide about 1 to 5 nH per 800 microns of length without loss of magnetic permeability due to curvature effects. Inductor 200 may also provide advantageous characteristics with respect to high or increasing currents. For example, inductor 200 may not lose inductance up to 1 or 1.5 amperes of current (e.g., inductor 200 may handle up to or over one ampere of current prior to exhibiting any magnetic saturation effects). Furthermore, inductor 200 may provide a higher peak Q (or operating Q) with respect to prior inductors.

As discussed, inductor 200 may be disposed adjacent to one or more additional inductors such as inductor 500 and, in some embodiments, inductive coupling between such inductors may be tuned to about 0.2 to 0.6 k via the widths of inductors 200, 500 or other characteristics, which may allow for relatively simple compensation in power management integrated circuits such as those including buck circuits or the like. For example, inductors 200, 500 may provide controlled coupling that may allow for optimization of compensation circuits or the like.

As discussed, inductor 200 may provided with a range of structures, topologies, sizes, and/or materials. Such characteristics may be modified to provide a range of electrical characteristics for inductor 200 and/or inductor 500. For example, at a length of about 800 microns and widths in the range of about 100 to 150 microns, about 2 nH of inductance and a

peak Q of about 10 may be provided at a frequency of about 100 MHz, which may be particularly advantageous for power management integrated circuits. Furthermore, inductors 200, 500 with such characteristics may have low coupling (k) of about 0.2 up to a frequency of about 1 GHz. In some examples, a peak Q of about 14 at about 1 GHz may be attained, which may be particularly advantageous for radio frequency integrated circuits.

Also, as discussed, inductor 200 and/or inductor 500 may offer the advantage of providing a wide design space with respect to coupling, inductance, and Q factor, which may offer efficient circuit implementations in voltage regulation (e.g., via a power management integrated circuit) or the like. For example, by varying the width of magnetic layers 205, 206, 306, 406 and/or the width of metal trace 201, the inductance of inductor 200 may be controlled to between about 1 and 5 nH per about 800 microns of inductor length. Mutual inductance between inductors 200, 500 may be controlled between about 0.15 to 0.5 using the same or similar widths.

FIG. 6 is a flow diagram illustrating an example process 600 for fabricating magnetic thin film inductors, arranged in accordance with at least some implementations of the present disclosure. For example, process 600 may be implemented to fabricate any example structure of inductor 200 as discussed herein. In the illustrated implementation, process 600 may include one or more operations as illustrated by operations 601-605. However, embodiments herein may include additional operations, certain operations being omitted, or operations being performed out of the order provided.

Process 600 may begin at operation 601, "Pattern a First Magnetic Layer over a Substrate", where a magnetic layer may be patterned over a substrate. The magnetic layer may be patterned using any suitable technique or techniques such as deposition and photolithography techniques or the like. In an embodiment, magnetic layer 205 may be pattered over substrate 221 as discussed herein with respect to FIG. 7A.

Process 600 may continue at operation 602, "Dispose a First Dielectric Layer over the First Magnetic Layer", where a dielectric layer may be disposed over the first magnetic layer. The dielectric layer may be formed using any suitable techniques such as chemical vapor deposition techniques or the like. In an embodiment, dielectric layer 303 may be disposed over magnetic layer 205 as discussed herein with respect to FIG. 7B. In another embodiment, dielectric layer 203 may be formed over magnetic layer 205 as shown with respect to FIG. 2A.

Process 600 may continue at operation 603, "Dispose a Metal Trace over the First Dielectric Layer", where a metal trace may be disposed over the first dielectric layer. The metal trace may be disposed over the first dielectric layer using any suitable technique or techniques such as electroplating and photolithography techniques or the like. In an embodiment, metal trace 201 may be disposed over dielectric layer 303 as discussed herein with respect to FIG. 7C. In another embodiment, metal trace 201 may be disposed over dielectric layer 203 as shown with respect to FIG. 2A.

Process 600 may continue at operation 604, "Dispose a Second Dielectric Layer over the Metal Trace", where a second dielectric layer may be disposed over the metal trace. The second dielectric layer may be formed using any suitable techniques such as chemical vapor deposition techniques, spin on techniques, bulk deposition and planarization techniques, or the like. In an embodiment, dielectric layer 705 and/or dielectric layer 707 may be disposed over metal trace 201 as discussed herein with respect to FIGS. 7D and 7E. In other embodiments, dielectric layer 204 may be disposed over metal trace 201 as shown in FIG. 2A, dielectric layer 304 may be disposed over metal trace 201 as shown in FIG. 3, dielectric layer 404 may be disposed over metal trace 201 as shown in FIG. 4, or dielectric layer 504 may be disposed over metal trace 201 as shown in FIG. 5.

Process 600 may continue at operation 605, "Pattern a Second Magnetic Layer over the Second Dielectric Layer", where a second magnetic layer may be patterned over the second dielectric layer. The second magnetic layer may be patterned using any suitable technique or techniques such as deposition and photolithography techniques or the like. In an embodiment, magnetic layer 709 may be pattered over dielectric layer 707 and/or dielectric layer 705 as discussed herein with respect to FIG. 7F. In other embodiments, magnetic layer 206 may be patterned over dielectric layer 204 as shown in FIG. 2A, magnetic layer 306 may be patterned over dielectric layer 304 as shown in FIG. 3, magnetic layer 406 may be patterned over dielectric layer 404 as shown in FIG. 4, or magnetic layer 306 may be patterned over dielectric layer 504 as shown in FIG. 5.

Process 600 may be utilized to generate any inductor structure as discussed herein such as those discussed with respect to inductor 200. In an embodiment, process 600 may generate an example structure of a magnetic thin film inductor as shown with respect to FIG. 7F. In some embodiments, process 600 may generate multiple inductors such as inductors 200, 500 as shown in FIG. 5. Process 600 and the inductor structures discussed herein may provide for cost effective

inductor manufacture including use of less magnetic material as compared to prior processes and inductor structures.

FIGS. 7A, 7B, 7C, 7D, 7E, and 7F are cross-sectional views of example inductor structures as particular fabrication operations are performed and FIG. 7F is another example structure of magnetic thin film inductor 200, arranged in accordance with at least some implementations of the present disclosure. FIG. 7A illustrates a cross-sectional view of an inductor structure 701 taken along plane A as shown in the plan view of FIG. 2B. As shown in FIG. 7A, inductor structure 701 includes substrate 221 and magnetic layer 205. For example, substrate 221 may be any substrate as discussed herein such as a substrate including metallization interconnect layers for integrated circuits or electronic devices such as transistors, memories, capacitors, resistors, optoelectronic devices, switches, or any other active or passive electronic devices separated by an electrically insulating layer. In some embodiments, substrate 221 may include power management integrated circuit components or radio frequency integrated circuit components or the like.

Also as shown in FIG. 7A, magnetic layer 205 may be patterned over substrate 221. In an embodiment, a bulk magnetic material or layers of magnetic material may be deposited over substrate 221 and photolithography techniques may be utilized to pattern magnetic layer 205. In another embodiment, a bulk magnetic material or layers of magnetic material may be provided as a laminate on substrate and photolithography techniques or other printing techniques may be utilized to pattern magnetic layer 205. Magnetic layer 205 may include any materials and characteristics as discussed herein such as with respect to FIGS. 2A and 2B. In an embodiment, magnetic layer 205 may be about 100 microns wide by about 800 microns long by about 8 microns thick (e.g., in the x-axis, y-axis, and z-axis directions respectively, please refer to FIGS. 2A and 2B). As discussed, magnetic layer 205 may be linear or curved in various embodiments. In some embodiments, magnetic layer 205 may include slots (not shown) running along the x-axis (please refer to FIG. 2B). For example, such slots may separate magnetic layer 205 into segments. For example, such slots may be about one to five microns in width and may have a pitch of about 100 microns to 200 microns. Such slots may, for example, reduce undesirable eddy currents during the operation of inductor 200.

FIG. 7B illustrates an inductor structure 702 similar to inductor structure 701, after the formation of dielectric layer 303. Dielectric layer 303 may be formed using any suitable technique or techniques such as chemical vapor deposition, plasma enhanced chemical vapor

deposition, physical vapor deposition, atomic layer deposition, or the like. In some embodiments, dielectric layer 303 may be a conformal dielectric layer as shown in FIG. 7B. Dielectric layer 303 may include any characteristics as discussed elsewhere herein such as with respect to FIG. 3.

FIG. 7C illustrates an inductor structure 703 similar to inductor structure 702, after the formation of metal trace. Metal trace 201 may be formed using any suitable technique or techniques such as electroplating and photolithography techniques or the like. As discussed, in some embodiments, metal trace 201 may be aluminum or copper or the like. Metal trace 201 may include any characteristics as discussed elsewhere herein such as those discussed with respect to FIGS. 2A and 2B.

FIG. 7D illustrates an inductor structure 704 similar to inductor structure 703, after the formation of dielectric layer 705. Dielectric layer 705 may be formed using any suitable technique or techniques such as chemical vapor deposition, plasma enhanced chemical vapor deposition, physical vapor deposition, atomic layer deposition, or the like. In some embodiments, dielectric layer 705 may be a conformal dielectric layer as shown in FIG. 7D. Dielectric layer 705 may include any suitable material or materials and any suitable thickness. In some embodiments, dielectric layer 705 may include an oxide or a nitride or the like. In some embodiments, dielectric layer 705 may have a thickness in the range of 0.1 to 3 microns.

FIG. 7E illustrates an inductor structure 706 similar to inductor structure 704, after the formation of dielectric layer 707. Dielectric layer 303 may be formed using any suitable technique or techniques such as spin on dielectric techniques, self planarizing dielectric techniques, bulk deposition and planarization (e.g., polish) techniques, or the like. In some embodiments, dielectric layer 705 may be a self planarizing dielectric layer. As shown, in some embodiments, dielectric layer 707 may provide a substantially planar layer over inductor structure 704. Dielectric layer 707 may include any suitable material or materials and any suitable thickness. In some embodiments, dielectric layer 705 may include a spin on glass material or the like. In some embodiments, dielectric layer 707 may have a thickness over metal trace in the range of 0.1 to 3 microns and a thickness over substrate 221 in the range of about 4 to 30 microns.

FIG. 7F illustrates an inductor structure 708 similar to inductor structure 704, after the formation of magnetic layer 709. For example, inductor structure 708 may be another example structure of magnetic thin film inductor 200. Magnetic layer 709 may be patterned over substrate

221 using any suitable technique or techniques such as those discussed with respect to magnetic layer 205 such as deposition and photolithography techniques. Magnetic layer 709 may have any suitable size and shape and may include any suitable magnetic material or materials. In some embodiments, magnetic layer 709 may have a width in the range of 80 to 350 microns, a thickness in the range of 0.5 to 6 microns, and a length in the range of 200 microns to 1600 microns or more. In some embodiments, magnetic layer 709 may be cobalt zirconium tantalum, iron aluminum oxide, cobalt iron hafnium oxide, or a combination thereof. In some embodiments, magnetic layer 709 may be a lamination of materials such as a lamination of CoZrTa/FeAlOxide, a lamination of CoZrTa/Aluminum Nitride (AlN), or the like. Such laminations may include any number of alternating layers of such materials having any suitable thicknesses. In some embodiments, magnetic layer 709 may include slots (not shown) running along the x-axis (please refer to FIG. 2B) to separate magnetic layer 709 into segments. For example, such slots may be about one to five microns in width and may have a pitch of about 100 microns to 200 microns. In some embodiments magnetic layers 205, 709 may include the same material or materials and, in other embodiments, they may be or may include different materials.

In the illustrated embodiment, magnetic layer 709 is laterally within metal trace 201 as discussed with respect to FIG. 3. However, magnetic layer 709 may extend laterally beyond metal trace 201 or be the same size and aligned with respect to metal trace 201 as discussed with respect to FIGS. 2A and 2B.

The example structure of inductor 200 may offer the advantages of the electrical isolation characteristics of dielectric layer 705 between metal trace 201 and magnetic layer 709 and a substantially planar structure.

FIGS. 7A-7F illustrate an example process flow for fabricating an example structure of magnetic thin film inductor 200. Furthermore, the discussed process flow may be modified to fabricate other example structures of magnetic thin film inductor 200. In some embodiments, a magnetic layer may be formed over inductor structure 704 as shown in FIG. 7D to form the inductor structure as shown in FIG. 3 (e.g., when the magnetic layer is laterally within metal trace 201) or the inductor structure as shown in FIG. 4 (e.g., when the magnetic layer that extends laterally beyond the edges of metal trace 201). In other embodiments, such process operations may be utilized to generate inductors 200, 500 as shown in FIG. 5 by skipping the formation of dielectric layer 705 as shown in FIG. 7D.

Furthermore, in some embodiments, the process flow may be utilized to form multiple inductors having the same structures. In other embodiments, the width, for example, of magnetic layer 709 (please refer to FIG. 7F) for different inductors may be varied to form inductors having different sizes, structures, or topologies such as one or more inductors having a magnetic layer laterally within metal trace 201, one or more other inductors having a magnetic layer that extends laterally beyond the edges of metal trace 201, one or more other inductors having magnetic layers that are the same size and vertically aligned with metal trace, and/or any other combination of inductor structures as discussed herein. Furthermore, additional operations such as masking operations (and associated mask removal operations) may be used to provide different magnetic layer materials, different metal trace materials, and/or different dielectric layer structures between different inductors.

As discussed, the inductors described herein such as inductor 200 and/or inductor 500 may be utilized in power management integrated circuits, radio frequency integrated circuits, or the like. For example, a system may include a processor, a memory coupled to a processor, and a power management integrated circuit or radio frequency integrated circuit including any inductor or combination of inductors discussed herein.

FIG. 8 illustrates a system 800 in which a mobile computing platform 805 and/or a data server machine 806 employs a magnetic thin film inductor, arranged in accordance with at least some implementations of the present disclosure. Data server machine 806 may be any commercial server, for example, including any number of high-performance computing platforms disposed within a rack and networked together for electronic data processing, which in the exemplary embodiment includes a packaged device 850. For example, device 850 may include a power management integrated circuit (PMIC) having one or more magnetic thin film inductors (MTFI) such as any magnetic thin film inductor discussed herein. As discussed below, in some examples, device 850 may include a system on a chip (SOC) such as SOC 860, which is illustrated with respect to mobile computing platform 805.

Mobile computing platform 805 may be any portable device configured for each of electronic data display, electronic data processing, wireless electronic data transmission, or the like. For example, mobile computing platform 805 may be any of a tablet, a smart phone, a laptop computer, etc., and may include a display screen (e.g., a capacitive, inductive, resistive, or optical touchscreen), a chip-level or package-level integrated system 810, and a battery 815. Although illustrated with respect to mobile computing platform 805, the magnetic thin film

inductors discussed herein may also be employed via a PMIC and/or RFIC of a desktop computer or the like.

Whether disposed within the integrated system 810 illustrated in the expanded view 820, or as a stand-alone packaged device within data server machine 806, SOC 860 may include memory circuitry and/or processor circuitry 840 (e.g., RAM, a microprocessor, a multi-core microprocessor, graphics processor, etc.), a PMIC 830, a controller 835, and a radio frequency integrated circuit (RFIC) 825 (e.g., including a wideband RF transmitter and/or receiver (TX/RX)). As shown, one or more magnetic thin film inductors such as any magnetic thin film inductor discussed herein may be employed via PMIC 830 and/or RFIC 825. In some embodiments, RFIC 825 includes a digital baseband and an analog front end module further comprising a power amplifier on a transmit path and a low noise amplifier on a receive path).

Functionally, PMIC 830 may perform battery power regulation, DC-to-DC conversion, etc., and so has an input coupled to battery 815, and an output providing a current supply to other functional modules. As further illustrated in FIG. 8, in the exemplary embodiment, RFIC 825 has an output coupled to an antenna (not shown) to implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. In alternative implementations, each of these SoC modules may be integrated onto separate ICs coupled to a package substrate, interposer, or board.

FIG. 9 is a functional block diagram of a computing device 900, arranged in accordance with at least some implementations of the present disclosure. Computing device 900 or portions thereof may be implemented via one or both of data server machine 806 or mobile computing platform 805, for example, and further includes a motherboard 902 hosting a number of components, such as but not limited to a processor 901 (e.g., an applications processor) and one or more communications chips 904, 905. Processor 901 may be physically and/or electrically coupled to motherboard 902. In some examples, processor 901 includes an integrated circuit die packaged within the processor 901. In general, the term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

In various examples, one or more communication chips 904, 905 may also be physically and/or electrically coupled to the motherboard 902. In further implementations, communication chips 904 may be part of processor 901. Depending on its applications, computing device 900 may include other components that may or may not be physically and electrically coupled to motherboard 902. These other components may include, but are not limited to, volatile memory (e.g., DRAM) 907, 908, non-volatile memory (e.g., ROM) 910, a graphics processor 912, flash memory, global positioning system (GPS) device 913, compass 914, a chipset 906, an antenna 916, a power amplifier 909, a touchscreen controller 911, a touchscreen display 917, a speaker 915, a camera 903, and a battery 918, as illustrated, and other components such as a digital signal processor, a crypto processor, an audio codec, a video codec, an accelerometer, a gyroscope, and a mass storage device (such as hard disk drive, solid state drive (SSD), compact disk (CD), digital versatile disk (DVD), and so forth), or the like.

Communication chips 904, 905 may enables wireless communications for the transfer of data to and from the computing device 900. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. Communication chips 904, 905 may implement any of a number of wireless standards or protocols, including but not limited to those described elsewhere herein. As discussed, computing device 900 may include a plurality of communication chips 904, 905. For example, a first communication chip may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others. For example, any component of computing device 900 may include or utilize one or more magnetic thin film inductors such as any magnetic thin film inductor discussed herein.

As used in any implementation described herein, the term "module" refers to any combination of software, firmware and/or hardware configured to provide the functionality described herein. The software may be embodied as a software package, code and/or instruction set or instructions, and "hardware", as used in any implementation described herein, may include, for example, singly or in any combination, hardwired circuitry, programmable circuitry, state machine circuitry, and/or firmware that stores instructions executed by programmable circuitry.

The modules may, collectively or individually, be embodied as circuitry that forms part of a larger system, for example, an integrated circuit (IC), system on-chip (SoC), and so forth.

While certain features set forth herein have been described with reference to various implementations, this description is not intended to be construed in a limiting sense. Hence, various modifications of the implementations described herein, as well as other implementations, which are apparent to persons skilled in the art to which the present disclosure pertains are deemed to lie within the spirit and scope of the present disclosure.

The following examples pertain to further embodiments.

In one or more first embodiments, a magnetic thin film inductor comprises a first magnetic layer over a substrate, a first dielectric layer over the first magnetic layer, a metal trace over the first dielectric layer, a second dielectric layer over the metal trace, and a second magnetic layer over the second dielectric layer, wherein the first magnetic layer and the second magnetic layer are separated to provide edge gaps along lateral edges of the metal trace having a gap size not less than one-fourth of a thickness of the metal trace.

Further to the first embodiments, the edge gaps extend along the entire lateral edges of the metal trace.

Further to the first embodiments, the first and second magnetic layers each extend laterally beyond both the lateral edges of the metal trace.

Further to the first embodiments, the first and second magnetic layers each extend laterally beyond both the lateral edges of the metal trace, a top surface of the first magnetic layer is entirely below a bottom surface of the metal trace, and a bottom surface of the second magnetic layer is entirely above a top surface of the metal trace

Further to the first embodiments, the first and second magnetic layers each extend laterally beyond both the lateral edges of the metal trace, a top surface of the first magnetic layer is entirely below a bottom surface of the metal trace, and a portion of a bottom surface of the second magnetic layer is below a top surface of the metal trace.

Further to the first embodiments, the second magnetic layer is laterally within the lateral edges of the metal trace.

Further to the first embodiments, the first magnetic layer and the second magnetic layer have lateral edges that are vertically aligned with the lateral edges of the metal trace.

Further to the first embodiments, the metal trace comprises copper and the first and second magnetic layers both comprise at least one of cobalt zirconium tantalum, iron aluminum oxide, or cobalt iron hafnium oxide.

Further to the first embodiments, the first and second magnetic layers comprise different magnetic materials.

Further to the first embodiments, at least one of the first magnetic layer, the first dielectric layer, the second dielectric layer, or the second magnetic layer comprises a lamination of multiple materials.

Further to the first embodiments, the metal trace comprises at least one of a linear trace or a curved trace.

Further to the first embodiments, the first and second magnetic layers comprise different magnetic materials and/or at least one of the first magnetic layer, the first dielectric layer, the second dielectric layer, or the second magnetic layer comprises a lamination of multiple materials and/or the metal trace comprises at least one of a linear trace or a curved trace.

Further to the first embodiments, a width of the metal trace is in the range of 80 to 350 microns, the thickness of the metal trace is in the range of 4 to 12 microns, and the gap size is not less than the thickness of the metal trace.

In one or more second embodiments, a system comprises a processor, a memory coupled to the processor, and at least one of a power management integrated circuit or a radio frequency integrated circuit including an inductor comprising a metal trace disposed within at least one dielectric material, a first magnetic layer adjacent to the at least one dielectric material, and a second magnetic layer adjacent to the at least one dielectric material, wherein the metal trace is between at least a portion of the first magnetic layer and at least a portion of the second magnetic layer, and wherein the first magnetic layer and the second magnetic layer are separated to provide edge gaps along lateral edges of the metal trace having a gap size not less than one-fourth of a thickness of the metal trace.

Further to the second embodiments, the power management integrated circuit or the radio frequency integrated circuit further comprises a second inductor inductively coupled to the inductor, the second inductor comprising a second metal trace disposed within at least one second dielectric material, a third magnetic layer adjacent to the at least one second dielectric material, and a fourth magnetic layer adjacent to the at least one second dielectric material, wherein the second metal trace is between at least a portion of the third magnetic layer and at least a portion of the fourth magnetic layer, and wherein the third magnetic layer and the fourth magnetic layer are separated to provide second edge gaps along lateral edges of the second metal trace.

Further to the second embodiments, the power management integrated circuit or the radio frequency integrated circuit further comprises a second inductor inductively coupled to the inductor, the second inductor comprising a second metal trace disposed within at least one second dielectric material, a third magnetic layer adjacent to the at least one second dielectric material, and a fourth magnetic layer adjacent to the at least one second dielectric material, wherein the second metal trace is between at least a portion of the third magnetic layer and at least a portion of the fourth magnetic layer, and wherein the third magnetic layer and the fourth magnetic layer are separated to provide second edge gaps along lateral edges of the second metal trace, wherein the first and second magnetic layers each extend laterally beyond both the lateral edges of the metal trace and the third magnetic layer is laterally within the lateral edges of the second metal trace.

Further to the second embodiments, the power management integrated circuit or the radio frequency integrated circuit further comprises a second inductor inductively coupled to the inductor, the second inductor comprising a second metal trace disposed within at least one second dielectric material, a third magnetic layer adjacent to the at least one second dielectric material, and a fourth magnetic layer adjacent to the at least one second dielectric material, wherein the second metal trace is between at least a portion of the third magnetic layer and at least a portion of the fourth magnetic layer, and wherein the third magnetic layer and the fourth magnetic layer are separated to provide second edge gaps along lateral edges of the second metal trace, wherein the first and third magnetic layers comprise a single continuous magnetic layer.

Further to the second embodiments, the second magnetic layer is laterally within the lateral edges of the metal trace.

Further to the second embodiments, the first magnetic layer and the second magnetic layer have lateral edges that are vertically aligned with the lateral edges of the metal trace.

Further to the second embodiments, the second magnetic layer is laterally within the lateral edges of the metal trace or the first magnetic layer and the second magnetic layer have lateral edges that are vertically aligned with the lateral edges of the metal trace.

Further to the second embodiments, the metal trace comprises copper, a width of the metal trace is in the range of 80 to 350 microns, the thickness of the metal trace is in the range of 4 to 25 microns, and the gap size is not less than the thickness of the metal trace.

In one or more third embodiments, a method for fabricating a magnetic thin film inductor comprises patterning a first magnetic layer over a substrate, disposing a first dielectric layer on the first magnetic layer, disposing a metal trace on the first dielectric layer, disposing a second dielectric layer on the metal trace, and patterning a second magnetic layer over the second dielectric layer, wherein the metal trace is disposed between at least a portion of the first magnetic layer and at least a portion of the second magnetic layer, and wherein the first magnetic layer and the second magnetic layer are separated to provide edge gaps along lateral edges of the metal trace having a gap size not less than one-fourth of a thickness of the metal trace.

Further to the third embodiments, the first dielectric layer comprises a conformal dielectric layer, the second dielectric layer comprises a spin on self planarizing dielectric layer, and the gap size is not less than the thickness of the metal trace.

Further to the third embodiments, the first and second dielectric layers comprise conformal dielectric layers and the method further comprises depositing a third dielectric layer having a planar top surface between the second dielectric layer and the metal trace, wherein the metal trace has first and second lateral edges, and the second magnetic layer has third and fourth lateral edges that are within the first and second lateral edges.

Further to the third embodiments, the first and second dielectric layers comprise conformal dielectric layers, the metal trace has first and second lateral edges, the first magnetic layer extends laterally beyond both the first and second lateral edges, the second magnetic layer extends laterally beyond both the first and second lateral edges, and a portion of a bottom surface of the second magnetic layer is below a top surface of the metal trace.

Further to the third embodiments, the metal trace comprises copper and the first and second magnetic layers both comprise at least one of cobalt zirconium tantalum, iron aluminum oxide, or cobalt iron hafnium oxide.

In one or more fourth embodiments, a mobile computing platform comprises any of the example structures discussed with respect to the first or second embodiments.

It will be recognized that the invention is not limited to the embodiments so described, but can be practiced with modification and alteration without departing from the scope of the appended claims. For example, the above embodiments may include specific combination of features. However, the above embodiments are not limited in this regard and, in various implementations, the above embodiments may include the undertaking only a subset of such features, undertaking a different order of such features, undertaking a different combination of such features, and/or undertaking additional features than those features explicitly listed. The scope of the invention should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

CLAIMS

What is claimed is:

1. A magnetic thin film inductor comprising:

a first magnetic layer over a substrate;

a first dielectric layer over the first magnetic layer;

a metal trace over the first dielectric layer;

a second dielectric layer over the metal trace; and

a second magnetic layer over the second dielectric layer, wherein the first magnetic layer and the second magnetic layer are separated to provide edge gaps along lateral edges of the metal trace having a gap size not less than one-fourth of a thickness of the metal trace.

2. The magnetic thin film inductor of claim 1, wherein the edge gaps extend along the entire lateral edges of the metal trace.

3. The magnetic thin film inductor of claim 1, wherein the first and second magnetic layers each extend laterally beyond both the lateral edges of the metal trace.

4. The magnetic thin film inductor of claim 3, wherein a top surface of the first magnetic layer is entirely below a bottom surface of the metal trace and a bottom surface of the second magnetic layer is entirely above a top surface of the metal trace.

5. The magnetic thin film inductor of claim 3, wherein a top surface of the first magnetic layer is entirely below a bottom surface of the metal trace and a portion of a bottom surface of the second magnetic layer is below a top surface of the metal trace.

6. The magnetic thin film inductor of claim 1, wherein the second magnetic layer is laterally within the lateral edges of the metal trace.

7. The magnetic thin film inductor of claim 1, wherein the first magnetic layer and the second magnetic layer have lateral edges that are vertically aligned with the lateral edges of the metal trace.

8. The magnetic thin film inductor of claim 1, wherein the metal trace comprises copper and the first and second magnetic layers both comprise at least one of cobalt zirconium tantalum, iron aluminum oxide, or cobalt iron hafnium oxide.

9. The magnetic thin film inductor of claim 1, wherein the first and second magnetic layers comprise different magnetic materials.

10. The magnetic thin film inductor of claim 1, wherein at least one of the first magnetic layer, the first dielectric layer, the second dielectric layer, or the second magnetic layer comprises a lamination of multiple materials.

11. The magnetic thin film inductor of claim 1, wherein the metal trace comprises at least one of a linear trace or a curved trace.

12. The magnetic thin film inductor of claim 1, wherein a width of the metal trace is in the range of 80 to 350 microns, the thickness of the metal trace is in the range of 4 to 12 microns, and the gap size is not less than the thickness of the metal trace.

13. A system comprising:

a processor;

a memory coupled to the processor; and

at least one of a power management integrated circuit or a radio frequency integrated circuit including an inductor comprising:

a metal trace disposed within at least one dielectric material; and

a first magnetic layer adjacent to the at least one dielectric material; and

a second magnetic layer adjacent to the at least one dielectric material, wherein the metal trace is between at least a portion of the first magnetic layer and at least a portion of the second magnetic layer, and wherein the first magnetic layer and the second magnetic layer are separated to provide edge gaps along lateral edges of the metal trace having a gap size not less than one-fourth of a thickness of the metal trace.

14. The system of claim 13, wherein the power management integrated circuit or the radio frequency integrated circuit further comprises a second inductor inductively coupled to the inductor, the second inductor comprising:

a second metal trace disposed within at least one second dielectric material; and

a third magnetic layer adjacent to the at least one second dielectric material; and

a fourth magnetic layer adjacent to the at least one second dielectric material, wherein the second metal trace is between at least a portion of the third magnetic layer and at least a portion of the fourth magnetic layer, and wherein the third magnetic layer and the fourth magnetic layer are separated to provide second edge gaps along lateral edges of the second metal trace.

15. The system of claim 14, wherein the first and second magnetic layers each extend laterally beyond both the lateral edges of the metal trace and the third magnetic layer is laterally within the lateral edges of the second metal trace.

16. The system of claim 14, wherein the first and third magnetic layers comprise a single continuous magnetic layer.

17. The system of claim 13, wherein the second magnetic layer is laterally within the lateral edges of the metal trace.

18. The system of claim 13, wherein the first magnetic layer and the second magnetic layer have lateral edges that are vertically aligned with the lateral edges of the metal trace.

19. The system of claim 13, wherein the metal trace comprises copper, a width of the metal trace is in the range of 80 to 350 microns, the thickness of the metal trace is in the range of 4 to 25 microns, and the gap size is not less than the thickness of the metal trace.

20. A method for fabricating a magnetic thin film inductor comprising

patterning a first magnetic layer over a substrate;

disposing a first dielectric layer on the first magnetic layer;

disposing a metal trace on the first dielectric layer;

disposing a second dielectric layer on the metal trace; and

patterning a second magnetic layer over the second dielectric layer, wherein the metal trace is disposed between at least a portion of the first magnetic layer and at least a portion of the second magnetic layer, and wherein the first magnetic layer and the second magnetic layer are

separated to provide edge gaps along lateral edges of the metal trace having a gap size not less than one-fourth of a thickness of the metal trace.

21. The method of claim 20, wherein the first dielectric layer comprises a conformal dielectric layer, the second dielectric layer comprises a spin on self planarizing dielectric layer, and the gap size is not less than the thickness of the metal trace.

22. The method of claim 20, wherein the first and second dielectric layers comprise conformal dielectric layers, the method further comprising:

depositing a third dielectric layer having a planar top surface between the second dielectric layer and the metal trace, wherein the metal trace has first and second lateral edges, and the second magnetic layer has third and fourth lateral edges that are within the first and second lateral edges.

23. The method of claim 20, wherein the first and second dielectric layers comprise conformal dielectric layers, the metal trace has first and second lateral edges, the first magnetic layer extends laterally beyond both the first and second lateral edges, the second magnetic layer extends laterally beyond both the first and second lateral edges, and a portion of a bottom surface of the second magnetic layer is below a top surface of the metal trace.

24. The method of claim 20, wherein the metal trace comprises copper and the first and second magnetic layers both comprise at least one of cobalt zirconium tantalum, iron aluminum oxide, or cobalt iron hafnium oxide.

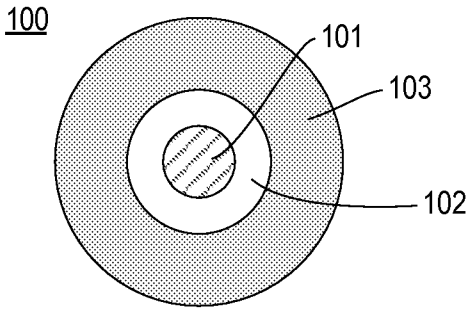

FIG. 1A
(PRIOR ART)

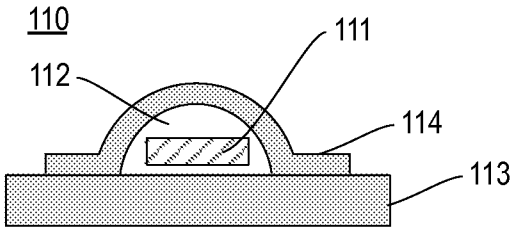

FIG. 1B
(PRIOR ART)

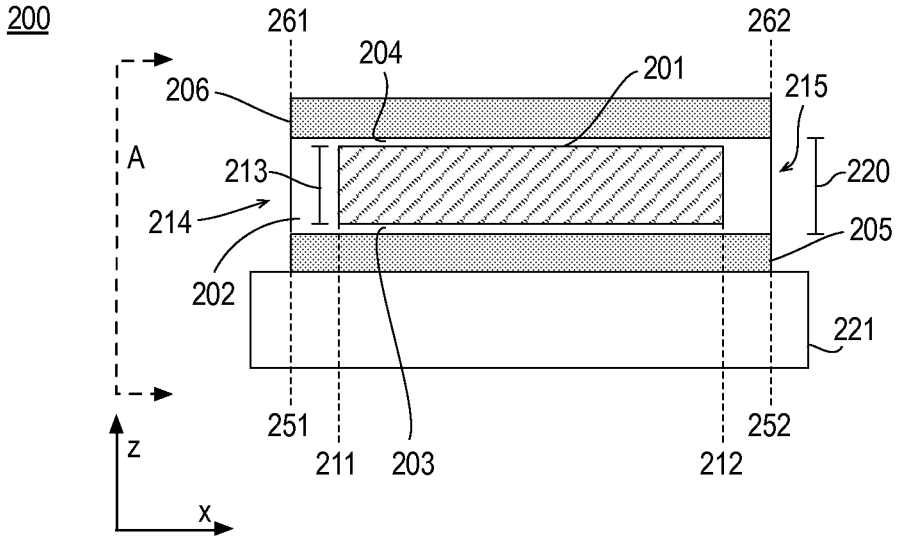

FIG. 2A

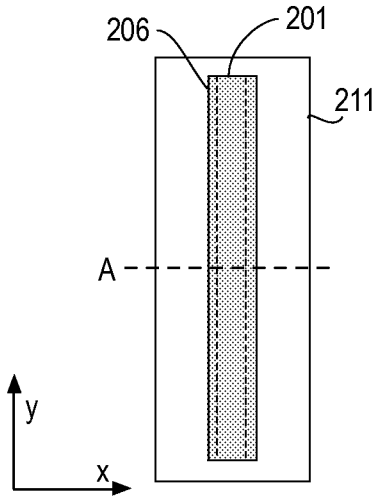

FIG. 2B

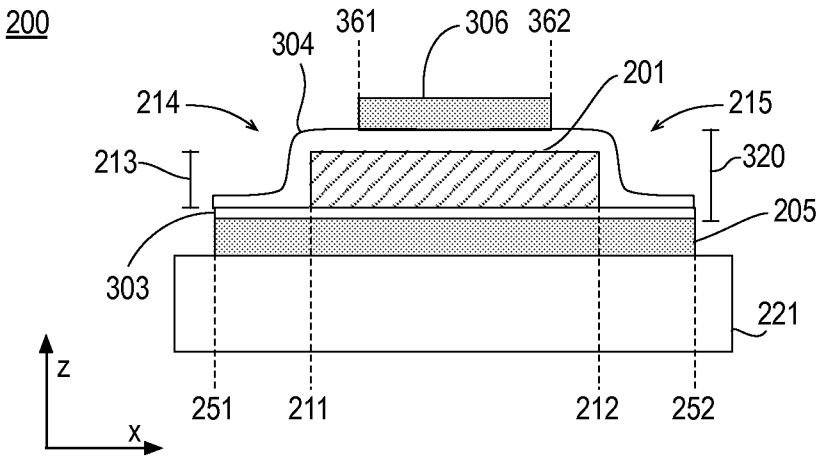

FIG. 3

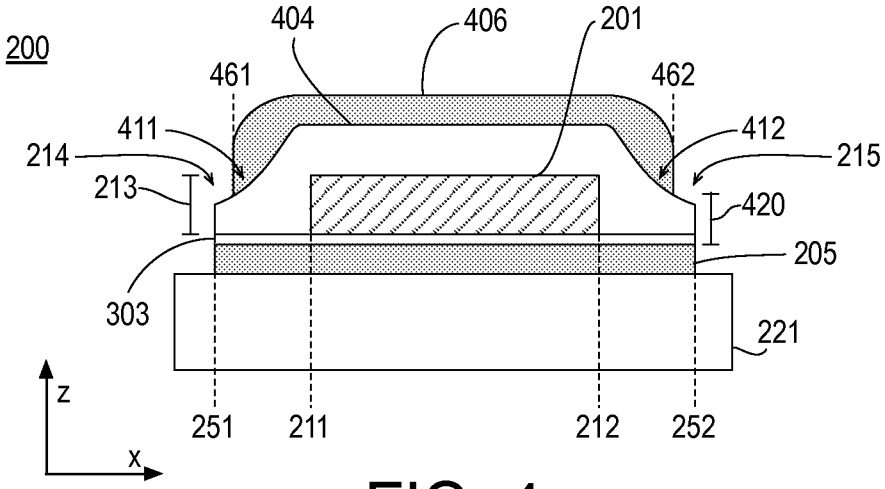

FIG. 4

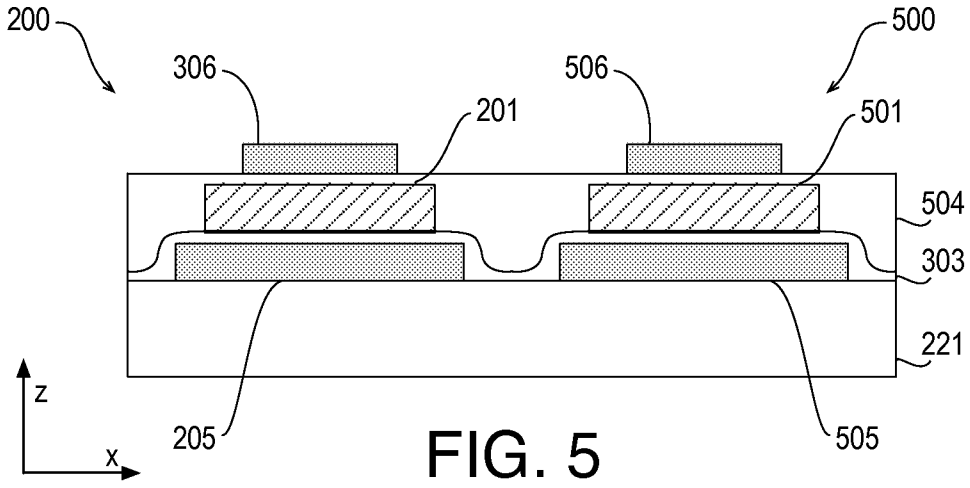

FIG. 5

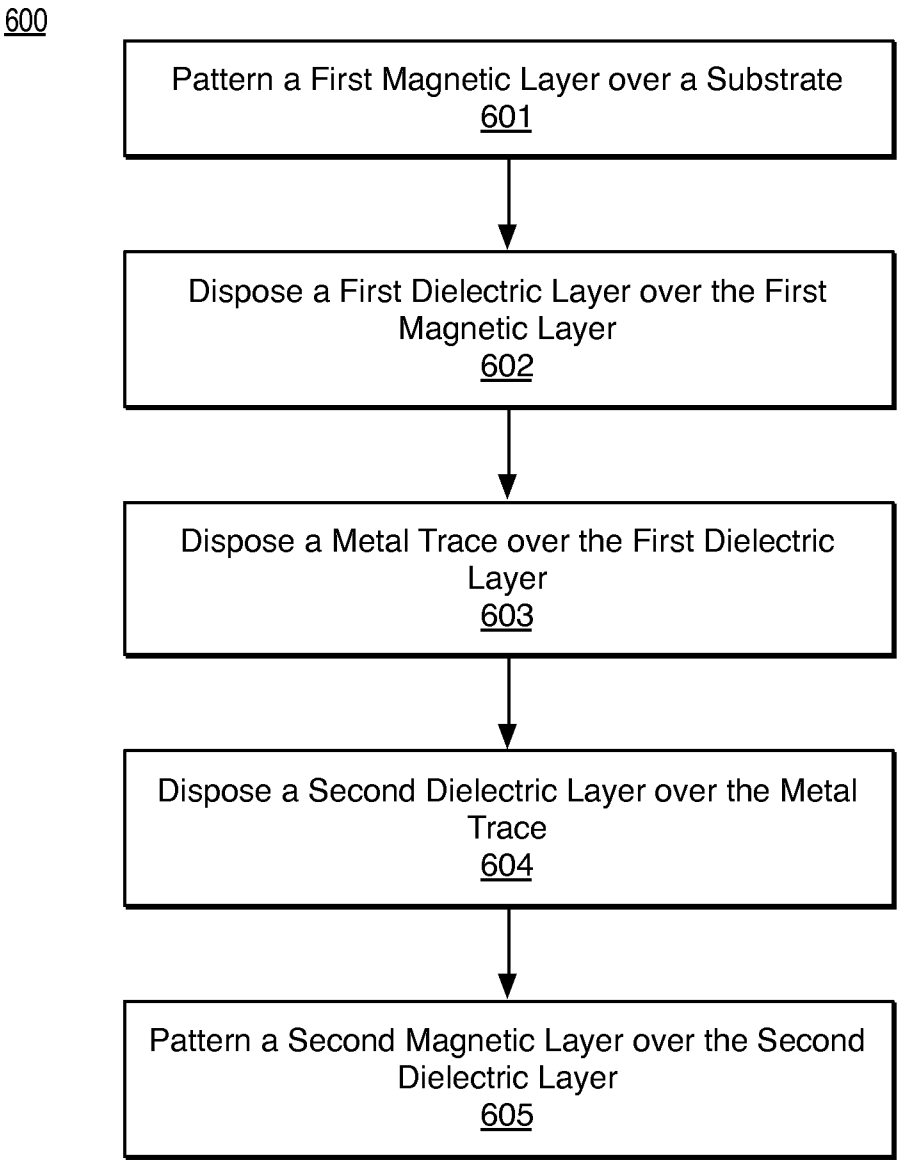
600
Pattern a First Magnetic Layer over a Substrate
601
Dispose a First Dielectric Layer over the First Magnetic Layer
602
Dispose a Metal Trace over the First Dielectric Layer
603
Dispose a Second Dielectric Layer over the Metal Trace
604
Pattern a Second Magnetic Layer over the Second Dielectric Layer
605

FIG. 6

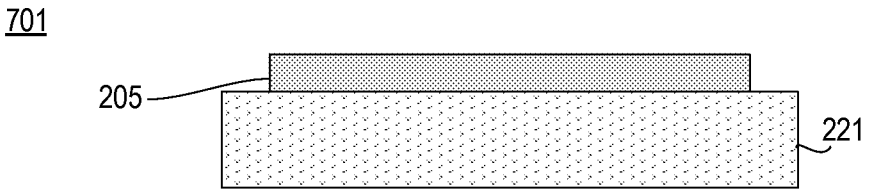

FIG. 7A

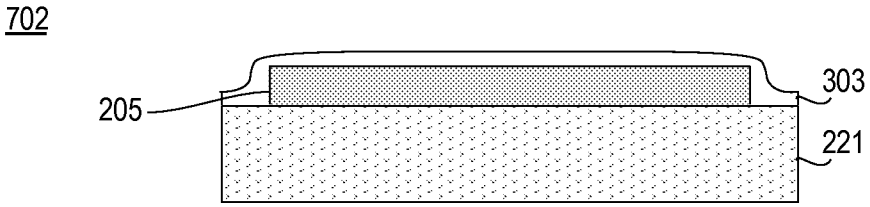

FIG. 7B

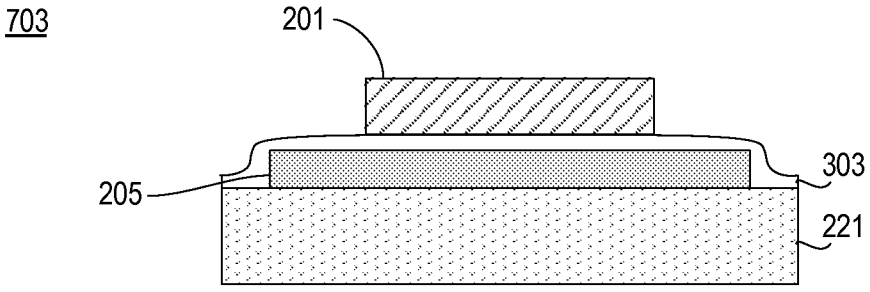

FIG. 7C

704

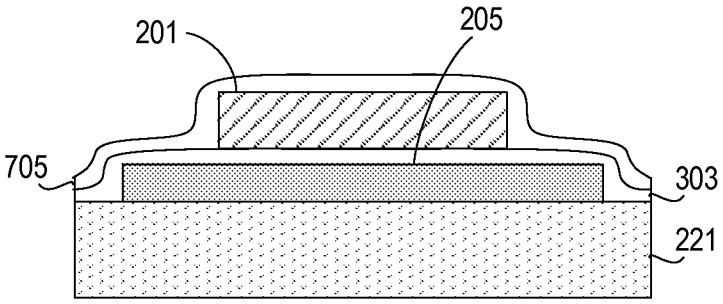

FIG. 7D

706

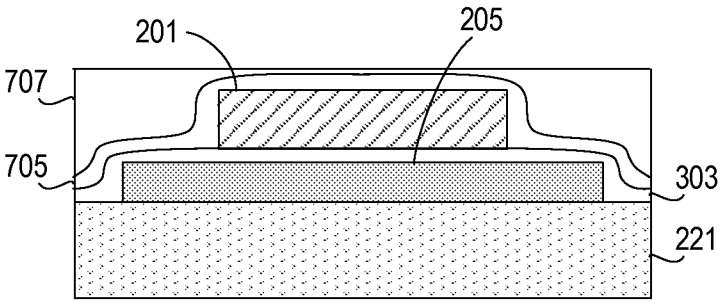

FIG. 7E

708

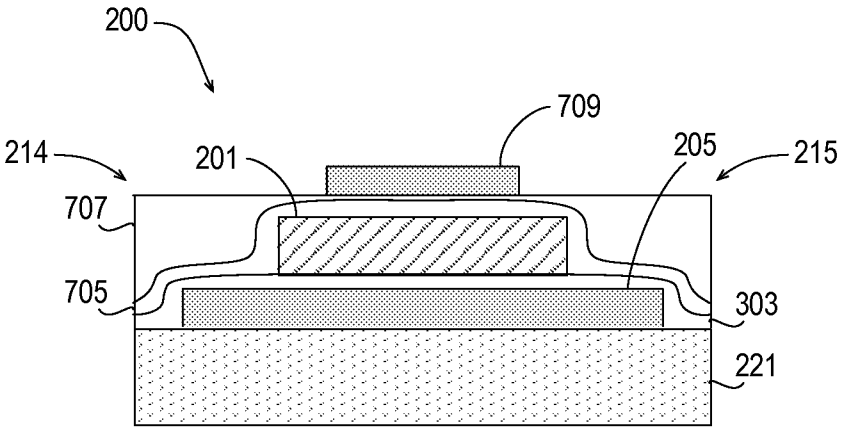

FIG. 7F

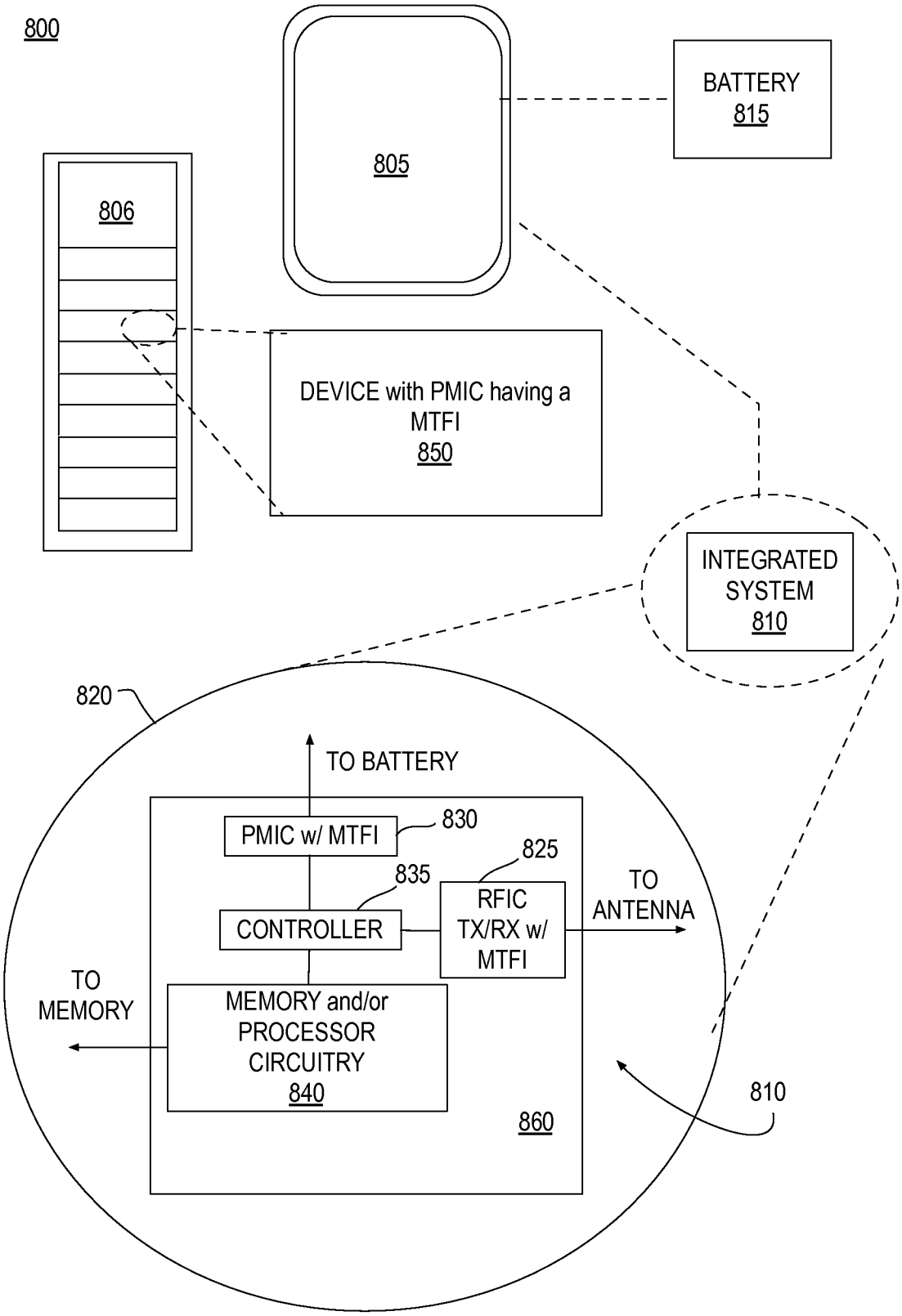
800
805
BATTERY
815
806
DEVICE with PMIC having a MTFI
850
INTEGRATED SYSTEM
810
820
TO BATTERY
PMIC w/ MTFI
830
825
835
RFIC TX/RX w/ MTFI
TO ANTENNA
CONTROLLER
TO MEMORY
MEMORY and/or PROCESSOR CIRCUITRY
840
860
810

FIG. 8

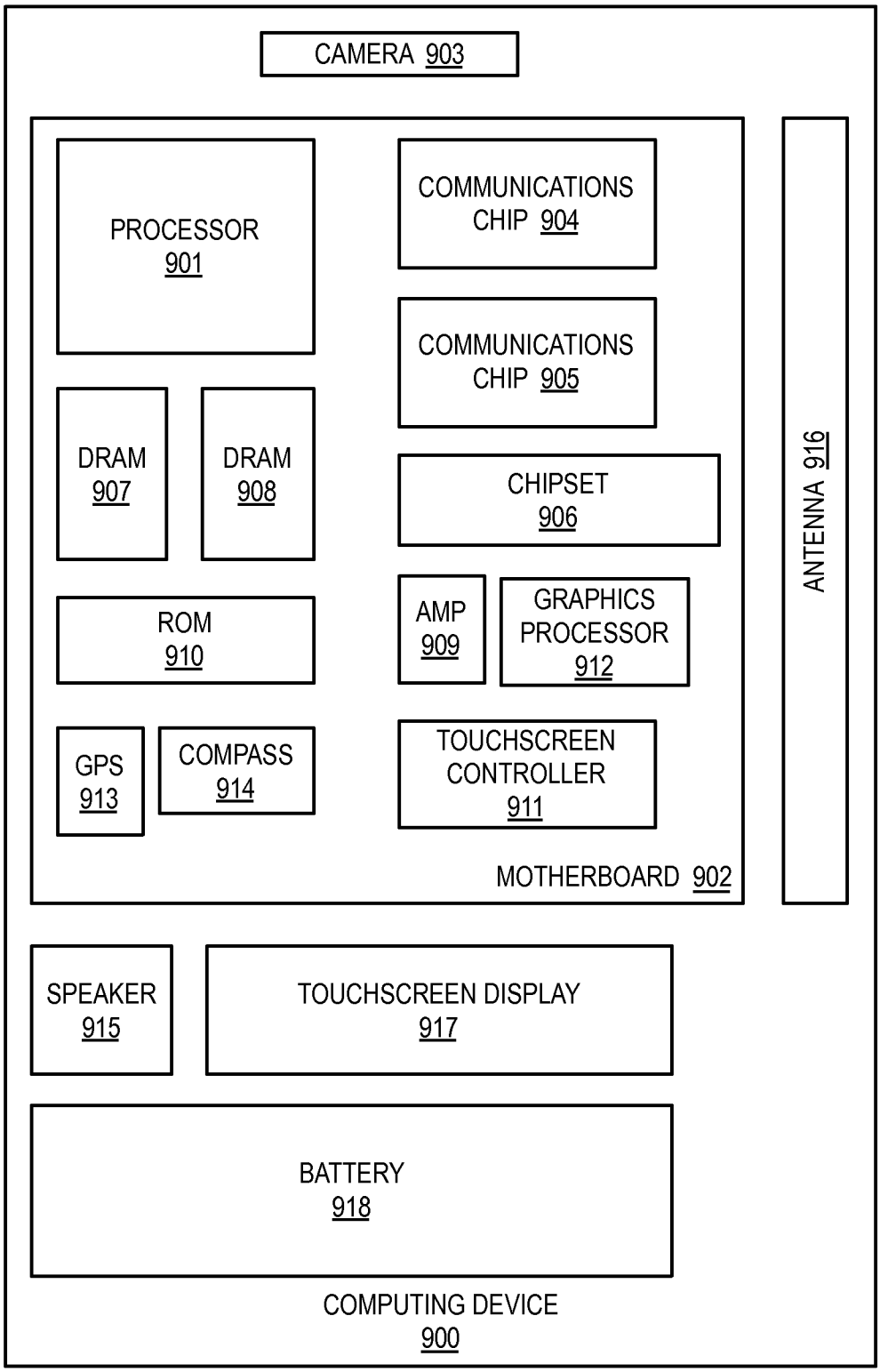
CAMERA 903
PROCESSOR 901
COMMUNICATIONS CHIP 904
COMMUNICATIONS CHIP 905
DRAM 907
DRAM 908
CHIPSET 906
ROM 910
AMP 909
GRAPHICS PROCESSOR 912
GPS 913
COMPASS 914
TOUCHSCREEN CONTROLLER 911
MOTHERBOARD 902
ANTENNA 916
SPEAKER 915
TOUCHSCREEN DISPLAY 917
BATTERY 918
COMPUTING DEVICE 900

FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/051658

A. CLASSIFICATION OF SUBJECT MATTER

HOIF 17/00(2006.01)i, H01F 27/29(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01F 17/00; H01F 17/06; H01F 5/00; G11B 5/39; H01F 10/08; H05K 1/16; H01F 17/04; A61N 2/02; H01F 27/29

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: magnetic thin film inductor, dielectric layer, metal trace, edge gap

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009-0207576 A1 (DONALD S. GARDNER et al.) 20 August 2009 See abstract, paragraphs [0017H0018], [0024H0026], claims 1, 10 and figures 1, 3.	1-9, 12-19
Y		10-11, 20-24
Y	US 6441715 B1 (F. SCOTT JOHNSON) 27 August 2002 See column 2, line 50 - column 3, line 49, claim 1 and figures 1a-2.	11, 20-24
Y	US 5850325 A (DAISUKE MIYAUCHI et al.) 15 December 1998 See column 5, line 25 - column 8, line 62, claim 1 and figure 5.	10
A	JP 10-135040 A (FUJI ELECTRIC CO., LTD.) 22 May 1998 See paragraphs [0016]- [0029], claims 1, 4 and figures 1, 4.	1-24
A	US 2006-0271129 A1 (YU-CHONG TAI et al.) 30 November 2006 See paragraph [0096], claims 1, 37 and figures 2A-2D.	1-24

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 June 2016 (22.06.2016)	**22 June 2016 (22.06.2016)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
KANG, Min Jeong
Telephone No. +82-42-481-8131

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/051658

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2009-0207576 Al	20/08/2009	US 2008-0001699 Al	03/01/2008
		US 7518481 B2	14/04/2009
		US 8108984 B2	07/02/2012
US 6441715 Bl	27/08/2002	US 2002-0097129 Al	25/07/2002
US 5850325 A	15/12/1998	GB 2311889 A	08/10/1997
		JP 09-326105 A	16/12/1997
		JP 3520170 B2	19/04/2004
		US 06047462 A	11/04/2000
JP 10-135040 A	22/05/1998	JP 3580054 B2	20/10/2004
US 2006-0271129 Al	30/11/2006	US 8112157 B2	07/02/2012