

[54] **ELECTRIC FENCE SHOCKER CIRCUIT**

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321/27 R

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209 CD, 241; 123/148 E, 148 F

[57]

ABSTRACT

Two silicon controlled rectifiers (SCRs) whose anode-cathode circuits are coupled in series are simultaneously triggered to discharge a capacitor through a transformer primary to generate shock pulses in an electric fence. One of the SCR's is triggered through a diode and the other is triggered through a capacitor. If either of the SCR's tends to fire early, the other SCR holds the series circuit open until the trigger pulse for the SCR's is applied thereto.

[56] **References Cited**

UNITED STATES PATENTS

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2 Claims, 5 Drawing Figures

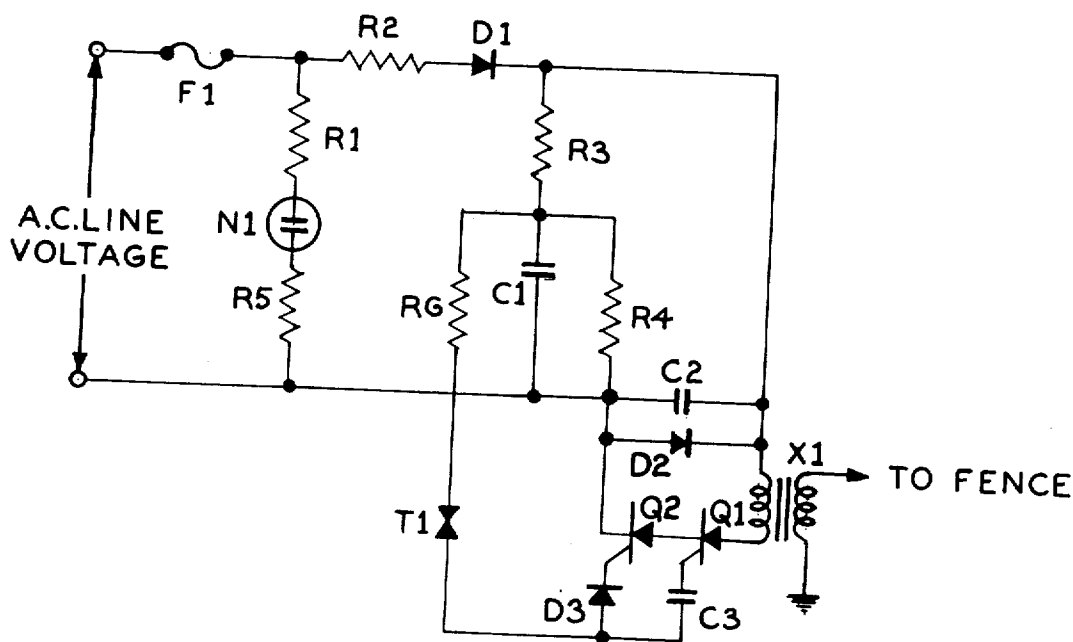


Fig. 1 (PRIOR ART)

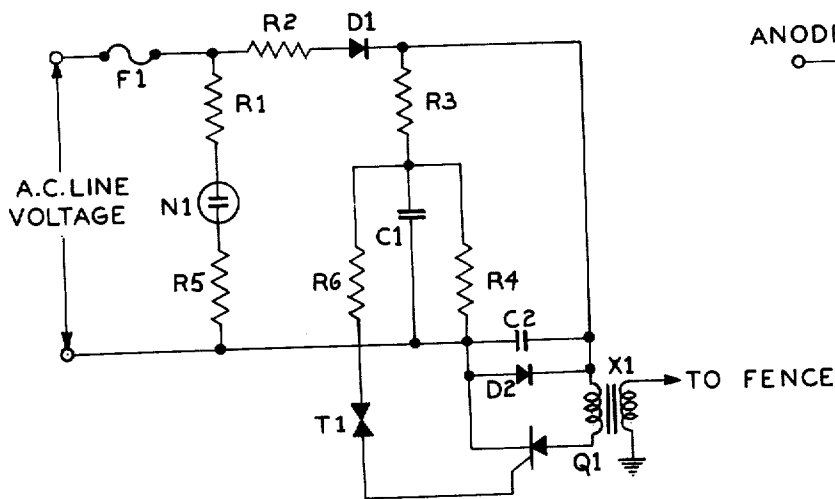


Fig. 2 (PRIOR ART)

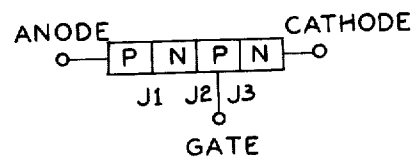


Fig. 3

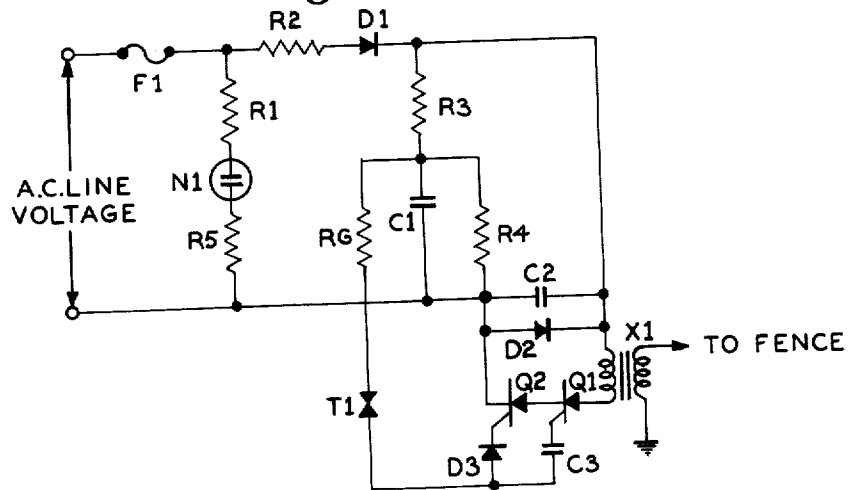


Fig. 4



Fig. 5



ELECTRIC FENCE SHOCKER CIRCUIT

BACKGROUND OF THE INVENTION

This invention relates to electric fence shocker circuits such as used on farms and ranches for keeping animals within a fenced-in area. In the past, a single SCR has been used in such fence shocker circuits to periodically discharge a capacitor through a transformer primarily to generate shock pulses at a rate of approximately 1.1 pulses per second. This pulse repetition rate allows enough time for a shocked animal to move away from the fence with only a single shock after it contacts the fence. However, it is possible for the SCR to suffer what is known as an interim failure mode in which the SCR spontaneously fires before it is triggered. In the interim failure mode, the pulse repetition rate of the SCR may rise to 60 pulses per second, and since the output pulses of the circuit are in the order of 20,000 volts in the open circuit condition, an animal or human touching the fence may be killed or seriously injured by multiple shocks before they can move out of contact with the fence.

The principal object of this invention is to provide an improved SCR circuit in which an interim failure of the SCR will not cause an increase in the pulse repetition rate.

An additional object of this invention is to provide an improved fence shocker circuit which is more reliable in operation than those heretofore known.

Other objects, advantages, and features of the invention will be apparent to those skilled in the art from the description which follows.

SUMMARY OF THE INVENTION

Two SCRs whose anode-cathode circuits are coupled in series are simultaneously triggered on their gate electrodes. One of the SCRs is preferably triggered through a diode and the other is preferably triggered through a capacitor. If either of the SCRs tends to fire early, the other SCR holds the series circuit open until the trigger pulse for the SCRs is applied thereto.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic circuit diagram of a prior art electric fence shocker circuit.

FIG. 2 is a diagrammatic representation of a prior art SCR.

FIG. 3 is a schematic circuit diagram of an improved fence shocker circuit of this invention.

FIG. 4 is a waveform of the voltage across C3 without D3 in the circuit diode.

FIG. 5 is a waveform of the voltage across C3 with D3 in the circuit.

DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 is a schematic circuit diagram of a prior art electric fence shocker circuit. In this circuit, an AC input voltage is rectified by diode D1 and the rectified voltage is applied in parallel to capacitors C1 and C2. Capacitor C1 is the timing capacitor and capacitor C2 is the main pulse charging capacitor. Resistor R2 is a current limiting resistor for both capacitors. Resistors R2 and R3 taken together control the charging time for capacitor C1. When the charge on capacitor C1 reaches a predetermined voltage level, it triggers a bilateral trigger diode T1 and applies a gating pulse to the

gate terminal of SCR Q1, thereby switching SCR Q1 into conduction. Capacitor C2 then discharges through the anode-cathode circuit of SCR Q1 and through the primary winding of voltage step-up transformer X1. The resulting output pulse on the secondary of transformer X1 is coupled to the electric fence. Diode D2 protects capacitor C2 against negative voltage surges due to the inductive kickback of transformer X1. Resistors R1 and R5 are current limiting resistors for a neon lamp N1 which glows whenever the circuit is energized. Resistor R4 is a bleeder resistor for capacitor C1. R6 is a series limiting resistor for T1. F1 is a slow blow fuse for over-current protection.

There are three modes of SCR failure that can affect the foregoing circuit: (1) an open anode-cathode circuit, (2) a shorted anode-cathode circuit, and (3) the interim failure mode in which the SCR fires spontaneously before it is triggered by the trigger pulse from the bilateral trigger diode T1. In the open circuit mode, the circuit is inoperative. In the shorted mode, excessive current flow causes fuse F1 to blow. In the interim mode, the normal turn-on turn-off mechanism of the SCR is no longer operable and the pulse repetition rate increases from 1.1 pulses per second to 60 pulses per second or to an intermediate value between 1.1 and 60 pulses per second. At high pulse repetition rates, the electric fence becomes a lethal weapon capable of killing or causing serious injury to animals and humans. Accordingly, it is highly desirable for the circuit to be protected against the fast firing rates that occur in the interim failure mode. Historical data indicates that approximately 1 in 750 SCRs is a potential candidate for the fast fire interim failure mode. Causes can be traced to poor crystal structure or poor passivation or other faults that cause the SCR to fire prematurely.

As shown in FIG. 2, an SCR has alternate P-type zones and N-type zones which are arranged in a PNPN pattern defining three PN junctions J1, J2, and J3. The outer P-type zone serves as the anode and the outer N-type zone serves as the cathode. The inner P-type zone serves as the gate.

In normal operation, when a forward voltage is initially applied across the SCR's cathode-anode circuit, junctions J1 and J3 will be forward biased and junction J2 will be reverse biased. As long as junction J2 remains reverse biased, the forward current is limited to a low forward leakage current level. When the forward voltage across the SCR's cathode-anode circuit is increased past the avalanche breakdown level for junction J2, or when avalanche breakdown is initiated by injecting current carriers into the gate electrode, junction J2 breaks down and begins to conduct significant levels of current in the reverse direction. Once the avalanche condition is reached, the current increases rapidly, the voltage across junction J2 drops, and the device is turned on. It has entered the high conduction region and will remain there as long as the anode current is greater than a minimum value called the holding current. When the anode current drops below the holding current level, the junction J2 will revert to its reverse biased state, thus turning the device off.

In the interim failure mode, the level of forward voltage required to initiate avalanche breakdown of junction J2 is lowered so that it falls within the normal charging range of capacitor C2, thereby causing the SCR to fire spontaneously before it is triggered. Also, should the holding current deteriorate, in addition to

the above, the fast fire mode may also occur. Thus, instead of firing at the 1.1 pulse per second rate set by the gate pulses, the SCR will fire at a faster rate that falls between 1.1 pulses per second and 60 pulses per second.

FIG. 3 shows the electric fence shocker circuit of this invention in which the circuit is protected against the adverse effects of an interim mode failure by means of an additional SCR Q2 whose cathode-anode circuit is connected in series with the cathode-anode circuit for SCR Q1 and whose gate is coupled in parallel with the gate of SCR Q1. In the circuit of this invention, if either of the SCRs should suffer an interim mode failure, the other SCR will hold the discharge path of C2 open until the trigger pulse from timing capacitor C1 is generated and applied to the gates of Q1 and Q2. Thus, the pulse repetition rate of the circuit does not increase if one of the SCRs should fire prematurely. The pulse repetition rate will be affected if both SCRs should suffer an interim mode failure at the same time, but since the chance of a single interim mode failure is 1 in 750, the chance of a double interim mode failure is only $1 \text{ in } 750 \times 750 = 562,500$.

If the gate terminals of the SCRs Q1 and Q2 were connected together directly, the interim mode failure of one SCR might trigger the other by conduction of charge carriers from the gate electrode of the defective SCR to the gate electrode of the good SCR. To prevent this, the gate electrodes of the two SCRs are isolated from each other by a capacitor C3 connected in series with the gate electrode of SCR Q1 and a diode D3 connected in series with the gate electrode of SCR Q2. Capacitor C3 provides DC isolation between the two gate electrodes. Diode D3 adds to the isolation with respect to negative pulses and extends the recombination time for current carriers in the SCRs, thus aiding in recovery in the junctions of the SCRs. The position of capacitor C3 and diode D3 in the circuit is not interchangeable. The voltage waveform across C3 is shown in FIG. 4 without diode D3 in the circuit. FIG. 5 shows the same waveform with diode D3 in the circuit.

It has been found by experiment that single SCRs which have suffered a fast-fire interim mode failure in the circuit of FIG. 1 may become shorted or open circuited in the circuit of FIG. 3. This is due to the good SCR passing relatively high levels of current through the bad SCR, thus significantly accelerating its total de-

terioration. This is desirable because with an open or short the fast fire problem is eliminated. Further, if C3 or D3 should fail, the probability of the fast fire device taking over the circuit is significantly lessened when the fast fire device fails to change to an open or short.

Although one illustrative example of this invention has been described herein, it should be understood that this invention is not limited to the disclosed embodiment since changes can be made in the disclosed circuit without departing from the basic principles of the invention. For example, although the invention has been described in connection with a fence shocker circuit, it is applicable to any circuit which utilizes an SCR, as, for example, an automobile ignition system. Similar modifications of the disclosed circuit will be apparent to those skilled in the art, and this invention includes all modifications falling within the scope of the following claims.

What I claim is:

1. In an electric fence shocker circuit including a capacitor, a transformer primary winding, and a silicon controlled rectifier, means connecting said capacitor, said transformer primary winding, and the anode-cathode circuit of said silicon controlled rectifier together in series, means for charging said capacitor, and trigger means coupled to the gate electrode of said silicon controlled rectifier for firing the same to discharge the charge on said capacitor through said transformer primary winding, the improvement comprising a second silicon controlled rectifier, means connecting the anode-cathode circuit of both silicon controlled rectifiers together in series, and means coupling trigger pulses to the gate electrodes of both silicon controlled rectifiers, whereby if one of the silicon controlled rectifiers should suffer an interim mode failure, the other silicon controlled rectifier will hold said series circuit open until the gate electrode of said other silicon controlled rectifier is triggered by said trigger means, there being a capacitor connected in series with the gate electrode of one silicon controlled rectifier and a diode connected in series with the gate electrode of the other silicon controlled rectifier.

2. An electric fence shocker circuit as defined in claim 1 wherein said capacitor is connected to the gate electrode of the silicon controlled rectifier nearest to said winding.

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