



- (51) International Patent Classification:
H01L 27/146 (2006.01)
- (21) International Application Number:
PCT/US2016/043929
- (22) International Filing Date:
25 July 2016 (25.07.2016)
- (25) Filing Language:
English
- (26) Publication Language:
English
- (30) Priority Data:

62/196,315	24 July 2015 (24.07.2015)	US
62/200,109	2 August 2015 (02.08.2015)	US
62/204,460	13 August 2015 (13.08.2015)	US
62/205,003	14 August 2015 (14.08.2015)	US

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

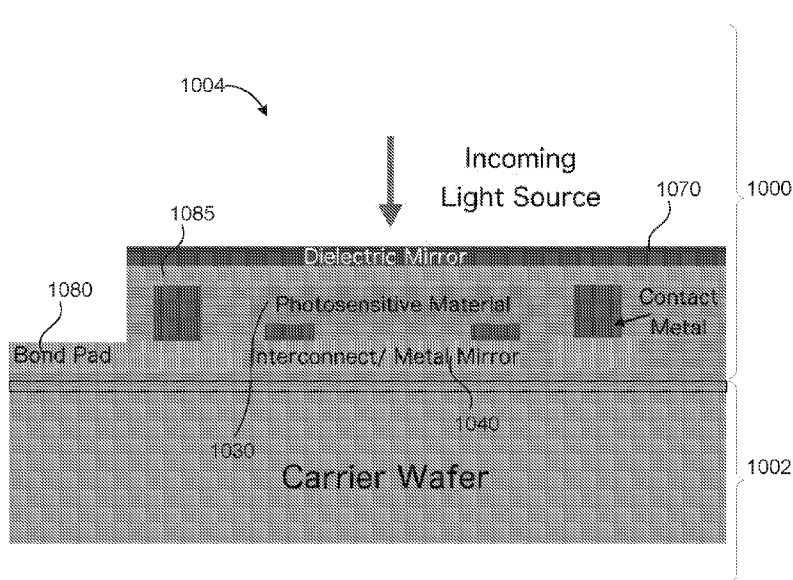
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

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Published:
— with international search report (Art. 21(3))

(54) Title: MULTI-WAFER BASED LIGHT ABSORPTION APPARATUS AND APPLICATIONS THEREOF



(57) Abstract: Structures and techniques introduced here enable the design and fabrication of photodetectors (PDs) and/or other electronic circuits using typical semiconductor device manufacturing technologies meanwhile reducing the adverse impacts on PDs' performance. Examples of the various structures and techniques introduced here include, but not limited to, a pre-PD homogeneous wafer bonding technique, a pre-PD heterogeneous wafer bonding technique, a post-PD wafer bonding technique, their combinations, and a number of mirror equipped PD structures. With the introduced structures and techniques, it is possible to implement PDs using typical direct growth material epitaxy technology while reducing the adverse impact of the defect layer at the material interface caused by lattice mismatch.

FIG. 10C

WO 2017/019632 A1

MULTI-WAFER BASED LIGHT ABSORPTION APPARATUS AND APPLICATIONS THEREOF

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. Provisional Patent Application No. 5 62/196,315, entitled "HIGH SPEED HYBRID WAVEGUIDE-BASED MULTIPLE CHANNEL OPTICAL MODULE," filed July 24, 2015; U.S. Provisional Patent Application No. 62/200,109, entitled "PHOTODETECTOR AND INTEGRATION WITH INTEGRATED CIRCUITS," filed August 2, 2015; U.S. Provisional Patent Application No. 62/204,460, entitled "SILICON GERMANIUM PHOTODIODE," filed August 13, 10 2015; and U.S. Provisional Patent Application No. 62/205,003, entitled "SILICON GERMANIUM PHOTODIODE," filed August 14, 2015; all of which are incorporated by reference herein in their entireties.

TECHNICAL FIELD

[0002] Embodiments of the present disclosure relate to semiconductor device 15 design, and more particularly, to multi-wafer based semiconductor photodetectors and other devices.

BACKGROUND

[0003] Fueled by big data, cloud computing, as well as other computer network and telecommunication applications, there is an ever increasing demand for high 20 speed telecommunication means. High speed optical transmitters and receivers (or collectively referred to herein as "transceivers") that are capable of exceeding a transmission rate of 25 Gbps have attracted the public's attention.

[0004] While optical transceivers are gaining popularity, semiconductor photodetector (PD) design and manufacturing technology is often different and 25 sometimes even incompatible with other kinds of traditional semiconductor device manufacturing technologies, such as those for metal oxide semiconductor (MOS) transistors. As an example, a direct growth of silicon germanium (SiGe) materials on silicon material substrates can often cause a defect layer, laden with lattice mismatch between Ge and Si. This defect layer can result in leakage current and degraded PD 30 performance characteristics (e.g., signal-to-noise ratio (SNR)).

[0005] It is beneficial to have improved device design and fabrication techniques that enable PDs and/or other electronic circuits using typical semiconductor device manufacturing technologies meanwhile reducing the adverse impacts on PDs' performance.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0006] One or more embodiments of the present disclosure are illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar elements. These drawings are not necessarily
10 drawn to scale.

[0007] FIGS. 1A-1C are cross-sectional views of embodiments of a carrier wafer.

[0008] FIGS. 2A-2B are example processes that can be performed on a donor wafer (also referred to as a transfer wafer) for forming photosensitive materials on the
15 donor wafer.

[0009] FIGS. 3A-3C are example processes that can be performed on the donor wafer for passivation bonding layer preparation.

[0010] FIG. 4 is a cross-sectional view of an embodiment after a wafer bonding process, bonding the donor wafer and the carrier wafer together.

20 [0011] FIG. 5 is a cross-sectional view of an embodiment after a post-bonding material removal process.

[0012] FIGS. 6A-6B are embodiments of photodetectors fabricated with components that are formed using techniques introduced here.

25 [0013] FIG. 7 is an alternative example process that can be performed on the donor wafer for forming photosensitive materials on the donor wafer.

[0014] FIG. 8 is a cross-sectional view of an alternative embodiment after a wafer bonding process, bonding the donor wafer and the carrier wafer together.

[0015] FIG. 9 is a cross-sectional view of the alternative embodiment of FIG. 8 after a post-bonding material removal process.

30 [0016] FIGS. 10A-10C are an example flow for bonding a donor wafer and a carrier wafer after forming the photodetectors on the donor wafer.

[0017] FIGS. 11A-11E show an alternative embodiment for bonding a donor wafer and a carrier wafer after forming the photodetectors on the donor wafer.

[0018] FIGS. 12A-12D show a process of forming two alternative embodiments of a photodetector with mirror structures.

[0019] FIGS. 13A-13C show another alternative embodiment of a photodetector with mirror structures and integrated circuits (ICs).

5 [0020] FIG. 14 shows yet another alternative embodiment that includes a through-silicon via (TSV) formed on the carrier wafer.

[0021] FIGS. 15A-15B show two example schemes of integration of front side incidence double mirror photodetectors and integrated circuits.

10 [0022] FIGS. 16A-16B show two alternative example schemes of integration, with integrated circuits bonded on front side incidence double mirror photodetectors.

[0023] FIGS. 17A-17B show two alternative example schemes of integration, with back side incidence photodetectors bonded on integrated circuits.

[0024] FIGS. 18A-18B show two additional examples of front side incidence single mirror photodetectors and their integration applications.

15 [0025] FIG. 19 shows a cross-sectional view of a waveguide structure that can be utilized with the photodetectors introduced here.

[0026] FIG. 20 shows an example schematic of a waveguide system embodying one or more techniques introduced here.

20 [0027] FIG. 21 shows an example schematic of another waveguide system embodying one or more techniques introduced here.

[0028] FIGS. 22A-22B show examples of multi-channel receiver modules that can be realized with embodiments of the present disclosure.

DETAILED DESCRIPTION

25 [0029] Germanium (Ge) based or silicon germanium (SiGe) based optical sensors (e.g., photodetectors or photodiodes (generally referred to as PD herein), avalanche photodiodes (APD), or image sensors) have long been applauded for their better sensitivity to near infra-red (NIR) wavelength optical signals. In addition, SiGe based material systems are relatively compatible to contemporary, high volume
30 complementary metal oxide semiconductor (CMOS) manufacturing technologies, and therefore the integration potentials with integrated circuits of such material systems are much favored. With the advancement in Ge epitaxy technology, direct growth of $\text{Si}_x\text{Ge}_{1-x}$ (where $0 \leq x < 1$) materials on silicon (Si) material substrates have become

popular. (Note that $\text{Si}_x\text{Ge}_{1-x}$ (where $0 \leq x < 1$) here includes all suitable SiGe composition combinations from 100% Ge to almost 100% Si.)

[0030] However, it is observed that, due to a large lattice mismatch (i.e., about 4%) between Ge and Si, a dense defect layer typically can form near the interface of the Si substrate and deposited $\text{Si}_x\text{Ge}_{1-x}$ film to relax the strain energy generated from this large lattice mismatch. This dense defect layer is typically at least 30 nm in thickness and is highly dependent on the Ge content of the film. The large number of defects can act as carrier generation and recombination centers if these defects are located within or close to the electrical fields or intrinsic regions of the PD devices, which can severely increase the leakage current of such devices. This leakage current in PD, also known as the "dark current," is a major source of noise current for PDs that can severely degrade a photodetector's signal-to-noise (SNR) ratio. This relatively high threading dislocation density (TDD) issue makes Ge or $\text{Si}_x\text{Ge}_{1-x}$ based photodiodes' dark current characteristics inferior when compared to competing photodiode materials systems such as pure silicon and III-V materials (e.g., GaAs or InGaAs). The magnitude of dark current have been shown to be positively correlated with the TDD. Furthermore, the high TDD layer has been observed to be horizontally conductive, posing detrimental effects to device performance if the direction of the device's primary current flow coincided with the horizontal direction of the high TDD layer. There has been attempts to use germanium substrate wafers to form the high quality germanium material layer that is to be transferred to other wafers. Yet, generally speaking, germanium substrate wafers are expensive, limited in size and difficult to handle due to its fragile nature, therefore making such approach difficult to scale for production.

[0031] Accordingly, introduced here are a number of device design and fabrication techniques that enable PDs and/or other electronic circuits using typical semiconductor device manufacturing technologies meanwhile reducing the adverse impacts on PDs' performance. Examples of the various techniques introduced here include, but not limited to, a pre-PD homogeneous wafer bonding technique, a pre-PD heterogeneous wafer bonding technique, a post-PD wafer bonding technique, a number of multi-stack PD device structures, as well as other structures and techniques related to integration and optoelectronic-related applications. With the introduced techniques, it is possible to fabricate PDs and/or other electronic circuits using typical

semiconductor device manufacturing technologies, such as direct growth of $\text{Si}_x\text{Ge}_{1-x}$ on Si substrate, while reducing the adverse impacts of the leakage current caused by the dense defect layer on PDs' performance.

[0032] In the following description, the example of a Si/SiGe material system PD is used, for illustrative purposes only, to explain various techniques that can be implemented for manufacturing the PD using typical direct growth material epitaxy technology while reducing the adverse impact of the defect layer at the material interface caused by lattice mismatch. Note, however, that the techniques introduced here are not limited in applicability to any particular kind of PD and/or transistors. For example, even though one or more figures introduced in connection with the techniques disclosed here (e.g., FIGS. 10A-10C, 15A-15B, and 16A-16B) illustrate a front side incidence double mirror PD structure, the techniques are applicable in a similar manner to other types of PD structure including, but not limited to, a single mirror PD structure, a back side incidence PD, or any suitable combination thereof.

[0033] For purposes of discussion herein, a PD is a semiconductor apparatus that converts an optical signal into a photo-generated electrical signal. Examples of PD devices include a P-I-N photodiode, an avalanche photodiode (APD), a uni-traveling carrier photodiode, or an image sensor (including, for example, a near-infrared (NIR) sensor). A typical P-I-N diode includes two highly-doped semiconductor layers with opposite electrical polarity (i.e., one "p-type" and one "n-type") and a photon absorption layer (i.e., "intrinsic") sandwiched in between the two layers. In the context of P-I-N PDs, the term "highly-doped" typically may be understood as having a doping concentration above 10^{18} cm^{-3} ; the term "intrinsic" typically may be understood as having a doping concentration below 10^{17} cm^{-3} in $\text{Si}_x\text{Ge}_{1-x}$ material systems.

[0034] Further, in the following description, numerous specific details are set forth to provide a thorough understanding of the present disclosure. It will be apparent to one skilled in the art that the techniques introduced here may be practiced without these specific details. In other instances, well-known features, such as specific fabrication techniques, are not described in detail in order to not unnecessarily obscure the present disclosure. References in this description to "an embodiment," "one embodiment," or the like, mean that a particular feature, structure, material, or characteristic being described is included in at least one embodiment of the present

disclosure. Thus, the appearances of such phrases in this specification do not necessarily all refer to the same embodiment. On the other hand, such references are not necessarily mutually exclusive either. Furthermore, the particular features, structures, materials, or characteristics may be combined in any suitable manner in one or more embodiments. Also, it is to be understood that the various exemplary embodiments shown in the figures are merely illustrative representations and are not necessarily drawn to scale.

[0035] The terms “coupled” and “connected,” along with their derivatives, may be used herein to describe structural relationships between components. It should be understood that these terms are not intended as synonyms for each other. Rather, in particular embodiments, “connected” may be used to indicate that two or more elements are in direct physical or electrical contact with each other. Unless otherwise made apparent in the context, the term “coupled” may be used to indicate that two or more elements are in either direct or indirect (with other intervening elements between them) physical or electrical contact with each other, and/or that the two or more elements co-operate or interact with each other (e.g., as in a cause and effect relationship).

[0036] The terms “over,” “under,” “between,” and “on” as used herein refer to a relative position of one material layer with respect to other material layers. As such, for example, one layer disposed “over” or “under” another layer may be directly in contact with the other layer or may have one or more intervening layers. Moreover, one layer disposed “between” two layers may be directly in contact with the two layers or may have one or more intervening layers. In contrast, a first layer “on” a second layer is in contact with that second layer. Additionally, the relative position of one layer with respect to other layers is provided assuming operations are performed relative to a substrate without consideration of the absolute orientation of the substrate. The term “atop” means “on the top of.”

[0037] Similarly, the terms “above” and “below” are generally used herein for describing the relative physical location of different devices, layers, sections, portions, etc., with respect to their shortest distances to the semiconductor substrate. For example, a first layer “above” a second layer means that, when measured from the substrate at the same horizontal level, the first layer is farther away in distance from the substrate than the second layer. Conversely, a first layer “below” a second layer

means that, when measured from the substrate at the same horizontal level, the first layer is closer in distance from the substrate than the second layer. As used herein, "horizontal" means parallel to the planar surface of the substrate, such as the horizontal axis 101 illustrated in FIG. 1A.

5 [0038] The terms "front side" and "back side" are used in a relative sense, from the perspective of an individual object that the terms modify or otherwise describe. As such, the terms "front side" and "back side" do not indicate an absolute direction; rather, the direction being referred to depends on the object that the term "front side" or "back side" modifies. For example, a "back side" of a donor wafer (e.g., wafer 100,
10 FIG. 1A) may eventually become a "front side" of the resulting PD structure (e.g., structure 400, FIG. 4).

[0039] The term "immediately" or "directly" may be construed as "in physical contact," as will be made apparent by the context; for example, unless contradictory to the context, a first layer "immediately above" or "directly above" a second layer means
15 that the first layer is above and in physical contact with the second layer.

[0040] As used herein, "contact plug," "contact via," or simply "contact" for a device refers to any substantially vertical wire between with the doped regions for the device and the first interconnect layer for the device. The term "interconnect" refers to any substantially horizontal wire between devices for inter-device signal
20 transmission/communication. The "first" interconnect layer refers to the lowest interconnect layer. Notably, with the techniques introduces here, the first interconnect layer is device specific; that is to say, in some embodiments, the first interconnect for one device may be different than that for another device, even when both devices are fabricated on the same wafer.

25 PRE-PD HOMOGENEOUS BONDING

[0041] FIGS. 1A-1C are cross-sectional views of embodiments 100, 102, and 104 of a carrier wafer. To reduce or even completely avoid the aforementioned leakage current issue caused by the dense defect layer, one approach is to first prepare high quality $\text{Si}_x\text{Ge}_{1-x}$ on a substrate of a donor wafer (may also be referred to
30 herein as a transfer wafer), and then transfer the high quality material to a separate Si material substrate via "wafer bonding" to a carrier wafer. The introduced fabrication technique involves wafer bonding of at least two wafers: a donor (transfer) wafer, and a carrier wafer. The donor wafer is a substrate wafer with the high quality

photosensitive material layers to be transferred. The carrier wafer is a substrate wafer to which the desired transfer material is to be transferred. Note that the term "donor wafer" and "carrier wafer" are used in a relative sense. It is possible to combine the pre-PD wafer bonding techniques (e.g., pre-PD homogeneous wafer bonding or pre-PD heterogeneous wafer bonding) with other suitable wafer bonding techniques (e.g., the post-PD wafer bonding) introduced here; therefore, there may exist multiple carrier wafers if multiple wafer bonding steps are implemented in a certain application.

[0042] In FIG. 1A, the prepared carrier wafer 100 is a silicon (Si) wafer. The carrier wafer 100 can be doped with N-type dopants 110 at the surface of the wafer 100. The doped layer 110 can be accomplished by various known methods, such as implantation, or in-situ doping and diffusion. In one or more examples, the carrier wafer may not be doped with impurities, such as the carrier wafer 102 shown in FIG. 1B. Alternatively, as shown in FIG. 1C, the carrier wafer 104 may be of a silicon-on-insulator (SOI) type. Each carrier wafer can be doped differently, in terms of the doping profile and the impurity type, according to a desired photodiode design.

[0043] FIGS. 2A-2B are example processes that can be performed on a donor wafer 200 for forming photosensitive materials 210 on the donor wafer 200.

[0044] In the embodiment shown in FIG. 2A, the donor wafer 200 includes an optional separation layer 220 within the Si donor wafer 200. The exact depth of the separation layer 220 may vary according to the PD design. The separation layer 220 may be created by, for example, hydrogen implantation and/or impurity implantation. The doping profile of the donor wafer 200 can be customized to a specific PD design. Note that if a hydrogen implantation approach is used to form the separation layer 220, then the hydrogen implantation approach should be applied after the photosensitive materials are formed.

[0045] Then, the photosensitive material layer 210 that contains the main target of the transfer can be formed by epitaxial growth. In this example, the photosensitive material includes germanium (Ge). The Ge layer 210 can be formed by blanket epitaxy growth or selective epitaxy growth. As discussed above, a direct epitaxial growth of Ge on top of Si may result in a defect layer 212 high in threading dislocation density (TDD) due to a 4% lattice mismatch between Si and Ge materials. This dense defect layer 212 is typically at least 30 nm in thickness. As the material continues to

grow above the high TDD Ge layer 212, the Ge material quality typically improves significantly.

[0046] In accordance with a number of embodiments, the layers that are the actual target of the transfer in the photosensitive material layer 210 include a pure Ge layer 216 and two $\text{Si}_x\text{Ge}_{1-x}$ layers 214 and 218. The $\text{Si}_x\text{Ge}_{1-x}$ layers may be formed unintentionally by thermal-induced intermixing or intentionally for various purposes including, for example, as an etch/polish stop, a diffusion barrier, a TDD blocking layer, a quantum well, and/or for bandgap engineering purposes. The dimension and other properties of the photosensitive material layers 214, 216, and 218 may be configured according to the photodiode device design of choice. Additionally, the epitaxially grown layer 210 may be annealed at a high temperature (e.g., between 700 °C to 900 °C) after the growth to improve crystal quality. Note that the definition of $\text{Si}_x\text{Ge}_{1-x}$ (where $0 \leq x < 1$) layer naturally include the pure Ge layer; therefore, it should be understood that the term $\text{Si}_x\text{Ge}_{1-x}$ layer should encompass all Ge layers that are grown on Si. However, for purposes of easier illustration, $\text{Si}_x\text{Ge}_{1-x}$ layers having different Si/Ge ratios are shown as different layers. Therefore, a person having ordinary skills in the art should understand that these layers are illustrated in a relative sense, and that there may not be an exact boundary between given two consecutive $\text{Si}_x\text{Ge}_{1-x}$ layers.

[0047] In the embodiment of donor wafer 202 shown in FIG. 2B, the photosensitive material layer 210 include only one $\text{Si}_x\text{Ge}_{1-x}$ layer 214, but include a P doped Ge layer 215 between the $\text{Si}_x\text{Ge}_{1-x}$ layer 214 and the Ge layer 216. As discussed, the $\text{Si}_x\text{Ge}_{1-x}$ film(s) may be doped to certain doping profiles according to desired device designs. It is noted that, in some variations, the high TDD Ge Layer 212 may not necessarily exist. In other variants, the separation layer 220 and the one or more $\text{Si}_x\text{Ge}_{1-x}$ layers may not be present. Additionally or alternatively, there may be more than one $\text{Si}_x\text{Ge}_{1-x}$ layer of various "x" values present, and/or the $\text{Si}_x\text{Ge}_{1-x}$ layer may be a film of continuously graded "x" value. In yet some other embodiments, the photosensitive material layer 210 may be formed on or sourced from a germanium-on-insulator (GOI) wafer or a Ge substrate wafer.

[0048] FIGS. 3A-3C are example processes that can be performed on the donor wafer for passivation bonding layer preparation.

[0049] In the embodiment shown in FIG. 3A, an amorphous Si layer 230 ("a-Si") is deposited on the $\text{Si}_x\text{Ge}_{1-x}$ film layer 218's surface as a passivation layer. Specifically, the a-Si layer 230 is to be formed on the separately prepared $\text{Si}_x\text{Ge}_{1-x}$ layer 218's surface prior to the wafer bonding. Example thickness for this a-Si layer 230 can be from 20 nm to 2 μm . In one example, the thickness of the a-Si layer 230 is around 50 nm to 100 nm. Besides a-Si, other materials for the passivation layer 230 can include poly-crystalline Si, single-crystalline Silicon, or any suitable combination thereof. Note that depositing single or poly crystalline Si passivation layers over Ge could as well lead to TDD formation due to the 4% lattice mismatch. However, the formed TDD in this particular case would be located mainly inside the Si passivation layer 230 rather than the Ge photosensitive layer 210, and therefore the TDD formed here has a much less impact to the PD's performance compared to those defects located inside the Ge photosensitive layer 210.

[0050] Furthermore, this a-Si layer 230 and the $\text{Si}_x\text{Ge}_{1-x}$ layer 218 can be both implanted with dopants, such as phosphorus (P), arsenic (As), antimony (Sb) for N-type dopants, or boron (B) for P-type dopants. The implantation depth of the dopants may vary as needed by the device design. The implanted dopants can be activated processes such as rapid thermal annealing (RTA). Note that the a-Si passivation layer 230 may change into poly-crystalline Si during doping activation.

[0051] After the passivation layer 230 is formed atop of the photosensitive material layer 210, the smoothness of the top surface of the a-Si passivation layer 230 should be maintained for a successful wafer bonding process later. Other processes can also be performed to the donor wafer prior to the wafer bonding process to improve the material quality and/or enhance the wafer bonding process if needed. For example, according to one or more embodiments, the bonding surface should be smooth for better wafer bonding results. These processes may include, but not limited to, impurity doping, wafer polishing, capping layer forming, laser annealing, and/or pattern etching.

[0052] With simultaneous reference to FIG. 1A, in the embodiment shown in FIG. 3A, the bonding surface material layer 230 is deliberately selected to be of the same doping type as the surface layer 110 of the carrier wafer 100, that is, "N-type" a-Si layer 230 to "N-type" Si layer 110 bond. This type of bonding is desirable because high level of common type doping can prevent a photodiode depletion region (or

"quasi-neutral region") from extending into the defective interface-layer, which is a main reason for the detrimental device leakage current to incur at the defect sites.

[0053] There are several advantages of this passivation layer formation introduced here. It has been demonstrated that device leakage current can be reduced by applying passivating materials to $\text{Si}_x\text{Ge}_{1-x}$ surface. Here, the a-Si layer 230 may serve as a passivation layer for the $\text{Si}_x\text{Ge}_{1-x}$ material surface 218. This can generally reduce surface dangling bonds, thereby reducing device leakage current. The Si material is also more stable than the $\text{Si}_x\text{Ge}_{1-x}$ material (especially for high Ge contents), and therefore the technique introduced here changes the bonding interface from " $\text{Si}_x\text{Ge}_{1-x}$ to Si" to "Si to Si," thereby simplifying the wafer bonding process as well as improving the bonding results. In addition, the bonding surface (i.e., the resulting material interface layer after the bonding) will not be in direct contact with the $\text{Si}_x\text{Ge}_{1-x}$ material layers that are critical to device performance, thereby reducing or avoiding common negative impacts to device performance, yield, and reliability, that are induced by interface layer bonded with heterogeneous materials.

[0054] In some alternative embodiments, the a-Si layer 230 may be partially or entirely replaced by any semiconductor material that is not $\text{Si}_x\text{Ge}_{1-x}$ while possessing passivation effects to the $\text{Si}_x\text{Ge}_{1-x}$ surface. An example of such semiconductor material is gallium arsenide (GaAs) with lattice matched to Ge.

[0055] FIGS. 3B and 3C show two additional embodiments. In FIG. 3B, the carrier wafer is a Ge substrate wafer and there is no $\text{Si}_x\text{Ge}_{1-x}$ surface. Instead, the a-Si passivation layer 230 is formed on a N-doped Ge layer 219. In FIG. 3C, the carrier wafer is a GOI wafer and there is no $\text{Si}_x\text{Ge}_{1-x}$ surface or separation layer. Similar to the embodiment shown in FIG. 3B, the a-Si passivation layer 230 is formed on a N-doped Ge layer 219. The buffered oxide (BOX) layer in the GOI wafer can serve as the separation layer. More specifically, in some examples, the BOX layer can serve as an etching stop layer during post-bonding material removal processes. Notably, in these alternative embodiments, there is no high TDD Ge layer 212 since there is no direct growth of Ge on Si.

[0056] FIG. 4 is a cross-sectional view of an embodiment 400 after a wafer bonding process that bonds the donor wafer 200 and the carrier wafer 100 together. As illustrated in FIG. 4, the Si donor wafer 200 is flipped up-side-down, and then wafer bonded to the Si carrier wafer 100. In various embodiments, both the donor wafer

200's bonding surface and the carrier wafer 100's bonding surface should be smooth for successful wafer bonding. As discussed above, material layers similar to the passivation layer 230 may be deposited on the surface of the carrier wafer 100 if needed. The wafer bonding process may include, but not limited to, dry wafer bonding, wet wafer bonding, chemical wafer bonding, direct bonding, plasma activated bonding, or surface activated bonding. In some embodiments, a number of thermal or pressurized processes may be applied to enhance bonding strength of the wafers. In some embodiments, the Si carrier wafer may be patterned before the bonding, depending on the design.

10 [0057] It is noted that the technique introduced above may correspond to a set of unique structure orientations that include: a layer of Si material (e.g., amorphous Si, poly-crystalline Si, single crystalline Si, or a combination thereof) between a single-crystalline $\text{Si}_x\text{Ge}_{1-x}$ layer and a single-crystalline Si material substrate; and/or a layer of semiconductor material that is not $\text{Si}_x\text{Ge}_{1-x}$, between a single-crystalline $\text{Si}_x\text{Ge}_{1-x}$ layer and a single-crystalline Si material substrate.

15 [0058] FIG. 5 is a cross-sectional view of an embodiment 500, which is the embodiment 400 after a post-bonding material removal process.

[0059] In the embodiment shown in FIG. 5, the Si substrate from the donor wafer 200 has been removed. Material removal may be accomplished by, for example, wafer splitting, chemical etching, chemical-mechanical-polish (CMP) or wafer lapping. The separation layer 220 (see FIG. 2A) can function as a stop layer such that a faster but coarser-grain material removal process (e.g., CMP) can be first applied, and then a slower but finer-grain material removal process (e.g., chemical etching with high selectivity chemicals) can be used thereafter.

25 [0060] As shown in FIG. 5, the high TDD Ge layer 212 is also removed. This layer 212's removal is optional depending on the quality of the transfer film (e.g., generally, the photosensitive $\text{Si}_x\text{Ge}_{1-x}$ material layers 210). It is noted, nonetheless, that the ability to remove the high TDD Ge layer 212 can alleviate the leakage current issue of the PD devices, and therefore is considered one of the major benefits that the current technique provides. For the removal of the high TDD Ge layer 212, the $\text{Si}_x\text{Ge}_{1-x}$ layer 214 may be used as an etch/polishing stop layer. Optionally, the $\text{Si}_x\text{Ge}_{1-x}$ 214 is removed, such as shown in FIG. 5. Whether to remove this layer 214 depends on device design. In some implementations, the high TDD Ge layer 212 may

be removed, for example, by applying laser annealing techniques to recover this highly defective region.

[0061] FIGS. 6A-6B are embodiments of photodetectors fabricated with components that are formed using techniques introduced here. With the structure created in FIG. 5, PD with high quality photosensitive materials and without the high TDD Ge layer 212 can be fabricated.

[0062] In the embodiment shown in FIG. 6A, an isolated "island" shape structure, called "mesa," is etched on the embodiment 500 to create the main photodiode structure for PD 600. P-type dopants are implanted into the top surface of the photodiode mesa forming a P Ge layer 610 for the P contact, thereby creating a P-I-N photodiode structure. As shown in FIG. 6A, a passivation layer 620 may be optionally applied to cover the PD 600's photodiode mesa. The passivation layer 620 can include, but not limited to, a-Si, poly-crystalline Si, single crystalline Si, silicon oxide, silicon nitride, aluminum oxide, or any combination thereof. Thereafter, a dielectric layer 630 is deposited and planarized. Contact vias 640 are then formed, filled with contact materials (e.g., metal). Next, one or more anti-reflection coating (ARC) layers (not shown for simplicity) may be formed on top of PD 600 to improve quantum efficiency. In some implementations, the passivation layer 620 can be formed after the formation of the dielectric layer 630. In these implementations, the dielectric layer 630 can be formed, for example, either before or after the wafer bonding process described above. Note that, in these examples, the passivation layer 620 may not exist between the interface of dielectric layer 630 and the N-Si layer 110.

[0063] Shown in FIG. 6B is an alternative PD embodiment 602 where the polarity of the photodiode is the opposite of PD 600. Other PD variants include different doping profiles and/or different layer structures within the transfer film.

PRE-PD HETEROGENEOUS BONDING

[0064] FIG. 7 is an alternative example process that can be performed on the donor wafer for forming photosensitive materials on the donor wafer. In the alternative process, the carrier wafer preparation steps are the same as those introduced in FIGS. 1A-1C. The photosensitive material growth steps are also similar to those introduced in FIGS. 2A-2B, but with some variations. However, this alternative process does not include the passivation layer formation steps that are introduced in FIGS. 3A-3C above.

[0065] More specifically, after the hetero-epitaxial growth of photosensitive material Ge on a Si material donor wafer 700 (forming, in the growing process, the high TDD Ge layer 712, the thin film $\text{Si}_x\text{Ge}_{1-x}$ layers 714 and eventually the pure Ge layer 716), this alternative process proceeds directly to the wafer bonding and the layer transfer of $\text{Si}_x\text{Ge}_{1-x}$ films 710 to a separate Si material carrier wafer (e.g., carrier wafer 100).

[0066] The Ge material layer structure 710 may include different layer material composition, impurity doping profile and impurity dopant species. In some embodiments, the Si material donor wafer 700 may be of other types of wafer substrates, such as SOI wafers. The materials layers may be configured according to specific photodiode designs if needed. For example, the $\text{Si}_x\text{Ge}_{1-x}$ films may be doped to specific doping profiles. Specific doping profiles may be used for purposes such as Ohmic contact formation, electric field control, and/or surface states passivation. In some embodiments, the transfer $\text{Si}_x\text{Ge}_{1-x}$ film may consist of various $\text{Si}_x\text{Ge}_{1-x}$ layers with different "x" composition values. Such layers may have specific effects such as, but not limited to, diffusion block, quantum well, TDD propagation blocking, bandgap engineering, and/or etch stop.

[0067] As shown in the embodiment of FIG. 7, the top surface of the $\text{Si}_x\text{Ge}_{1-x}$ epitaxial layer is doped with N-type dopant to form an N-type Ge layer 719. In one or more embodiments, the doping concentrations is $\geq 5 \times 10^{18} \text{ cm}^{-3}$ within a depth of about 10 nm to 200 nm.

[0068] Specifically, it is noted that transferring high quality $\text{Si}_x\text{Ge}_{1-x}$ from a transfer carrier substrate to a separate Si material substrate via "wafer bonding" techniques may have an adverse impact on the resulting PD's dark current characteristics. This is because such wafer bonding approaches often result in a heterogeneous interface layer (typically only a few nanometers in thickness) between bonded materials. However, this heterogeneous interface layer is often found to contain elements such as oxygen and carbon. It may also contain any contaminants present on the wafer surfaces prior to bonding, such as oxidized materials, compounds. These contaminants are detrimental to device operation if found within the active region of semiconductor devices.

[0069] With the technique introduced here, the bonding interface, where the heterogeneous interface layer is, is encompassed within high dopant concentration

regions. According to the present disclosure, the bonding surface of $\text{Si}_x\text{Ge}_{1-x}$ layers on wafer 700 and the surface of Si material carrier wafer 100 should not be of highly opposite doping polarity that can form a p-n junction. An p-n junction, if formed by and at the heterogeneous bonding interface, can be severely detrimental to the device performance. Such p-n junction can be avoided if the heterogeneous bonding interface is buried (implanted) within high doping levels of the same dopant types, because then the photodiode active region will terminate prior to reaching the highly doped heterogeneous bonding interface. For purposes of discussion herein, high opposite doping polarity is defined as both layers being doped with opposite dopant types at concentrations of $> 1 \times 10^{17} \text{ cm}^{-3}$.

[0070] In some implementations, the $\text{Si}_x\text{Ge}_{1-x}$ and Si material substrate surface are both doped as high N-type. As an alternative, they can be both doped as high P-type. In other examples, one of the two surfaces of $\text{Si}_x\text{Ge}_{1-x}$ and Si material substrate is doped high as N-type and the other surface is intrinsic or unintentionally doped by either dopant types at less than a doping concentration level of $1 \times 10^{17} \text{ cm}^{-3}$. Note that the high level of N-dopants may diffuse over the heterogeneous bonding interface in the fabrication steps that are after the wafer bonding process. In variations, one of the two surfaces of $\text{Si}_x\text{Ge}_{1-x}$ and Si material substrate is doped high as P-type and the other surface is intrinsic or unintentionally doped by either dopant types at less than a doping concentration level of $1 \times 10^{17} \text{ cm}^{-3}$. Note that the high level of P-dopants may diffuse over the heterogeneous bonding interface in the fabrication steps that are after the wafer bonding process.

[0071] FIG. 8 is a cross-sectional view of an alternative embodiment 800 after a wafer bonding process, bonding the donor wafer 700 and the carrier wafer 100 together. Specifically, in this example embodiment 800, the Si transfer wafer 700 is flipped up-side-down and wafer bonded to the Si carrier wafer 100. According to at least some embodiments of the present disclosure, the Si carrier wafer 100's surface should be smooth for successful wafer bonding. The wafer bonding process may be achieved by, for example, dry wafer bonding, wet wafer bonding, chemical wafer bonding, direct bonding, plasma assisted wafer bonding, or surface activated bonding. Thermal processes may be applied to enhance bonding strength of the wafers.

[0072] FIG. 9 is a cross-sectional view of the alternative embodiment of FIG. 8 after a post-bonding material removal process.

[0073] In the embodiment shown in FIG. 9, the Si substrate from the donor wafer 700 has been removed. Material removal may be accomplished by, for example, wafer splitting, chemical etching, chemical-mechanical-polish (CMP) or wafer lapping. The high TDD Ge layer 712 is also removed. This layer 712's removal may be optional depending on the quality of the transfer film. It is noted, nonetheless, that the ability to remove the high TDD Ge layer 712 can alleviate the leakage current issue of the PD devices, and therefore is considered one of the major benefits that the current technique provides. For the removal of the high TDD Ge layer 712, the $\text{Si}_x\text{Ge}_{1-x}$ layer 714 may be used as an etch/polishing stop layer. Optionally, the $\text{Si}_x\text{Ge}_{1-x}$ 714 is removed, such as shown in FIG. 9. Whether to remove this layer 714 depends on device design. In some implementations, the high TDD Ge layer 712 may be removed, for example, by applying laser annealing techniques to recover this highly defective region.

[0074] The technique may serve as a simplified version of the FIGS. 1A-5, and provide the benefits of (1) reduced leakage current (dark current) originated from the high threading dislocation defect density layer, which is originated from Ge and Si lattice mismatch during hetero-epitaxial $\text{Si}_x\text{Ge}_{1-x}$ material growth; (2) reduced photo-generated carrier recombination loss from the high threading dislocation defect density layer; (3) mitigated negative performance impact to photodiode from wafer bonding hetero-interface layer by encompassing the hetero-interface layer within high impurity dopants; and (4) improved dopant diffusion control within photodiode from reduced thermal budget as a result of the wafer bonded photodiode fabrication.

[0075] It is noted that the technique introduced above may correspond to a unique structure that includes: the lacking of high TDD region within photodiode's $\text{Si}_x\text{Ge}_{1-x}$ layer; the hetero-interface layer due to wafer bonding is buried under high levels of dopant concentration ($> 1 \times 10^{17} \text{ cm}^{-3}$); and the fabricated photodiode becomes located in between the transferred material film and the Si substrate material. In other words, the resulting photodiode is not completely confined within the transferred material film.

POST-PD BONDING

[0076] FIGS. 10A-10C are an example flow for bonding a donor wafer and a carrier wafer after forming the photodetectors on the donor wafer. For purposes of discussion herein, a high performance PD (or "multi-pass PD") includes one or more

mirror structures for reflecting the incident light so as to create multiple passes of the incident light in the light absorption or photosensitive region of the PD. The mirror structure(s) can, therefore, generally increase the quantum efficiency of the PD. Some example HP-PD designs include, for example, a double mirror photonic lock PD, and single mirror multiple pass PD.

[0077] Aside from the dark current issue caused by the high TDD layer in Ge mentioned above, it is further observed that the design and fabrication of a normal incidence high performance PD (HP-PD) is generally limited by the following constraints.

[0078] First, back side incidence design. Due to process feasibility, a conventional, mirror-equipped PD may be inclined to adopt a back side incidence type of design (where light is incident from the back side of the wafer that carries the photodetector such that a reflective mirror can be formed on the front side of the photodetector). However, the back side incidence type PD is often limited in the spectrum range--the range is generally narrower because being limited by substrate absorption.

[0079] Second, semiconductor-on-insulator (SOI) wafer. In certain occasions, an SOI wafer is called for by the design of an HP-PD because the PD design may use the buried oxide (BOX) layer in the SOI wafer as a dielectric mirror. However, processing SOI wafers is generally more difficult in many semiconductor fabrication foundries due to reliability concerns, and hence having to use SOI wafers is not favorable for integration of normal incidence PDs and CMOS field effect transistors (FETs).

[0080] Accordingly, with the aforementioned pre-PD wafer bonding techniques in mind, a post-PD wafer bonding technique is introduced below. The disclosed HP-PD structure and their associated technique can enable high performance PD designs with one or more mirror structures without the need to use SOI wafers. The technique introduced here utilizes a series of bulk substrate to implement high performance PD structures based on wafer-to-wafer bonding. Utilizing bulk semiconductor wafers instead of SOI wafers makes HP-PD designs easier to fit into mainstream CMOS processes. The aforementioned substrate absorption related issues for back side incidence HP-PDs can also be reduced or even avoided. Note

that this technique is applicable to both discrete PDs and the integration of PDs and CMOS based ICs.

[0081] In FIG. 10A, a PD 1010 has been fabricated on a donor wafer 1000. Specifically, an optional separation layer 1020 and then a photon-absorption layer 1030 are formed on the donor wafer 1000. The separation layer 1020 can be, for example, a different doping layer, a proton implanted layer, or any layer with etching selectivity or mechanical property difference with respect to the rest of the substrate. A metal mirror layer 1040 can be deposited on top of the Ge photon absorption layer 1030 as a single optical mirror or a portion of a reflective region (i.e., one or more mirror layers that function together as one composite mirror). For example, an optional dielectric mirror layer 1045 can be formed in between the metal layer 1040 and the Ge photon absorption region 1030. The optional dielectric mirror layer 1045 can act as an additional optical mirror layer and function together with the metal mirror layer 1040 as a single reflective region. Optionally, the donor wafer 1000 can be covered by a dielectric material (e.g., SiO₂) layer 1050, and then prepared (e.g., polished) for wafer bonding. In some implementations, the dielectric mirror layer 1045 may include a single layer of silicon dioxide, silicon nitride, amorphous silicon, or poly silicon. Alternatively, the dielectric mirror layer 1045 may include a multi-layer structure having a combination of the aforementioned materials. In other implementations, a distributed Bragg reflector (DBR) mirror can be used to replace the metal mirror 1040.

[0082] In FIG. 10B, a carrier wafer 1002 is prepared (e.g., bonding layer 1060 formation followed by polishing, the bonding layer 1060's material including dielectric, metal, or other materials) for wafer bonding with one or more techniques described here. The optional bonding layer 1060 is preferably the same type of material and/or having the same doping profile as the layer 1050 for improved bonding results. For example, if a dielectric bonding process is used, then the bonding layer 1060 should include a dielectric layer. If a metal bonding process is used, then the bonding layer 1060 should include a metal layer. If a hybrid bonding process is used, then the bonding layer 1060 should be partially dielectric and partially metal. In some implementations, when hybrid bonding is used, at least a part of the metal layer 1040 can serve as an optical mirror, an electrical contact, or their combinations.

[0083] In FIG. 10C, the donor wafer 1000 and the carrier wafer 1002 are bonded together. After the bonding, the substrate layer of the donor wafer 1000 (which is originally beneath but now above the Ge absorption layer 1030) is at least partially removed, with its removal depth controlled by etching processes or marked by the optional separation layer 1020. Optionally, a surface clean-up process such as wet-etching or CMP can be performed. Then, to form a double mirror HP-PD 1004 as shown in the FIG. 10C's example, a dielectric mirror 1070 is formed above the photosensitive material layer 1030. The resulting HP-PD 1004 is a front side incidence double mirror PD system, with one metal mirror 1040 and one dielectric mirror 1070. The two mirrors can enhance optical absorption by confining the incoming incident light. In some implementations, the resulting HP-PD 1004 can be a front side incidence single mirror (i.e., mirror 1040) multi-pass PD system if an ARC layer is coated instead of a dielectric mirror 1070.

[0084] Optionally, the carrier wafer 1002 can include electronic circuits such as an amplifier, an analog to digital convertor (ADC), a serial-to-parallel interface (SerDes), or a digital circuit such as encoder or decoder. With the technique introduced here, the resulting PD 1004 can be integrated with the electronic circuits. More examples of integration are provided and discussed below.

[0085] FIGS. 11A-11E show an alternative embodiment for bonding a donor wafer and a carrier wafer after forming the photodetectors on the donor wafer. With simultaneous reference to FIGS. 10A-10C, in the first step (FIG. 11A), all the PD components 1010 and one side of the mirror 1040 are formed on the donor wafer 1000 before the wafer bonding. An optional separation layer 1020 is placed inside the substrate of the donor wafer 1000. The separation layer 1020 is located at the stopping position for the following substrate removal. In the second step (FIG. 11B), the donor wafer 1000 that has the PD 1010 is flipped over and bonded to a carrier wafer 1002. A photodetector structure with a single crystalline donor substrate on the top of and overlapping with a single crystalline photosensitive material in the bonded wafer. Corresponding to this technique, in one or more examples, the area of the single crystalline donor substrate is no smaller than the area of the single crystalline photosensitive material.

[0086] In the third step (FIG. 11C), the substrate of the donor wafer 1000 and the separation layer 1020 is removed. In the optional fourth step (FIG. 11D), a second

dielectric mirror 1070 is deposited on the top of the PD 1010 to form a light absorption cavity between the two mirrors 1040 and 1070. In some implementations, the resulting HP-PD is a front side incidence single mirror (i.e., mirror 1040) multi-pass PD system if there no second dielectric mirror 1070 is formed, such as illustrated in FIG.

5 11C. Optionally, an ARC layer can be added onto the mirror 1040 to form a front side incidence multi-pass PD system. In the fifth step (FIG. 11E), bond pads 1080 are opened for the following packaging processes. Notably, the bond pad formation approach shown in FIG. 11E is merely an example; other suitable approaches may apply.

10 **[0087]** According to some examples, the single crystalline donor substrate can be Si. The photosensitive material can be Ge. A top contact area 1085 that is created for the PD 1010 can be Si, SiGe, or partially-doped Ge layer. In some implementations, the contact area 1085 of the Si or SiGe or partially-doped Ge layer can be larger than or overlapping the area of the Ge absorption layer, so that the Si,
15 SiGe, or partially-doped Ge layer 1085 can partially be used as electrical contacts to provide the electrical field in the Ge absorption region. That is to say, the width of the top contact area 1085 can be larger than the width the Ge absorption layer 1030.

[0088] In some implementations, an anti-reflection coating (ARC) layer can be deposited on top of the front side reflector (e.g., the dielectric mirror 1070). Optionally,
20 the bottom of the carrier wafer 1002 can be thinned as needed, for example, by etching or polishing. If the PD is a back side incidence PD, then an ARC layer can then be deposited on the back side (e.g., the carrier wafer's bottom) and the metal mirror 1040 can be replaced with an opening to allow incident light to travel through the opening into the photosensitive material. The electrical contact can be made on the
25 bond pad 1080 from the donor side by etching through the now top surface of the bonded wafer, such as shown in FIGS. 10C and 11E. Additionally or alternatively, the electrical contact can be made by etching from the bottom surface of the bonded wafer, forming a TSV structure (e.g., in a manner similar to the TSV structure for the IC in FIG. 15B, discussed below).

30 **[0089]** FIGS. 12A-12D show a process of forming two alternative embodiments of a photodetector with mirror structures. Instead of resulting in a front side incidence double mirror HP-PD, such as the flow of FIGS. 10A-10C, the flow of FIGS. 12A-12C can result in a back side incidence double mirror HP-PD. Similar to the flow of FIGS.

10A-10C, a single or double mirror system may be used for HP-PD; however, the incident light now comes from the bottom of the PD (i.e., from the carrier wafer 1202's bottom). The PD device 1210 and an optional dielectric mirror 1240 (or a DBR mirror) may be formed on a donor wafer 1200 and bonded to a carrier wafer 1202. The
5 substrate (of the donor wafer 1202) originally underneath but now above the PD structure is then at least partially removed, and a metal mirror 1270 (or DBR mirror) is placed to form the light absorption cavity for the PD 1210. A top contact area 1285 that is created for the PD 1210 can be Si, SiGe, or partially-doped Ge layer. In some implementations, the contact area 1285 of the Si or SiGe or partially-doped Ge layer
10 can be larger than or overlapping the area of the Ge absorption layer, so that the Si, SiGe, or partially-doped Ge layer 1285 can partially be used as electrical contacts to provide the electrical field in the Ge absorption region. That is to say, the width of the top contact area 1285 can be larger than the width the Ge absorption layer 1230.

[0090] For FIG. 12D, as an alternative embodiment 1206 to having a double mirror structure as illustrated in FIG. 12C (i.e., mirrors 1240 and 1270), a single mirror
15 structure can be implemented. The dielectric mirror 1240's function, which is illustrated and discussed with respect to FIG. 12C, is not implemented in FIG. 12D (e.g., which can be a simple opening instead) and may allow light to pass directly from the backside of the carrier wafer 1202 into the photosensitive material 1230. Thus, the
20 embodiment 1206 constitutes a single mirror back-side incidence PD structure.

[0091] Also shown in FIG. 12D is an optional dielectric mirror layer 1275 that can be included between the metal mirror 1270 and the photosensitive material 1230. The dielectric mirror layer 1275 can function together with the metal mirror 1270 as a
25 single composite mirror, which may improve and/or provide more process control over the overall mirror's reflectivity. In some implementations, the dielectric mirror layer 1275 may include a single layer of silicon dioxide, silicon nitride, amorphous silicon, or poly silicon. Alternatively, the dielectric mirror layer 1275 may include a multi-layer structure having a combination of the aforementioned materials. In some
implementations, either an SOI or Si substrate may be used as the donor wafer.

[0092] Similar to what is described for the front side incidence double mirror
30 HP-PD in FIGS. 10A-10C, wafer-to-wafer dielectric bonding, or hybrid bonding, can be used in this structure. The separation layer 1220 can be, for example, a different doping layer, a proton implanted layer, or any suitable layer with etching selectivity or

mechanical property difference with respect to the rest of the donor wafer 1200's substrate.

[0093] FIGS. 13A-13C show another alternative embodiment of a photodetector with mirror structures and integrated circuits (ICs). In this embodiment, the front side incidence double mirror HP-PD on a donor wafer 1300 is bonded to a carrier wafer 1302 that includes a CMOS IC 1390. The IC 1390 includes at least one CMOS transistor that is fabricated on the carrier wafer 1302. On the other hand, the PD 1310 is fabricated on the donor wafer 1300. A wafer-to-wafer hybrid bond process (metal-plus-dielectric bond) is used here to bond the donor wafer 1300 and the carrier wafer 1302 together, forming a structure 1304 shown in FIG. 13C. As shown in FIG. 13C, the electrical connection between the PD 1310 and the IC 1390 can be implemented by metal bonding. This technique can be applied in a similar way for a back side incidence single or double mirror HP-PD.

[0094] FIG. 14 shows yet another alternative embodiment 1404 that includes a through-silicon via 1492 (TSV) formed on the carrier wafer 1402. In the implementation shown, the IC circuit 1490's output is connected to the TSV 1492 on the side of the carrier wafer 1402. This technique can be applied in a similar way for a back side incidence single or double mirror HP-PD.

INTEGRATION WITH OTHER ELECTRONIC CIRCUITS

[0095] FIGS. 15A-15B show two example schemes of integration of front side incidence double mirror photodetectors and integrated circuits. As noted above, while a double mirror PD is shown in the figures, these techniques are generally applicable to a single mirror PD, for example, by eliminating the top mirror between the photosensitive material and the light source. A double mirror system including HP-PD 1510 is shown here as an example. An IC 1590 is integrated to the PD 1510 on the same wafer using the techniques introduced here. In FIG. 15A, the IC 1510's output is connected to a bond pad 1580. In some implementations, such as shown in FIG. 15B, the IC 1510's output is connected to a TSV 1592 on carrier wafer side. Note that these integration techniques introduced here are not limited to any specific kind of PD system; they can be applied in a similar way for other PD system including, for example, a back side incidence double mirror HP-PD, or a single mirror HP-PD.

[0096] FIGS. 16A-16B show two alternative example schemes of integration, with integrated circuits bonded on front side incidence double mirror photodetectors.

Here, the double mirror system is shown here as an example, and the PD 1610 is bonded on the carrier wafer 1602 using the techniques disclosed here. The IC 1690 is then bonded on the PD structure via a flip-chip bonding process. The flip-chip bonding process can be either chip-to-chip or chip-to-wafer. In FIG. 16A, the IC 1690's output is connected to bond pads 1680 via solder balls, copper (Cu) pillars 1694, or other similar techniques. In FIG. 16B, the IC 1690's output is connected to a TSV 1692 on the IC's wafer 1606.

[0097] FIGS. 17A-17B show two alternative example schemes of integration, with back side incidence photodetectors bonded on integrated circuits.

[0098] The embodiments shown in FIGS. 17A-17B utilize a back side incidence HP-PD design (which can be, for example, single or double mirror), which is bonded onto the carrier wafer 1702. The PD 1710 is then diced into chips and bonded on the IC 1790 via a flip-chip bonding process. In FIG. 17A, the IC 1790's output is connected to a bond pad 1780 on IC side, which can be suitable for making electrical contact to other chips or printed circuit boards (PCBs). In FIG. 17B, the IC 1790's output is connected to a TSV 1792 on the IC's wafer 1706.

[0099] FIGS. 18A-18B show two additional examples of front side incidence single mirror photodetectors and their integration applications. The embodiments shown in FIGS. 18A-18B utilize a front side incidence single mirror system for the HP-PD design. Shown in FIG. 18A is a discrete PD 1810, in which the HP-PD is directly bonded to a carrier wafer 1802. Shown in FIGS. 18B is an integration application of PD and IC, where the PD 1810 and IC 1890 are integrated on the same wafer, and then bonded on the carrier wafer 1802.

[00100] Generally speaking, for purposes of discussion here (especially with regard to the description and figures related to post-PD bonding techniques), it is optional to implement a dielectric layer that is located between a photosensitive materials and the initial light incidence source and acts as a mirror to partially transmit the incident light and partially reflect the light reflected by another mirror.

[00101] Furthermore, "back side incidence" and "front side incidence" are relative terms, typically used to describe where light is incident from relative to the PD device. For purposes of discussion here, because multiple wafers may be involved, the terms "back side incidence" and "front side incidence" are used based on the optical path of the incident light relative to the positions of carrier and donor wafers.

Also, such terms used here may take reference to a particular PD's overall design, regardless of the actual existence of the donor wafer or the carrier wafer at the time of a particular described operation. Consequently, for example, if a PD's optical path of the incident light signal by design encounters the donor wafer prior to the carrier wafer, then the device may be referred to as a "front side incidence" type PD. Conversely, if a PD's optical path of the incident signal by design encounters the carrier wafer prior to the donor wafer, then the device may be referred to as a "back side incidence" type PD. It is worth noting that this usage may be different from the conventional notion of a "front side incidence" or a "back side incidence" photodetector, because conventional PD structures are not multi-wafer based.

[00102] Furthermore, an ARC layer or/and a lens structure may be included between the photo-sensitive materials and the initial light incidence source, or alternatively, between a dielectric partial mirror and the initial light incidence source if such dielectric partial mirror is included. The lens structure can be a curved silicon surface formed by etching, a number of polymer based materials shaped into a curved structure, or a number of photonic crystal structures with multiple layers of silicon and dielectric. In some implementations, the lens structure may be hemisphere-like. In some other examples, the lens structure may be photonic crystal-like, in which multiple holes, recesses, rods, rings, mesas are arranged inside. The lens can be made of suitable materials including, for example, crystalline, polymeric, organic or inorganic materials.

WAVEGUIDE AND MULTI-CHANNEL OPTICAL TRANSCEIVER APPLICATION

[00103] With the above-introduced techniques, a high speed hybrid waveguide-based multiple channel optical transceiver module may be further implemented. For example, a receiver module can include normal incidence PDs bonded to a waveguide-based multiple channel passive system. Pulse-amplitude modulation (PAM) or other modulation schemes can be used to boost up the communication speed. A transmitter module can also be implemented by replacing the PDs introduced above with vertical-cavity surface-emitting laser (VCSEL) diodes.

[00104] This approach provides some potential economic benefits as compared to fully integrated waveguide-based photodetector systems that traditionally are suitable for mid-range data communication applications. For long range links, avalanche PD (APD) bonded systems can be used. Using bonded APDs introduced

here may have potential cost advantage than the traditional integrated waveguide-based APD systems.

[00105] FIG. 19 shows a cross-sectional view of a waveguide structure 1900 that can be utilized with the photodetectors introduced here. The waveguide structure 1900 is implemented on an SOI wafer 1902. The SOI wafer 1902 includes a buried oxide (BOX) layer 1910. The silicon (Si) on the SOI wafer 1902 has been patterned to include Si waveguide 1920 and couplers 1930. Additionally, a bond pad 1980 is formed on a portion of the Si waveguide 1920. Note that the drawings are provided here for illustration purposes, and that other forms of optical components (such as other types of optical couplers) can be applicable.

[00106] FIG. 20 shows an example schematic of a waveguide receiver system 2000 embodying one or more techniques introduced here. More specifically, the waveguide receiver system 2000 includes the waveguide structure 1900, as well as a fiber 2010 coupled to one of the couplers 1930. The waveguide receiver system 2000 also includes a front side incidence PD 2020 flip-chip bonded to the bonding pad 1980 and coupled to another one of the couplers 1930. The PD 2020 is positioned to receive and detect the optical signals transmitted from the fiber 2010. In other implementations, a direct fiber to waveguide coupling approach can be used to reduce the coupling loss from the waveguide to the fiber coupler. In addition, the waveguide receiver system 2000 includes an integrated circuit (IC) 2090, also bonded to the bond pad 1980 through wire bonding as shown in FIG. 20 or through flip-chip bonding (not shown for simplicity). The IC 2090 is configured to process the output from the PD 2020. In other implementations, the IC 2090 can be integrated with the PD 2020 on the same chip using techniques introduced previously.

[00107] FIG. 21 shows an example schematic of another waveguide system 2100 embodying one or more techniques introduced here. Compared to the system 2000, system 2100 includes a back side incidence HP-PD 2025 (e.g., a single or double mirror PD). The HP-PD 2025 is bonded to the bonding pad 1980. Light signals are directed into the in-plane Si waveguide system 2100 through couplers 1930. Light signals travel in the Si waveguides 1900 and, in some examples, can split into multiple channels through a splitter such as demultiplexer (DeMUX). Each channel of light can be then re-directed out-of-plane to the bonded PD 2025 for signal collection. More examples of the multi-channel application are discussed in FIGS. 22A-22B.

[00108] The extracted electrical signals from the PD 2025 are sent to the IC 2190. The signal can be transferred through bond wire or flip-chip bonding pad. In the example shown in FIG. 21, the IC 2190 is wire bonded to another side of the HP-PD 2025. The IC 2190 is configured to process the output from the PD 2025.

5 **[00109]** FIGS. 22A-22B show examples of multi-channel receiver modules that can be realized with embodiments of the present disclosure. Advantages of utilizing a waveguide-based wavelength-division multiplexing (WDM) system as disclosed here can include reduced fiber cost compared to traditional, non-WDM systems, noting that the fiber cost typically is a major factor for mid-to-long-range applications.

10 **[00110]** Shown in FIG. 22A is a top view of a dual-channel Si waveguide passive system 2200 with a DeMUX 2210, an Si waveguide 2220 and couplers 2230. Two 25 Gbps PDs 2240 are bonded on the top of their respective couplers 2230 (obscured by the PDs 2240) to enable a 50 Gbps receiver module. In some embodiments, with the implementation of four-level pulse-amplitude modulation (PAM-4) signal, the
15 bandwidth of the receiver module can be boosted up to 100 Gbps. The PDs 2240 can be single or double mirror PDs. In some implementations, the target wavelength is single mode near 1310 nm or single mode near 1550 nm.

[00111] Shown in FIG. 22B is a top view of a quad-channel Si waveguide passive system 2205 with a DeMUX 2215, an Si waveguide 2225 and couplers 2235. Four 25
20 Gbps PDs 2245 are bonded on the top of their respective couplers 2235 to enable a 100 Gbps receiver module. With the implementation of PAM-4 signal, the receiver module's bandwidth can be boosted up to 200 Gbps. Other PAM schemes, such as PAM-8, PAM-16, and so forth, or other modulation and encoding/decoding schemes may also be applicable.

25 CONCLUSION

[00112] Unless contrary to physical possibility, it is envisioned that (i) the methods/steps described above may be performed in any sequence and/or in any combination, and that (ii) the design, structures, or components of respective embodiments may be combined in any manner.

30 **[00113]** Note that any and all of the embodiments described above can be combined with each other, except to the extent that it may be stated otherwise above or to the extent that any such embodiments might be mutually exclusive in function and/or structure.

[00114] Although the present disclosure has been described with reference to specific exemplary embodiments, it will be recognized that the invention is not limited to the embodiments described, but can be practiced with modification and alteration within the scope of the appended claims. Accordingly, the specification and drawings are to be regarded in an illustrative sense rather than a restrictive sense.

EXAMPLES OF CERTAIN EMBODIMENTS

[00115] To summarize, therefore, some example implementations of the disclosed techniques introduced herein are as recited in the following numbered clauses:

10 **[00116]** (A) for pre-PD wafer bonding techniques:

1. A method for fabricating a photodetector using a donor wafer and a carrier wafer, the method comprising:

forming a photosensitive material layer on a front side of the donor wafer;

forming a passivation layer on top of the photosensitive material layer;

15 performing a wafer bonding process to bond together the donor wafer and the carrier wafer, the passivation layer facing a front side of the carrier wafer; and

removing at least a part of threading dislocation density (TDD) defects near an interface between the photosensitive material layer and a substrate of the donor wafer by removing at least a portion of a back side of the donor wafer.

20

2. The method of clause 1, wherein the photosensitive material layer comprises a number of $\text{Si}_x\text{Ge}_{(1-x)}$ layers, wherein $0 \leq x < 1$.

25 3. The method of clause 2, wherein, in the number of $\text{Si}_x\text{Ge}_{(1-x)}$ layers, an x value of one $\text{Si}_x\text{Ge}_{(1-x)}$ layer is different than another $\text{Si}_x\text{Ge}_{(1-x)}$ layer.

4. The method of clause 1, wherein the passivation layer comprises a material also contained on top of the carrier wafer.

30 5. The method of clause 4, wherein the material also contained on top of the carrier wafer comprises silicon.

6. The method of clause 1, wherein the passivation layer comprises a semiconductor material that is not silicon-germanium based but exhibits a passivation effect to the photosensitive material layer.
- 5 7. The method of clause 1, wherein the passivation layer comprises a semiconductor material that is lattice-matched to germanium.
8. The method of clause 7, where the semiconductor material is gallium arsenide.
- 10 9. The method of clause 1, wherein forming the photosensitive material layer comprises:
doping the photosensitive material layer according to a predetermined doping profile suitable for the photodetector.
- 15 10. The method of clause 1, further comprising:
doping the passivation layer by impurities.
11. The method of clause 1, further comprising:
doping the passivation layer and the carrier wafer by a same kind of dopant.
- 20 12. The method of clause 11, wherein the dopant is N-type.
13. The method of clause 1, further comprising:
polishing the front side of the donor wafer after forming the passivation layer
25 and prior to performing the wafer bonding process.
14. The method of clause 1, further comprising:
annealing the donor wafer after forming the passivation layer and prior to
performing the wafer bonding process.
- 30 15. The method of clause 1, further comprising:
patterning the carrier wafer prior to the wafer bonding process.

16. The method of clause 1, further comprising:
forming another passivation layer on the front side of the carrier wafer prior to the wafer bonding process.

5 17. The method of clause 1, wherein the wafer bonding process includes one or more of: a dry wafer bonding, a wet wafer bonding, a chemical wafer bonding, or a plasma assisted wafer bonding.

10 18. The method of clause 1, further comprising:
fabricating other portions of the photodetector on the carrier wafer.

19. The method of clause 1, further comprising:
prior to forming the photosensitive material layer, forming a separation layer on the donor wafer.

15

20. The method of clause 1, wherein the method is performed prior to a completion of active components of the photodetector.

20 21. A semiconductor structure comprising:
a first silicon wafer having a front side;
a photosensitive material layer deposited on the front side of the first silicon wafer, the photosensitive material layer including a number of $\text{Si}_x\text{Ge}_{(1-x)}$ layers, wherein $0 \leq x < 1$;
a silicon passivation layer on top of the photosensitive material layer; and
25 a second silicon wafer having a front side,
wherein the first silicon wafer and the second silicon wafer is bonded together with the silicon passivation layer facing the front side of the second silicon wafer.

[00117] (B) for post-PD wafer bonding techniques:

30 1. A method for fabricating a light absorption apparatus using a donor wafer and a carrier wafer, the method comprising:
forming a light absorption region on a front side of the donor wafer;

after the light absorption region is formed, performing a wafer bonding process to bond together the donor wafer and the carrier wafer, with the surface having the light absorption region facing a surface of the carrier wafer; and removing at least a portion of a back side of the donor wafer.

5

2. The method of clause 1, further comprising:

after removing at least a portion of the back side of the donor wafer, depositing a first layered structure above the back side of the donor wafer.

10 3. The method of clause 2, wherein the first layer structure includes metal and is configured as an optical mirror for the light absorption region.

4. The method of clause 3, wherein the first layer structure further includes a dielectric layer between the metal layer and the light absorption region.

15

5. The method of clause 1, further comprising:

before the wafer bonding process, forming a dielectric layer structure on top of the light absorption region and above the donor wafer, or on top of the carrier wafer, wherein the dielectric layer structure is configured as a partial light reflector.

20

6. The method of clause 1, further comprising:

forming an anti-reflection coating (ARC) layer on the back side of the carrier wafer, wherein light for the light absorption region is incident from the back side of the carrier wafer.

25

7. The method of clause 1, further comprising:

prior to the wafer bonding process, forming a second layer structure on top of the light absorption region and above the donor wafer, or on top of the carrier wafer, or a combination thereof.

30

8. The method of clause 7, wherein the second layer structure includes metal and is configured as an optical mirror for the light absorption region.

9. The method of clause 8, wherein the second layer structure further includes a dielectric layer between the metal layer and the light absorption region.

5 10. The method of clause 7, further comprising:
after removing at least a portion of the back side of the donor wafer, depositing a third layer structure above the back side of the donor wafer as a partial optical reflector for the light absorption region

10 11. The method of clause 7, further comprising:
forming an anti-reflection coating (ARC) layer on the back side of the donor wafer, wherein light for the light absorption region is incident from the back side of the donor wafer.

15 12. The method of clause 7, further comprising:
before the wafer bonding process, fabricating an electronic component on the carrier wafer and/or the donor wafer,
wherein light for the light absorption region is incident from the back side of the donor wafer.

20 13. The method of clause 12, wherein the electronic component comprises one or more of: an amplifier, an analog-to-digital (ADC) converter, a serial-to-parallel (SerDes) interface, or a digital circuit.

25 14. The method of clause 1, wherein the wafer bonding process includes one or more of: a dielectric-to-dielectric bonding, a metal-to-metal bonding, or a combination thereof.

30 15. The method of clause 1, further comprising:
after removing the portion of the back side of the donor wafer, forming an anti-reflection coating (ARC) layer on the back side of the donor wafer.

16. The method of clause 1, wherein the donor and the carrier wafers both are bulk semiconductor wafers instead of silicon-on-insulator (SOI) wafers.

17. The method of clause 1, wherein the light absorption apparatus includes at
5 least one mirror structure between the light absorption region and the carrier wafer.

18. The method of clause 1, wherein the light absorption apparatus includes at least one mirror structure on the back side of the donor wafer.

10 19. The method of clause 1, wherein the light absorption region is formed on another wafer and bonded to the donor wafer.

20. The method of clause 1, further comprising:

15 bonding the light absorption apparatus onto another wafer including a waveguide and an optical coupler, wherein the light absorption apparatus is located above the optical coupler.

20

CLAIMS

What is claimed is:

1. A multi-wafer based semiconductor light absorption structure comprising:
5 a first wafer bonded with a second wafer;
a light absorption region located in the first wafer;
a contact region located in the first wafer, immediately above the light
absorption region and in physical contact with the light absorption region; and
a bonding interface between the first wafer and the second wafer, the bonding
10 interface located below the light absorption region and not in physical contact with the
light absorption region.
2. The structure of claim 1, further comprising:
a first mirror region, wherein the light absorption region is located in between
15 the first mirror region and the contact region.
3. The structure of claim 2, wherein the first mirror region comprises a plurality of
mirror layers, and wherein at least two mirror layers are separated by the bonding
interface.
20
4. The structure of claim 2, wherein at least a part of the first mirror region is
located in the first wafer, the first mirror region including a first mirror layer and a
second mirror layer, the second mirror layer being closer to light absorption region,
wherein the first mirror layer is metal and the second mirror layer is dielectric.
25
5. The structure of claim 2, further comprising:
a second mirror region, wherein the contact region is located in between the
second mirror region and the light absorption region.
- 30 6. The structure of claim 5, wherein the second mirror region is a partial mirror and
the first mirror region is a full mirror.

7. The structure of claim 6, further comprising:
an optical passage configured to allow incident light to enter the light absorption region through the second mirror region.
- 5 8. The structure of claim 5, wherein the second mirror region is a full mirror and the first mirror region is a partial mirror.
9. The structure of claim 8, wherein incident light is to enter from the second wafer.
- 10 10. The structure of claim 9, further comprising:
an optical passage configured to allow incident light to enter the light absorption region through the first mirror region.
- 15 11. The structure of claim 2, wherein incident light is to enter from the first wafer through the contact region to the light absorption region, being reflected by the first mirror region and back to the light absorption region.
- 20 12. The structure of claim 1, further comprising:
a first mirror region and a second mirror region, wherein one of the first and second mirror regions is a partial mirror through which the incident light for the light absorption region is to enter.
- 25 13. The structure of claim 1, further comprising:
a first mirror region located above the contact region.
14. The structure of claim 13, wherein the first mirror region is completely located in the first wafer.
- 30 15. The structure of claim 1, wherein incident light is to enter from the second wafer, through the bonding interface, into the light absorption region.

16. The structure of claim 15, further comprising:
an optical passage located in the second wafer and configured to allow incident light to enter the light absorption region.

5 17. The structure of claim 1, wherein a width of the contact region is larger than a width of the light absorption region.

18. The structure of claim 1, further comprising:
a vertical contact via in electrical contact with the contact region and extending
10 toward the bonding interface.

19. A light absorption apparatus comprising:
a contact region;
a light absorption region beneath the contact region, wherein light is incident
15 from the contact region traveling along a first direction toward the light absorption region, the light absorption region having a smaller width than the contact region; and
an optical mirror structure coupled to the light absorption region, such that the light is incident through the contact region and the light absorption region to the optical mirror structure and reflected back to the light absorption region,
20 wherein the optical mirror structure includes a plurality of mirror layers, at least two mirror layers being separated by a bonding interface between two wafers.

20. The structure of claim 19, wherein the contact region and light absorption region have a different doping polarity, and wherein photo-generated electrical carriers
25 flow primarily in parallel to the first direction.

21. The structure of claim 19, wherein the optical mirror structure includes (1) a metal layer and (2) a dielectric layer located between the metal layer and the light absorption region.
30

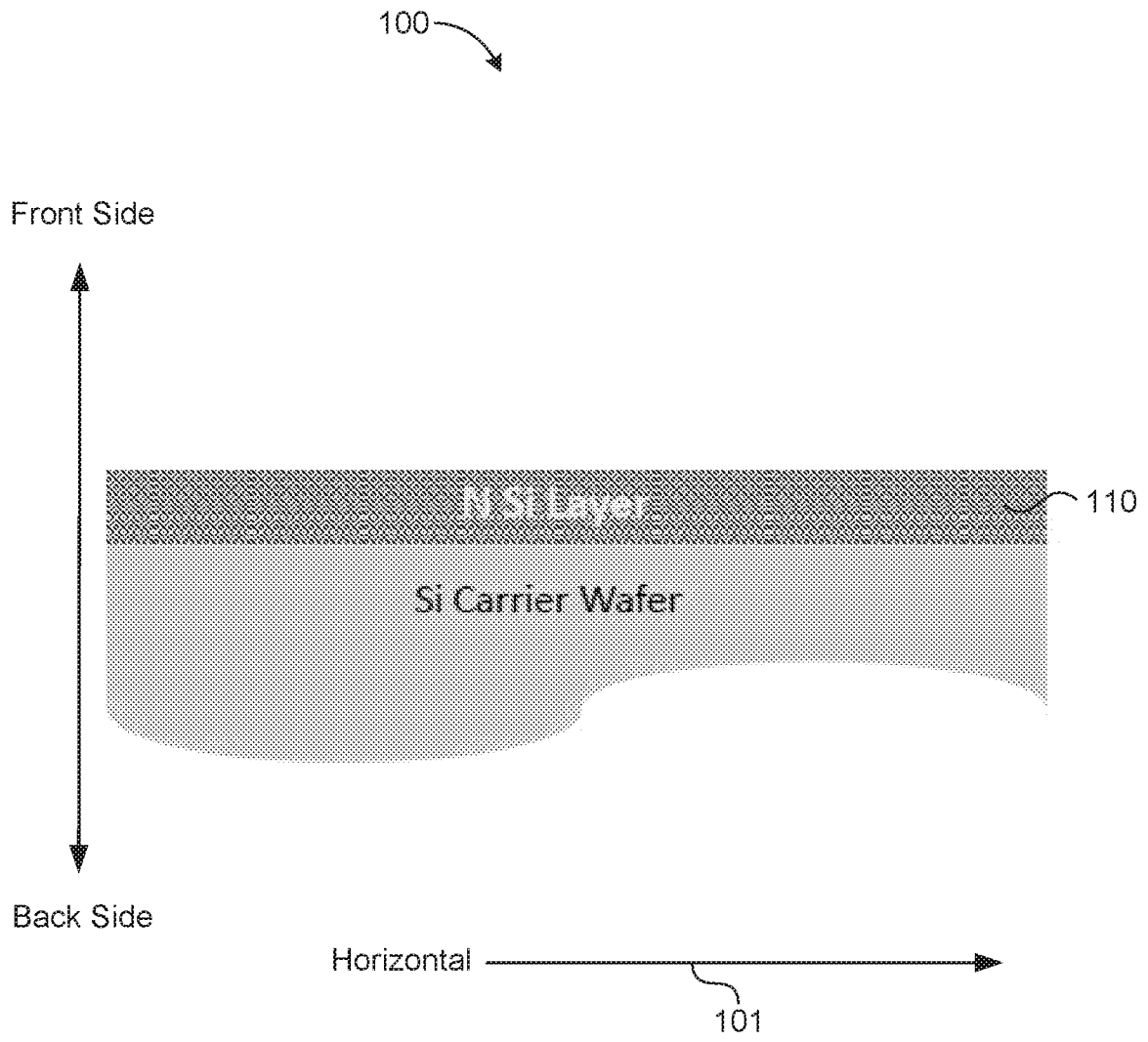


FIG. 1A

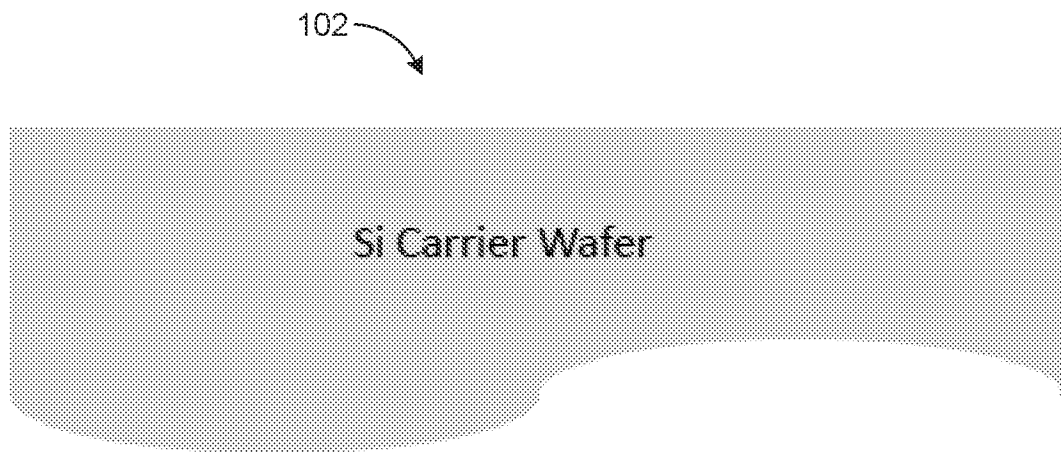


FIG. 1B

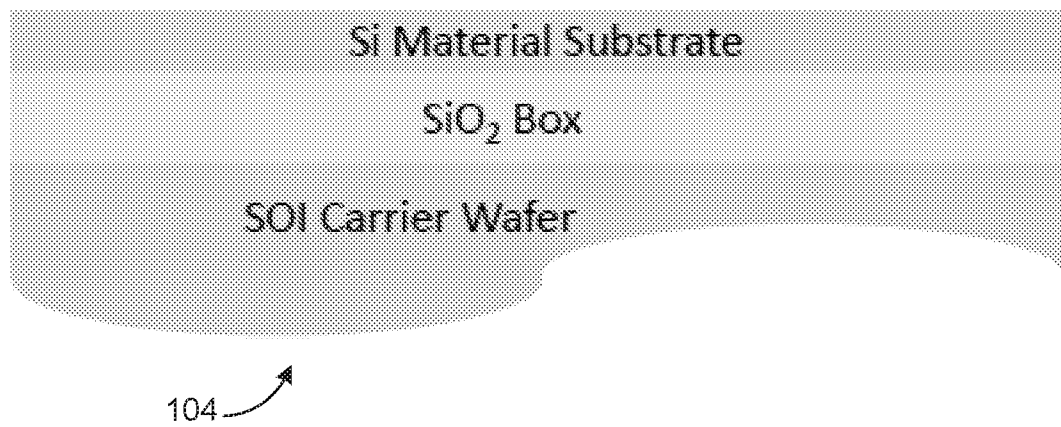


FIG. 1C

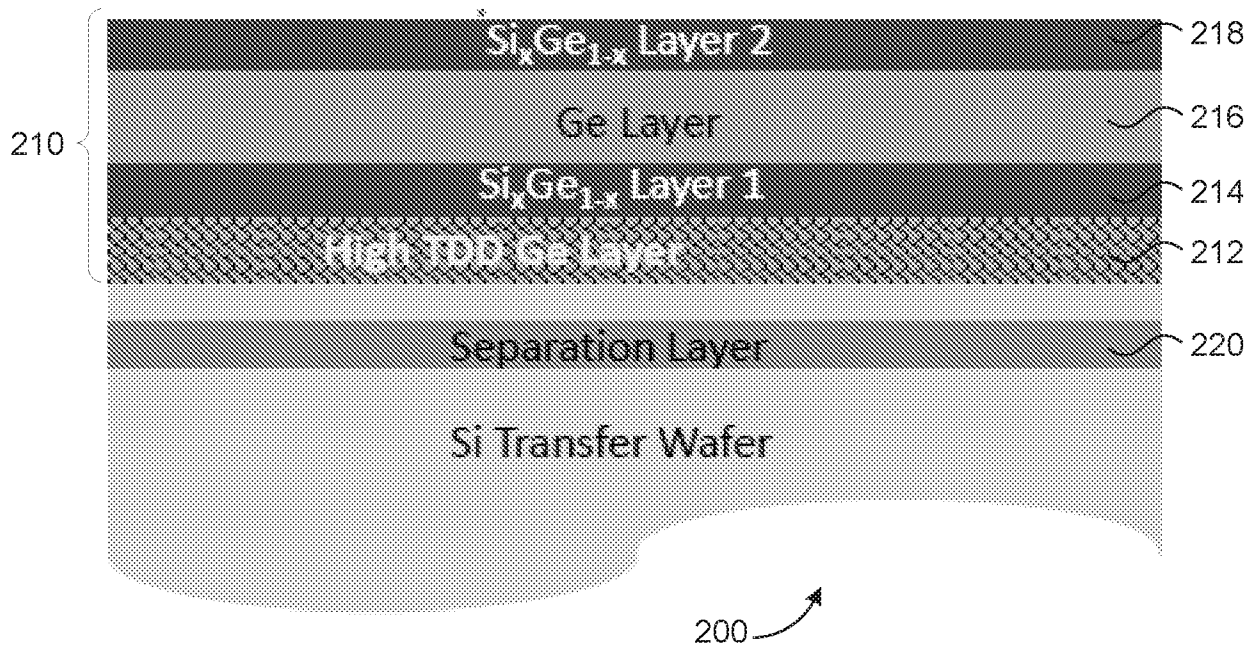


FIG. 2A

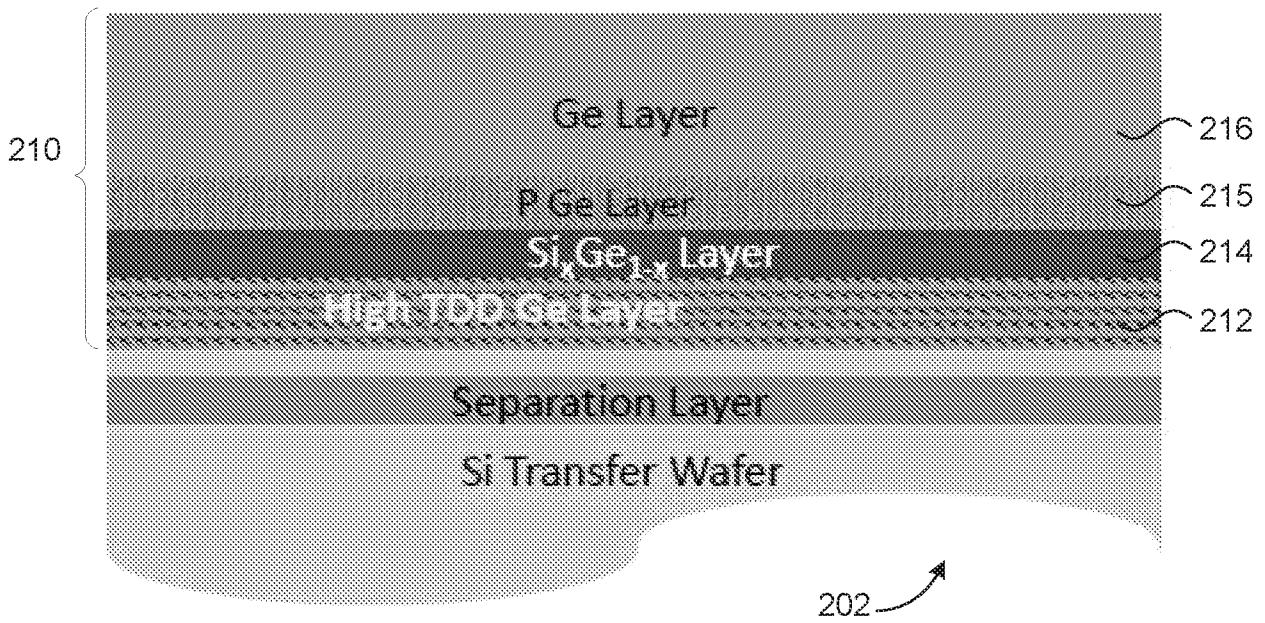


FIG. 2B

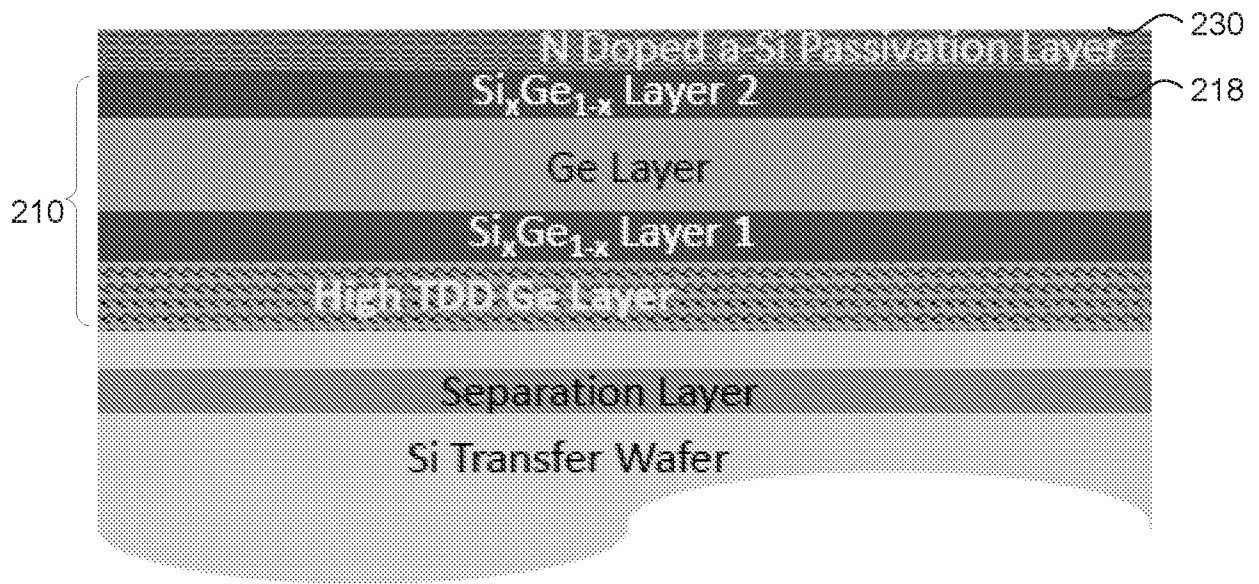


FIG. 3A

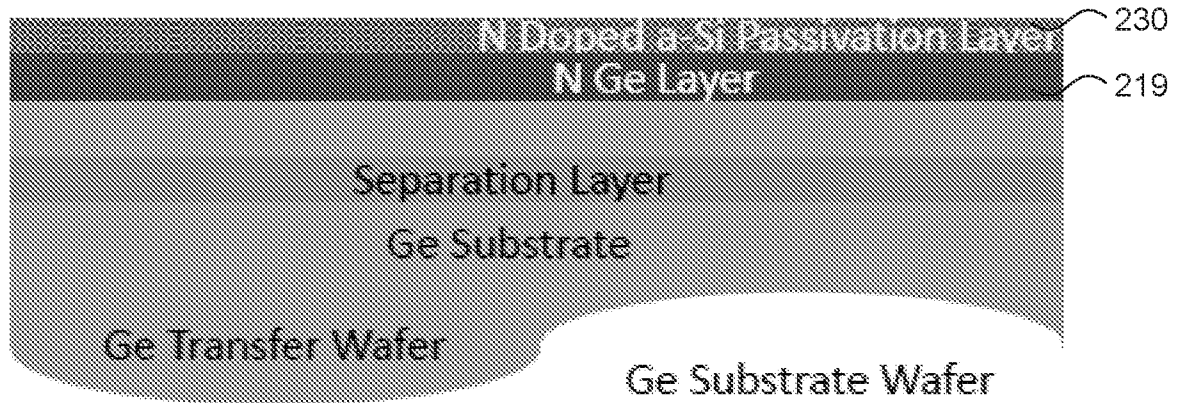


FIG. 3B

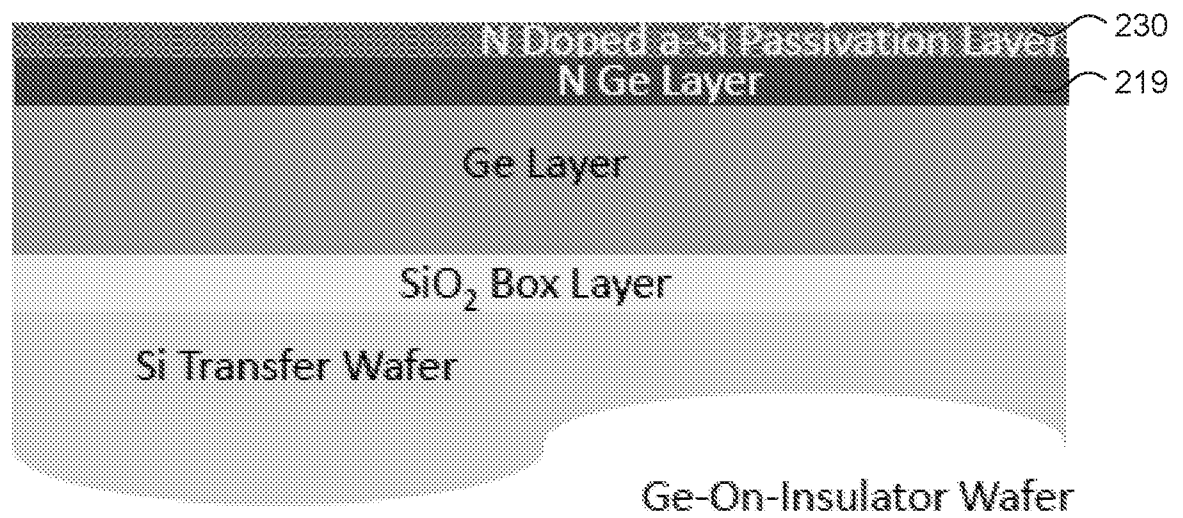


FIG. 3C

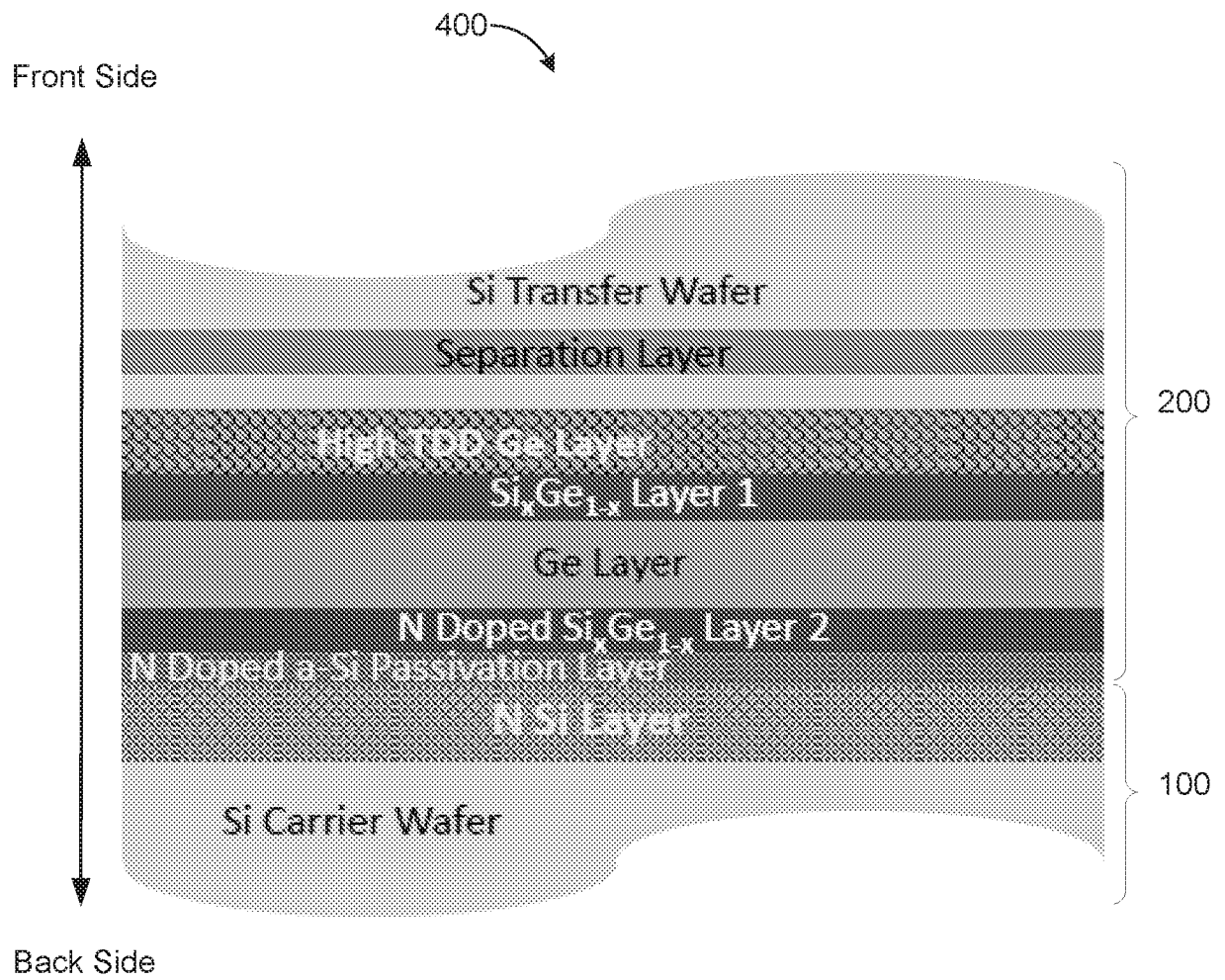


FIG. 4

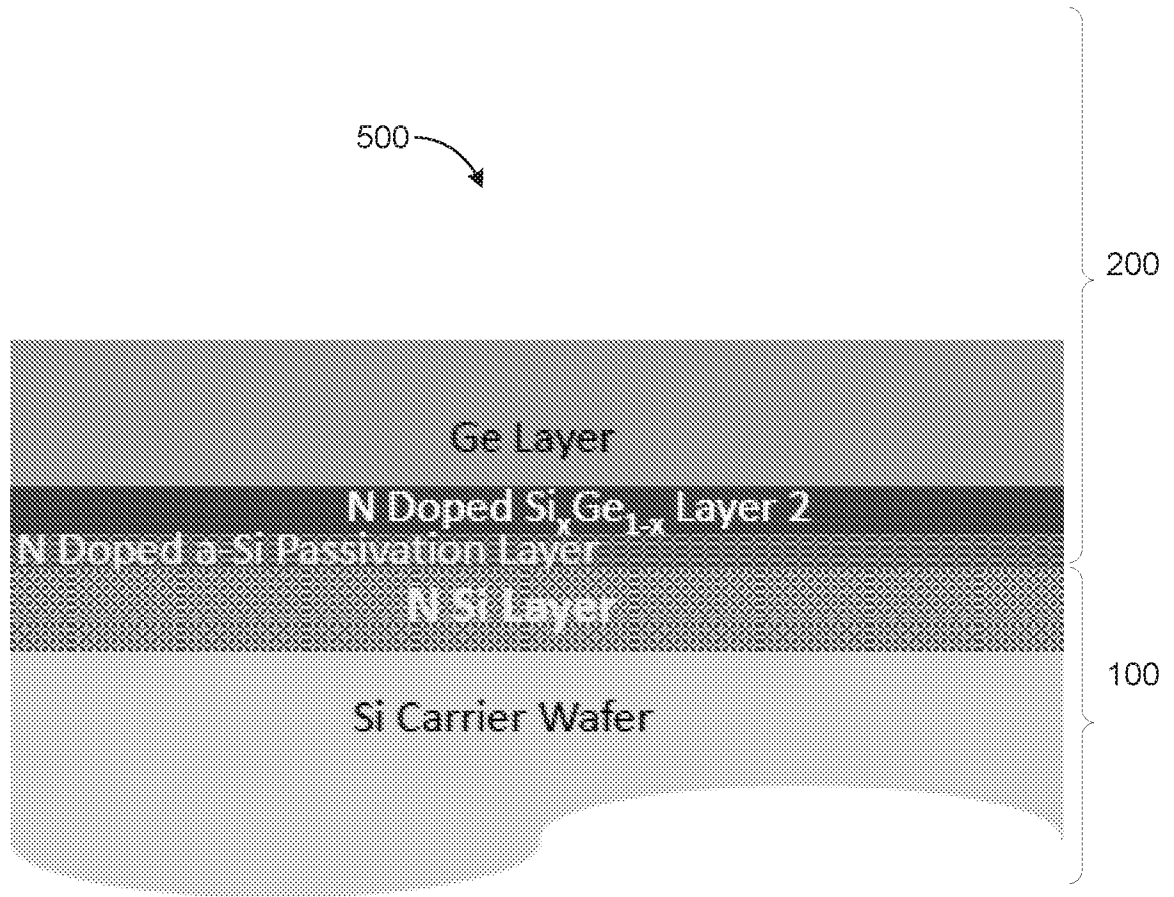


FIG. 5

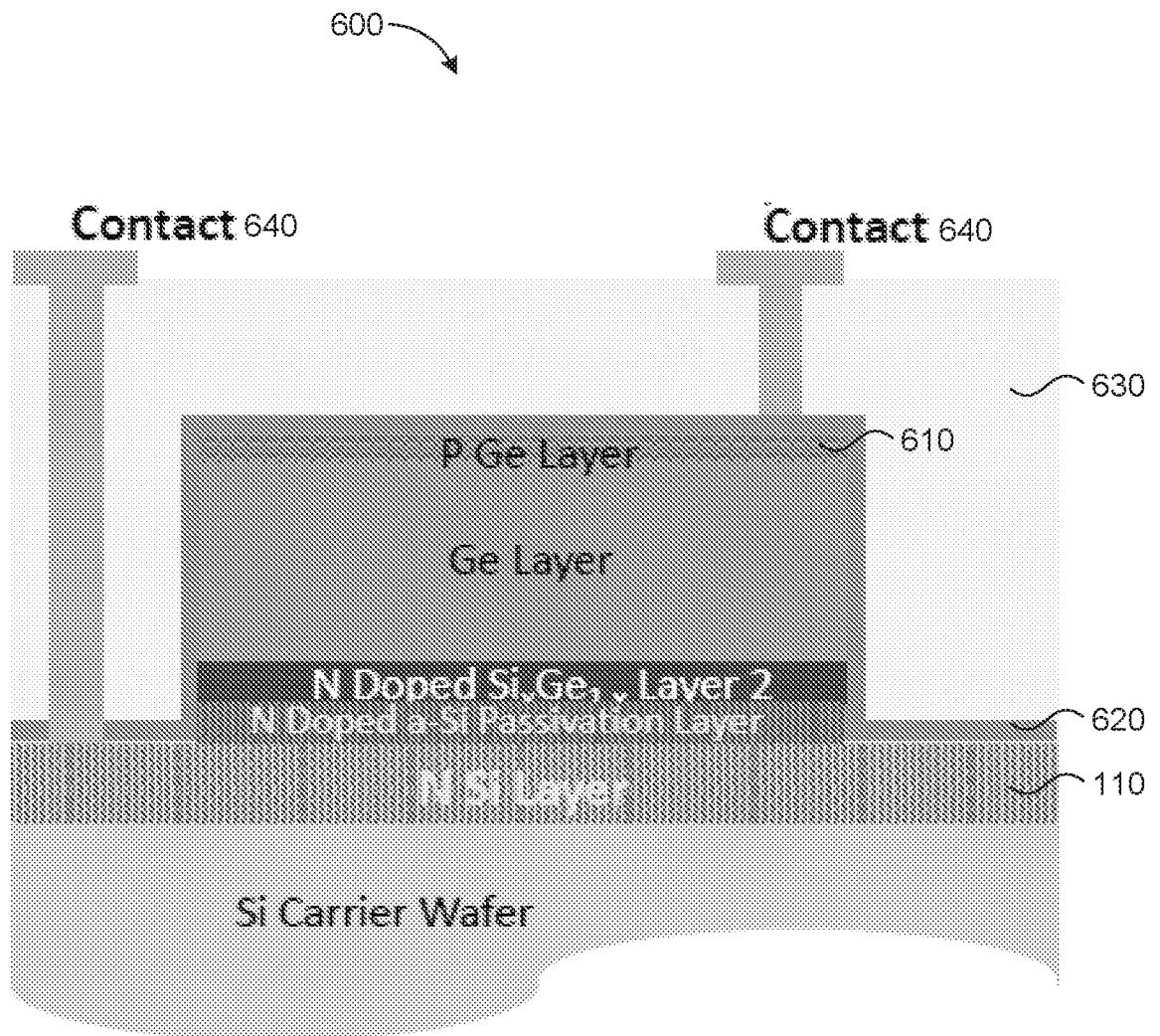


FIG. 6A

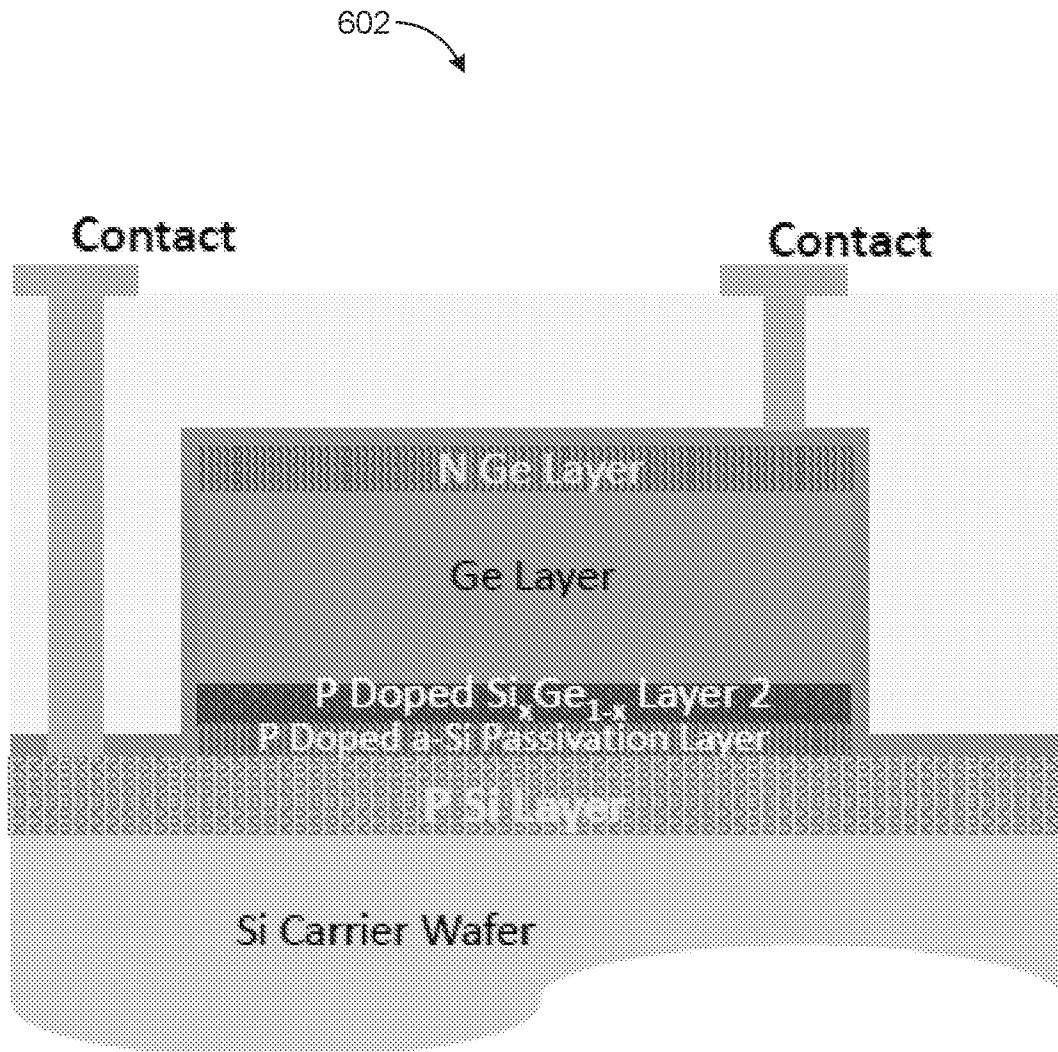


FIG. 6B

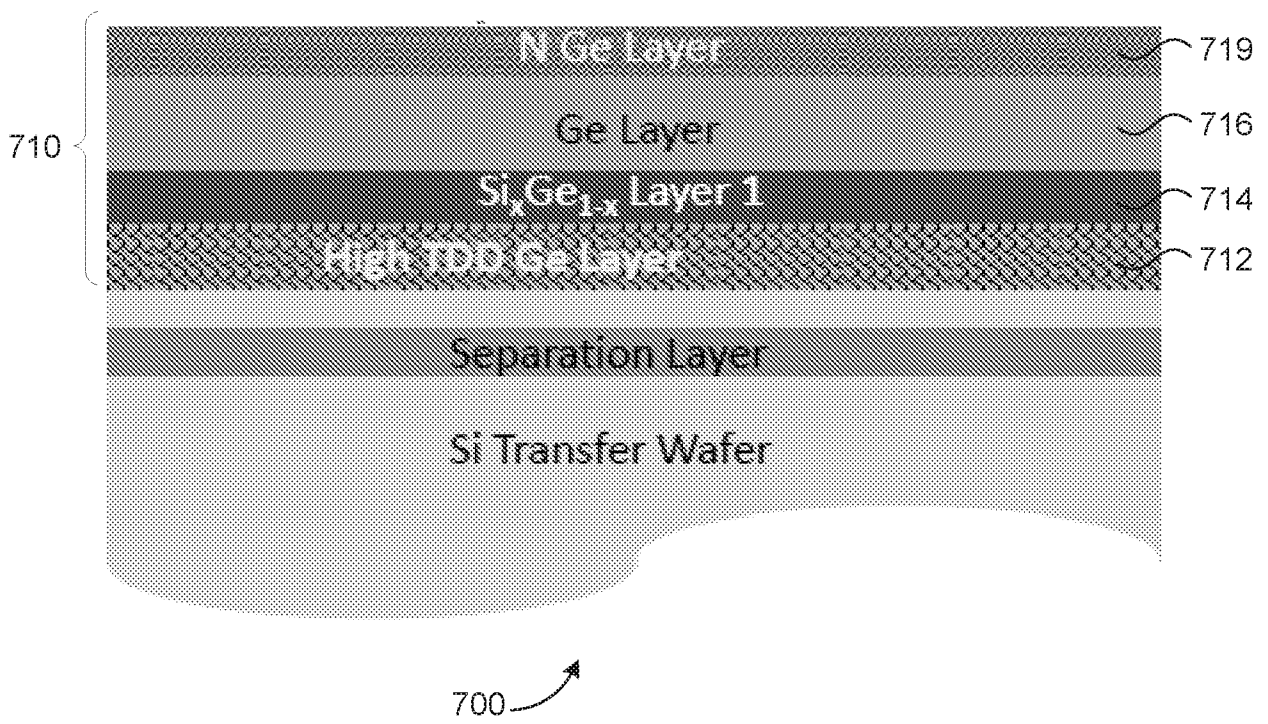


FIG. 7

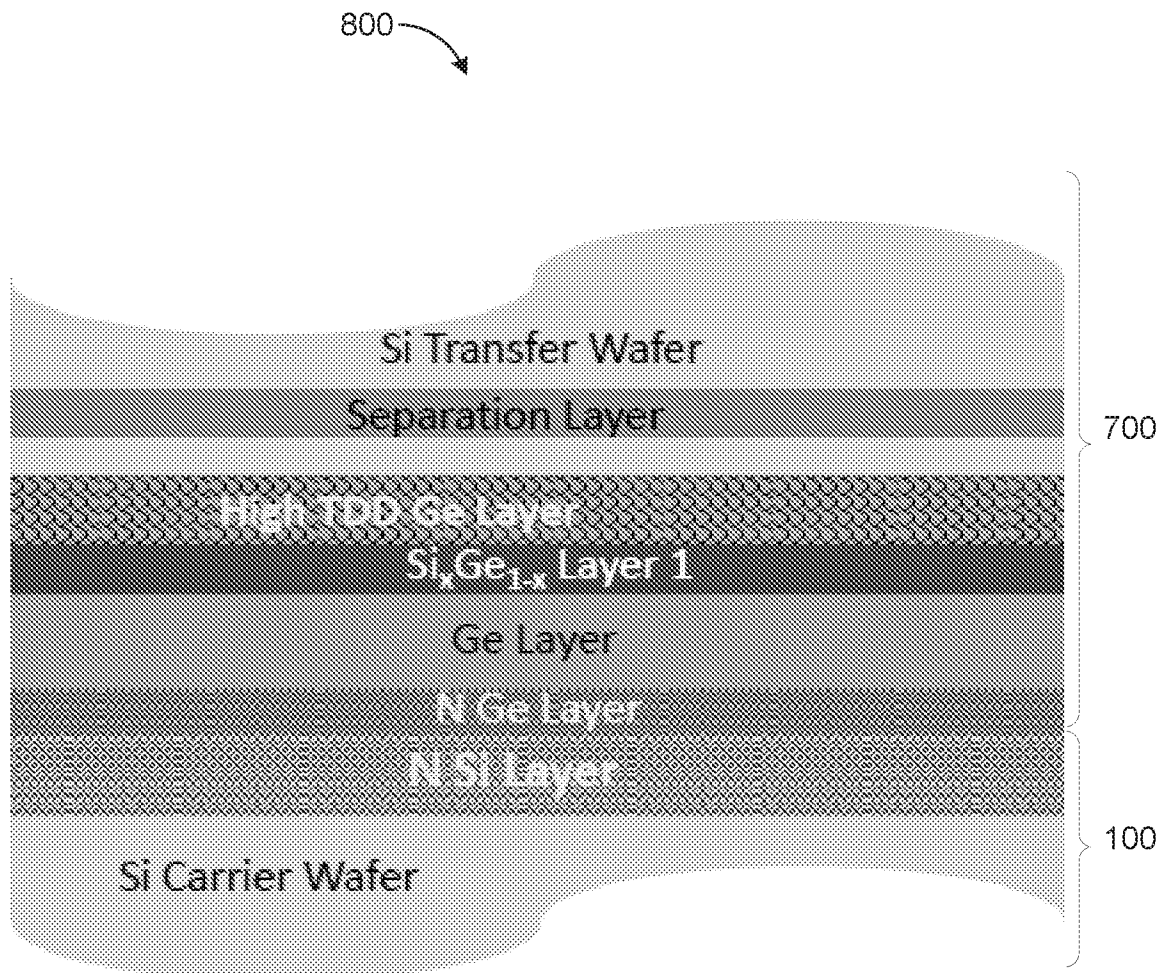


FIG. 8

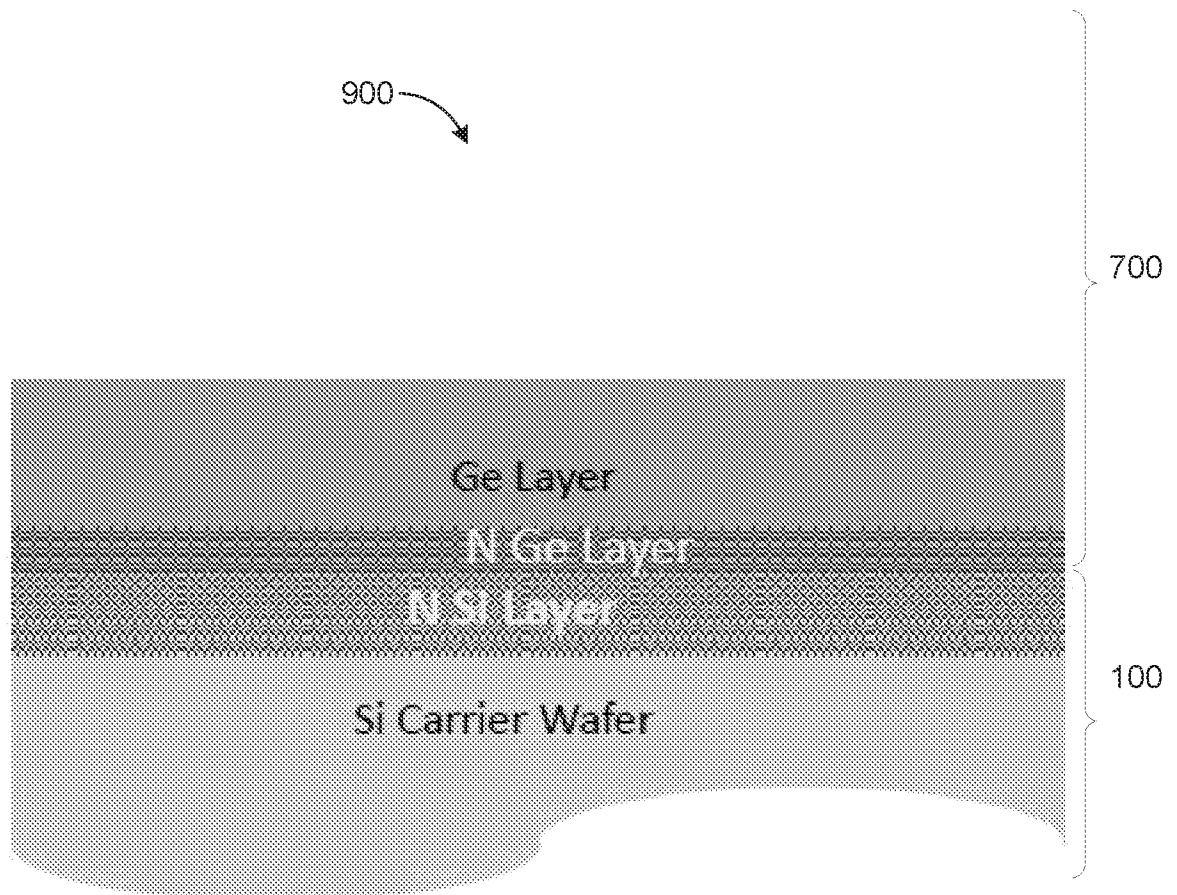


FIG. 9

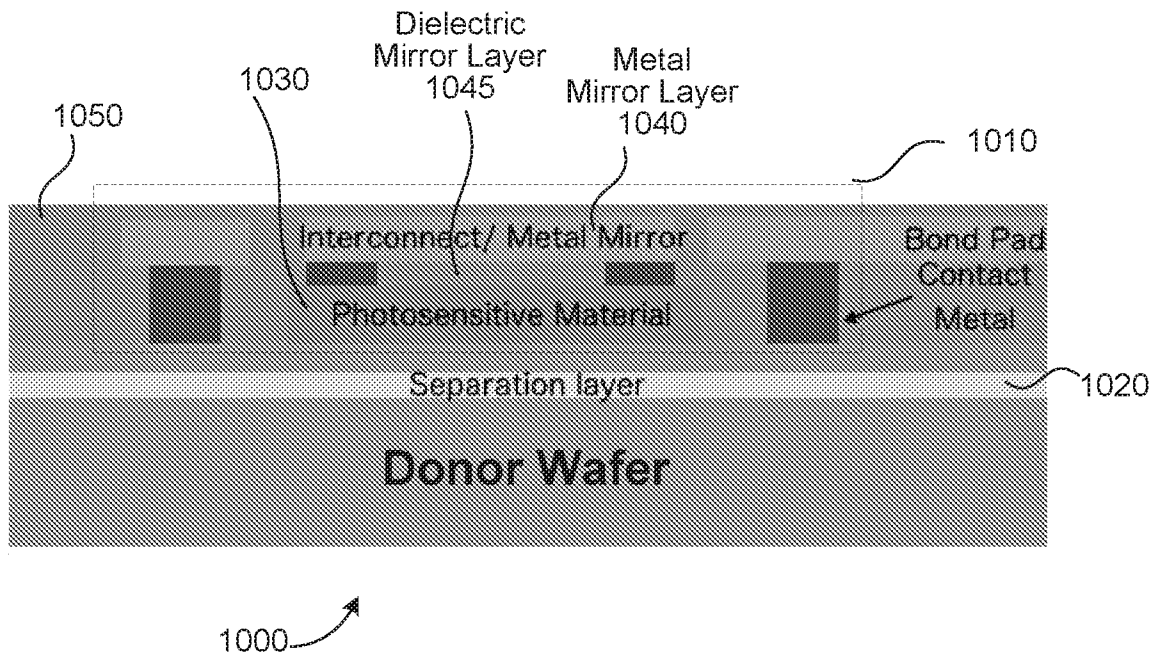


FIG. 10A

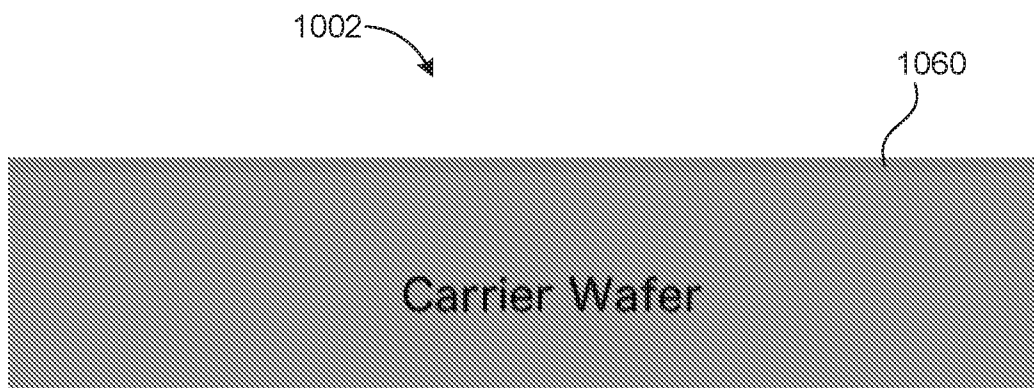


FIG. 10B

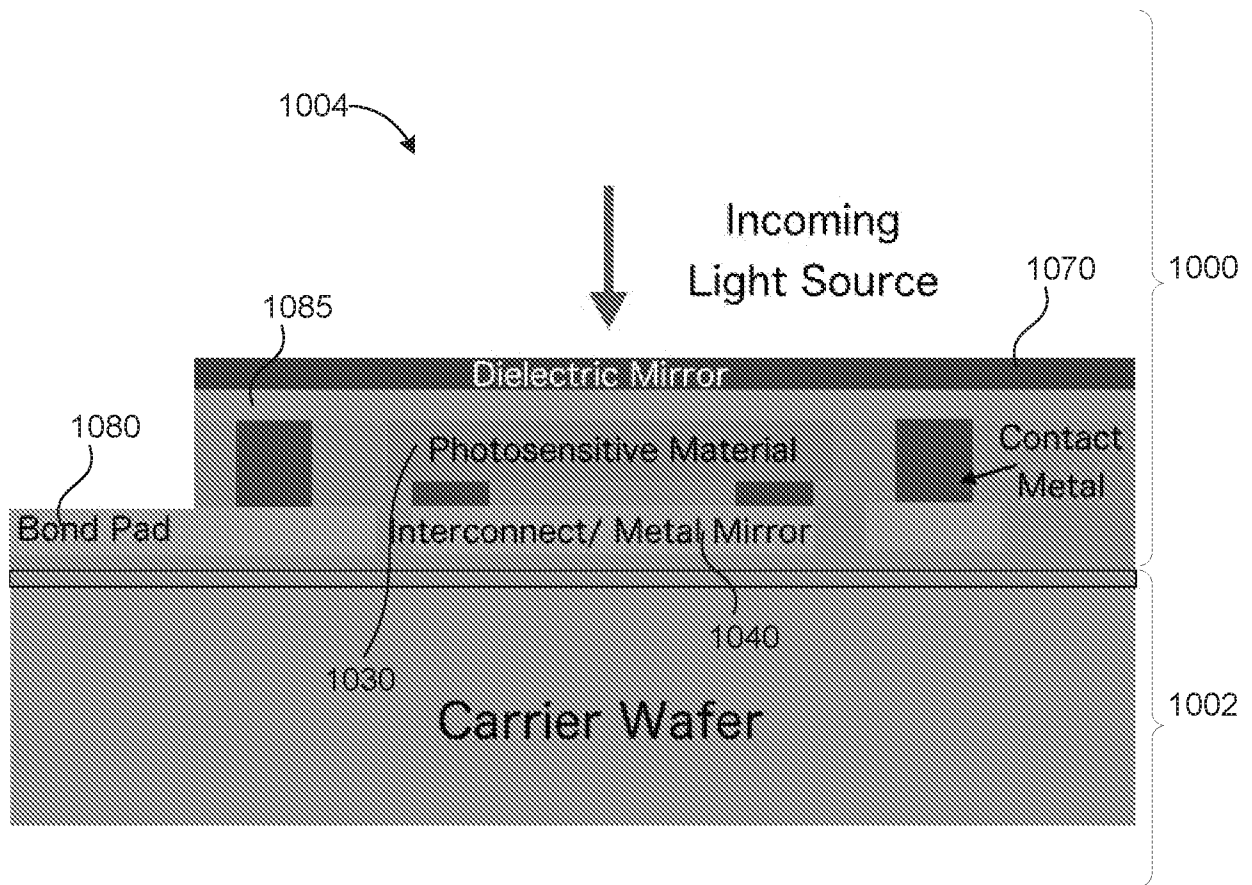


FIG. 10C

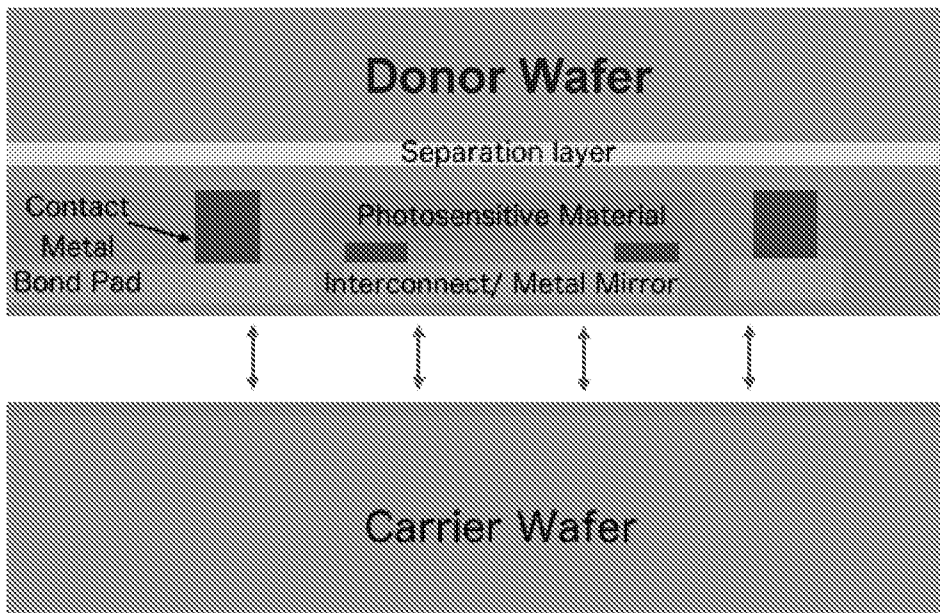


FIG. 11A

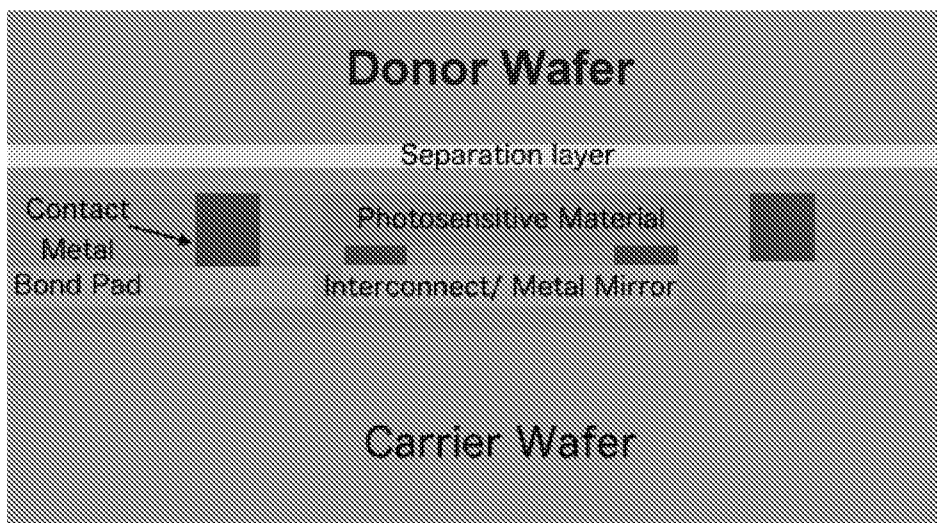


FIG. 11B

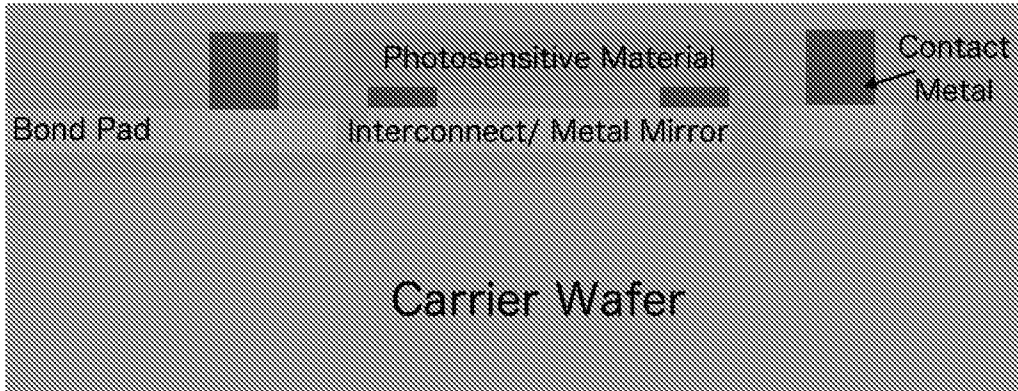


FIG. 11C



FIG. 11D

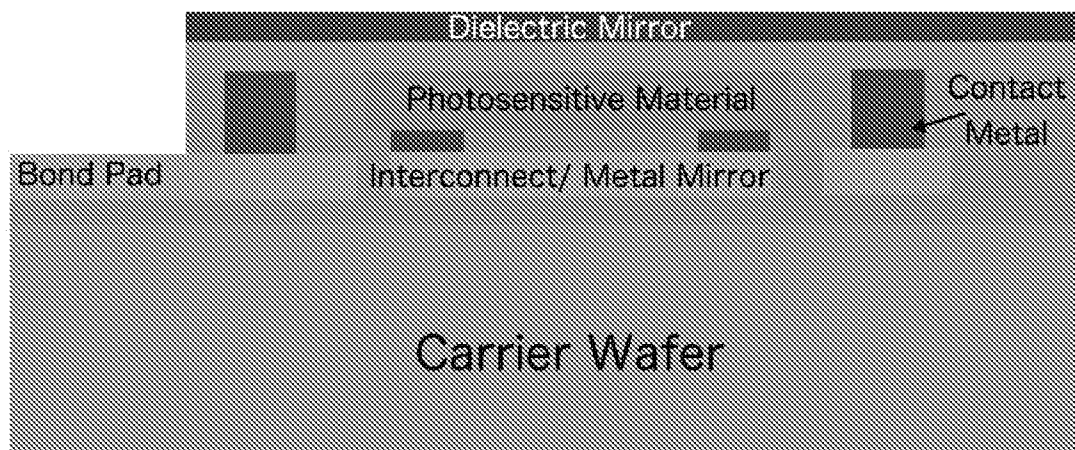


FIG. 11E

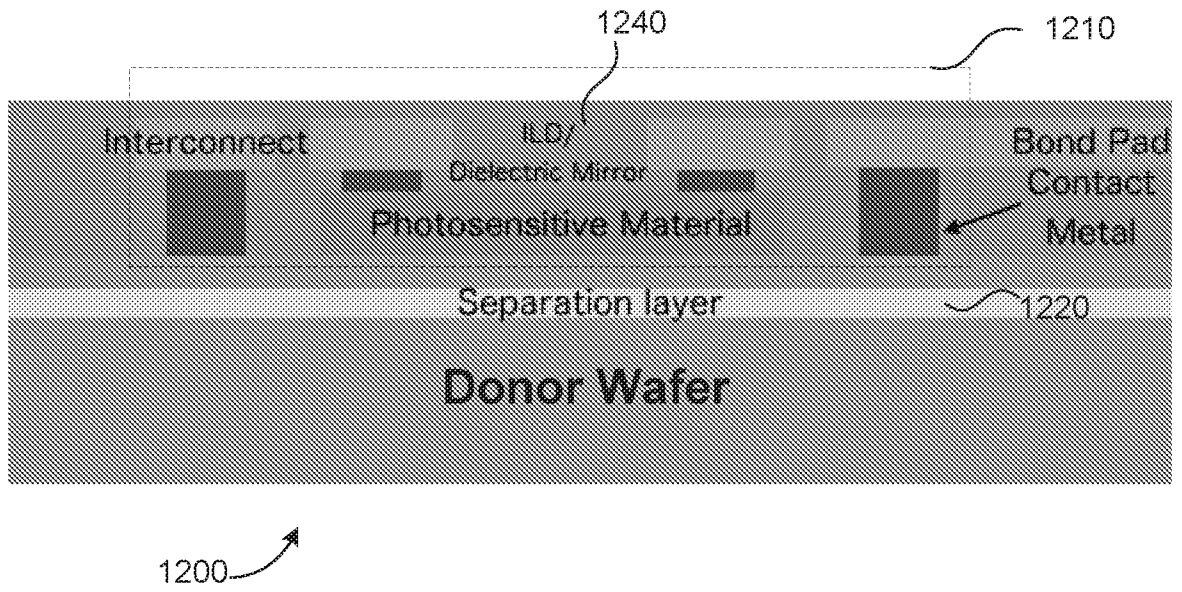


FIG. 12A

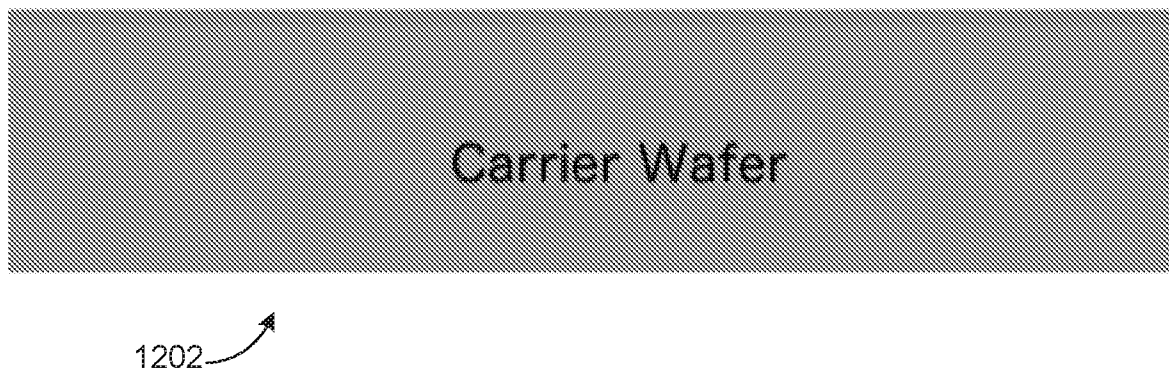


FIG. 12B

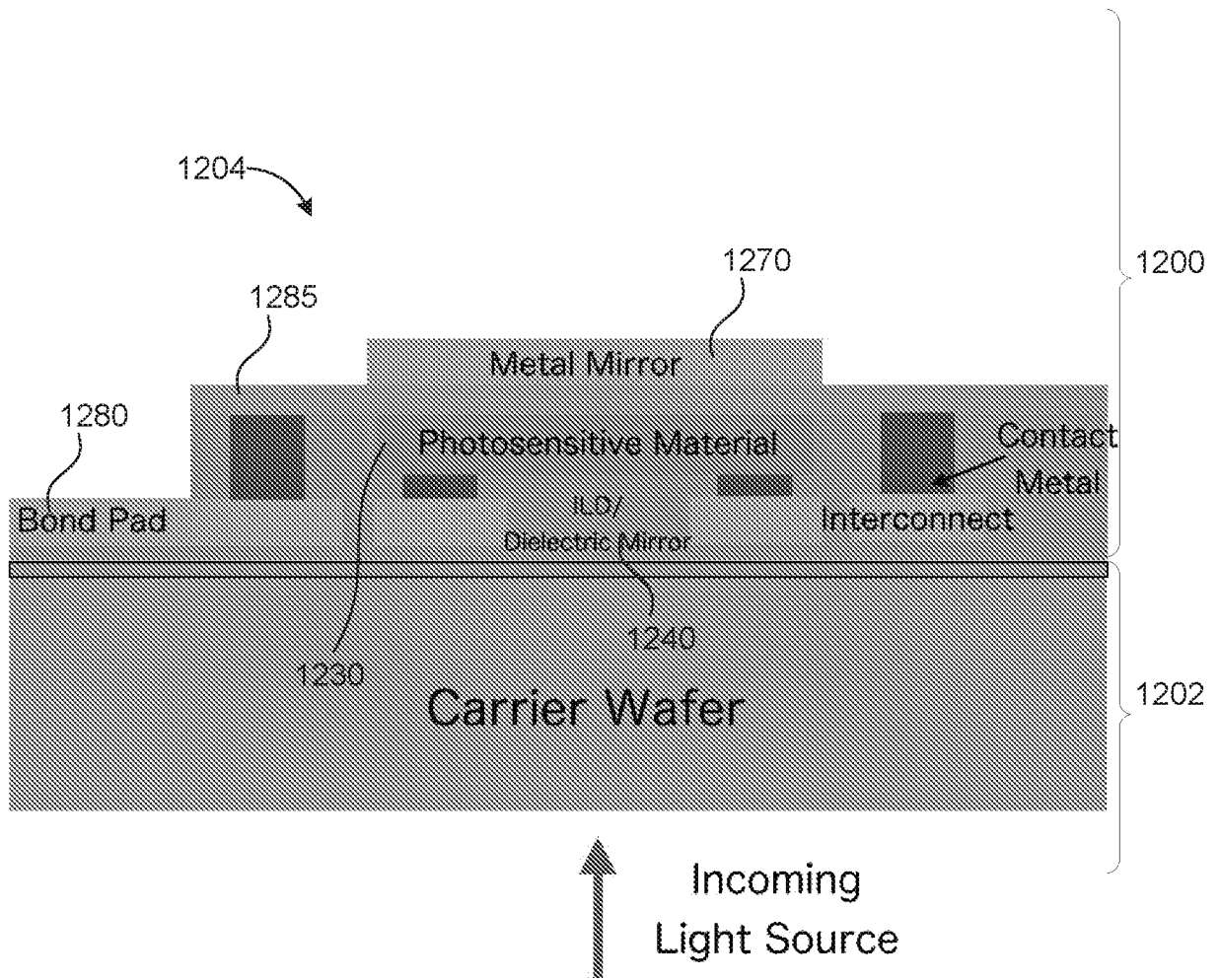


FIG. 12C

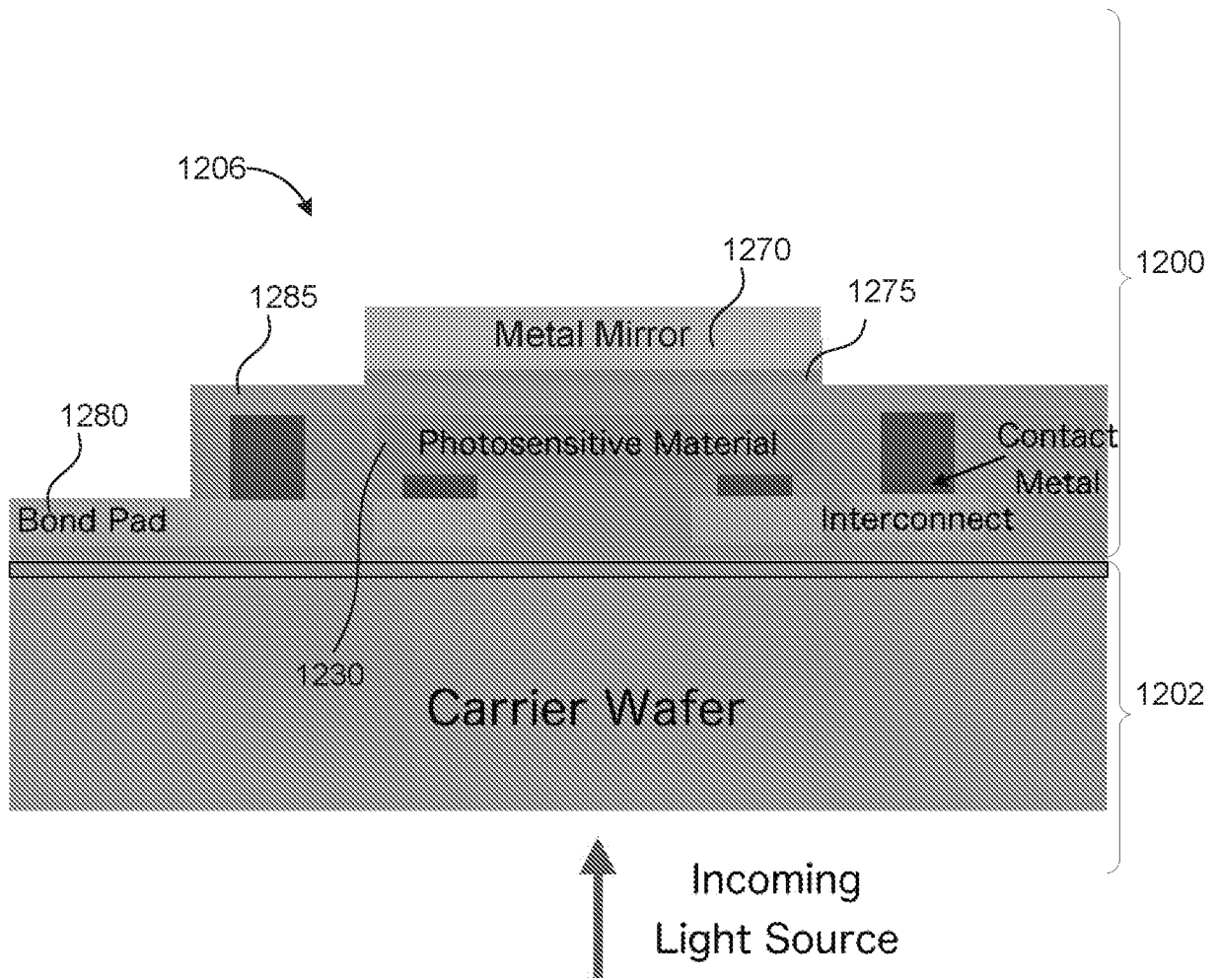


FIG. 12D

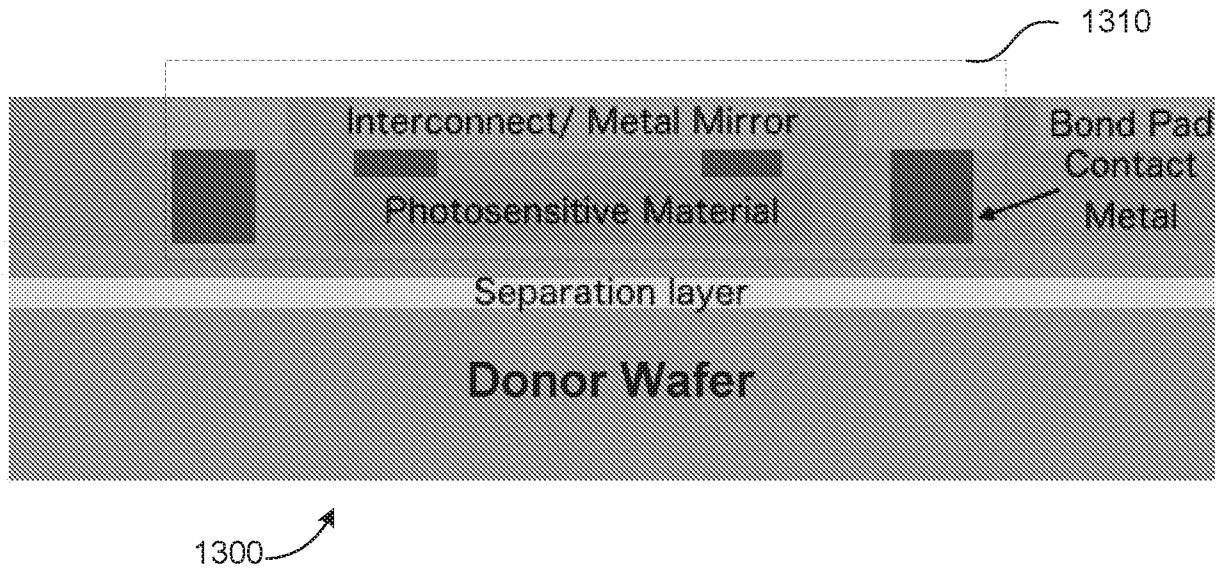


FIG. 13A

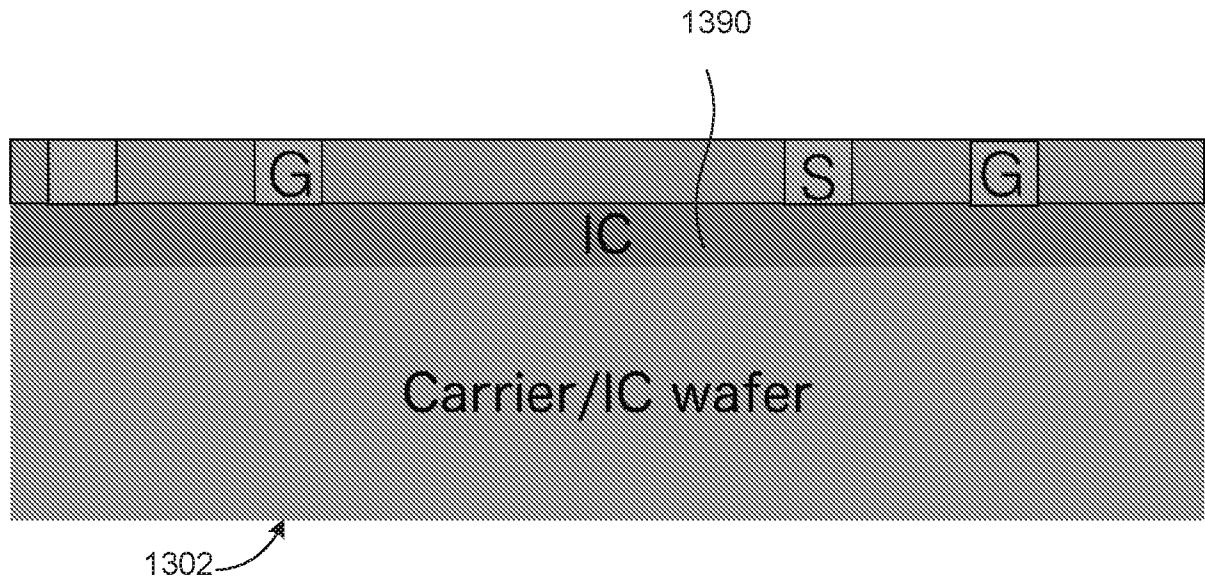
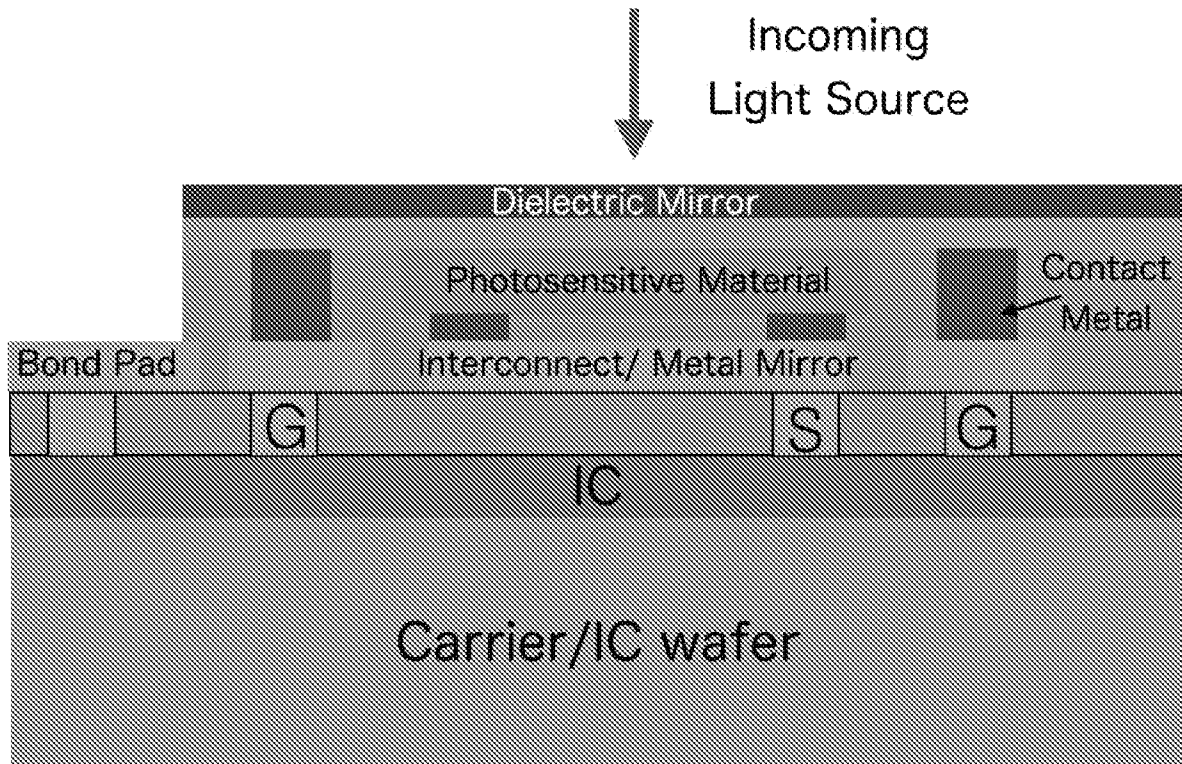


FIG. 13B



1304 ↗

FIG. 13C

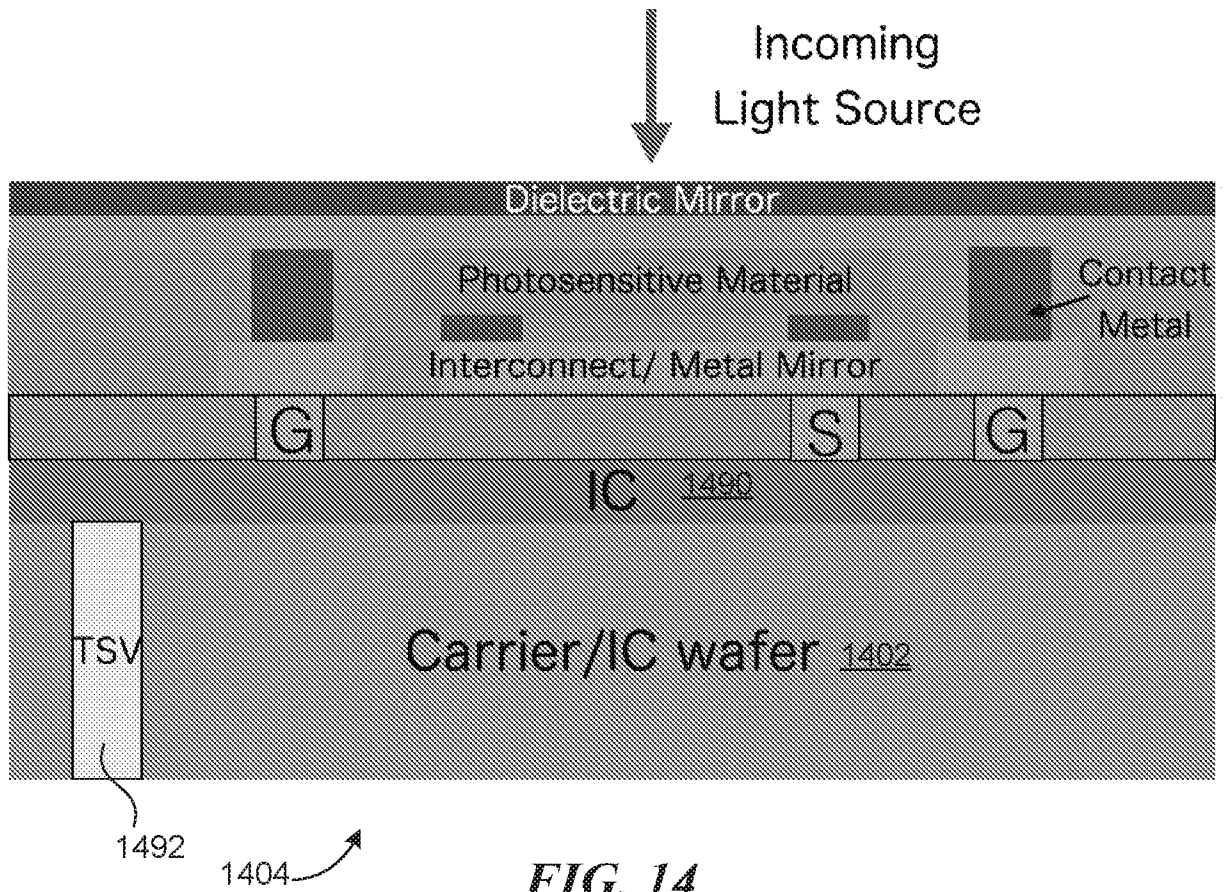


FIG. 14

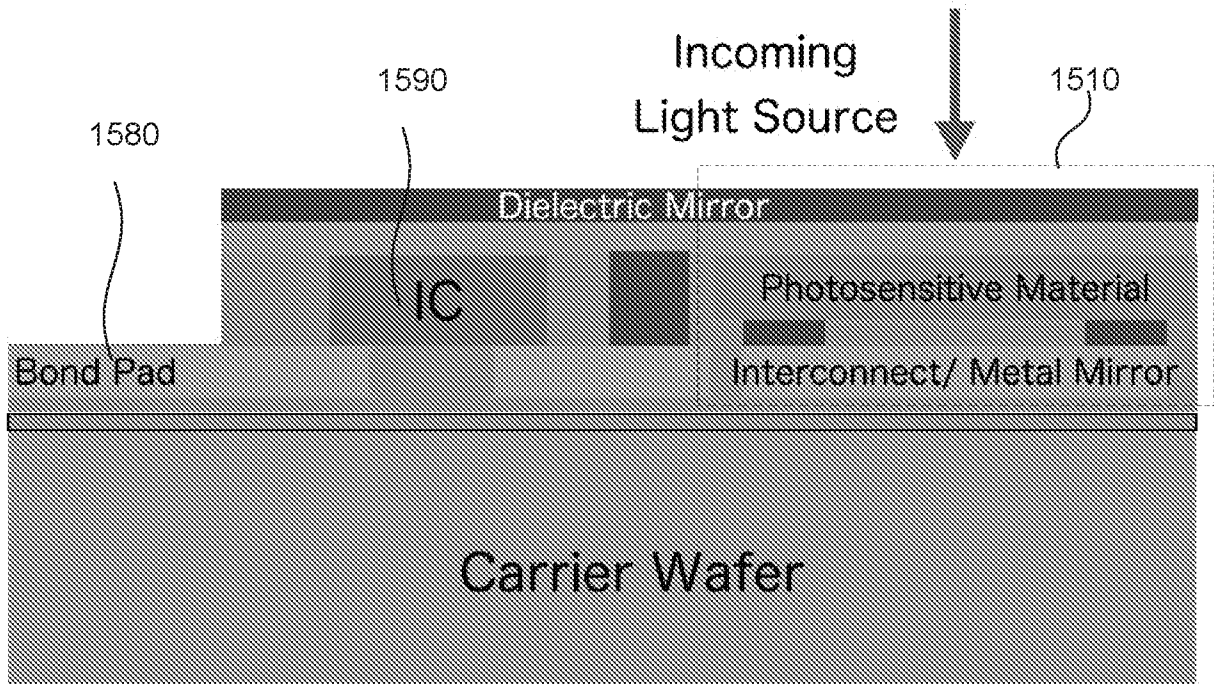


FIG. 15A

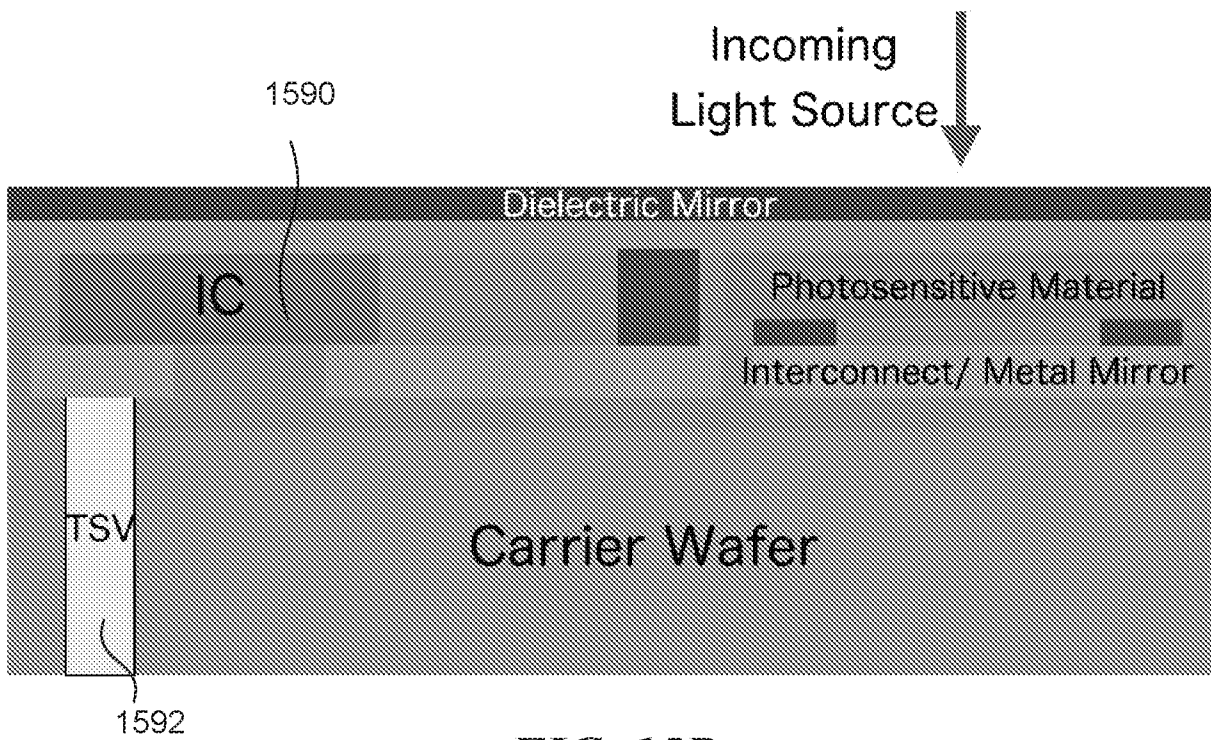


FIG. 15B

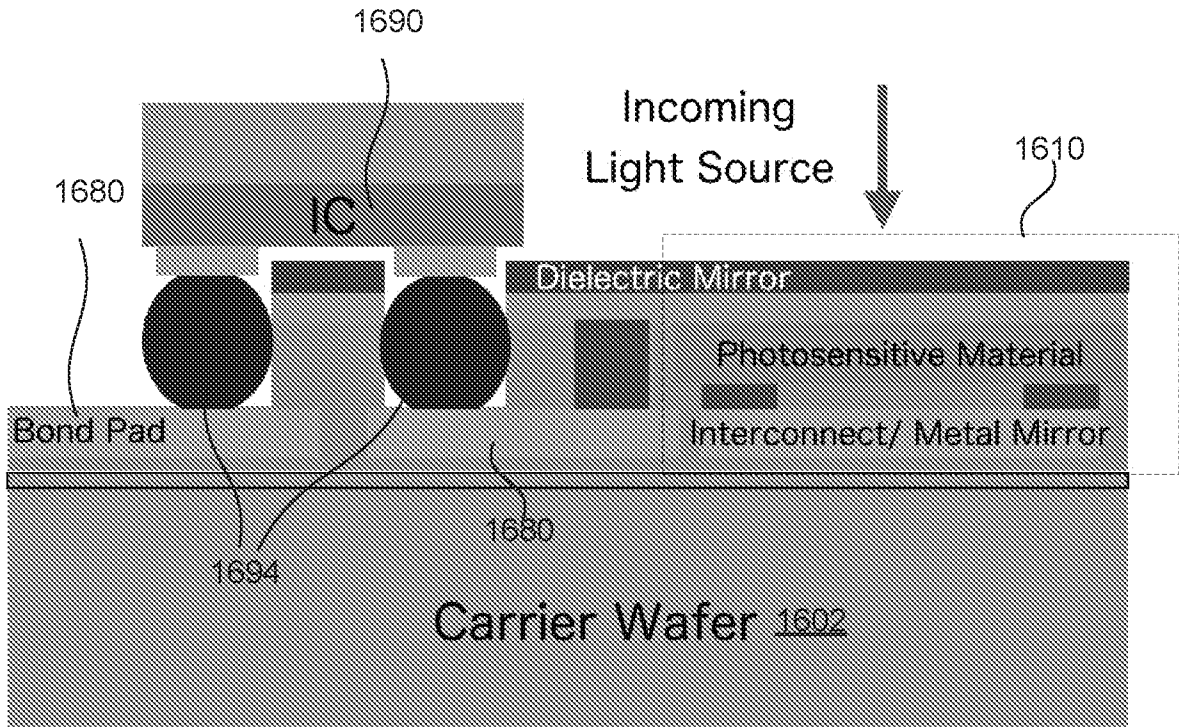


FIG. 16A

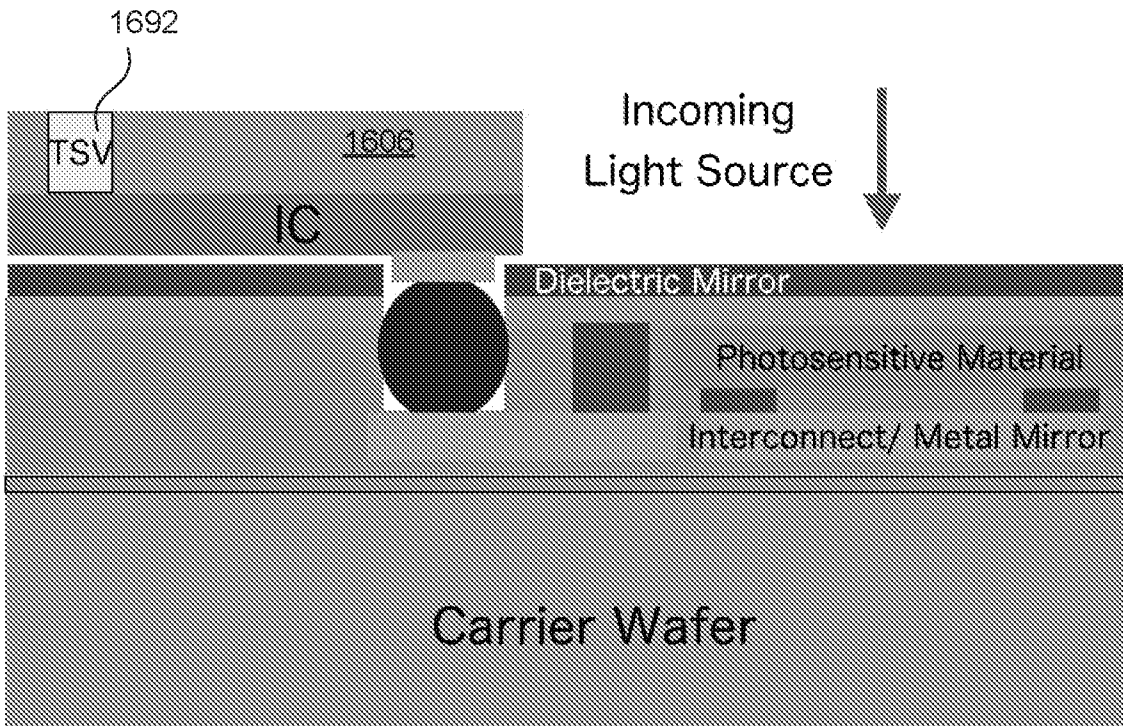


FIG. 16B

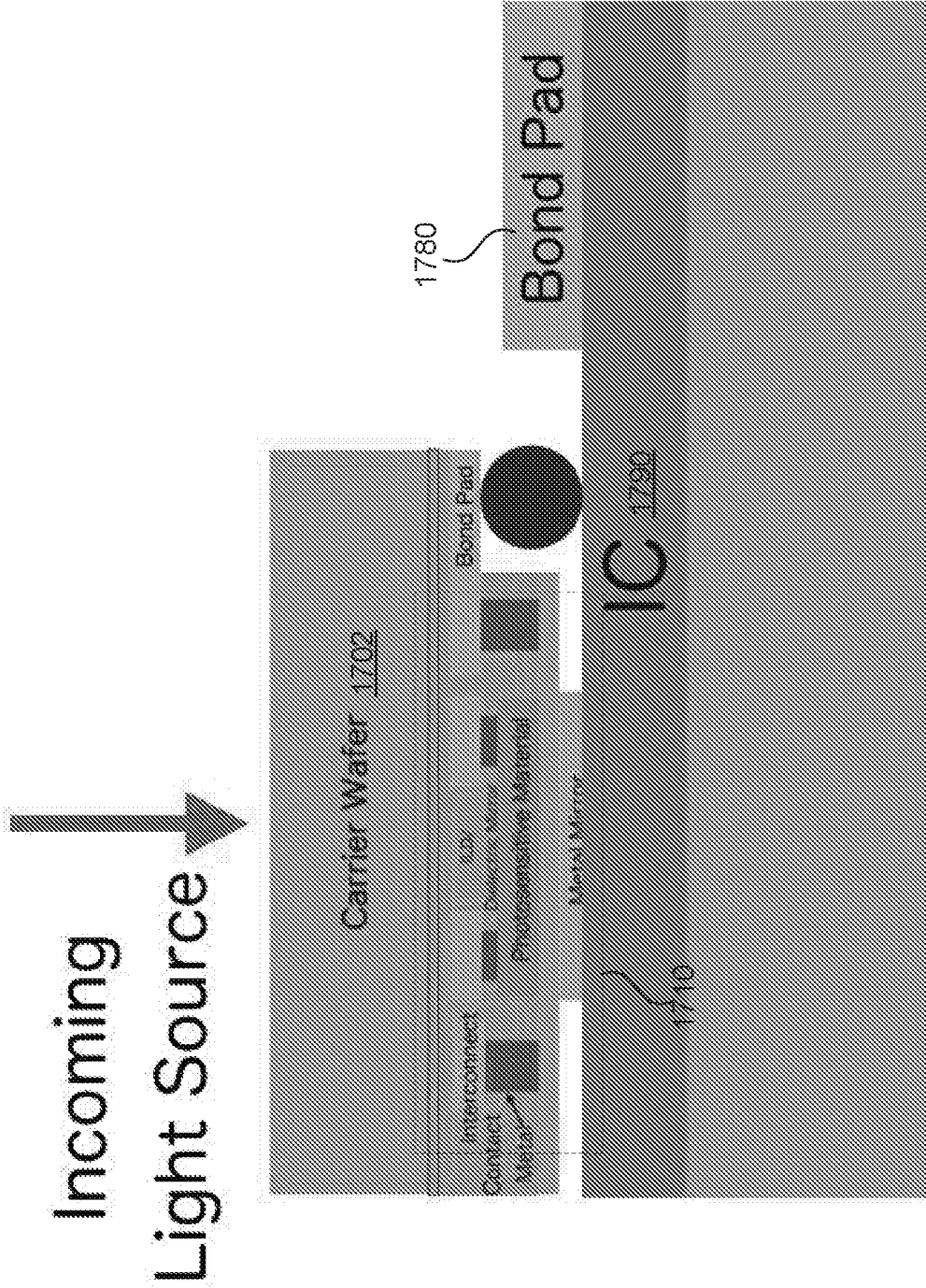


FIG. 17A

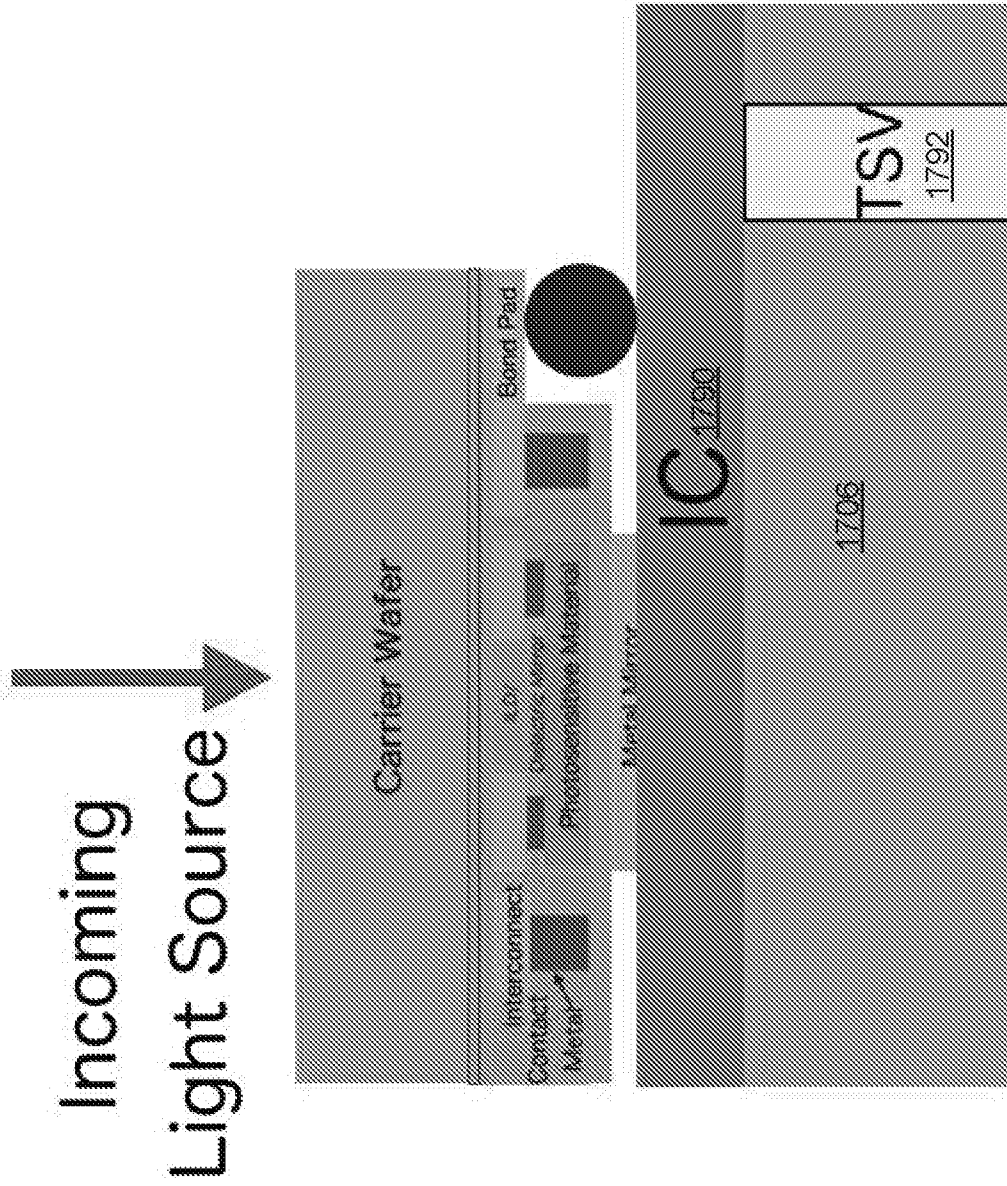


FIG. 17B

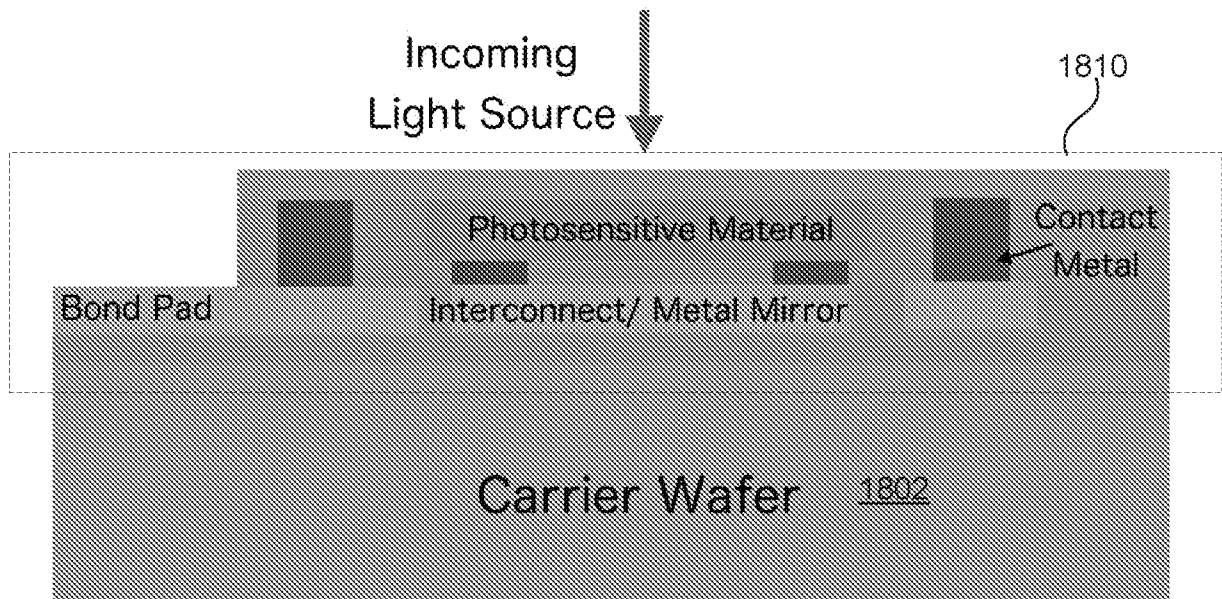


FIG. 18A

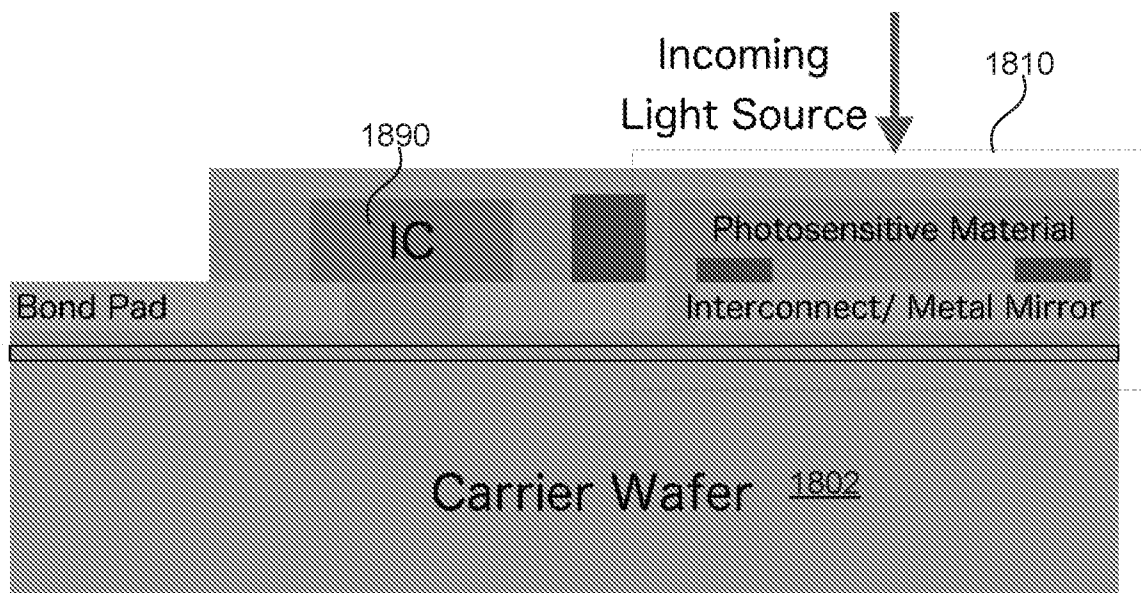


FIG. 18B

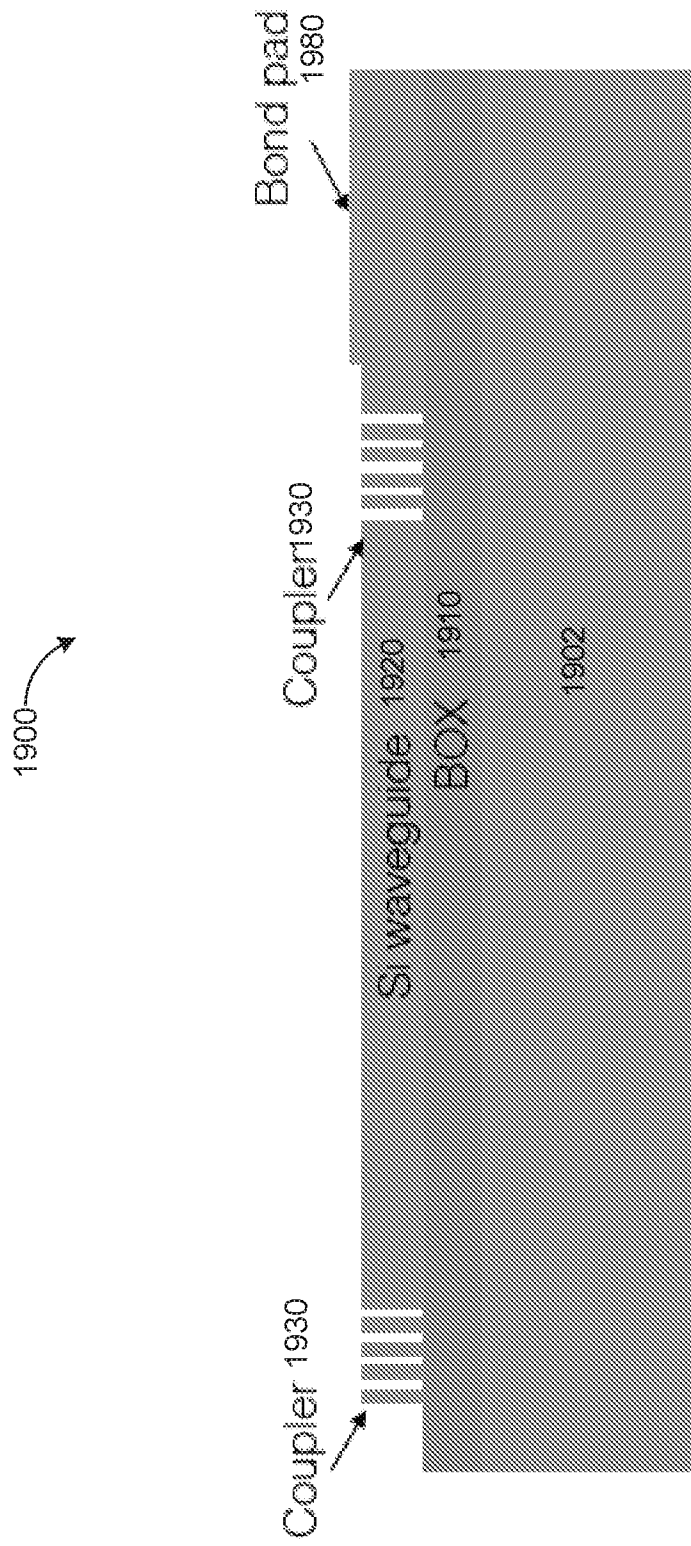


FIG. 19

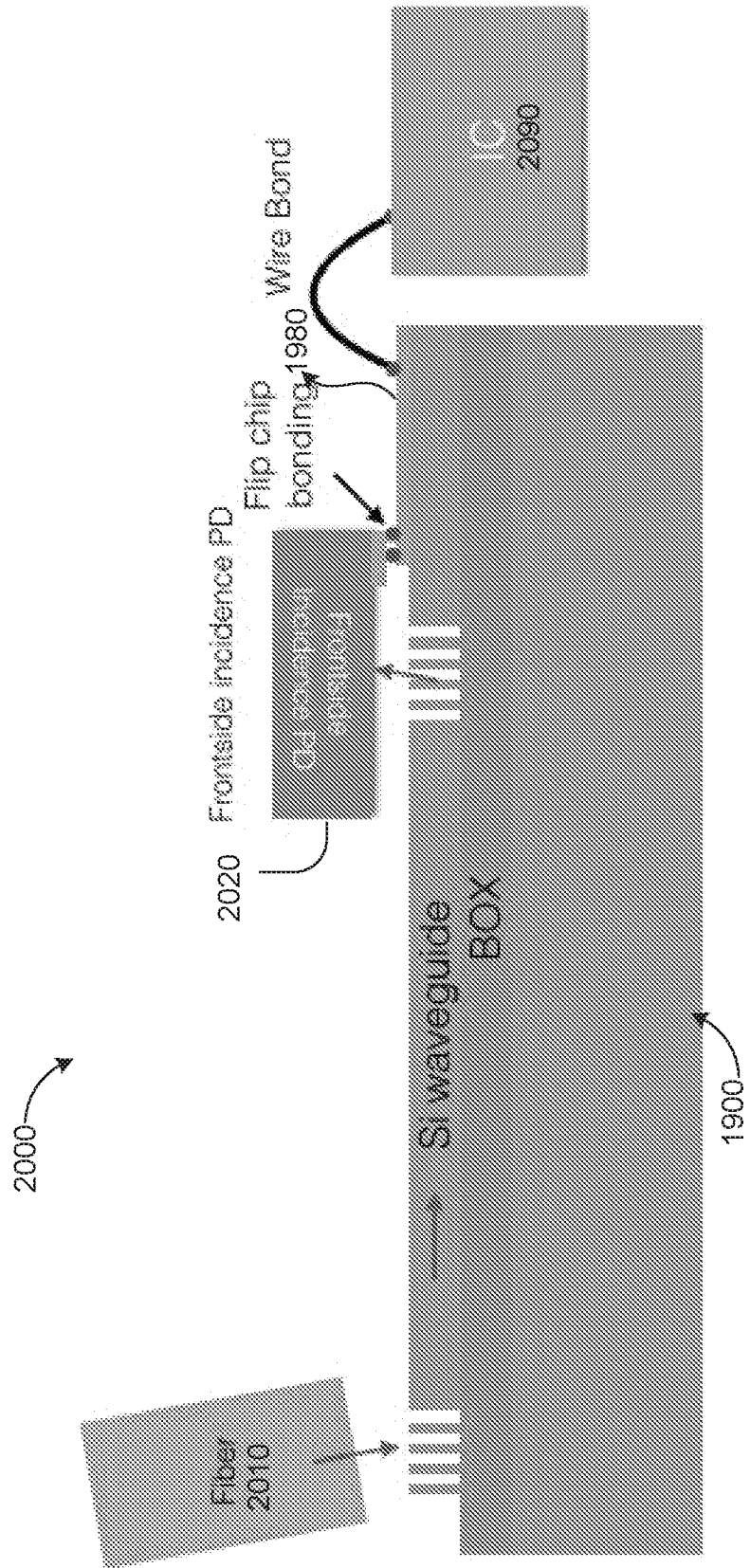


FIG. 20

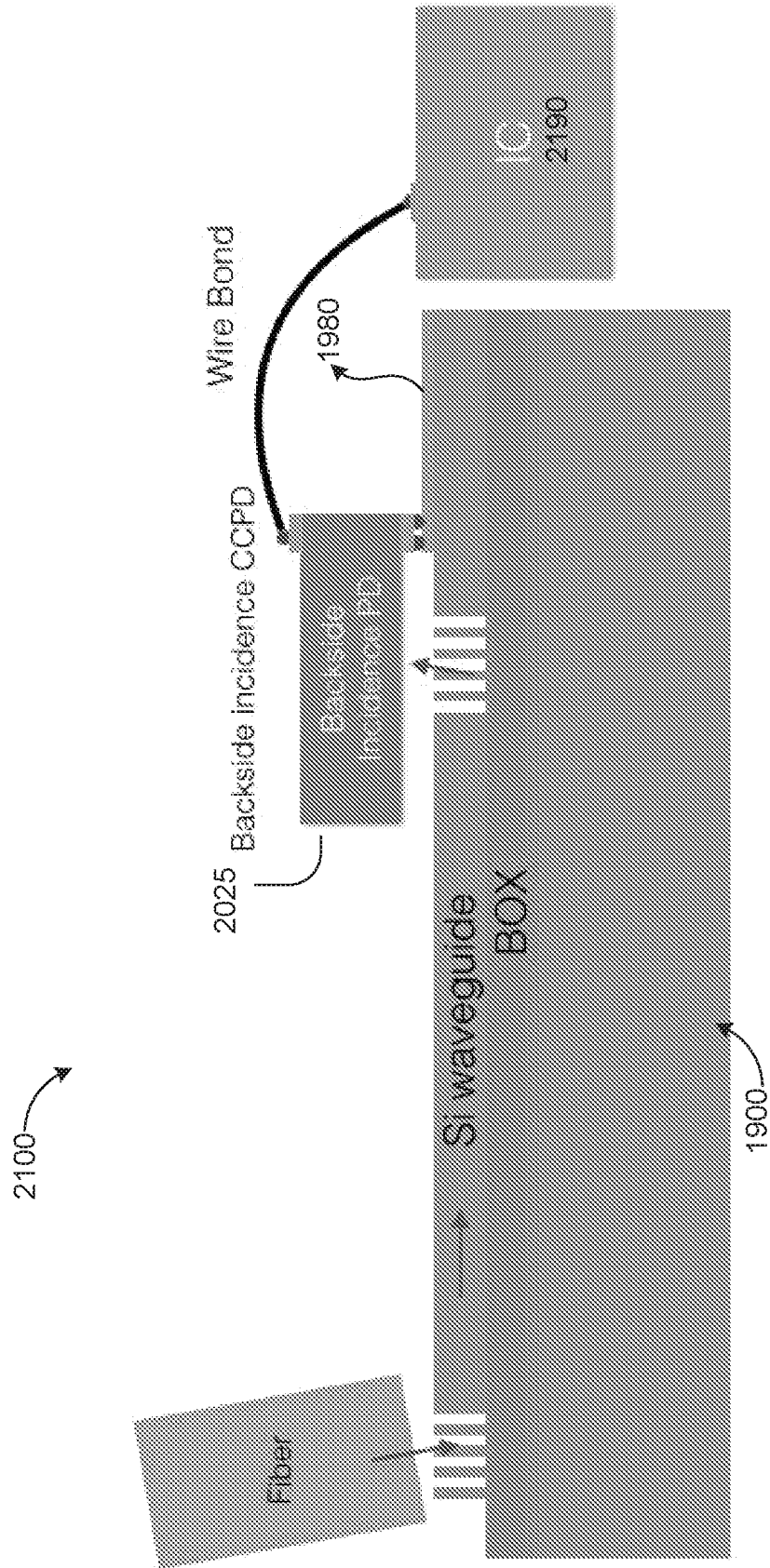


FIG. 21

50G RX

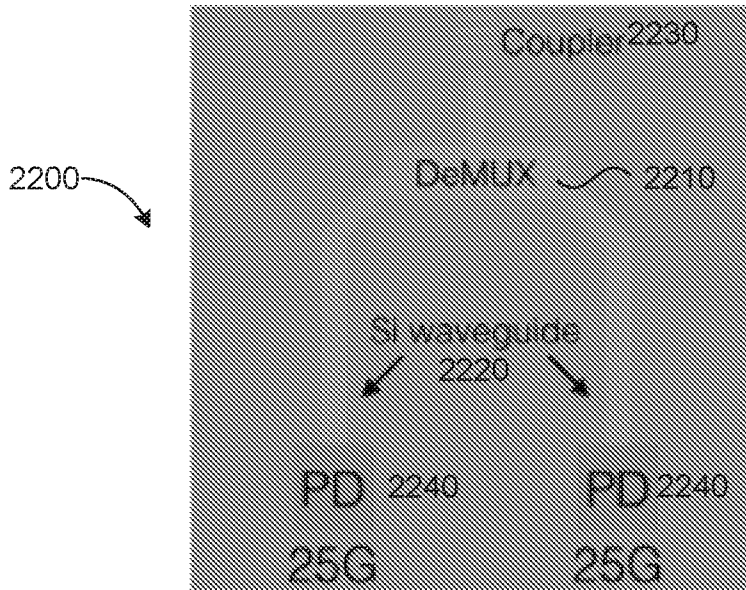


FIG. 22A

100G RX

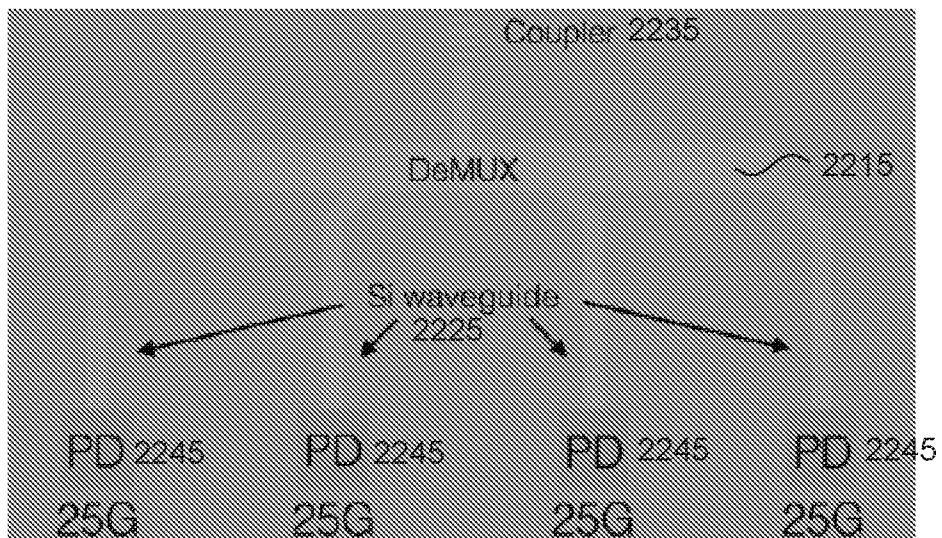


FIG. 22B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/043929**A. CLASSIFICATION OF SUBJECT MATTER****H01L 27/146(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 27/146; H01L 31/0336; H01L 31/0328; G01J 5/02; H01L 31/18; H01S 5/00; H01L 31/0232; G02F 1/19; H01L 21/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: light absorption, wafer, photodetector, mirror, bonding, interface

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2007-0190681 A1 (JONG-JAN LEE et al.) 16 August 2007 See claim 1 and figures 7-10.	1-21
A	US 2007-0002917 A1 (HONGYU DENG) 04 January 2007 See claim 1 and figures 2-4.	1-21
A	US 2014-0284450 A1 (FORELUX, INC.) 25 September 2014 See claim 1 and figure 2.	1-21
A	US 6130441 A (JOHN E. BOWERS et al.) 10 October 2000 See claim 1 and figure 4A.	1-21
A	US 8921794 B2 (JOHAN STIENS et al.) 30 December 2014 See claim 1 and figure 4a.	1-21

 Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

31 October 2016 (31.10.2016)

Date of mailing of the international search report

31 October 2016 (31.10.2016)

Name and mailing address of the ISA/KR

International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

Jang, Gijeong

Telephone No. +82-42-481-8364



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/043929

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2007-0190681 A1	16/08/2007	None	
US 2007-0002917 A1	04/01/2007	TW 200703830 A US 7983572 B2 WO 2007-005566 A2 WO 2007-005566 A3	16/01/2007 19/07/2011 11/01/2007 05/04/2007
US 2014-0284450 A1	25/09/2014	US 2015-318411 A9 US 9362428 B2	05/11/2015 07/06/2016
US 6130441 A	10/10/2000	AU 1998-78775 B2 CN 1171020 C CN 1213045 A CN 1279300 C CN 1538072 A EP 0896157 A1 EP 0896157 B1 EP 1321679 A1 EP 1321679 B1 JP 11-132197 A JP 3091179 B2 KR 10-0297572 B1 TW 402666 A US 5895204 A US 5988977 A US 6074892 A US 6147391 A US 6465803 B1 WO 97-42665 A1	06/09/2001 13/10/2004 07/04/1999 11/10/2006 20/10/2004 10/02/1999 01/10/2003 25/06/2003 06/10/2004 18/05/1999 25/09/2000 27/10/2001 21/08/2000 20/04/1999 23/11/1999 13/06/2000 14/11/2000 15/10/2002 13/11/1997
US 8921794 B2	30/12/2014	EP 2526457 A1 EP 2526457 B1 US 2012-0286163 A1 WO 2011-089243 A1	28/11/2012 20/01/2016 15/11/2012 28/07/2011