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H03D 13/00 , H03L 7/08

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H3R RFPD

(56) Documents Cited
GB 2257316 A **US 4598217 A** **US 4122404 A**

(58) Field of Search
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INT CL[5] **H03D , H03L**
Online databases: WPI, EDOC

(54) Frequency/phase comparators

(57) A frequency/phase comparator comprises two D-type flip-flops 26, 27 which are fed at respective clock ports with to signals to be compared one signal to each port, a NAND gate 28 coupled to the flip-flops so as to define a latch arrangement, and a transistor/diode voltage multiplier arrangement 30 - 33 responsive to output signals from the latch arrangement for providing an output signal in dependence upon the frequency/phase difference between the two signals to be compared. The frequency/phase comparator is intended to be operated from a small battery voltage and to provide a large error voltage to a following voltage controlled oscillator. The frequency/phase comparator may form part of a phase locked loop frequency synthesiser.

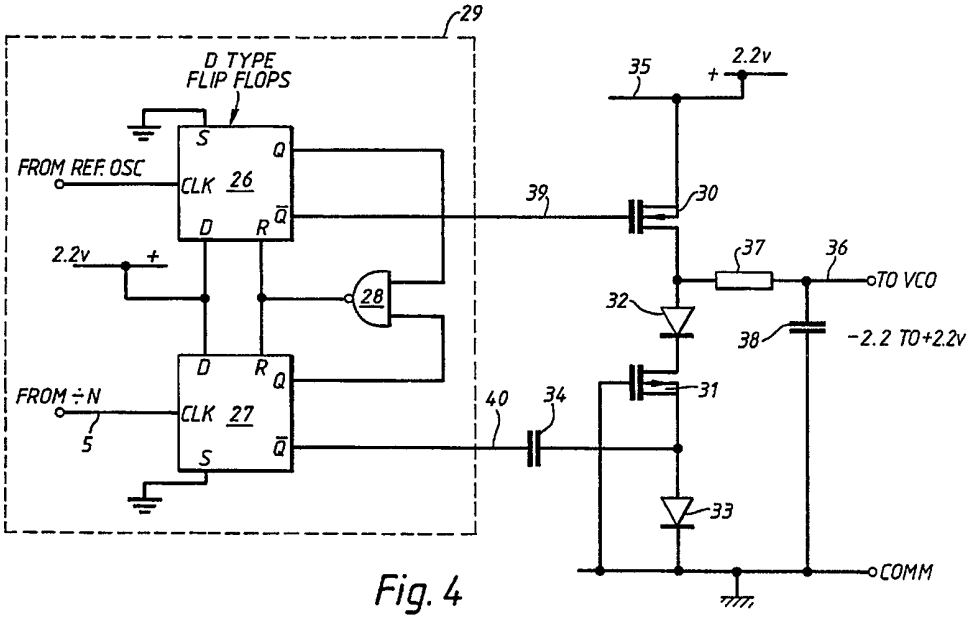

Fig. 4

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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

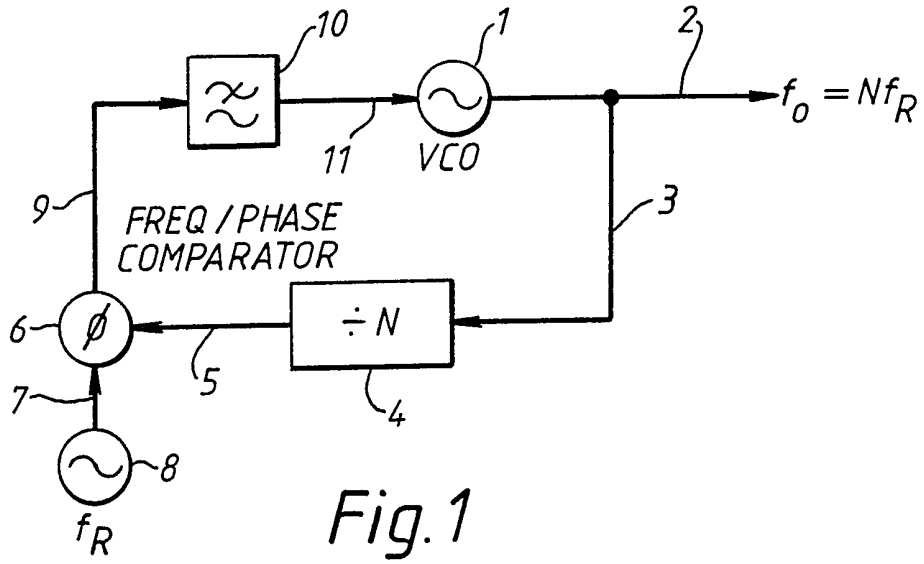

Fig. 1

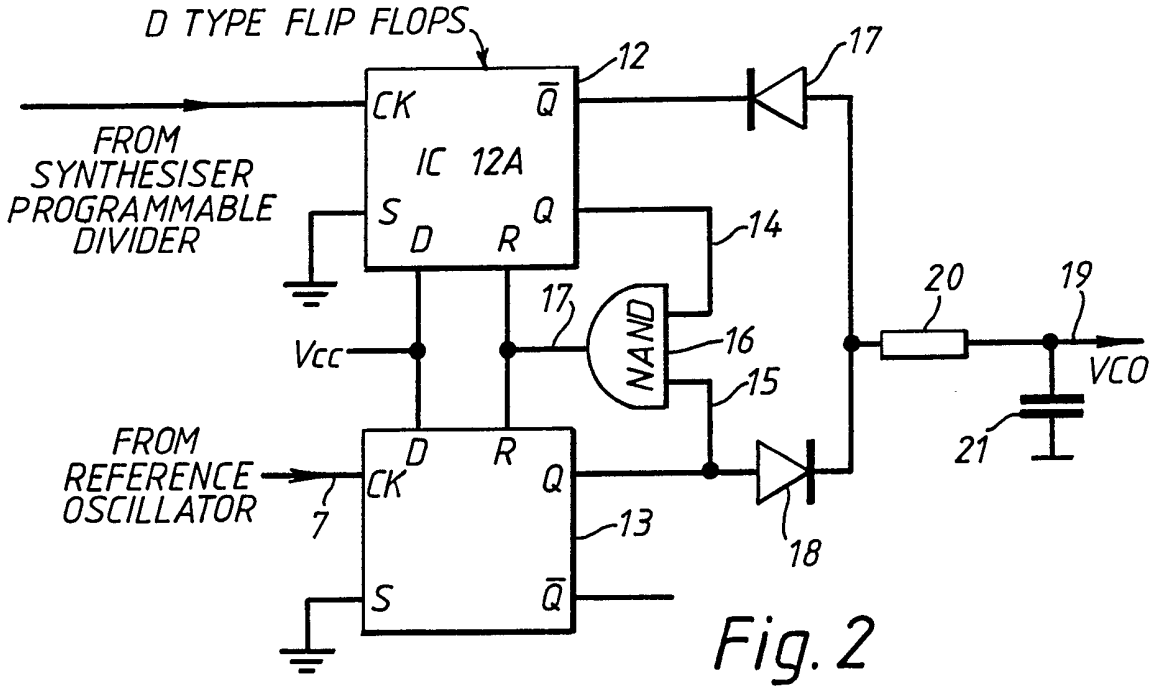

Fig. 2

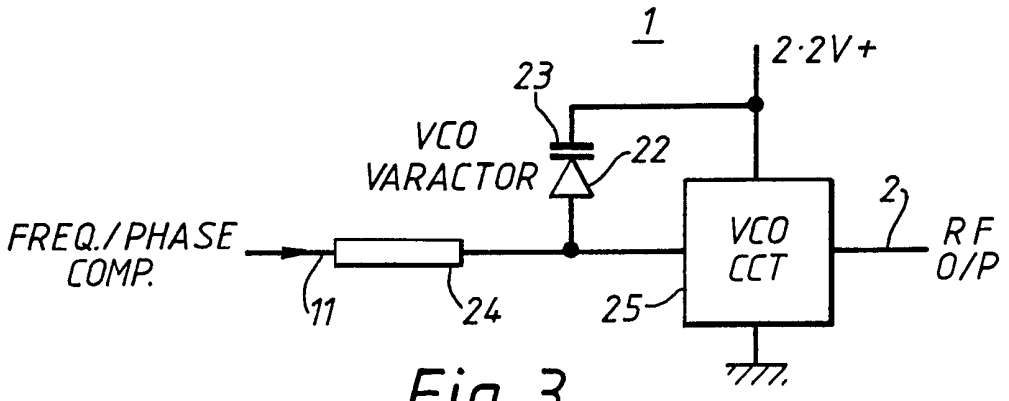

Fig. 3

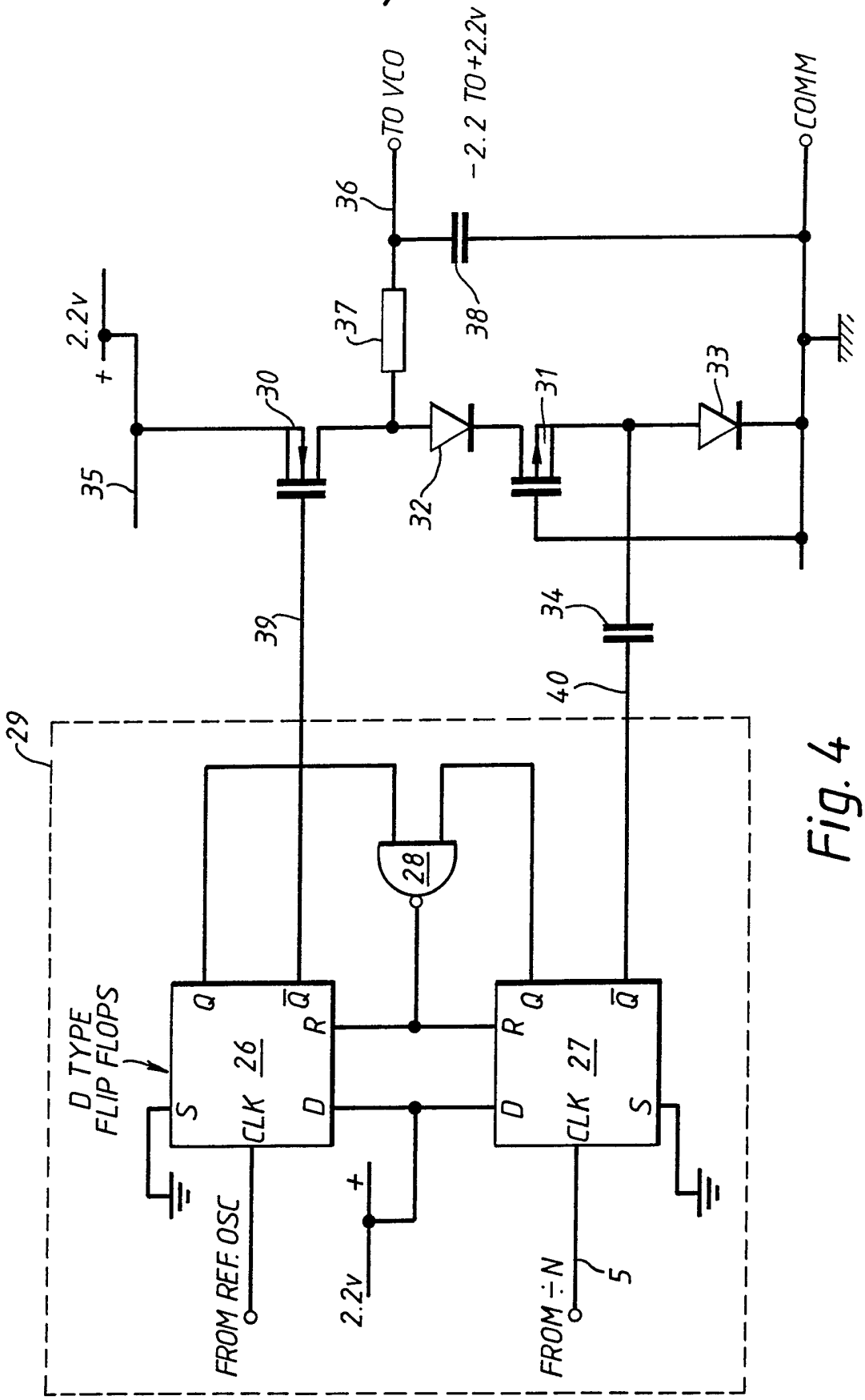
TO VCO
-2.2 TO +2.2v
COMM
2.2v
+
36
37
38
30
31
33
35
32
39
34
40
29
28
D TYPE
FLIP FLOPS
Q
$\bar{Q}$
R
S
CLK
26
D
27
FROM REF. OSC
2.2v
FROM ÷N
5

Fig. 4

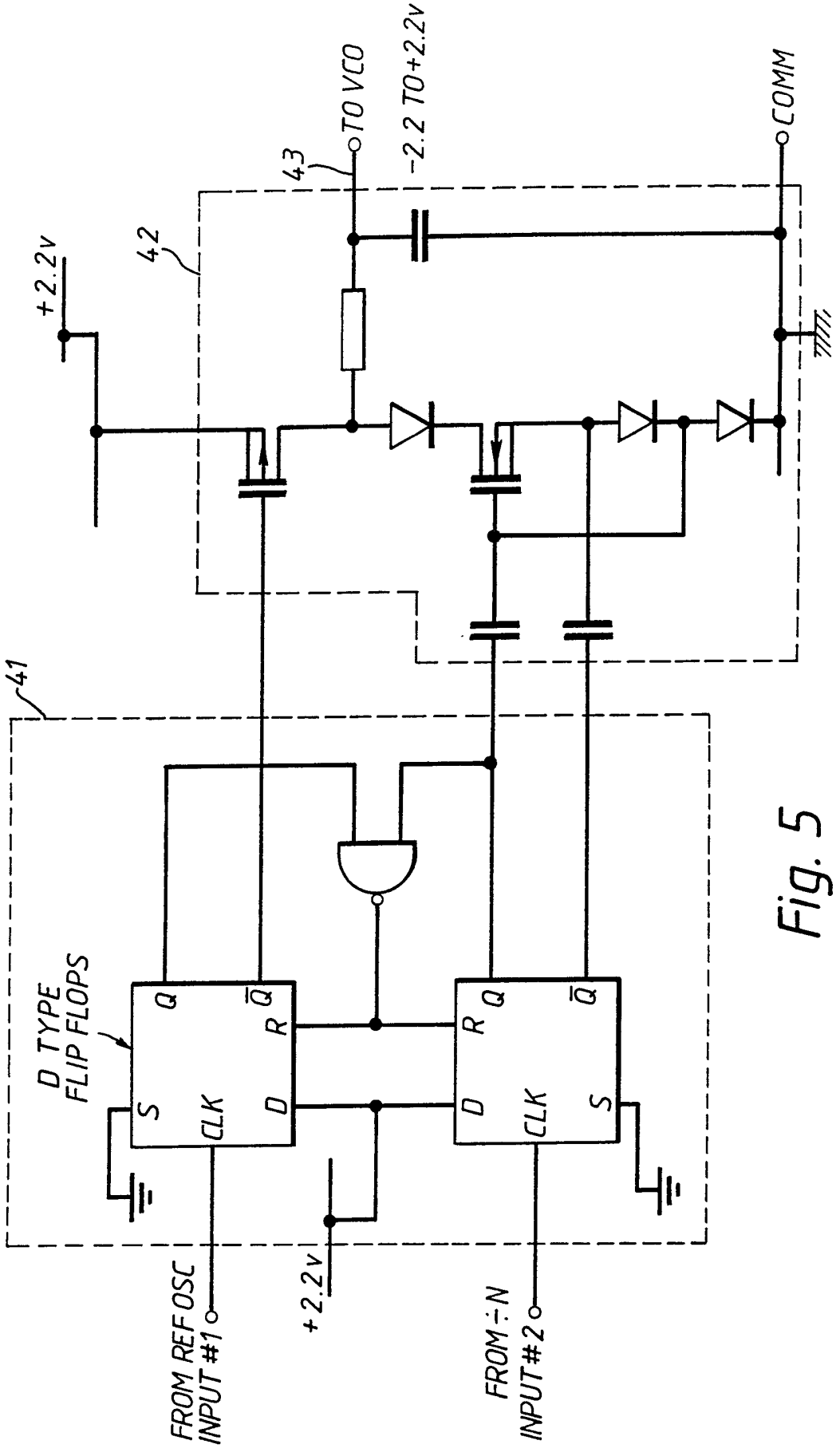
TO VCO
-2.2 TO+2.2v
COMM
43
42
+2.2v
41
D TYPE
FLIP FLOPS
Q
$\bar{Q}$
R
S
CLK
D
FROM REF OSC
INPUT #1
+2.2v
FROM ÷N
INPUT #2

Fig. 5

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IMPROVEMENTS IN OR RELATING TO FREQUENCY/PHASE COMPARATORS

This invention relates to frequency/phase comparators. More especially it relates to frequency/phase comparators for use in digital frequency synthesisers.

Digital frequency synthesisers are well known and comprise an oscillator which provides an output signal fo, which output signal is frequency/phase locked to a reference signal fr, by means of a digital phase locked loop. The term digital phase locked loop, when used herein, is defined to comprise a frequency/phase comparator and a variable divider, which variable divider serves to divide the oscillator signal fo, by a factor n so as to produce a signal fo/n which is compared in the frequency/phase comparator with the reference signal fr, thereby to provide a control signal which affords frequency control for the oscillator so that the frequency fo tends to fr.n.

Frequency/phase comparators for some applications are required to work at quite small battery voltages, i.e. 2 to 3 volts, which would normally limit the amplitude of any signal available for controlling the voltage controlled oscillator (VCO) of a synthesiser, and thus the frequency control range of the oscillator. It will be apparent to those skilled in the synthesiser art that a limited frequency control range is a serious basic design limitation and moreover small reductions in a normally low battery voltage cannot be tolerated.

It is an object of the present invention therefore to provide a frequency/phase comparator which will operate from a relatively small battery voltage and yet provide a relatively large output control voltage swing for a voltage controlled oscillator.

According to the present invention, a frequency/phase comparator comprises two D-type flip-flops which are fed at respective clock ports with two signals to be compared one signal to each port, a NAND gate coupled to the flip-flop so as to define a latch arrangement, and a transistor/diode voltage multiplier arrangement responsive to output signals from the latch arrangement for providing an output signal in dependence upon the frequency/phase difference between the said two signals to be compared.

According to one aspect of the present invention, a frequency/phase comparator comprises two D-type flip-flops which are fed at respective clock ports with two signals to be compared, one signal to each port, a NAND gate coupled to the D-type flip-flops so as to be responsive to respective Q ports of the said D-type flip-flops and to provide signals for the R ports of each flip-flop, and a transistor/diode voltage multiplier arrangement responsive to respective $\overline{Q}$ ports for providing an output signal in dependence upon the frequency/phase difference between the said two signals to be compared.

According to another aspect of the invention, a complimentary latch arrangement may be provided wherein the NAND gate is coupled to respective $\overline{Q}$ ports of the flip-flops and

wherein the transistor/diode multiplier is arranged to be responsive to respective Q ports for providing the output signal.

By using a voltage multiplier arrangement, the output voltage from the flip-flops is effectively enhanced.

The voltage multiplier arrangement may comprise two transistors and two diodes serially coupled to define a voltage doubler chain.

The voltage multiplier arrangement may alternatively comprise two transistors and three diodes serially coupled to define a voltage tripler chain.

The transistors may be complimentary metal oxide silicon field effect transistors (C-MOSFETS).

The frequency/phase comparator may form a part of a digital frequency synthesiser.

The digital frequency synthesiser may include a phase locked loop, as hereinbefore defined, which includes the said frequency/phase comparator.

One embodiment of the invention will now be described by way of example only with reference to the accompanying drawings, in which,

FIGURE 1 is a generally schematic block/circuit diagram of a digital frequency synthesiser;

FIGURE 2 is a block/circuit diagram of a known frequency/phase comparator;

FIGURE 3 is a simplified block/circuit diagram of a VCO arrangement;

FIGURE 4 is a generally schematic block/circuit diagram of a frequency/phase comparator, according to one embodiment of the present invention; and

FIGURE 5 is a generally schematic block/circuit diagram of a frequency/phase comparator, according to an alternative embodiment of this invention.

Referring now to Figure 1, a digital frequency synthesiser comprises a VCO 1 which provides an output signal fo on a line 2. A sample of the output signal is fed via a line 3 to a variable divider 4 which divides by a factor n, so as to provide one signal on a line 5 for a frequency/phase comparator 6. The other signal input for the frequency/phase comparator is fed thereto on a line 7 from a reference frequency generator 8 which produces a reference frequency fr. An output signal from the frequency/phase comparator is provided on a line 9 and fed via a low pass filter 10 to a control port 11 of the VCO 1. The digital frequency synthesiser just before described is a conventional divide by n synthesiser. The output signal fo is divided down by the divider 4 which may be a programmable divider, the programmable divider being designed to divide by any whole number up to a maximum determined by the complexity of the arrangement. The output signal from the divider on the line 5 is compared with the frequency of the reference frequency source fr in the frequency/phase comparator 6. Thus, it will be appreciated that the frequency of the VCO 1 is controlled in dependence upon the signal on the line 9, so that the frequency of the signal from the variable divider 4 on the line 5 is phase locked to the

frequency of the reference frequency oscillator 8. It will also be appreciated that the output frequency of the VCO 1 is n times the frequency fr. If fr is the channel frequency spacing then it is apparent that a desired channel can be selected in accordance with the setting of n.

Referring now to Figure 2, a typical frequency/phase comparator corresponding to the frequency/phase comparator 6, shown in Figure 1, comprises two D-type flip-flops 12 and 13. The D-type flip-flop 12 is fed via the line 5, as shown in Figure 1, from the variable divider 4 and the D-type flip-flop 13 is fed via the line 7, as shown in Figure 1, from the reference frequency oscillator 8. The lines 5 and 6 are connected to the clock ports ck of the D-type flip-flops 12 and 13 respectively. Q ports of the flip-flops 12 and 13 respectively, are connected via lines 14 and 15 respectively, to a NAND gate 16 thereby to define a latch arrangement. An output line 17 from the NAND gate 16 is connected to R ports of the flip-flops 12 and 13 respectively. S ports of the flip-flops 12 and 13 are respectively earthed and D ports of the flip-flops are respectively connected a voltage supply rail VCC. Output signals from the $\bar{Q}$ port of the D-type flip-flop 12 and the Q port of the D-type flip-flop 13 are fed via diodes 17 and 18 respectively, to an output line 19 via resistive and capacative smoothing components 20 and 21 respectively.

The frequency/phase detector just before described with reference to Figure 1 is a well known arrangement which comprises in effect a conventional latch arrangement. In

operation, the $\overline{Q}$ outputs of one or other of the D-type flip-flops (latches) goes 'low' depending upon whether the two signals applied to the clock inputs ck are leading or lagging each other. Thus, a signal is developed on the line 19, the amplitude of which is dependent upon the relative phase relationship between the signals on the lines 5 and 7. This voltage is applied as shown in Figure 1 to the VCO 1, which is shown in greater detail in Figure 3.

Referring now to Figure 3, the VCO 1 is fed via the input port 11 from the frequency/phase comparator 6. The VCO comprises a varactor diode 22 having a capacitance 23 (shown schematically), which varies in accordance with the voltage applied thereto from the line 11 via an input resistor 24. The capacitance 23 forms part of a VCO oscillator circuit 25, which is not shown in detail, and thus the frequency of the output signal on the line 2 from the VCO 1 will be varied in accordance with the amplitude of the voltage applied on the line 11.

As hereinbefore explained, one of the problems with this known arrangement is that if the supply voltage VCC, as shown in Figure 2, of the frequency/phase comparator is small, a correspondingly small voltage will be applied to the VCO input line 11 which will produce a correspondingly small frequency swing on the line 2, as shown in Figure 3.

In order to overcome this problem, in accordance with one embodiment of the invention, a frequency/phase comparator is provided, conventionally comprising D-type flip-flops 26 and 27, operatively associated with a NAND gate 28, as shown within the broken line 29, to define a latch arrangement, which feeds a

voltage doubler arrangement. The voltage doubler arrangement comprises complimentary C-MOS transistors 30 and 31, serially coupled with diodes 32 and 33. The gate of the C-MOS transistor 30 is fed from the $\bar{Q}$ port of the D-type flip-flop 26, and the drain of the C-MOS transistor 31 is fed from the Q port of D-type flip-flop 27 via a capacitor 34 at a junction between the drain and the diode 33. The serial voltage doubler chain thus produced is fed from a supply line 35, which is coupled to a 2.2 volt supply voltage source. An output signal is developed on a line 36 across resistive and capacitive smoothing components 37 and 38 respectively, which is variable between -2.2 volts and +2.2 volts in accordance with the frequency/phase relationship between the signals from the reference oscillator 8 on the line 7 and the divider 4 on the line 5. Thus, it will be appreciated that output signals from the D-type flip-flops 26 and 28, on lines 39 and 40 respectively, provide an output which pulses positive or negative in dependence upon whether the phases of the signals being compared are leading or lagging, and is high impedance if the two signals are in phase. The output signal produced is effectively filtered by the resistive/capacitive components 37, 38 to provide the dc control voltage. Thus, the most positive output voltage produced will be approximately equal to the supply voltage, and as will be appreciated by those skilled in the art, higher positive voltages are not normally permitted with the C-MOS technology used. The phase detector output can now however extend negative below ground potential due the voltage doubling action created by the diode 33 and the capacitor 34 associated with the n

type MOSFET 31, and for a 2.2 volt positive supply a negative excursion of -2.2 volt is available.

In order to provide still more voltage, a voltage tripler arrangement may be provided, as shown in Figure 5, wherein the conventional D-type flip-flops and NAND gate latch arrangement is enclosed within a broken line 41, which is arranged to feed a voltage tripler arrangement enclosed within a broken line 42, which feeds an output line 43 for a VCO. Operation of the voltage tripler arrangement will be well understood by those skilled in the art, and so further detailed operational discussion is believed to be unnecessary.

Various modifications may be made to the arrangement just before described without departing from the scope of the invention, and for example, it will be appreciated that although C-MOS transistors are used in the arrangement just before described, bi-polar transistors may equally well be used. Additionally it will be appreciated that a complimentary latch arrangement may be provided which may be suitable for some varactor controlled systems.

CLAIMS

1. A frequency/phase comparator comprising two D-type flip-flops which are fed at respective clock ports with two signals to be compared one signal to each port, a NAND gate coupled to the flip-flop so as to define a latch arrangement, and a transistor/diode voltage multiplier arrangement responsive to output signals from the latch arrangement for providing an output signal in dependence upon the frequency/phase difference between the said two signals to be compared.

2. A comparator as claimed in claim 1, wherein the NAND gate is coupled to the D-type flip-flops so as to be responsive to respective Q ports of the said D-type flip-flops and to provide signals for the R port of each flip-flop, and wherein the transistor/diode voltage multiplier arrangement is responsive to respective $\overline{Q}$ ports for providing the output signal in dependence upon the frequency/phase difference between the said two signals to be compared.

3. A comparator as claimed in claim 1 or claim 2, wherein the voltage multiplier arrangement comprises two transistors and two diodes serially coupled to define a voltage doubler chain.

4. A comparator as claimed in claim 1 or claim 2, wherein the voltage multiplier arrangement comprises two transistors and three diodes serially coupled to define a voltage tripler chain.

5. A comparator as claimed in claim 3 or claim 4, wherein the transistors are complementary metal oxide silicon field effect transistors (C-MOSFETS).

6. A frequency/phase comparator as claimed in claim 1 and as hereinbefore described with reference to the accompanying drawings.

7. A frequency synthesiser including a frequency/phase comparator as claimed in any preceding claim.

8. A synthesiser as claimed in claim 7, including a phase locked loop, as hereinbefore defined, which includes the said frequency/phase comparator.

9. A frequency synthesiser including a frequency/phase comparator as claimed in claim 1 and as hereinbefore described with reference to the accompanying drawings.

Patents Act 1977
Examiner's report to the Comptroller under Section 17 (The Search Report) -11-

Application number

GB 9310208.5

Relevant Technical fields

(i) UK Cl (Edition L) H3R: RFDX, RPDA, RFPD;
H3A: ASX, AXX

(ii) Int Cl (Edition 5) H03D, H03L

Search Examiner

MR S SATKURUNATH

Databases (see over)

(i) UK Patent Office

(ii) ONLINE DATABASES: WPI, EDOC

Date of Search

12 JULY 1993

Documents considered relevant following a search in respect of claims 1-9

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
A	GB 2257316 A (FERRANTI) see Figure 3	1
X	US 45982107 (PREDINA) see Figure 3 and lines 43-50 in column 2	1
A	US 4122404 (FUHRMAN) see Figures 1, 2	1

		Relevant to claim(s)

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

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