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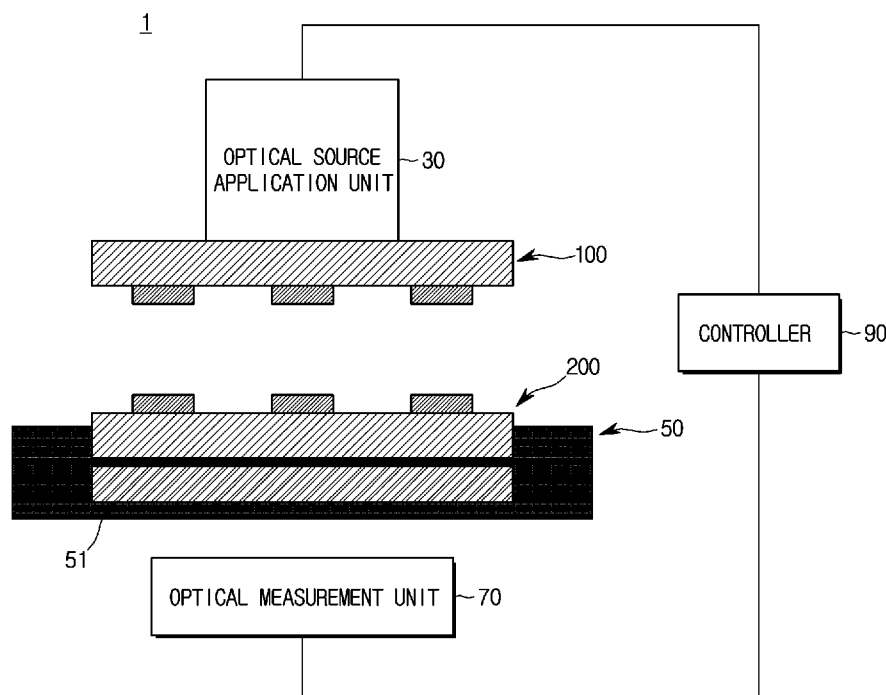
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(54) Title: WAFER PROBE CARD, ANALYSIS APPARATUS INCLUDING THE SAME, AND METHOD OF FABRICATING THE WAFER PROBE CARD



(57) Abstract: Provided are a wafer probe card that matches in one-to-one correspondence with an LED wafer by implementing a probe system having the same size as the LED wafer, and inspects brightness and wavelength of light emitted from a plurality of LEDs provided on the LED wafer at once by controlling the plurality of LEDs to emit light, an analysis apparatus including the same, and a method of fabricating the wafer probe card.

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Description

Title of Invention: WAFER PROBE CARD, ANALYSIS APPARATUS INCLUDING THE SAME, AND METHOD OF FABRICATING THE WAFER PROBE CARD

Technical Field

- [1] Example embodiments of the present disclosure relate to a wafer probe card for evaluating micro light emitting diodes (LEDs), an analysis apparatus including the same, and a method of fabricating the wafer probe card.

Background Art

- [2] Light-emitting devices such as light-emitting diodes (LED) or vertical cavity surface emitting laser diode (VCSELs) are inspected to evaluate electrical and optical characteristics thereof after completing the manufacture thereof.
- [3] According to conventional inspection methods, a small electrified probe may be brought into direct contact with an LED provided on a wafer to supply a current to the LED such that the LED emits light. An analysis system may acquire electrical and optical properties of light emitted from each LED provided on the wafer in the form of Blue Tape data.
- [4] Based on the data obtained as described above, manufacturers of high-brightness LED devices separate the LEDs from the wafer and supply the LEDs in accordance with wavelength and brightness required in a manufacturing process.
- [5] According to the conventional inspection methods, since LED devices including sapphire provided on a wafer may be larger in size, the LED devices may be sufficiently inspected by using the probe. However, in recent LED display apparatuses in which LEDs are used as display pixels, each LED is becoming smaller to several tens of micrometers (μm) in size.
- [6] When used to inspect LED devices having a size of several tens of micrometers (μm), the conventional inspection methods using a probe are not efficient since an inspection time increases due to inefficient supply of currents and frequent breakage of the probe.

Disclosure of Invention

Technical Problem

- [7] One or more example embodiments of the present disclosure provide a wafer probe card that matches in one-to-one correspondence with an LED wafer by implementing a probe system having the same size as the LED wafer and inspects brightness and wavelength of a plurality of LEDs at once by controlling the plurality of LEDs to emit light, an analysis apparatus including the same, and a method of fabricating the wafer

probe card.

Solution to Problem

- [8] According to an aspect of an example embodiment, there is provided a wafer probe card including a substrate, an insulating layer formed on the substrate, a plurality of first pads and a plurality of second pads formed on the insulating layer, and a plurality of rear pads respectively connected to the plurality of first pads and the plurality of second pads via through silicon vias (TSVs), wherein the plurality of first pads and the plurality of second pads are configured to transfer electrical signals to electrode pads of a light emitting diode (LED) wafer.
- [9] The plurality of first pads may be connected to each other by an electric wiring in a first direction through the TSVs, and the plurality of second pads are connected to each other using an electric wiring in a second direction through the TSVs
- [10] The substrate may be formed of silicon.
- [11] The wafer probe card may include holes for alignment with the LED wafer.
- [12] The plurality of first pads may be formed by deposition after etching the insulating layer.
- [13] An anisotropic conductive film (ACF) and a polyimide (PI) film may be formed on the plurality of rear pads.
- [14] According to an aspect of another example embodiment, there is provided an analysis apparatus including an optical source application unit configured to transmit power to a wafer probe card;
- [15] an optical measurement unit configured to collect light emitted from a plurality of light emitting diodes (LEDs); and
- [16] a controller processor configured to execute instructions to control the optical source application unit and analyze the plurality of LEDs based on measurement results received from the optical measurement unit, wherein the wafer probe card comprises a substrate, an insulating layer formed on the substrate, a plurality of first pads and a plurality of second pads formed on the insulating layer, and a plurality of rear pads connected to each of the plurality of first pads and the second pads using through silicon vias (TSVs), wherein the plurality of first pads and the second pads are configured to transfer power from the optical source application unit to the plurality of LEDs.
- [17] The processor may be further configured to control the optical source application unit to alternately apply the power.
- [18] The plurality of first pads may be connected to each other by an electric wiring in a first direction through the TSVs, and the plurality of second pads may be connected to

each other by an electric wiring in a second direction through the TSVs.

[19] The processor may be further configured to create map data on the plurality of LEDs based on the measurement results, and the analysis apparatus may be further comprise a storage unit configured to store the created map data.

[20] The processor may be further comprise a stage on which a wafer comprising the plurality of LEDs is placed, wherein the stage may be comprise a glass window configured to transmit emitted light, and the optical measurement unit may be further configured to collectcollects light passing through the glass window.

[21] According to an aspect of another example embodiment, there is provided a method of fabricating a wafer probe card, the method including preparing a substrate having an insulating layer formed to expose a plurality of first pads, forming a plurality of second pads on the insulating layer; and forming a plurality of rear pads formed on a surface opposite to a surface of the substrate provided with the insulating layer, wherein the plurality of rear pads are connected to the plurality of first pads and the plurality of second pads using through silicon vias (TSVs).

[22] The method may further include leveling the plurality of first pads and the plurality of second pads.

[23] The method may further include forming an anisotropic conductive film (ACF) to the plurality of rear pads, and forming a polyimide (PI) film on the ACF.

[24] The preparing of the substrate may include etching a photoresist and depositing the plurality of first pads after forming the insulating layer on the substrate, and the forming of the plurality of first pads may include etching the insulating layer provided with the first pads and re-depositing the first pads after depositing the second pads.

Advantageous Effects of Invention

[25] According to the wafer probe card, the analysis apparatus including the same, and the method of fabricating the wafer probe card, the wafer probe card may match in one-to-one correspondence with the LED wafer by implementing a probe system having the same size as the LED wafer and inspect brightness and wavelength of a plurality of LEDs at once by controlling the plurality of LEDs to emit light.

Brief Description of Drawings

[26] The above and/or other aspects of the disclosure will become apparent and more readily appreciated from the following description of the example embodiments, taken in conjunction with the accompanying drawings of which:

[27] FIG. 1 is a schematic diagram illustrating an analysis apparatus including a wafer probe card according to an example embodiment;

[28] FIG. 2 is a view for comparing a wafer probe card and an LED wafer according to an example embodiment;

- [29] FIGs. 3A and 3B are examples describing the operation of analysis apparatuses including different wafer probe cards according to example embodiments;
- [30] FIGs. 4A and 4B are top and bottom views of a wafer probe card according to an example embodiment;
- [31] FIG. 5 is a view for describing an operating method of a wafer probe card 100 according to an example embodiment;
- [32] FIG. 6 is a flowchart for describing a method of fabricating a wafer probe card according to an example embodiment; and
- [33] FIGs. 7 to 20 are diagrams for describing the method of fabricating the wafer probe card according to example embodiments.

Best Mode for Carrying out the Invention

- [34] Reference will now be made in detail to the example embodiments of the present disclosure, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to like elements throughout. This specification does not describe all elements of the embodiments of the present disclosure and detailed descriptions on what are well known in the art or redundant descriptions on substantially the same configurations may be omitted. As used herein, the terms "unit," "module," "member," and "block" may be implemented using a software or hardware component. According to an example embodiment, a plurality of "units," "modules," "members," and "blocks" may also be implemented using one element, and one "unit," "module," "member," and "block" may include a plurality of elements.
- [35] Throughout the specification, when an element is referred to as being "connected to" another element, it may be directly or indirectly connected to the other element and the "indirectly connected to" includes connected to the other element via a wireless communication network.
- [36] Also, it is to be understood that the terms "comprise," "include," and "have" indicate the existence of elements disclosed in the specification, but does not preclude the possibility that one or more other elements may exist or may be added.
- [37] Throughout the specification, it will be understood that when one element, is referred to as being "on" another element, it can be directly on the other element, or intervening elements may also be present therebetween.
- [38] It will be understood that, although the terms "first", "second", etc., may be used herein to describe various elements, these elements should not be limited by these terms. The above terms are used only to distinguish one component from another.
- [39] An expression used in the singular encompasses the expression of the plural, unless it has a clearly different meaning in the context.
- [40] The reference numerals used in operations are used for descriptive convenience and

are not intended to describe the order of operations and the operations may be performed in a different order unless otherwise stated.

[41] FIG. 1 is a schematic diagram illustrating an analysis apparatus including a wafer probe card according to an example embodiment.

[42] Referring to FIG. 1, an analysis apparatus 1 may include a wafer probe card 100, an optical source application unit 30 configured to apply a current or voltage to the wafer probe card 100, a light-emitting diode (LED) wafer 200 configured to emit light upon receiving the current or voltage from the wafer probe card 100, a glass window 51 configured to transmit light emitted from LEDs included in the LED wafer 200, an optical measurement unit 70 configured to measure wavelength or brightness of light emitted from the LEDs included in the LED wafer 200, and a controller 90 configured to create map data based on signals received from the optical measurement unit 70 and control the overall operation of the analysis apparatus 1.

[43] Particularly, the wafer probe card 100 may be provided in the same size as the LED wafer 200 to correspond to the LED wafer 200 and may transfer a current or voltage to the LED wafer 200 through pads 110 and 130 as illustrated in FIG. 3.

[44] The LED wafer 200 is a target object to be analyzed by the analysis apparatus 1 and placed on a stage 50 of the analysis apparatus 1.

[45] The LED wafer 200 includes LEDs of a predetermined size which includes electrode pads 210 and 230 as illustrated in FIG. 3 which may be brought into contact with the pads 110 and 130 of the wafer probe card 100, respectively.

[46] The optical source application unit 30 may transmit a voltage or current to the wafer probe card 100 in accordance with a control signal of the controller 90 and is connected specifically to a polyimide (PI) film 170 as illustrated in FIG. 20 included in the wafer probe card 100.

[47] The optical measurement unit 70 may receive light emitted from the LEDs and transmit the measurement results to the controller 90. Specifically, the optical measurement unit 70 may measure an amount of the emitted light and collect a spectrum of light. The optical measurement unit 70 may convert the received light into an electrical signal by analyzing brightness or wavelength of the received light and may transmit the electrical signal to the controller 90.

[48] The controller 90 may be a processor configured to control the overall operation of the analysis apparatus 1. Particularly, the controller 90 may control the optical source application unit 30, the optical measurement unit 70, and the stage 50, and output map data including evaluation results of the LEDs created by receiving the measurement results from the optical measurement unit 70.

[49] The controller 90 may be implemented using a memory to store data on algorithms for controlling operations of the elements of the analysis apparatus 1 or programs for

realizing the algorithms and a processor to perform the operations by using data stored in the memory. In this regard, the memory and the processor may be implemented using separate chips or integrated into a single chip.

- [50] The controller 90 may be connected to a storage unit configured to store the processed data. The storage unit may be implemented using at least one of a non-volatile memory such as read only memory (ROM), programmable ROM (PROM), erasable programmable ROM (EPROM), electrically erasable programmable ROM (EEPROM), and flash memory, a volatile memory such as random access memory (RAM), or a storage medium such as hard disk drive (HDD) and CD-ROM, without being limited thereto. The storage unit may be a memory implemented as a separate chip from the processor described above with reference to the controller 90 or a memory integrated with the processor as a single chip.
- [51] The analysis apparatus 1 may further include one or more elements in addition to the elements illustrated in FIG. 1, or at least one of the elements illustrated in FIG. 1 may be excluded therefrom.
- [52] For example, the analysis apparatus 1 may further include an interface configured to output data processed by the controller 90 and receive an input command of a user, and a communication module configured to transmit the processed data to an external device.
- [53] The interface may be connected to a display configured to display the map data created by the controller 90. The display may be implemented using a cathode ray tube (CRT), a digital light processing (DLP) panel, a plasma display panel (PDP), a liquid crystal display (LCD) panel, an electro luminescence (EL) panel, an electrophoretic display (EPD) panel, an electrochromic display (ECD) panel, a light emitting diode (LED) panel, or an organic light emitting diode (OLED) panel, without being limited thereto.
- [54] In addition, the interface may be connected to a hardware device such as a button, a switch, a pedal, a keyboard, a mouse, a track-ball, a lever, a handle, and a stick which receive input commands of the user and a software device such as a graphic user interface (GUI), for example, a touch pad which connects a touch signal of the user together with the display.
- [55] FIG. 2 is a view comparing a wafer probe card 100 and an LED wafer 200 according to an example embodiment.
- [56] Referring to FIG. 2, the LED wafer 200 may include one or more LEDs 250. Two electrode pads 210 and 230 corresponding to P and N types are provided on each LED 250. Hereinafter, the P type electrode pad is referred to as a first LED electrode pad 210 and the N type electrode pad is referred to as a second LED electrode pad 230.
- [57] The wafer probe card 100 according to an example embodiment includes a first pad

110 and a second pad 130 to transfer a current or voltage respectively to the first LED electrode pad 210 and the second LED electrode pad 230 in direct contact therewith.

[58] In addition, the wafer probe card 100 may include the first pads 110 and the second pads 130 in the same number and same size as the first and second LED electrode pads 210 and 230 of the LEDs 250 provided on the LED wafer 200 to be inspected.

[59] Thus, all of the LEDs 250 may be simultaneously inspected by applying a current or voltage to the LEDs 250 by using the wafer probe card 100. Therefore, efficiency of the inspection may be increased according to an example embodiment.

[60] FIGs. 3A and 3B are views for describing the operation of analysis apparatuses including different wafer probe cards according to example embodiments.

[61] Referring to FIG. 3A, the optical source application unit 30 may transmit a current or voltage required for inspection of the first pad 110 and the second pad 130 of the wafer probe card 100 based on the control of the controller 90.

[62] The wafer probe card 100 may transfer the voltage or current to the first LED electrode pad 210 and the second LED electrode pad 230 provided on the LED wafer 200 through the first pad 110 and the second pad 130, respectively.

[63] The LED 250 may emit light upon receiving power from each of the first and second electrode pads 210 and 230.

[64] Light emitted from the LED 250 may be transferred to the optical measurement unit 70 through the glass window 51 provided in the stage 50 and the optical measurement unit 70 collects the emitted light and analyzes brightness or wavelength of the light emitted from the LED 250.

[65] According to an example embodiment, as illustrated in FIG. 3B, an optical measurement unit 70 included in an analysis apparatus 1 may be disposed in the same direction as the optical source application unit 30 with respect to the wafer probe card 100.

[66] Light may be emitted from the LED 250 not in a particular direction, and thus, the light emitted from the LED 250 may be reflected by the stage 50.

[67] Also, the wafer probe card 100 may include a silicon substrate on which the first pad 110 and the second pad 130 are mounted. Thus, light emitted from the LED 250 may be reflected by the first pad 110 and the second pad 130. However, example embodiments are not limited thereto. For example, a wafer probe card 100 according to an example embodiment as illustrated in FIG. 3B may include through silicon vias (TSVs) 150 and may transmit light emitted from the LED 250 at predetermined intervals.

[68] Thus, the optical measurement unit 70 provided in the analysis apparatus 1 may collect light passing through the wafer probe card 100 of FIG. 3B and transfer the light to the controller 90.

- [69] FIGs. 3A and 3B schematically illustrate examples of the present disclosure, but example embodiments are not limited thereto.
- [70] FIGs. 4A and 4B are top and bottom views of a wafer probe card 100 according to an example embodiment.
- [71] Specifically, FIG. 4A illustrates a bottom surface 101 of the wafer probe card 100 and FIG. 4B illustrates a top surface 102 of the wafer probe card 100.
- [72] As described above, the structure of the wafer probe card 100 may include the first pad 110 and the second pad 130 which are in one-to-one correspondence with the first LED electrode pad 210 and the second LED electrode pad 230 provided on the LED wafer 200 to be inspected. The first pad 110 and the second pad 130 may have the same size.
- [73] In addition, the wafer probe card 100 has align holes 190 for the purpose of alignment with the LEDs and the LED wafer 200. When the align holes 190 are formed in the bottom surface 101 and the top surface 102 of the wafer probe card 100, the align holes 190 are penetrated through the wafer probe card 100. The user may prevent the LED wafer 200 in contact with the wafer probe card 100 from being dislocated by using the align holes 190.
- [74] In the wafer probe card 100 illustrated in FIG. 4A, one first pad 110 may be connected with another first pad 110 in a longitudinal direction (first direction) in a line-by-line manner via an electric wire. Also, one second pad 130 may be connected to another second pad 130 in a lateral direction (second direction) via an electric wire.
- [75] In addition, in the wafer probe card 100, the electric wiring connecting the first pads 110 and the electric wiring connecting the second pads 130 are connected to TSV points 115 and 135 which are finally connected to an upper surface of the wafer probe card 100. The TSV points 115 and 135 are may be the through silicon vias (TSVs).
- [76] The TSV points 115 and 135 are pathways through which the first pad 110 and the second pad 130 are connected to the top surface and the bottom surface.
- [77] The TSV points 115 and 135 correspond to positive and negative poles of the power delivered by the optical source application unit 30. That is, the wafer probe card 100 may apply the current or voltage selectively to the first pads 110 and the second pads 130 of the wafer probe card 100 by controlling only the TSV points 115 and 135, and without connecting each of the first pads 110 and the second pads 130 with the positive and negative poles of the optical source application unit 30 in a one-to-one correspondence manner with each other.
- [78] For example, in order to apply a current or voltage to a first pad 110 and a second pad 130 indicated by reference numerals 110 and 130 illustrated in FIG. 4A, the current or voltage may be applied to a first TSV point 115 indicated by the reference numeral 115 in FIG. 4A and a second TSV point 135 in a second row from the last row

and a column indicated by the reference numeral 135 of FIG. 4A

[79] According to this example configuration, materials and structures required for conventional analysis apparatuses such as a substrate, a mold, and gold may be omitted. Since the first and second pads 110 and 130 may allow all LEDs 250 provided on the LED wafer 200 to emit light simultaneously, it is possible to omit separation/re-alignment processes performed by the conventional analysis apparatuses and it is possible to shorten an analysis time since a device for moving the analysis apparatus 1 such as a chuck is not required.

[80] In the top surface 102 of the wafer probe card 100 shown in FIG. 4B, holes 155 are formed as TSVs between the first pads 110 and the second pads 130. The holes 155 may be filled with a conductive metal on the top surface 102 of the wafer probe card 100.

[81] FIG. 5 is a view for describing an operating method of a wafer probe card 100 according to an example embodiment.

[82] A wafer probe card 100 according to an example embodiment may alternately apply negative power and positive power to the first TSV point 115 and the second TSV point 135 in a manner different from the example embodiment described above with reference to FIGs. 4A and 4B.

[83] When this structure is shown in a circuit diagram, diodes illustrated in FIG. 5 correspond to the first pads 110 and the second pads 130 respectively. In order to control an LED in contact with the first and second pads 110 and 130 corresponding to a diode D1 to emit light, a negative power is applied to a first gate G1 and a positive power is applied to a first source S1. In order to control an LED corresponding to a diode D1-2 to emit light, a positive power is applied to the first gate G1 and a negative power is applied to the first source S1.

[84] That is, when the wafer probe card 100 is fabricated as illustrated the circuit diagram of FIG. 5, two LEDs may emit light by using one wiring by alternately applying positive and negative powers by the optical source application unit 30.

[85] FIG. 6 is a flowchart for describing a method of fabricating a wafer probe card according to an example embodiment. In addition, FIGs. 7 to 20 are diagrams for describing the method of fabricating the wafer probe card.

[86] A method of fabricating the wafer probe card 100 includes coating a photoresist 400 on a silicon wafer 105 as illustrated in FIG. 7 (300).

[87] Next, the photoresist 400 is etched to correspond to a position of the first pad 110 in accordance with the number of pixels (310).

[88] Specifically, a mask 500 corresponding to the position of the first pad 110 is used to form the first pad 110.

[89] According to the example method, the photoresist 400 is exposed to light by using an

exposure unit as illustrated in FIG. 8 and etched as illustrated in FIG. 9.

[90] After etching, the first pad 110 is deposited thereon and an insulating material is coated thereon to form an insulating layer 106 as illustrated in FIG. 11 (320).

[91] Specifically, the first pad 110 is formed on an etched region by deposition as illustrated in FIG. 10. Then, the insulating layer 106 is formed over the entire surface and the photoresist 400 is coated on the insulating layer 106 as illustrated in FIG. 11 to form a second pad 130. The insulating layer may be formed of silicon dioxide (SiO_2).

[92] According to the example method, the photoresist 400 is etched at a position where the second pad 130 will be formed (330).

[93] Specifically, according to the example fabrication method, the photoresist 400 and insulating layer 106 formed in the region of the first pad 110 is removed by light exposure before etching as illustrated in FIG. 12. Next, the photoresist 400 is etched at the position where the second pad 130 will be formed by using a mask 500 as illustrated in FIG. 13.

[94] According to the fabrication method, the second pad 130 is deposited and the photoresist 400 is coated thereon again (340).

[95] Specifically, the second pad 130 is deposited as illustrated in FIG. 14. Next, the photoresist 400 is coated thereon as illustrated in FIG. 15 to match flatness of each pad.

[96] According to the example fabrication method, the regions corresponding to the first pad 110 and the second pad 130 are etched as illustrated in FIG. 16 (350).

[97] Next, the first pad 110 is re-deposited on the position of the first pad 110 as illustrated in FIG. 17 (360).

[98] According to the fabrication method, a TSV process for connection of rear surface wiring is performed by using the mask 500 as illustrated in FIG. 18 (370).

[99] In the wafer probe card 100, a rear pad 104 is formed on the top surface of the silicon substrate 105 as illustrated in FIG. 19 via the TSV process.

[100] The wafer probe card 100 is bonded to an anisotropic conductive film (ACF) 160 and a polyimide (PI) film 170 as illustrated in FIG. 20 (380).

[101] Here, the ACF 160 is an anisotropic conductive film conducting electricity only in one direction and formed by mixing fine conductive particles with an adhesive resin, such as thermosetting resin, in a film state. The fine conductive particles included in the ACF 160 may be gold or silver.

[102] In addition, the PI film 170 that withstands a high temperature of 400°C or higher and a low temperature of -269°C or lower is connected to the optical source application unit 30.

[103] Meanwhile, the TSV 150 is formed between the rear pads 104 and the ACF 160 and the TSV 150 is connected to each of the first and second pads 110 and 130 such that electric wires are connected to form electrodes of the wafer probe card 100 as il-

lustrated in FIGs. 4A and 4B.

- [104] When the wafer probe card 100 is fabricated as described above, a conventional process of using a probe may be omitted, an inspection time may be reduced by matching the wafer probe card 100 and the LED wafer in a one-to-one correspondence manner, and process complexity may be reduced by simplifying wiring required for light emission of the LEDs.
- [105] The above-described fabrication method is merely an example of fabricating the wafer probe card 100 and various modified methods may also be used therefor.
- [106] As is apparent from the above description, according to the wafer probe card, the analysis apparatus including the same, and the method of fabricating the wafer probe card, the wafer probe card may match in one-to-one correspondence with the LED wafer by implementing a probe system having the same size as the LED wafer and inspect brightness and wavelength of a plurality of LEDs at once by controlling the plurality of LEDs to emit light.
- [107] Although example embodiments of the present disclosure have been shown and described, it would be appreciated by those skilled in the art that changes may be made in these example embodiments without departing from the principles and spirit of the disclosure, the scope of which is defined in the claims and their equivalents.

Claims

- [Claim 1] A wafer probe card comprising:
a substrate;
an insulating layer formed on the substrate;
a plurality of first pads and a plurality of second pads formed on the insulating layer; and
a plurality of rear pads connected to the plurality of first pads and the second pads, respectively, via through silicon vias (TSVs),
wherein the plurality of first pads and the plurality of second pads are configured to transfer electrical signals to electrode pads of a light emitting diode (LED) wafer.
- [Claim 2] The wafer probe card of claim 1, wherein the plurality of first pads are connected to each other by an electric wiring in a first direction through the TSVs, and
the plurality of second pads are connected to each other by an electric wiring in a second direction through the TSVs.
- [Claim 3] The wafer probe card of claim 1, wherein the substrate is formed of silicon.
- [Claim 4] The wafer probe card of claim 1, wherein the wafer probe card comprises holes for alignment with the LED wafer.
- [Claim 5] The wafer probe card of claim 1, wherein the plurality of first pads are formed by deposition after etching the insulating layer.
- [Claim 6] The wafer probe card of claim 1, wherein an anisotropic conductive film (ACF) and a polyimide (PI) film are formed on the plurality of rear pads.
- [Claim 7] An analysis apparatus comprising:
an optical source application unit configured to transmit power to a wafer probe card;
an optical measurement unit configured to collect light emitted from a plurality of light emitting diodes (LEDs) and transmit measurement results of the light collected; and
a processor configured to execute instructions to control the optical source application unit and analyze the plurality of LEDs based on the measurement results received from the optical measurement unit,
wherein the wafer probe card comprises:
a substrate;
an insulating layer formed on the substrate;

a plurality of first pads and a plurality of second pads formed on the insulating layer; and

a plurality of rear pads connected to each of the plurality of first pads and the plurality of second pads, respectively, using through silicon vias (TSVs),

wherein the plurality of first pads and the plurality of second pads are configured to transfer power from the optical source application unit to the plurality of LEDs.

[Claim 8] The analysis apparatus of claim 7, wherein the processor is further configured to control the optical source application unit to alternately apply the power.

[Claim 9] The analysis apparatus of claim 7, wherein in the wafer probe card, the plurality of first pads are connected to each other by an electric wiring in a first direction through the TSVs, and the plurality of second pads are connected to each other by an electric wiring in a second direction through the TSVs. the controller selectively applies power through the electric wiring in the first direction and the electric wiring in the second direction.

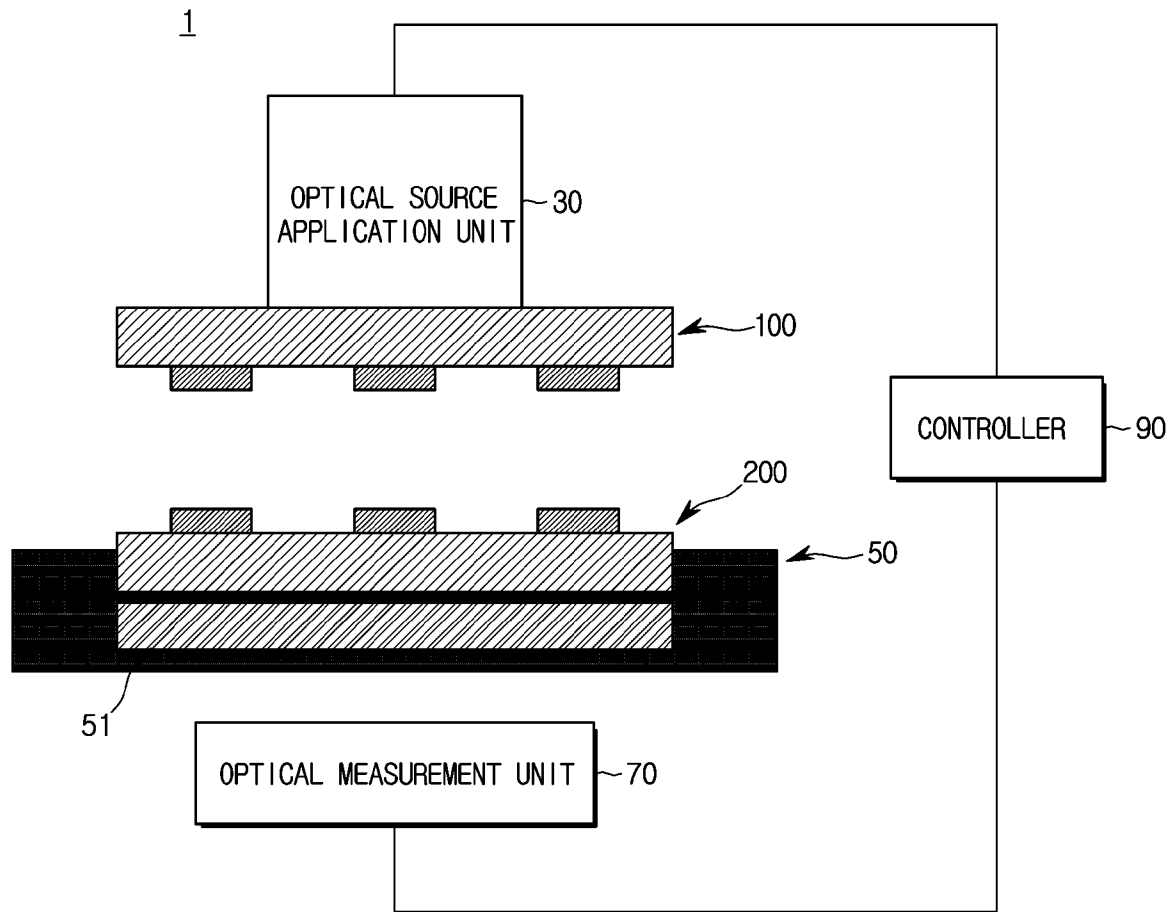
[Claim 10] The analysis apparatus of claim 7, wherein the processor is further configured to create controller creates map data on the plurality of LEDs based on the measurement results, and the analysis apparatus further comprises a storage unit configured to store the created map data.

[Claim 11] The analysis apparatus of claim 7, further comprising a stage on which a wafer comprising the plurality of LEDs is placed, wherein the stage comprises a glass window configured to transmit emitted light, and the optical measurement unit is further configured to collect collects light passing through the glass window.

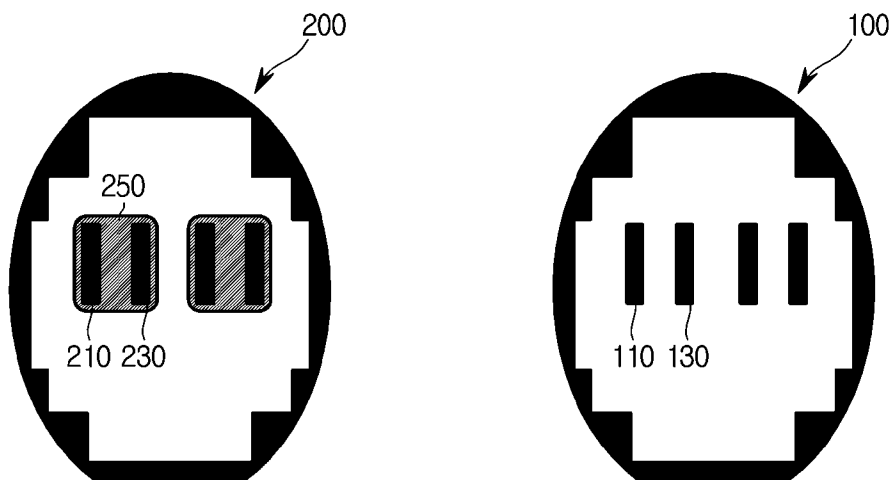
[Claim 12] A method of fabricating a wafer probe card, the method comprising: preparing a substrate having an insulating layer formed to expose a plurality of first pads; forming a plurality of second pads on the insulating layer; and forming a plurality of rear pads formed on a surface opposite to a surface of the substrate provided with the insulating layer, wherein the plurality of rear pads are connected to the plurality of first pads and the plurality of second pads using through silicon vias (TSVs).

- [Claim 13] The method of claim 12, further comprising leveling the plurality of first pads and the plurality of second pads.
- [Claim 14] The method of claim 12, further comprising bonding forming an anisotropic conductive film (ACF) to the plurality of rear pads, and forming a polyimide (PI) film on the ACF.
- [Claim 15] The method of claim 12, wherein the preparing of the substrate comprises etching a photoresist and depositing the plurality of first pads after forming the insulating layer on the substrate, and the forming of the plurality of rear first pads comprises etching the insulating layer provided with the plurality of first pads and re-depositing the a plurality of first pads after depositing the plurality of second pads.

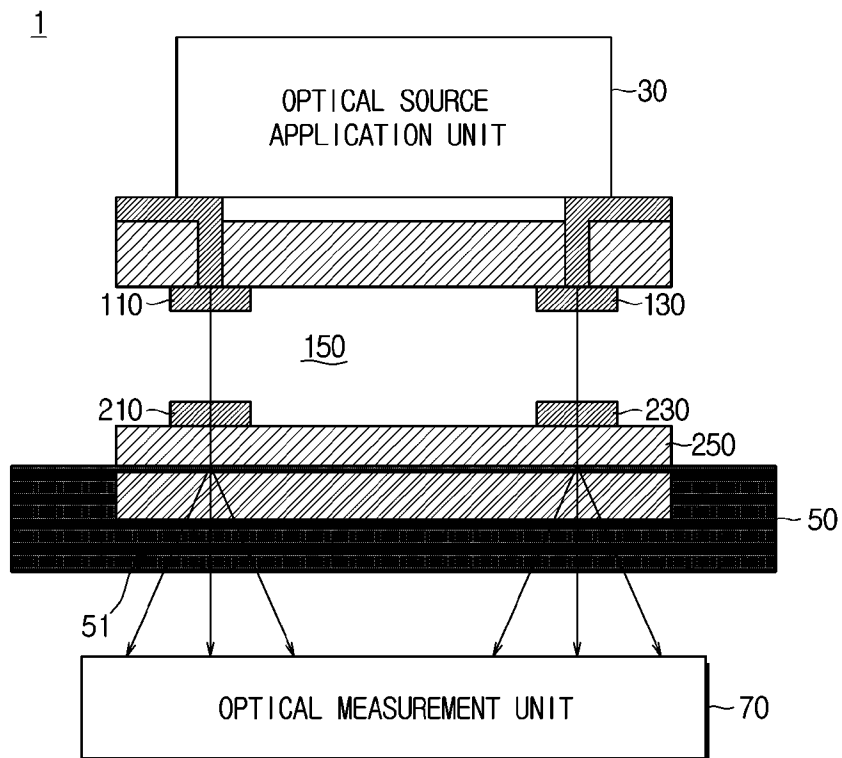
[Fig. 1]



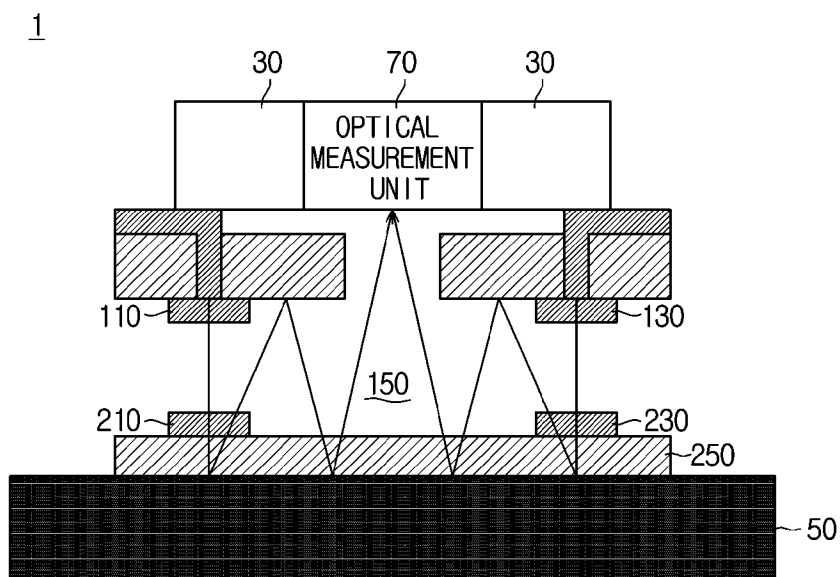
[Fig. 2]



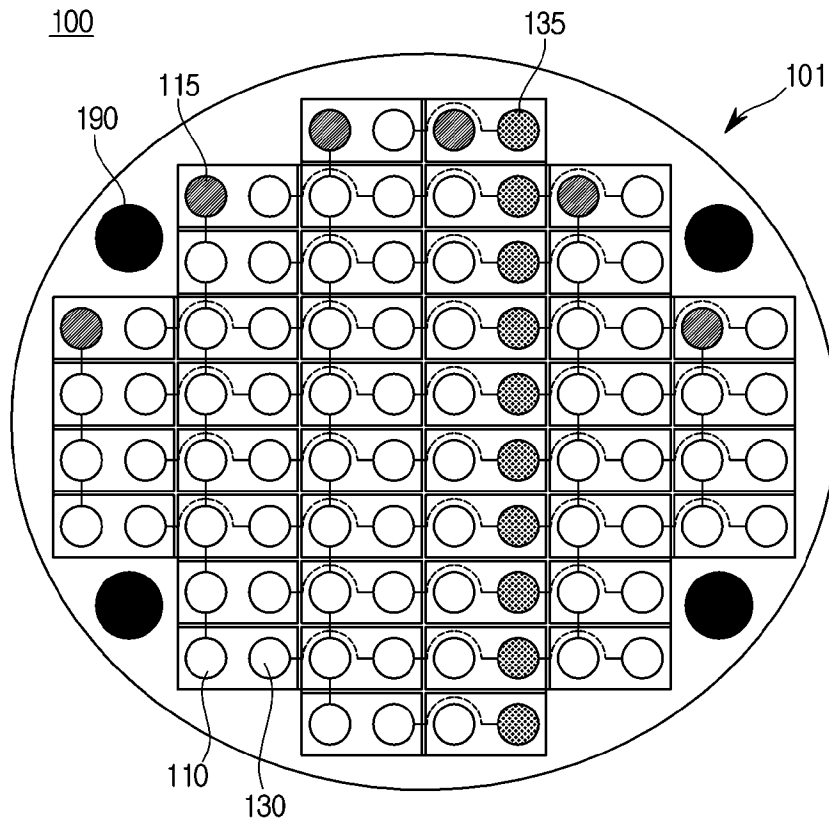
[Fig. 3a]



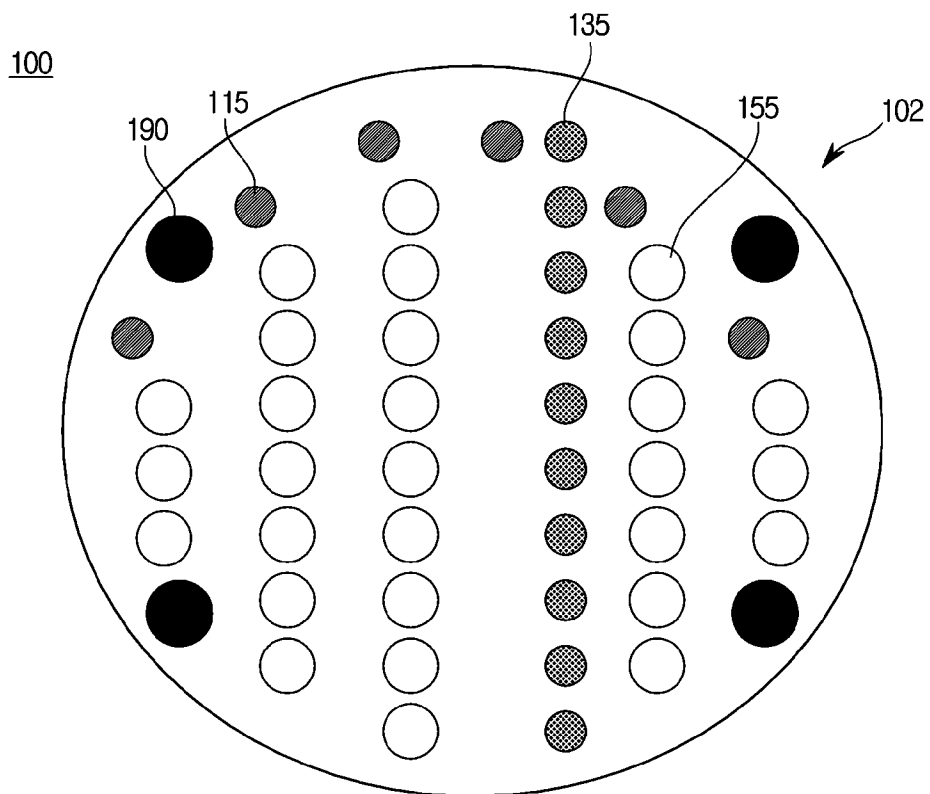
[Fig. 3b]



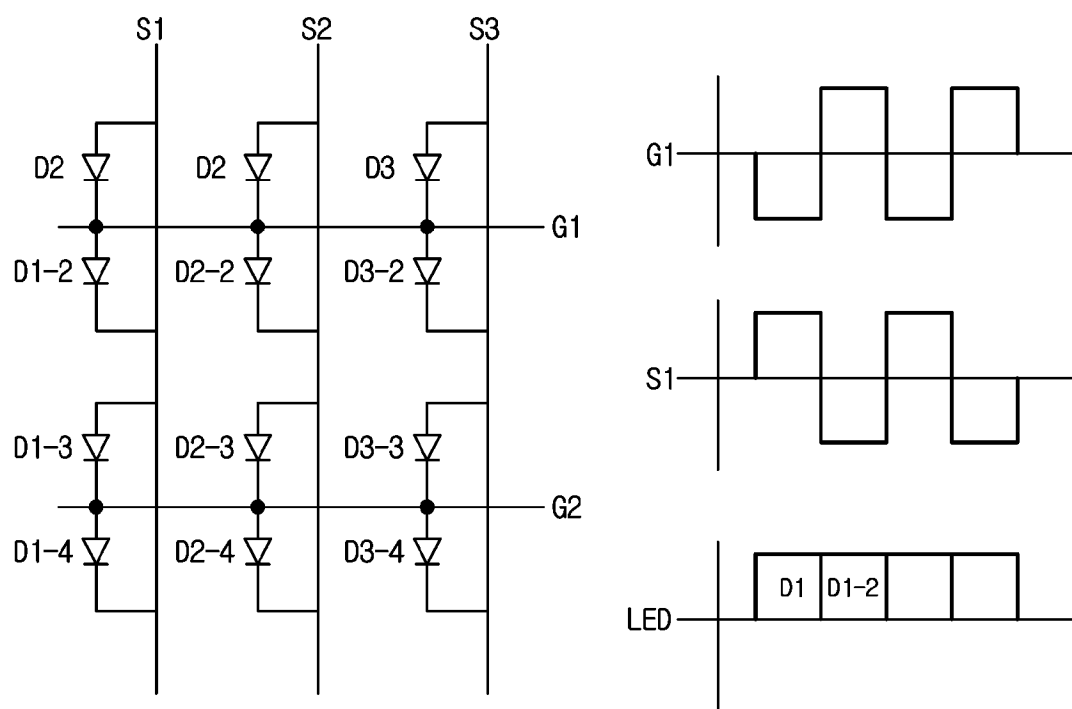
[Fig. 4a]



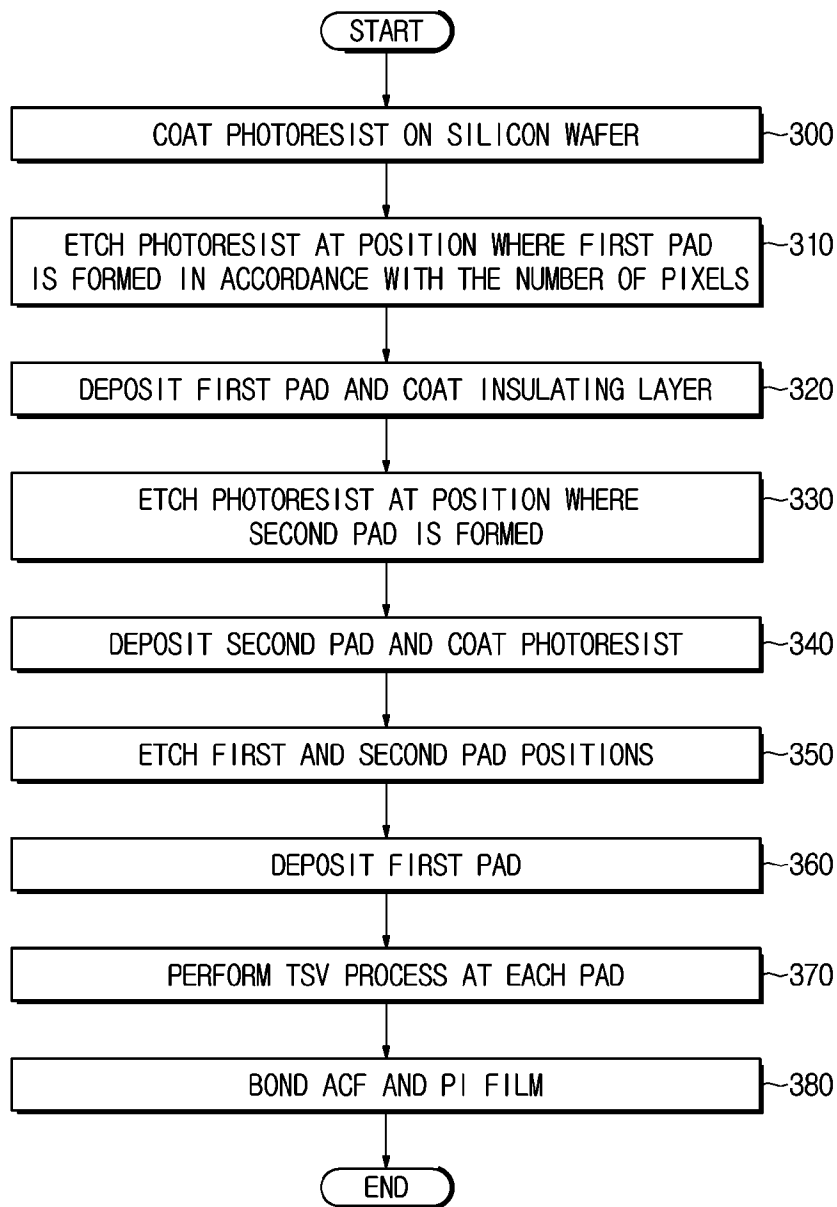
[Fig. 4b]



[Fig. 5]



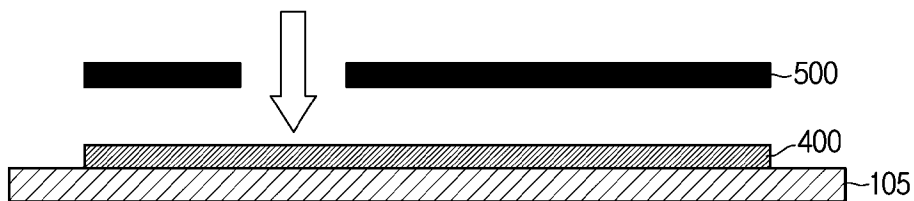
[Fig. 6]



[Fig. 7]



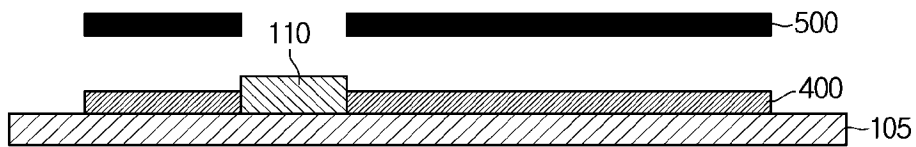
[Fig. 8]



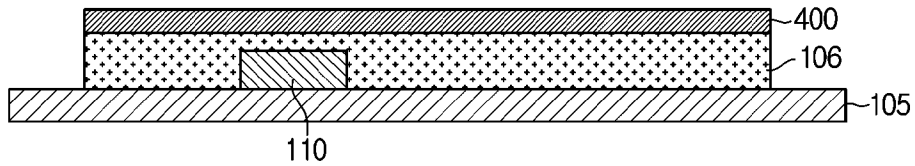
[Fig. 9]



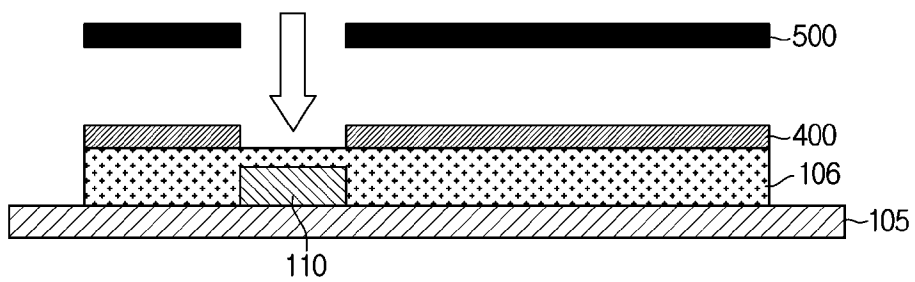
[Fig. 10]



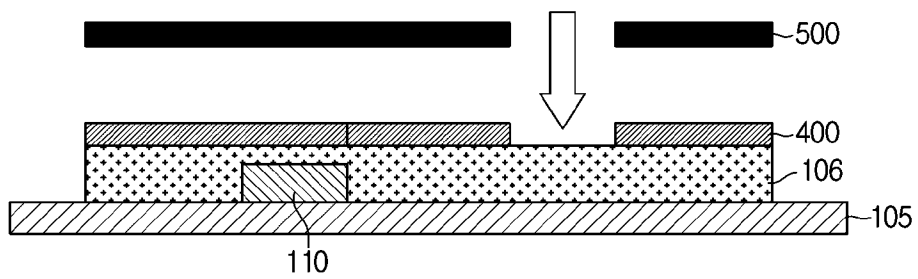
[Fig. 11]



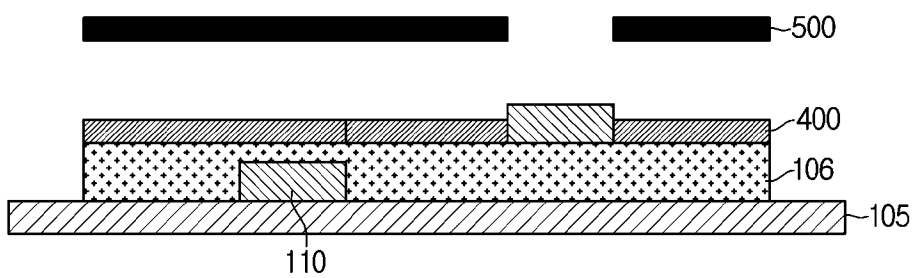
[Fig. 12]



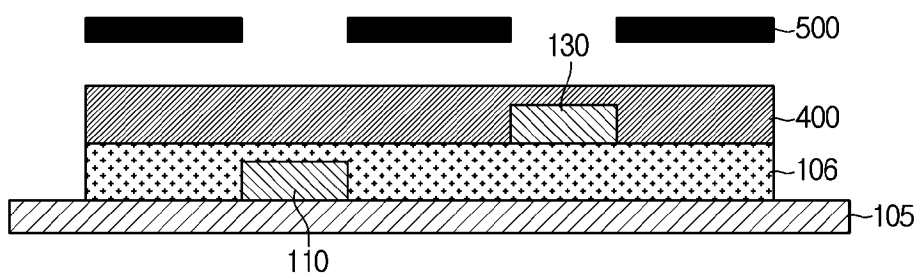
[Fig. 13]



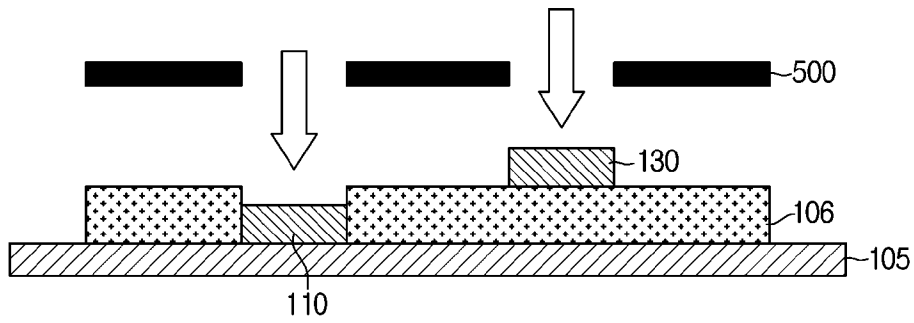
[Fig. 14]



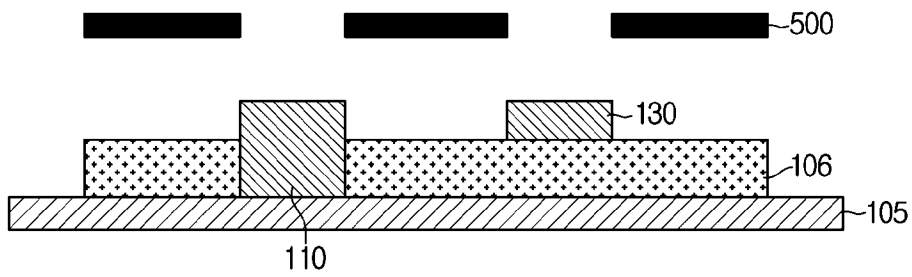
[Fig. 15]



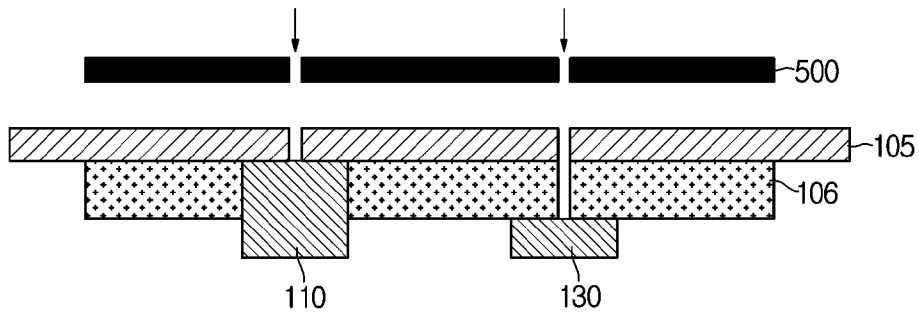
[Fig. 16]



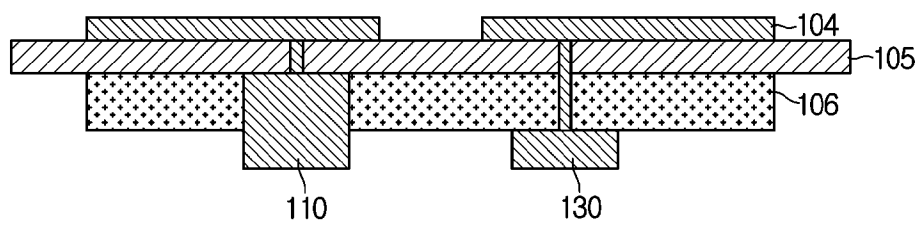
[Fig. 17]



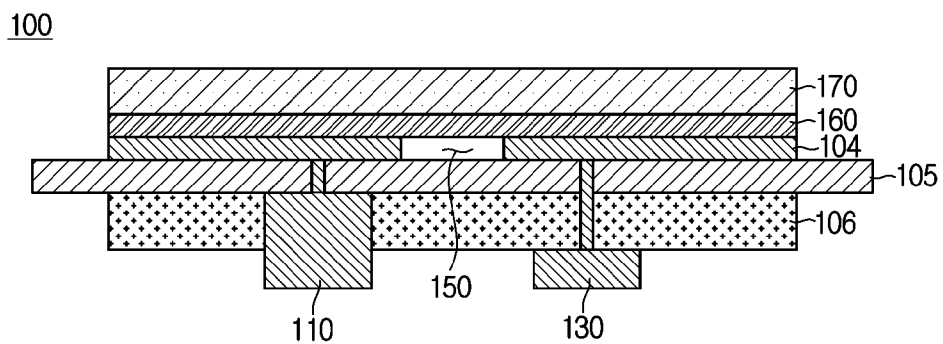
[Fig. 18]



[Fig. 19]



[Fig. 20]



A. CLASSIFICATION OF SUBJECT MATTER**G01R 31/26(2006.01)i, G01R 1/073(2006.01)i, G01J 1/42(2006.01)i, G01R 3/00(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G01R 31/26; G01R 1/067; G01J 1/44; G01J 1/04; G01M 11/02; H01L 21/66; G01R 1/073; G01J 1/42; G01R 3/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: wafer probe card, LED wafer, a plurality pads, rear pads, through silicon vias, electrical signal, ACF, PI

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2012-198194 A (SHINKO ELECTRIC IND. CO., LTD.) 18 October 2012 See paragraphs [0008]-[0042]; claims 1, 6; and figures 2-4.	1-15
Y	KR 10-2012-0037352 A (INDUSTRIAL TECHNOLOGY RESEARCH INSTITUTE) 19 April 2012 See paragraphs [0015]-[0024]; claims 11-12; and figures 2-3c.	1-15
Y	KR 10-2010-0057258 A (UBPRECISION CO., LTD.) 31 May 2010 See claims 1, 6, 10; and figures 3-9.	4, 6, 14
Y	KR 10-2010-0071750 A (AMST CO., LTD.) 29 June 2010 See paragraph [0012]; and figure 1.	13
A	US 2013-0001405 A1 (JAMES ALBERT WALKER) 03 January 2013 See paragraphs [0013]-[0022]; and figures 1-3.	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search

16 May 2018 (16.05.2018)

Date of mailing of the international search report

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Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/KR2018/001595

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