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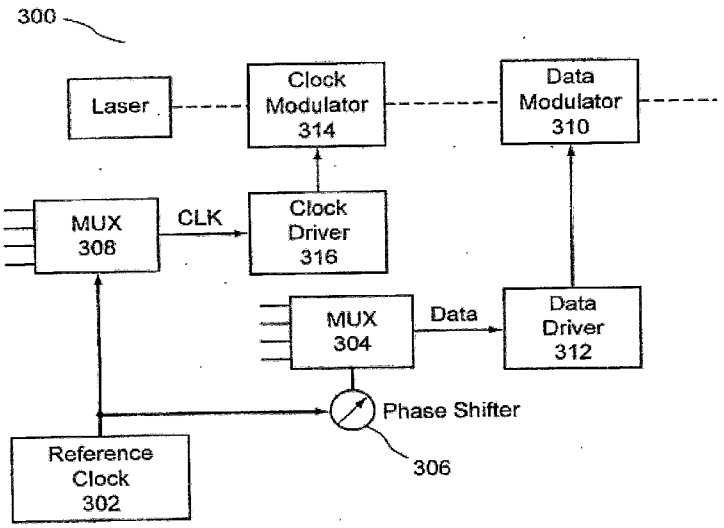
(54) **Title:** METHOD AND SYSTEM FOR KEEPING TIMING ALIGNMENT BETWEEN DRIVING SIGNALS IN OPTICAL DOUBLE MODULATION



(57) **Abstract:** A method and system is disclosed for making timing alignment for a data transmission system, the method comprising providing a reference clock signal with a first frequency to a multiplexer through a phase shifter, generating a multiplexed signal with a second frequency by the multiplexer, wherein the second frequency follows the first frequency and is higher than the first frequency by a predetermined proportion, sending the multiplexed signal to a modulator, and phase shifting the reference clock signal by the phase shifter before the reference clock signal is provided to the multiplexer, wherein a timing of the multiplexed signal at the second frequency level can be adjusted by adjusting a timing of the reference clock signal at the lower first frequency level.

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METHOD AND SYSTEM FOR KEEPING TIMING ALIGNMENT BETWEEN DRIVING SIGNALS IN OPTICAL DOUBLE MODULATION

Field of the invention

The present invention relates generally to optical data transmission, and, more particularly, to timing alignment among modulated signals in optical transmission systems.

Background of the invention

In optical transmission with data formats other than simple NRZ format, such as a returned to zero (RZ) format, a periodically modulated light source that generates a clocklike pulse stream instead of a continuous wave light source is often used.

To achieve stable and optimized operation, the optical data modulation needs to have a fixed time delay relative to the modulated light source. For example, optimal performance of RZ transmission is usually achieved when the peak of the modulated light overlaps with the center of the data bit slot.

A conventional method to make this timing alignment is to shift the timing of the modulated light. This is because it is much easier to make time delay on a clock signal than on a broadband data signal. The timing shift of clock is made available by placing a voltage-controlled phase shifter before or after the clock driver, which is used to drive a clock modulator or a direct modulated laser (DML). The phase shift is thus at the line rate frequency. For example, if the data rate is 10Gbps, the phase shift is at 10GHz. In some other conventional RZ pulse generation schemes, half rate frequency can also be used for over-driving a Mach-Zehnder (MZ) modulator to generate line rate clock pulse trains. In this case, the phase shift is at a half rate frequency. In order to prevent the slow drift over time from the optimal point caused by mechanical variation, thermal variation, or other environmental changes in the relative phase, a feedback loop is often implemented to lock the relative timing between the data modulation and the light source.

In more complex modulation formats for high capacity optical transmission, there are more than one driving data signals, such as double data modulation has two driving data signals. Relative timings between the multiple driving signals are adjusted in a similar

fashion, with the exception that variable delay lines are implemented rather than phase shifters, since the latter generally narrows frequency pass band and would distort the signals.

However, the high frequency phase shifters used in this conventional method are inherently complex and expensive, especially if the phase shift needs to cover a minimum 360 degrees, also known as one bit slot to those skilled in the art. For example, the insertion loss of the phase shifter may vary a lot over the phase shift range. It is also difficult to make phase shifters that have linear phase shift versus control voltage over the large range.

Variable delay lines with broad frequency responses used in double data modulation are even more expensive and difficult to use. Furthermore, when a feedback loop is used to lock the relative timing, the dithering phase shift may add undesirable time jitters to the output optical data signals.

Therefore, it is desirable to devise improved method and system for shifting and locking the timing among the driving signals in the above applications.

Summary of the invention

In view of the foregoing, a method and system is disclosed for making timing alignment for a data transmission system, the method comprising providing a reference clock signal with a first frequency to a multiplexer through a phase shifter, generating a multiplexed signal with a second frequency by the multiplexer, wherein the second frequency follows the first frequency and is higher than the first frequency by a predetermined proportion, sending the multiplexed signal to a modulator, and phase shifting the reference clock signal by the phase shifter before the reference clock signal is provided to the multiplexer, wherein a timing of the multiplexed signal at the second frequency level can be adjusted by adjusting a timing of the reference clock signal at the lower first frequency level.

The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

Brief description of the drawings

FIG. 1A illustrates a conventional RZ transmitter.

FIG. 1B illustrates a conventional RZ transmitter with a phase-locked loop.

FIG. 1C illustrates a conventional double data modulation transmitter using two data modulators.

FIG. 1D illustrates a conventional double data modulation transmitter using a dual drive data modulator.

FIG. 2 illustrates an electrical parallel to serial data converter.

FIG. 3A illustrates an RZ-like transmitter implemented with a low frequency phase shifter in accordance with one embodiment of the present invention.

FIG. 3B illustrates an RZ-like transmitter implemented with a low frequency phase shifter and an optical coupler phase-locked loop in accordance with one embodiment of the present invention.

FIG. 3C illustrates an RZ-like transmitter implemented with a low frequency phase shifter and an RF-mixer phase-locked loop in accordance with one embodiment of the present invention.

FIG. 4A illustrates a double data modulation transmitter implemented with a low frequency phase shifter in accordance with one embodiment of the present invention.

FIG. 4B illustrates a double data modulation transmitter using a dual drive data modulator and implemented with a low frequency phase shifter in accordance with one embodiment of the present invention.

FIG. 4C illustrates a double data modulation transmitter using a plurality of data modulators, and implemented with a low frequency phase shifter and an RF mixer phase-locked loop in accordance with one embodiment of the present invention.

Detailed description of preferred embodiments

The present disclosure provides a method and system that shifts and locks the phases of a plurality of signals, either a combination of a clock signal and a data signal or a plurality of data signals, using a low frequency phase shifter.

FIG. 1A illustrates a conventional RZ transmitter 100. This transmitter 100 is designed to shift the timing of the modulated light in order to provide the necessary timing alignments for stabilizing and optimizing the operation. The alignments with the broadband data signal can be done by making time delay on the clock signal.

The data of a returned-to-zero (RZ) format is generated in two stages as shown in the RZ transmitter 100. In the first stage, a carrier is generated by a continuous wave (CW) laser 102 and a clock modulator 104. A source unit 106 is designed to provide both a clock signal to a clock driver 108, as well as a set of non-returned to zero (NRZ) data to a data driver 110. The timing shift of the clock is done by placing a voltage controlled phase shifter 112 after the clock driver 108. This phase shifted time signal will drive the clock modulator 104. The phase shift is performed at the line rate frequency. For example, if the data rate is 10Gbps, the phase shift is at 10GHz. The periodically modulated carrier includes a stream of optical pulses shorter than a bit slot. In the other stage, a physical variable is modulated using a data modulator 114 to encode the data on the optical carrier. The data driver 110 is designed to provide the NRZ data from the source block 106 to the data modulator 114. Together with the encoded data and the periodically modulated carrier, the RZ format can be generated.

It is noted that a half rate frequency may also be used in some RZ pulse generation schemes to over-drive a Mach-Zehnder (MZ) modulator to generate line rate clock pulse trains. In this case, the phase shift is performed at a half rate frequency. However, in all return-to-zero optical transmitters, the degree of misalignment between the data and the clock paths varies with natural effects such as temperature and aging. With increasing bit rates and decreasing bit time slots, the timing variations can severely limit the transmitter performances.

FIG. 1B illustrates a conventional RZ transmitter 116, which includes the conventional RZ transmitter 100 and a phase lock loop. Data of the RZ format is generated using an encoded data and a carrier. As mentioned in description of FIG. 1A, the conventional RZ transmitter 100 may have misalignment between the data and the clock paths varied by

natural effects such as temperature, environmental changes, mechanical variations, aging, and much more.

To prevent the misalignment from causing relative timing drift from the optimal point, a feedback loop is typically implemented to help lock the relative timing between the data modulation and the light source. This is usually done by first monitoring and analyzing the optical output, and then varying the control voltage to keep the timing alignment at an optimal value. This feedback (phase lock) loop includes an optical coupler 118 to monitor the optical output. A photo detector 120 analyzes the optical signal before allowing a control unit 122 to adjust the control voltage at the phase shifter 112.

FIG. 1C illustrates a conventional double data modulation transmitter 124 with two data modulators. The transmitter 124 is designed to shift the timing of dual broadband data signals in order to provide the necessary timing alignments for stabilizing and optimizing the operation. The alignments of the dual broadband data signals can be done by making delays on one of the broadband data signals.

Data of a complex modulation format is generated in two stages as shown in the double data modulation transmitter 124. In the first stage, a carrier is generated by a continuous wave (CW) laser 102 and a data modulator 114 encodes data onto the carrier. A source block 106 is designed to provide a first data signal to a data driver 110. In the other stage, a data modulator 130 also encodes data onto the carrier. A source unit 126 is designed to provide a second data signal to a data driver 128. The first and the second signals may generally be nonidentical.

The time shift of the data signals with respect to one another is done by placing a variable delay line 132 after the data source block 126. This time shifted data signal will drive the data modulator 130. The time shift is also performed at the line rate frequency.

Similarly, FIG. 1D illustrates a conventional double modulation transmitter 134 with a dual drive data modulator 136 rather than two single data modulators. This transmitter 134 is designed to shift the timing of dual broadband data signals in order to provide the necessary timing alignments for stabilizing and optimizing the operation. The alignments of the dual broadband data signals can be done by making delays on one of the broadband data signals.

Data of a complex modulation format is generated in two stages in the transmitter 134 as shown in FIG. 1D. In the first stage, a carrier is generated by a continuous wave (CW) laser 102 and a dual drive data modulator 136 encodes data onto the carrier. A data source 106 is designed to provide a first data signal to a data driver 110. In the other stage, a data source 126 is designed to provide a second data signal to a data driver 128. The first and the second signals may generally be nonidentical.

The time shift of the one of the two data signals is done by placing a variable delay line 132 after the data source block 106. This time shifted data signal of data source block 106 will now be aligned with the un-shifted data signal of data source 126 to drive the dual drive data modulator 136. The time shift is also performed at the line rate frequency.

In general, the average output optical power of an RZ transmitter is at the maximum when the clock peaks are aligned to the center of the bit slots if the "eye" crossing point of the NRZ modulation is lower than 50% and at the minimum if the "eye" crossing point is higher than 50%. Thus the simplest feedback approach is to monitor the average output optical power, and vary the control voltage on the phase shifter to maximize (or minimize) the output power. To use this approach, the control unit 122 sends a dithering voltage to modulate the control voltage on the voltage controlled phase shifter 112. This dithering voltage can be in the range of tens of hertz to kilohertz.

However, the high frequency phase shifter used in conventional RZ transmitters 100 and 116 are inherently complex and expensive, especially if the phase shift needs to cover a minimum 360 degrees or one bit slot. Furthermore, when a feedback loop is used to lock the relative timing, the dithering phase shift may add undesirable time jitters to the output optical data signals.

So one embodiment of the present invention is to use low frequencies phase shifter, which is less expensive and easier to operate, to align timings of data at high, line-rate frequencies. A low frequency signal can be converted to high line rate frequency signal by a multiplexer chip.

FIG. 2 illustrates an electrical parallel-to-serial data converter 200 to be used in various embodiments of the present invention. The electrical parallel to serial data converter 200 comprises a multiplexer (MUX) chip 202 that works with an external reference clock 204.

The MUX chip 202 is designed to multiplex lower rate data inputs such as parallel outputs from some DSP chips to form outputs at a relatively high line rate. The parallel outputs of the DSP chips are typically at a data rate many times lower than the line rate. In this embodiment, therefore, the external reference clock 204 is designed to output at fractions of the line rate. Within the MUX chip 202, the clock frequency is up-converted to the line rate frequency, which is used to carry the data output. As shown in the block diagram 200, the MUX chip 202 is designed to receive N number of lower rate data inputs 206. After the up-conversion, the MUX chip 202 can provide a data output 208 and a clock output 210 to a transmitter.

Note that both the line rate clock and the data are designed to be in synchronization with the low frequency reference clock. By shifting the phase of the reference clock, both the clock and the data outputs can be adjusted more effectively. For example, since the frequency of the reference clock 204 is 1/N of the line rate, the phase shift or time shift on the line rate data output 208 or clock output 210 is N times larger.

FIG. 3A illustrates a RZ-like transmitter 300 implemented with a low frequency phase shifter in accordance with one embodiment of the present invention. This method uses a low frequency phase shifter 306 to align the timing between a clocklike light source and optical data modulation for the generation of RZ-like data signals.

Referring to FIG. 3A, a reference clock generator 302 is designed to provide a reference clock signal to both a MUX 304 through a low frequency phase shifter 306 and to a MUX 308. This reference clock signal is at a predetermined frequency lower than the line rate. The MUX 304 is coupled to a data modulator 310 through a data driver 312, while the MUX 308 is coupled to a clock modulator 314 through a clock driver 316. Similar to the conventional RZ transmitter 100 shown in FIG. 1, the clock modulator is further connected to a laser source so that a periodically modulated light source can be generated by the clock modulator 314. The MUX 304 functions just like it would in a NRZ transmitter, converting the lower rate parallel data signals to the line rate serial data. The line rate serial clock output of the MUX 304 is used to drive the clock modulator 314.

The parallel inputs of the MUX 308 can be idle, or they may all be connected to ground, as the MUX 308 is designed to provide a line rate clock signal to the clock driver 316 by taking a reference clock input from the reference clock generator 302. The phase shifter 306

is designed to perform a phase adjustment on the reference clock signal before the reference clock signal reaches the MUX 304. By placing a low frequency phase shifter 306 between the reference clock generator 302 and the MUX 304, the phase adjustment of the reference clock signal can be made at a lower frequency to align a timing of data modulator 310 with a periodically modulated light source of the clock modulator 314.

To avoid misalignment and relative timing drift from the optimal point, a feedback loop is implemented to this method as shown in FIG. 3B to help lock the relative timing to the optimal alignment by monitoring the average output optical power and controlling the voltage on the phase shifter accordingly.

FIG. 3B illustrates an RZ-like transmitter 318 implemented with a low frequency phase shifter and a phase lock loop in accordance with one embodiment of the present invention. In this embodiment, the RZ-like transmitter 318 includes both the RZ-like transmitter 300 as described in FIG. 3A and a phase lock loop 320. As described above, misalignment can occur between the data and the clock paths varied by natural effects such as temperature, environmental changes, mechanical variations, aging, and much more. To prevent the misalignment from causing relative timing drift from the optimal point, a feedback loop is typically implemented to help lock the relative timing between the data modulation and the light source. This is usually done by first monitoring and analyzing the optical output, and then by varying the control voltage to keep the timing alignment at an optimal value.

The phase lock loop 320, including an optical coupler 322, a photo detector 324, and a control unit 326, is implemented as a feedback loop for locking the relative timing to the optimal alignment. The optical coupler 322 is placed along with the clock modulator 314 and the data modulator 310 to monitor the optical output. The photo detector 324 analyzes the optical signal before allowing a control unit 326 to send a feedback control signal 328 for adjusting the control voltage at the phase shifter 306.

Since the average output optical power of a RZ transmitter is usually at the maximum when the clock peaks are aligned to the center of the bit slots, the simplest feedback approach is to monitor the average power of the optical output, and vary the control voltage on the phase shifter to maximize the output power. To use this approach, the control voltage on the phase shifter is usually dithered (e.g., small modulations in the range of tens of hertz to

kilohertz) to generate a necessary feedback signal. In this example, the average power of the optical output is monitored, and the control voltage on the phase shifter 306 may be dithered to generate the necessary feedback signal allowing the control voltage on the phase shifter 306 to be varied to maximize the output power.

FIG. 3C shows an alternative feedback loop to the one shown in FIG. 3B. Referring to FIG. 3C the feedback loop can be designed to have the MUX 304 and the MUX 308 provide an additional line rate clock signals, respectively, in addition to the signals they send to their respective drivers. By comparing these clock signals from the MUX 304 and the MUX 308, an error signal can be generated and fed back to the control unit 326 for further adjusting the phase shifter 306. For example, the phase difference between these two signals can be indicated by a DC voltage level derived from the error signal based on two clock signals using an RF mixer 362 to combine the signals.

It is also understood that the phase adjustment at the lower rate can be done on the clock side instead of the data side. In another embodiment, the low frequency phase shifter 306 is placed in the clock path before the MUX 308 instead of in the data path before the MUX 304. However, the preferred embodiment is to place the low frequency phase shifter 306 before the MUX 304, since the timing of the clocklike pulse stream will not be affected by the dithering processes, and the time jitter on the RZ output is thus minimized.

Turning to FIG. 4A, a double data modulation transmitter in accordance with one embodiment of the present invention is illustrated. A reference clock generator 402 is designed to provide a reference clock signal directly to a MUX 408 and also to a MUX 404 through a low frequency phase shifter 406. This reference clock signal is set at a predetermined frequency lower than the line rate frequency. The MUX 404 converts lower frequency parallel data signals to a line rate frequency serial data signal, which is then sent to a data modulator 410 through a data driver 412. Likewise, the MUX 408 converts lower frequency parallel data signals to another line rate frequency serial data signal, which is then sent to another data modulator 414 through another data driver 416. Similar to the conventional double data modulation transmitter 124 shown in FIG. 1C, the data modulator 410 and the data modulator 414 are further coupled to a laser source 418 so that a data encoded carrier can be generated.

Referring to FIG. 4A, a phase shifter 406 is designed to perform a phase adjustment on the reference clock signal before the reference clock signal reaches the MUX 404, so that the phase shifter 406 can be a low frequency phase shifter. This transmitter 400 can also achieve timing alignment between the data signal from the MUX 408 and the data signal from the MUX 404, yet, with the inexpensive and easy to operate low frequency phase shifter 406.

FIG. 4B illustrates a double data modulation transmitter using a dual drive data modulator and also implemented with a low frequency phase shifter in accordance with one embodiment of the present invention. A reference clock generator 402 is designed to provide a reference clock signal directly to a MUX 408 and also to a MUX 404 through a low frequency phase shifter 406. The reference clock signal is at a predetermined frequency lower than the line rate. The MUX 404 is coupled to a dual drive data modulator 422 through a data driver 412, and likewise the MUX 408 is also coupled to the dual drive data modulator 422 through a data driver 416. Similar to the conventional RZ transmitter 134 as shown in FIG. 1D, the dual drive data modulator 422 is further connected to a laser source 424 so that the data encoded carrier can be generated. The MUX 404 and the MUX 408 convert the lower rate parallel data signals to the line rate serial data signals. The line rate serial data signals from the MUX 404 and the MUX 408 are used to drive the dual drive data modulator 422.

The phase shifter 406 is designed to perform a phase adjustment on the reference clock signal before the reference clock signal reaches the MUX 404. By placing a low frequency phase shifter 406 between the reference clock generator 402 and the MUX 404, the phase adjustment of the reference clock signal can be made at a lower frequency to align timings of the data signals sent to the modulator 422.

It is also understood that the phase adjustment at the lower frequency can be done on either one of the two data signals, i.e., the phase shifter 406 can be instead placed before the MUX 408. It is also understood that the principle of using low frequency phase shifter to adjust timing alignment between line rate frequency data signals can be extended to more than two data modulators.

To avoid misalignment and relative timing drift from the optimal point, a feedback loop can be implemented to both transmitters 400 and 420 shown in FIGs. 4A and 4B, similar to the phase-locked loops 320 and 360 shown in FIGs. 3B and 3C, respectively.

As an example, FIG. 4C illustrates a transmitter 426 using a RF mixer 428 phase-locked loop to form a feedback for the double data modulation transmitter 400. The MUXs 404 and 408 are made to output two signals, one is a data signal, and the other is a clock signal. The clock signals from the MUX 404 and the MUX 408 are sent to a RF mixer 428, which detects any phase difference between the two clock signals. The phase difference is then provided to a control unit 430, which analyzes the phase difference and then generates a feedback voltage accordingly to control the phase shifter 406. A particular phase difference corresponds to the optimal overlap between the data modulator 410 and the data modulator 414. The control unit 430 then varies the low frequency shifter 406 to lock to an optimal voltage. To use this approach, the control voltage on the phase shifter is usually dithered (e.g., small modulations in the range of tens of hertz to kilohertz) to effect the desired alignment of the data modulators.

The above illustration provides many different embodiments or embodiments for implementing different features of the invention. Specific embodiments of components and processes are described to help clarify the invention. These are, of course, merely embodiments and are not intended to limit the invention from that described in the claims.

Although the invention is illustrated and described herein as embodied in one or more specific examples, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims. Accordingly, it is appropriate that the appended claims be construed broadly and in a manner consistent with the scope of the invention, as set forth in the following claims.

WHAT IS CLAIMED IS:

1. A method for making timing alignment for a data transmission system, the method comprising:

providing a reference clock signal with a first frequency to a first multiplexer through a phase shifter;

generating a first multiplexed signal with a second frequency by the first multiplexer, wherein the second frequency follows the first frequency and is higher than the first frequency by a predetermined proportion;

sending the first multiplexed signal to a first modulator; and

phase shifting the reference clock signal by the phase shifter before the reference clock signal is provided to the first multiplexer,

wherein a timing of the multiplexed signal at the second frequency level can be adjusted by adjusting a timing of the reference clock signal at the lower first frequency level.

2. The method of claim 1 further comprising driving before sending the first multiplexed signal to the first modulator.

3. The method of claim 1, wherein the first multiplexed signal is a clock signal; and the first modulator is a clock signal modulator.

4. The method of claim 1, wherein the first multiplexed signal is a data signal; and the first modulator is a data signal modulator.

5. The method of claim 1 further comprising:

providing the reference clock signal to a second multiplexer;

generating a second multiplexed signal by the second multiplexer based on the reference clock signal and according to the predetermined proportion; and

sending the second multiplexed signal to a second modulator,

wherein the timings of the first and second multiplexed signals are aligned.

6. The method of claim 5 further comprising driving before sending the second multiplexed signal to the second modulator.

7. The method of claim 5, wherein the second multiplexed signal is a clock signal; and the second modulator is a clock signal modulator.

8. The method of claim 5, wherein the second multiplexed signal is a data signal; and the second modulator is a data signal modulator.

9. The method of claim 5 further comprising:

generating a feedback control signal based on a phase difference between a first modulator output and a second modulator output; and

controlling the phase shifting by the phase shifter according to the feedback control signal,

wherein an optimal alignment of timings of the first and second multiplexed signals can be locked.

10. The method of claim 5 further comprising:

generating a first multiplexed clock signal identical to the first multiplexed signal by the first multiplexer;

generating a second multiplexed clock signal identical to the second multiplexed signal by the second multiplexer;

generating a feedback control signal based on a phase difference between the first multiplexed clock signal and the second multiplexed clock signal; and

controlling the phase shifting by the phase shifter according to the feedback control signal,

wherein an optimal alignment of timings of the first and second multiplexed signals can be locked.

11. A method for making timing alignment for a data transmission system, the method comprising:

providing a reference clock signal with a first frequency to a first multiplexer through a phase shifter;

providing the reference clock signal directly to a second multiplexer;

generating a first multiplexed signal with a second frequency by the first multiplexer, wherein the second frequency follows the first frequency and is higher than the first frequency by a predetermined proportion;

generating a second multiplexed signal based on the reference clock signal and according to the predetermined proportion;

sending the first multiplexed signal to a first modulator;

sending the second multiplexed signal to a second modulator; and

phase shifting the reference clock signal by the phase shifter before the reference clock signal is provided to the first multiplexer,

wherein timings of the first and second multiplexed signals can be aligned by adjusting a timing of the reference clock signal provided to the first multiplexer at the lower first frequency level.

12. The method of claim 11 further comprising driving before sending the first multiplexed signal to the first modulator.

13. The method of claim 11 further comprising driving before sending the second multiplexed signal to the second modulator.

14. The method of claim 11, wherein
the first multiplexed signal is a data signal;
the first modulator is a data signal modulator;
the second multiplexed signal is a clock signal; and
the second multiplexed signal is a clock signal modulator.

15. The method of claim 11, wherein
the first multiplexed signal is a clock signal;
the first modulator is a clock signal modulator;
the second multiplexed signal is a data signal; and
the second multiplexed signal is a data signal modulator.

16. The method of claim 11 further comprising:

generating a feedback control signal based on a phase difference between a first modulator output and a second modulator output; and

controlling the phase shifting by the phase shifter according to the feedback control signal,

wherein an optimal alignment of timings of the first and second multiplexed signals can be locked.

17. The method of claim 11 further comprising:

generating a first multiplexed clock signal identical to the first multiplexed signal by the first multiplexer;

generating a second multiplexed clock signal identical to the second multiplexed signal by the second multiplexer;

generating a feedback control signal based on a phase difference between the first multiplexed clock signal and the second multiplexed clock signal; and

controlling the phase shifting by the phase shifter according to the feedback control signal,

wherein an optimal alignment of timings of the first and second multiplexed signals can be locked.

18. A data transmission system with timing alignment, the system comprising:

a reference clock generating a first reference clock signal with a first frequency;

a first multiplexer receiving the first reference clock signal and generating a first multiplexed signal with a second frequency based on the first reference clock signal, wherein the second frequency follows the first frequency and is higher than the first frequency by a predetermined proportion;

a modulator coupled to the first multiplexer for modulating the first multiplexed signal; and

a phase shifter coupled between the reference clock and the first multiplexer for making phase adjustment to the first reference clock signal so that a timing of the multiplexed signal can be adjusted at the first frequency level.

19. The system of claim 18 further comprising a signal driver coupled between the first multiplexer and the first modulator for driving the first multiplexed signal.

20. The system of claim 18, wherein the first multiplexed signal is a clock signal; and the first modulator is a clock signal modulator.

21. The system of claim 18, wherein the first multiplexed signal is a data signal; and the first modulator is a data signal modulator.

22. The system of claim 18 further comprising:

the reference clock generating a second reference clock signal with the first frequency

a second multiplexer directly receiving the second reference signal and generating a second multiplexed signal based on the second reference signal and according to the predetermined proportion; and

a second modulator receiving the second multiplexed signal,

wherein the timings of the first and second multiplexed signals are aligned.

23. The system of claim 22 further comprising a second driver coupled between the second multiplexer and the second modulator for driving the second multiplexed signal.

24. The system of claim 22, wherein the second multiplexed signal is a clock signal; and the second modulator is a clock signal modulator.

25. The system of claim 22, wherein the second multiplexed signal is a data signal; and the second modulator is a data signal modulator.

26. The system of claim 22 further comprising:

one or more optical couplers coupled to a first output signal from the first modulator and a second output signal from the second modulator;

a photo detector coupled to the optical couples for analyzing a phase difference between the first output signal and the second output signal; and

a control unit coupled between the photo detector and the phase shifter for generating a control signal based on the phase difference to control the phase shifting,

wherein an optimal alignment of timings of the first and second multiplexed signals can be locked.

27. The system of claim 22 further comprising:

a first multiplexed clock signal identical to the first multiplexed signal both are generated by the first multiplexer;

a second multiplexed clock signal identical to the second multiplexed signal both are generated by the second multiplexer;

a radio frequency (RF) mixer coupled to both the first and second multiplexers for detecting a phase difference between the first and second multiplexed clock signals; and

a control unit coupled between the RF mixer and the phase shifter for generating a control signal based on the phase difference to control the phase shifting,

wherein an optimal alignment of timings of the first and second multiplexed signals can be locked.

28. A data transmission system with timing alignment, the system comprising:

a reference clock generating a first and a second reference clock signals both with a first frequency;

a first multiplexer receiving the first reference clock signal and generating a first multiplexed signal with a second frequency based on the first reference clock signal, wherein the second frequency follows the first frequency and is higher than the first frequency by a predetermined proportion;

a second multiplexer receiving the second reference clock signal and generating a second multiplexed signal based on the second reference clock signal and according to the predetermined proportion;

a first modulator coupled to the first multiplexer for modulating the first multiplexed signal;

a second modulator coupled to the second multiplexer for modulating the second multiplexed signal; and

a phase shifter coupled between the reference clock and the first multiplexer for making phase adjustment to the first reference clock signal so that a timing of the multiplexed signal can be adjusted at the first frequency level.

29. The system of claim 28 further comprising a first signal driver coupled between the first multiplexer and the first modulator for driving the first multiplexed signal.

30. The system of claim 28 further comprising a second signal driver coupled between the second multiplexer and the second modulator for driving the second multiplexed signal.

31. The system of claim 28, wherein

the first multiplexed signal is a data signal;

the first modulator is a data signal modulator;

the second multiplexed signal is a clock signal; and

the second multiplexed signal is a clock signal modulator.

32. The system of claim 28, wherein

the first multiplexed signal is a clock signal;

the first modulator is a clock signal modulator;

the second multiplexed signal is a data signal; and

the second multiplexed signal is a data signal modulator.

33. The system of claim 28 further comprising:

one or more optical couplers coupled to a the first output signal from the first modulator and a second output signal from the second modulator;

a photo detector coupled to the optical couples for analyzing a phase difference between the first output signal and the second output signal; and

a control unit coupled between the photo detector and the phase shifter for generating a control signal based on the phase difference to control the phase shifting,

wherein an optimal alignment of timings of the first and second multiplexed signals can be locked.

34. The system of claim 28 further comprising:

a first multiplexed clock signal identical to the first multiplexed signal both are generated by the first multiplexer;

a second multiplexed clock signal identical to the second multiplexed signal both are generated by the second multiplexer;

a radio frequency (RF) mixer coupled to both the first and second multiplexers for detecting a phase difference between the first and second multiplexed clock signals; and

a control unit coupled between the RF mixer and the phase shifter for generating a control signal based on the phase difference to control the phase shifting,

wherein an optimal alignment of timings of the first and second multiplexed signals can be locked.

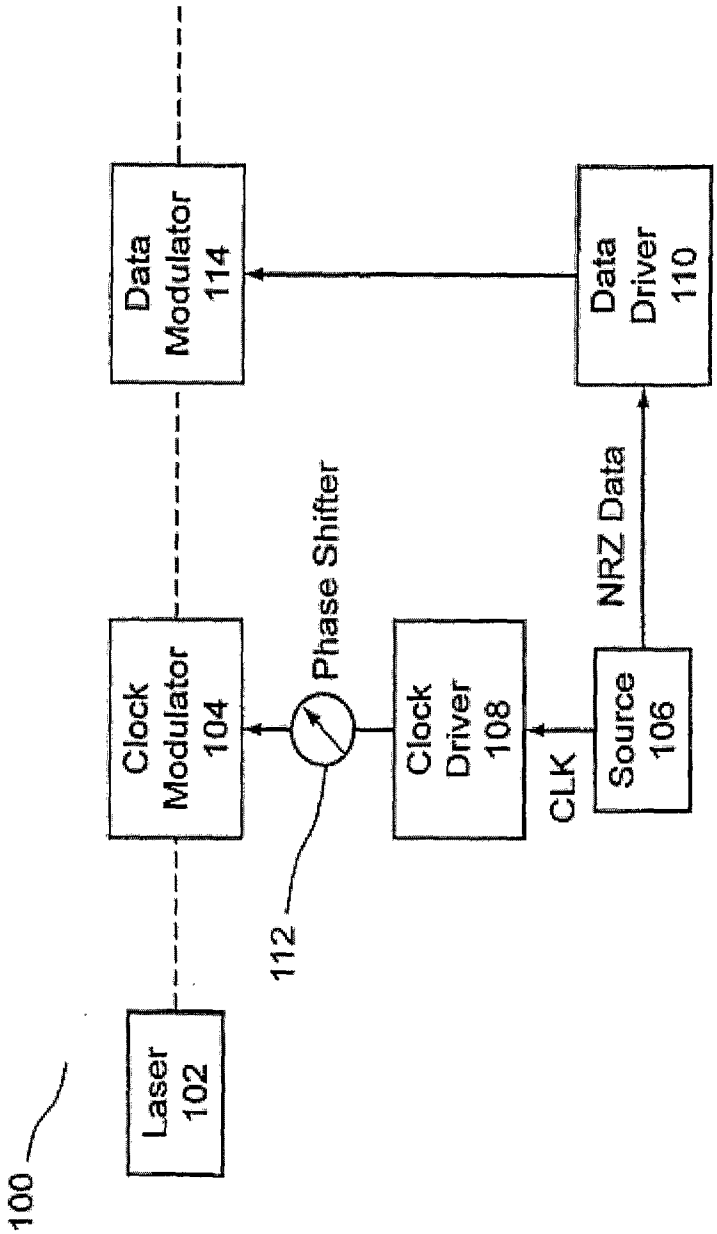
100
Laser 102
Clock Modulator 104
Data Modulator 114
112
Phase Shifter
Clock Driver 108
CLK
Source 106
NRZ Data
Data Driver 110

FIG. 1A

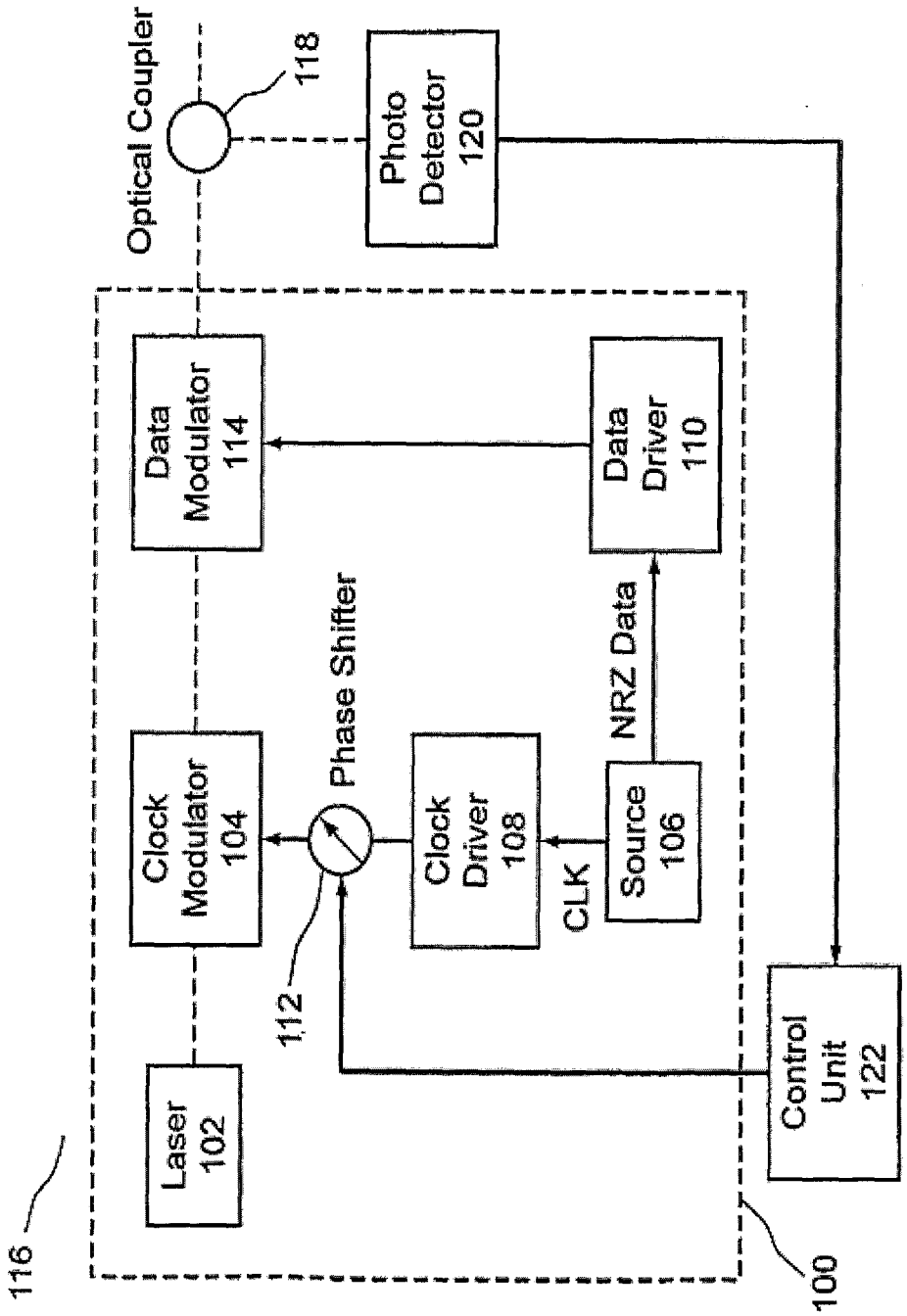
Optical Coupler
118
Photo Detector 120
Data Modulator 114
Data Driver 110
Clock Modulator 104
Phase Shifter
Clock Driver 108
NRZ Data
Source 106
CLK
112
Laser 102
Control Unit 122
116
100

FIG. 1B

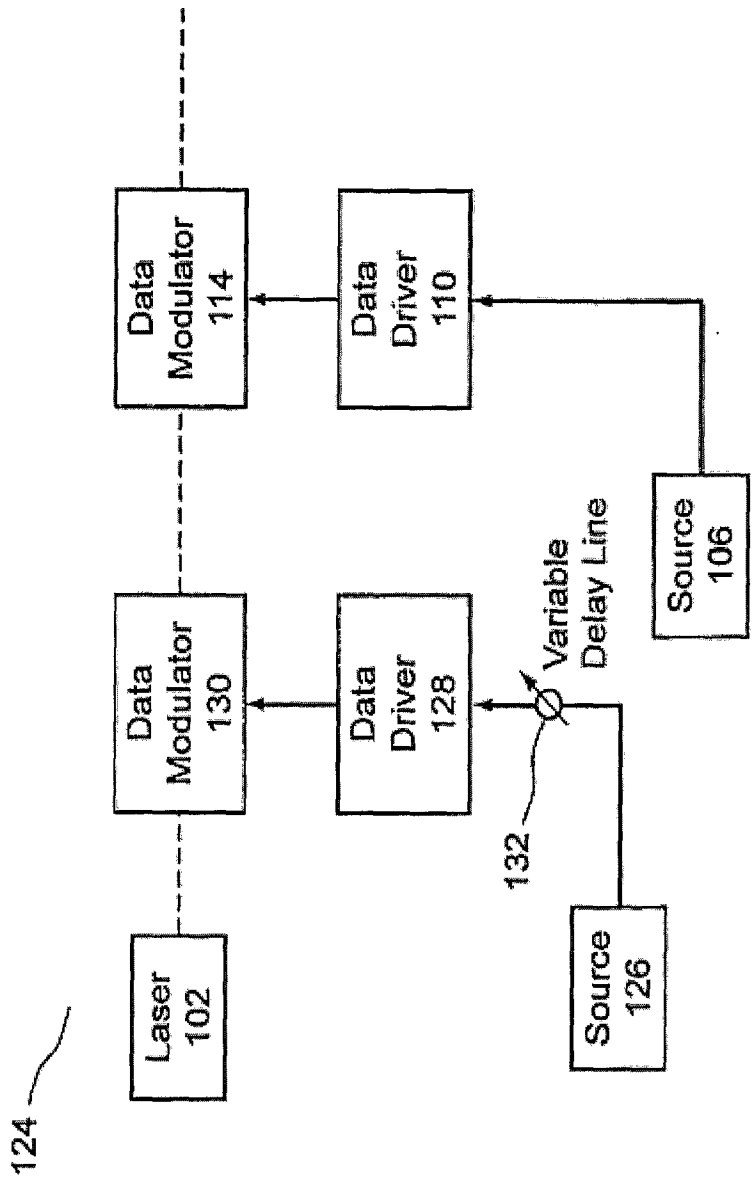
Data Modulator 114
Data Driver 110
Data Modulator 130
Data Driver 128
Variable Delay Line
Source 106
Source 126
Laser 102
132
124

FIG. 1C

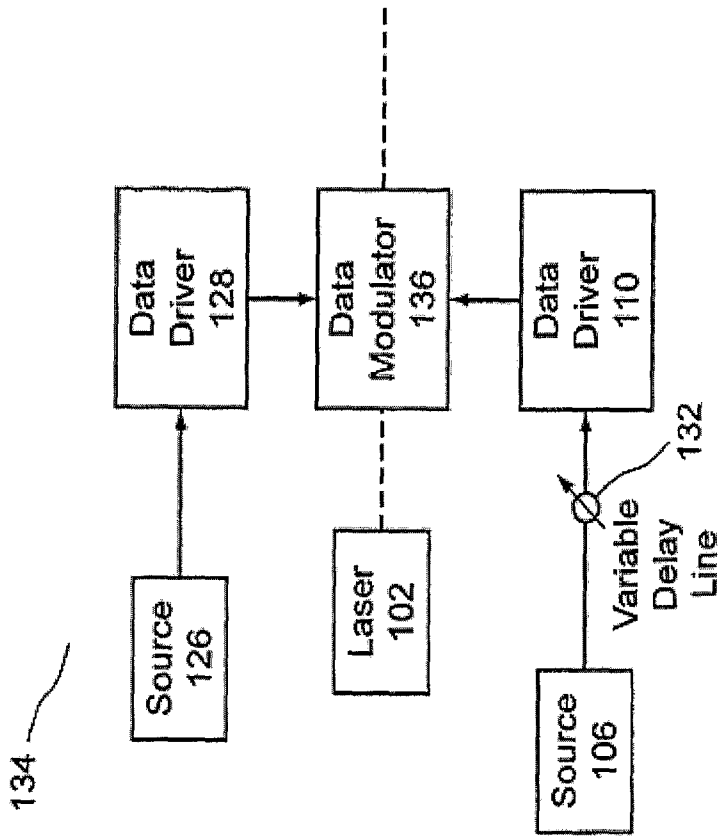
Data Driver 128
Data Modulator 136
Data Driver 110
Source 126
Laser 102
Variable Delay Line
132
Source 106
134

FIG. 1D

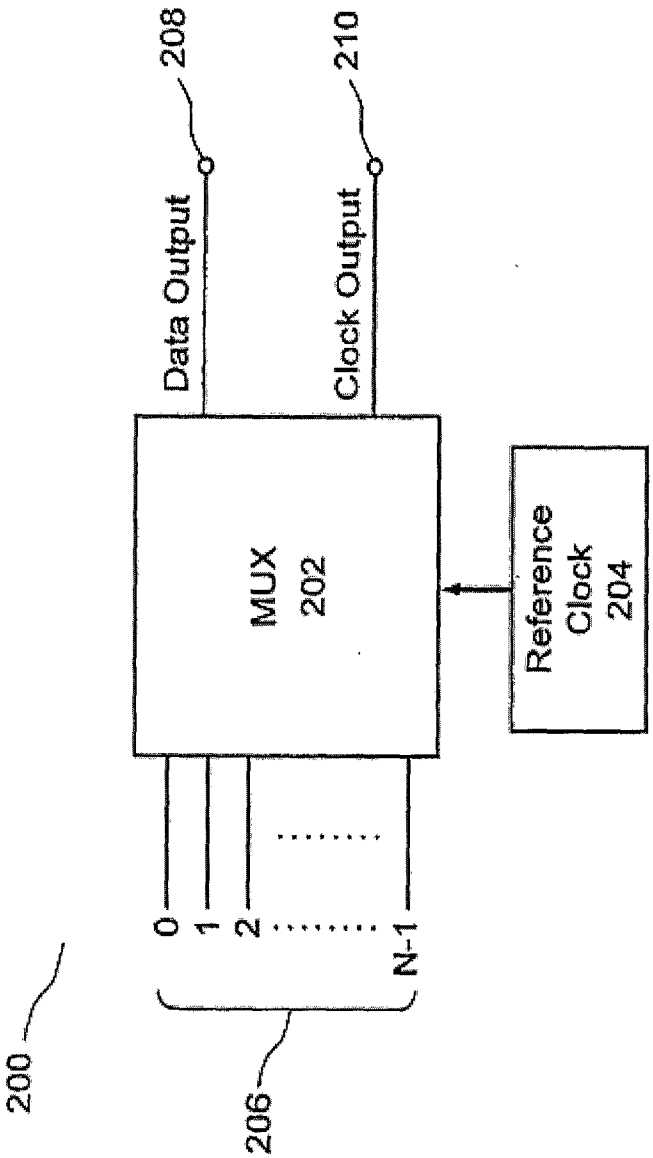
208
210
Data Output
Clock Output
MUX
202
Reference
Clock
204
0
1
2
N-1
200
206

FIG. 2

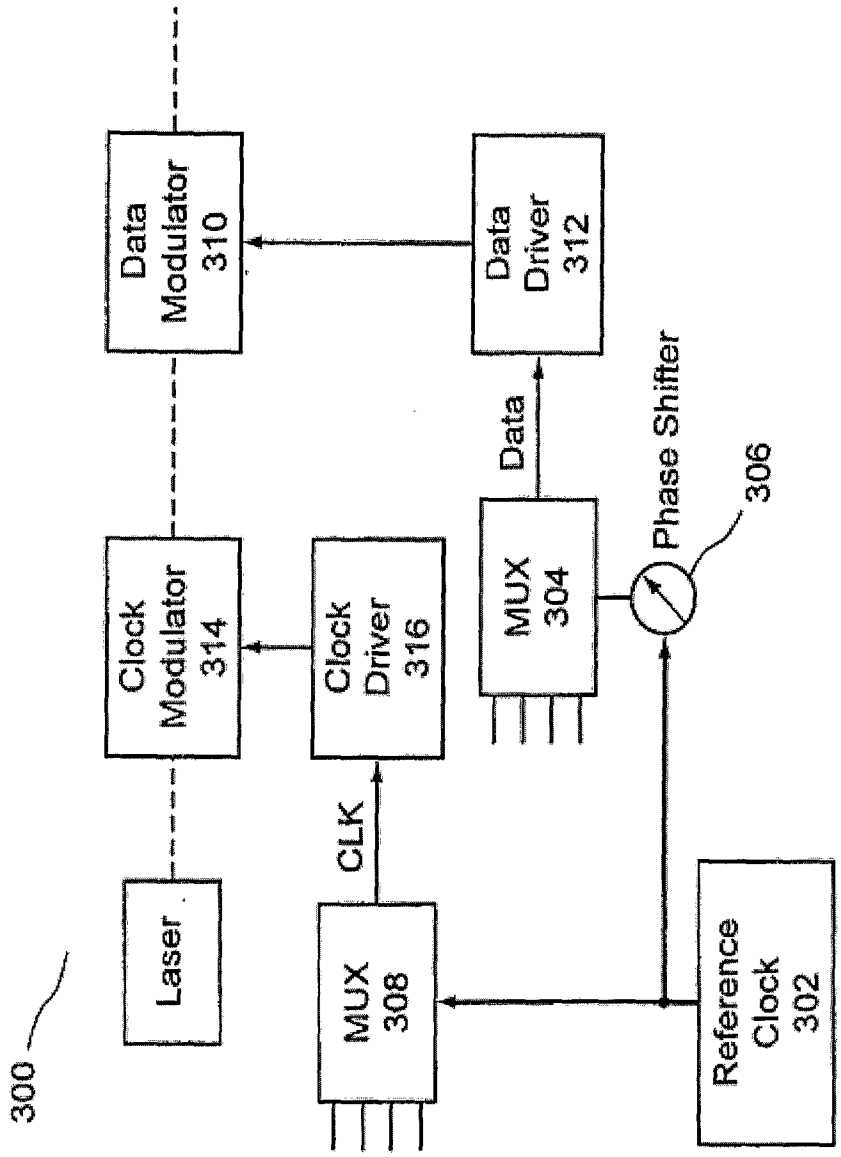
300
Laser
Clock Modulator 314
Data Modulator 310
CLK
Clock Driver 316
MUX 308
Data
MUX 304
Phase Shifter
306
Data Driver 312
Reference Clock 302

FIG. 3A

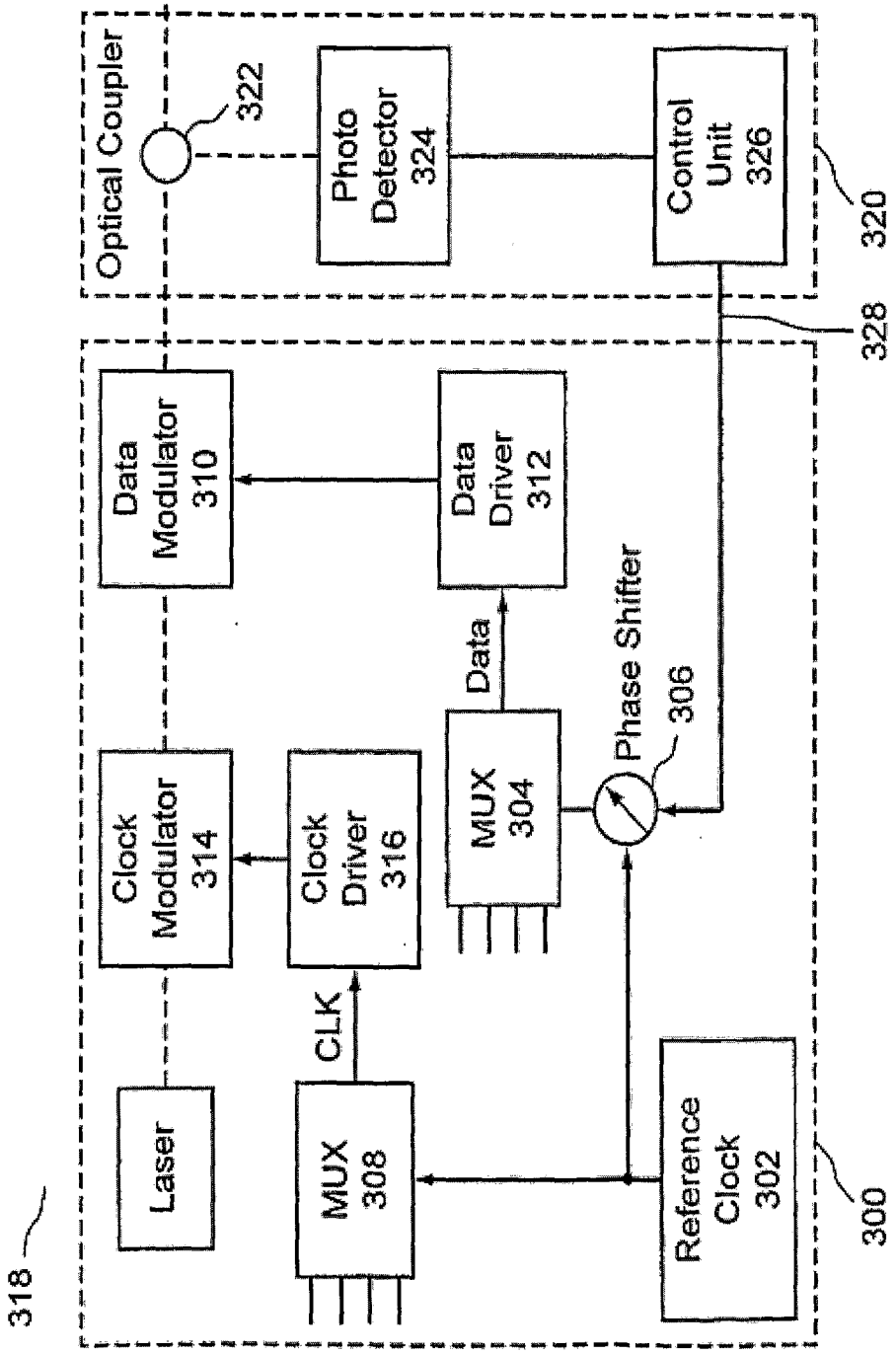
318
Optical Coupler
322
Photo Detector 324
Control Unit 326
320
328
Data Modulator 310
Data Driver 312
Clock Modulator 314
Clock Driver 316
MUX 304
Phase Shifter
306
Data
CLK
Laser
MUX 308
Reference Clock 302
300

FIG. 3B

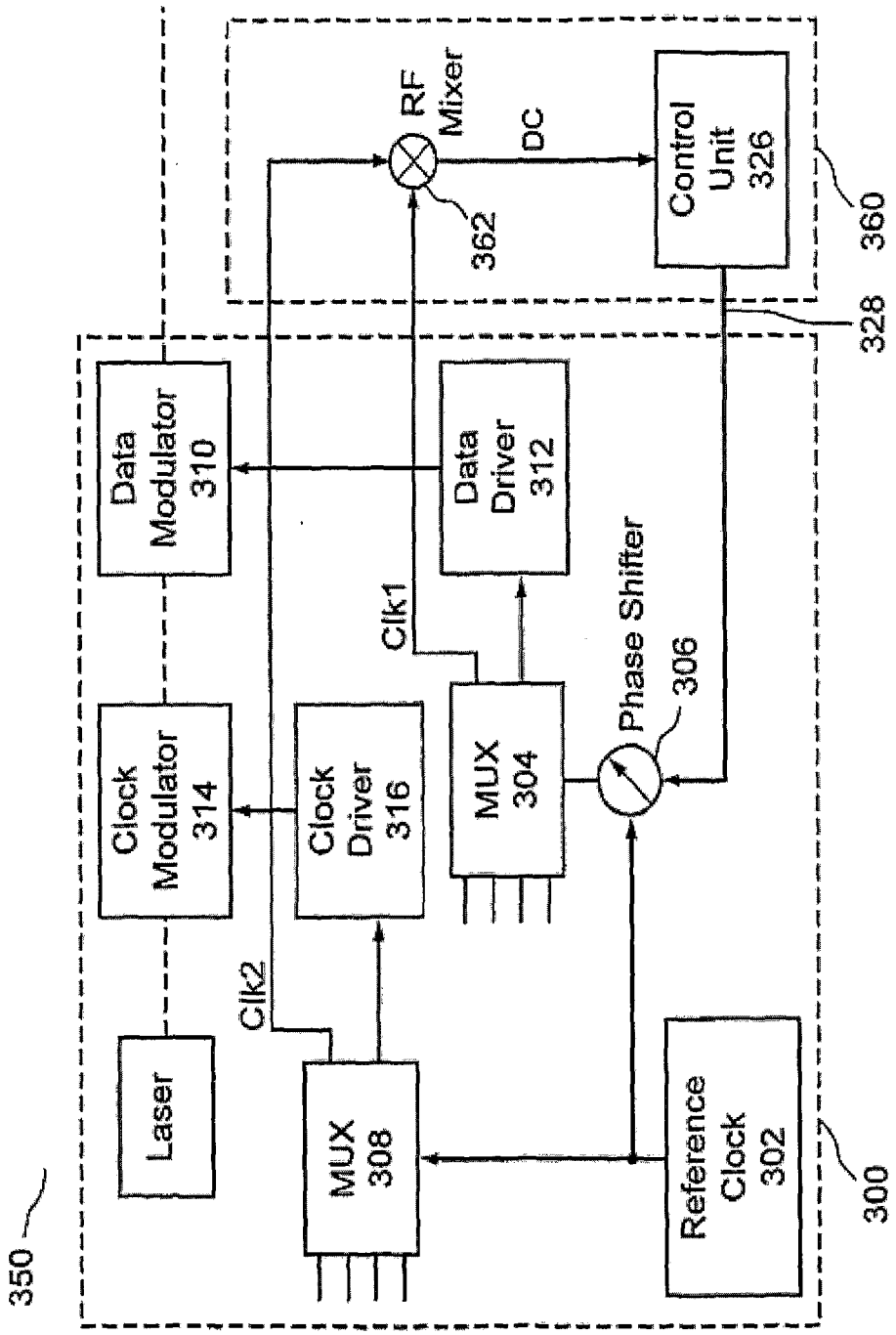
350
Laser
Clock Modulator 314
Data Modulator 310
MUX 308
Clock Driver 316
Data Driver 312
MUX 304
Clk1
Clk2
Phase Shifter
306
Reference Clock 302
300
328
RF Mixer
362
DC
Control Unit 326
360

FIG. 3C

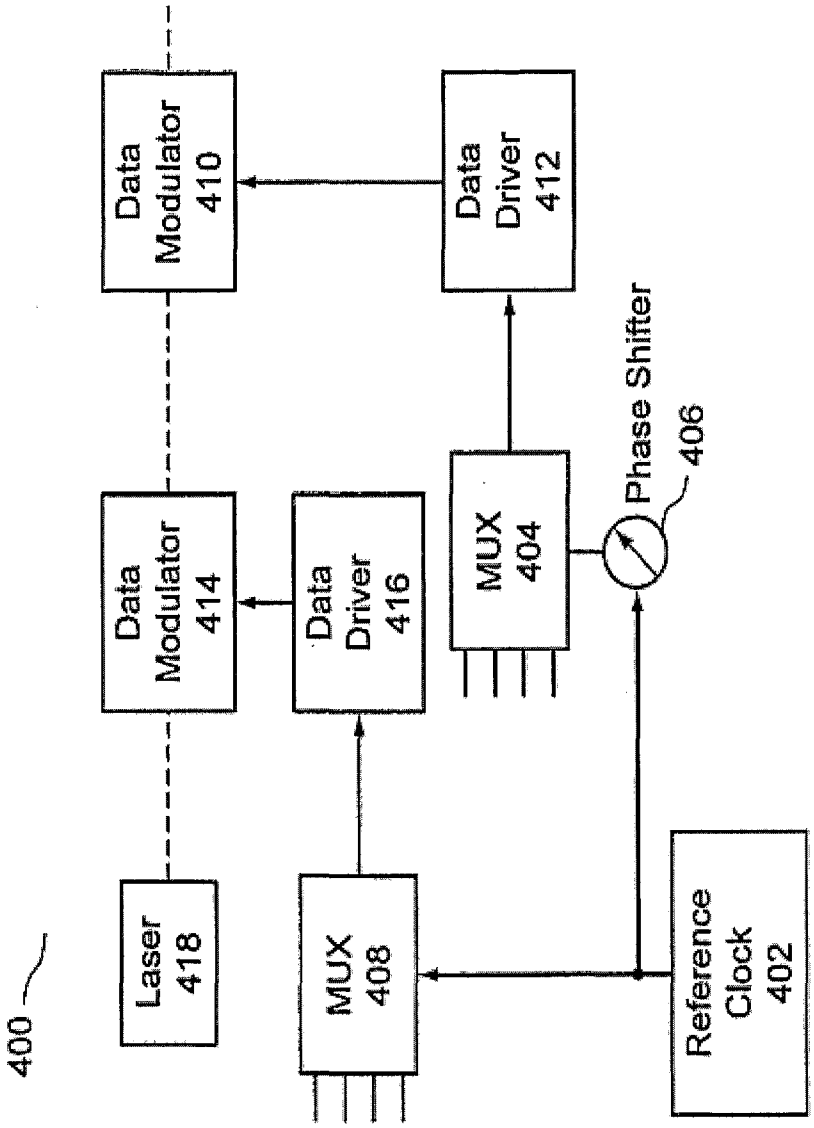
400
Laser 418
Data Modulator 414
Data Modulator 410
MUX 408
Data Driver 416
Data Driver 412
MUX 404
Phase Shifter 406
Reference Clock 402

FIG. 4A

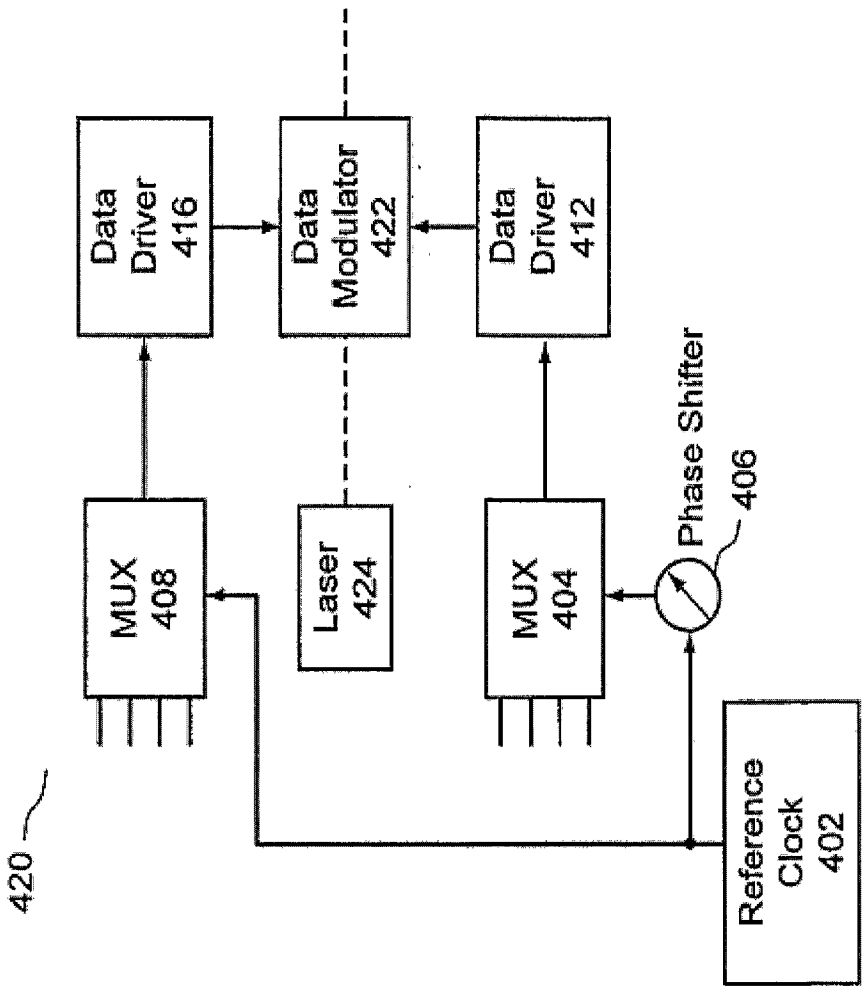
Data Driver 416
Data Modulator 422
Data Driver 412
MUX 408
Laser 424
MUX 404
Phase Shifter 406
Reference Clock 402
420

FIG. 4B

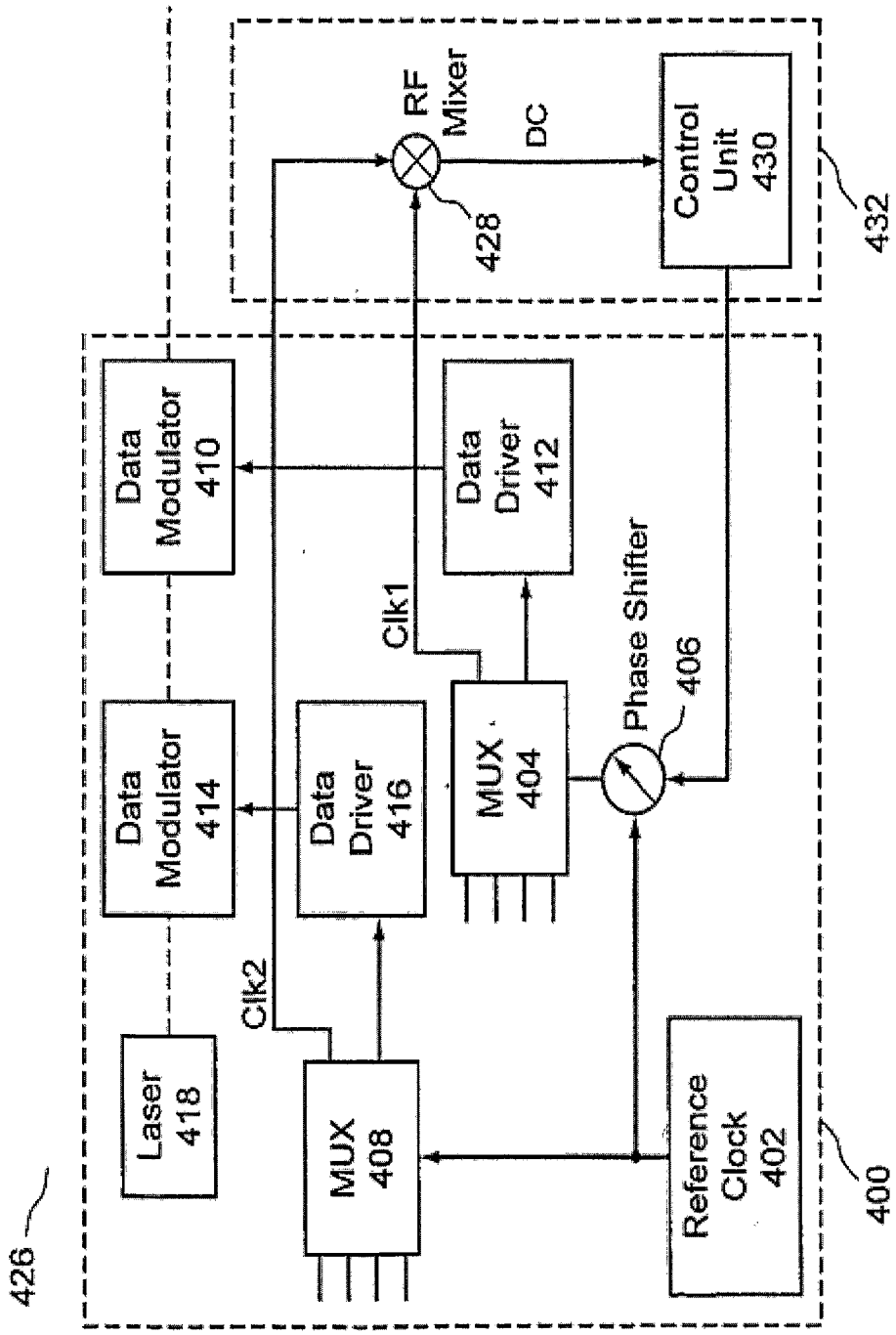
RF Mixer
DC
Control Unit 430
428
432
Data Modulator 410
Data Driver 412
Clk1
Phase Shifter
406
Data Modulator 414
Data Driver 416
MUX 404
Clk2
Laser 418
MUX 408
Reference Clock 402
400
426

FIG. 4C

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2007/000981

A. CLASSIFICATION OF SUBJECT MATTER

SEE EXTRA SHEET

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC:H04B10/12; H04B10/22; H04B10/24; H04B10/30; H04B10/18; H04B10/00; H04B10/08; H04B10/02;H04J14/08; H04J14/00;G02F1/35;G02F1/00;H03L7/07;H03L7/06;H03L7/00;H03L7/22;H03L7/16;H04L7/02;H04L7/00;H04J3/06;H04J3/02;H04J3/00;H03D3/18;H03D3/02;H03D3/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI;EPODOC;PAJ;CNPAT;CNKI;ALIGNMENT;TRANSMISSION;TRANSMITTING;TRANSMIT;OPTICAL;CLOCK;FREQUENCY;MULTIPLEXE+;PHASE; SHIFT+;MIDULATOR;FEEDBACK;RZ;NRZ;CONTROL+;ADJUST+;MONITOR+;DETECT+;RF;MODULE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX,L	WO2006/122503A (HUAWEI TECHNOLOGIES CO., LTD.), 23 November 2006 (23.11.2006), paragraph 2 of page 6 to paragraph 4 of page 8, and FIGs 3A,3B.	1-34
A	WO2005/109698A1 (HUAWEI TECHNOLOGIES CO., LTD.), 17 November 2005 (17.11.2005), the whole document	1-34
A	CN1463109A (CIT ALCATEL), 24 December 2003, (24.12.2003), the whole document	1-34
A	CN1174634A (CURTIN UNIV. OF TECHNOLOGY), 25 February 1998 , (25.02.1998), the whole document	1-34
A	JP 3-274835A (MITSUBISHI ELECTRIC CORP), 12 May 1991, (12.05.1991) , the whole document	1-34
A	US6763074B1 (Ganning Yang), 13 July 2004, (13.07. 2004) , the whole document	1-34

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
6 June 2007 (06.06.2007)	**05 Jul. 2007 (05.07.2007)**
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer WANG, Lishi Telephone No. (86-10)82336282

Form PCT/ISA /210 (second sheet) (April 2007)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2007/000981

CLASSIFICATION OF SUBJECT MATTER

H04B10/12(2006.01)i

H04B10/22(2006.01)i

H04B10/24(2006.01)i

H04B10/30(2006.01)i

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2007/000981

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
WO2006/122503A	23.11.2006	US2006280507A1	14.12.2006
		US2006264325 A1	23.11.2006
		US2006263095 A1	23.11.2006
WO2005/109698A1	17.11.2005	EP1714410 A1	25.10.2006
		US2005254825 A1	17.11.2005
CN1463109A	24.12.2003	DE60207690T	22.06.2006
		AT311700T	15.12.2005
		DE60207690D	05.01.2006
		US2003223753 A1	04.12.2003
		EP1367755 A1	03.12.2003
CN1174634A	25.02.1998	US6031428 A	29.02.2000
		EP0795234 A1	17.09.1997
		DE69513041T	08.06.2000
		DE69513041D	02.12.1999
		WO9617435 A1	06.06.1996
		AU3899695 A	19.06.1996
		AU710299B	16.09.1999
JP 3-274835A	12.05.1991	NONE	
US6763074 B1	13.07. 2004	NONE	