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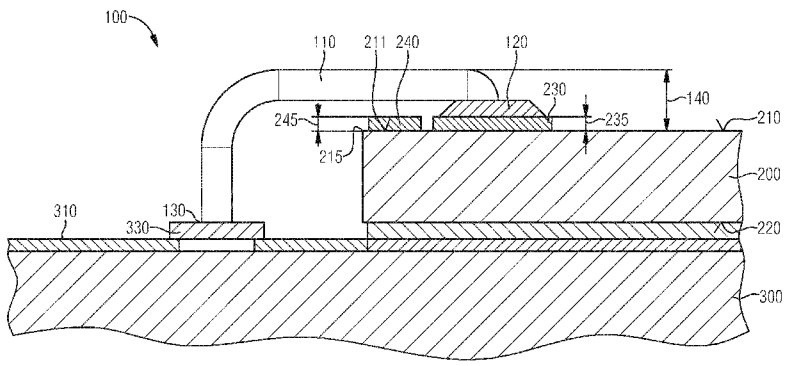
(54) Title: ELECTRONIC DEVICE AND METHOD FOR PRODUCING AN ELECTRONIC DEVICE

FIG 1



(57) Abstract: An electronic device comprises a semiconductor chip (200) with a surface. A bond pad (230) is arranged on said surface. A layer of electrically insulating material (240) is arranged on said surface in a section of said surface. The section is arranged between said bond pad (230) and an edge of said surface. A bond wire (110) is arranged between said bond pad (230) and a contact pad (330).

Description

Electronic device and method for producing an electronic device

The present invention relates to an electronic device according to claim 1 and to a method for producing an electronic device according to claim 11.

It is known in the state of the art to arrange semiconductor chips of electronic devices on boards. It is further known to electrically connect bond pads arranged on such semiconductor chips to contact pads arranged on such boards by bond wires. One known method of arranging a bond wire is the ball stitch on ball bonding sequence. This method allows for producing low-profile bond connections with bond wire loops that extend only to a limited height above a chip surface. The ball stitch on ball bonding sequence comprises a first step of forming a stud ball bump on a bond pad. In a second step the contact pad is reversely bonded to the bond pad by ball bonding onto the contact pad and stitch bonding onto the ball bump arranged on the bond pad.

It is necessary to prevent an electric short between a bond wire and a surface of a semiconductor chip. It is known in the state of the art to provide bond wires with electrically insulating coatings in order to prevent such short circuits. Such coating increases the cost of the bonding wire. It is also known to design electronic devices with defined minimal clearances between bond wires and chip surfaces or bond wires and neighbouring bond wires respectively to prevent wire shorts. This puts a limit on increasing the number of interconnections per unit area and the possibility of reducing the size of electronic devices.

It is an object of the present invention to provide an electronic device. This objective is achieved by an electronic

device with the features of claim 1. It is a further object of the present invention to provide a method for producing an electronic device. This objective is achieved by a method comprising the features of claim 11. Preferred embodiments are disclosed in the dependant claims.

An electronic device comprises a semiconductor chip with a surface. A bond pad is arranged on said surface. A layer of electrically insulating material is arranged on said surface in a section of said surface. The section is arranged between said bond pad and an edge of said surface. A bond wire is arranged between said bond pad and a contact pad. Advantageously, the layer of electrically insulating material of this electronic device prevents an electric short between the bond wire and the surface of the semiconductor chip. This allows for arranging the bond wire in a low loop above the surface of the semiconductor chip. Advantageously, this allows for providing the bond wire with a short length, allowing for arranging more interconnections per unit area. Consequently, signal wires and ground wires may be brought very closely together in order to minimize inductances. A short bond wire may also prevent the bond wire from swaying or sagging. Advantageously, this also prevents neighbouring bond wires from shorting.

In an embodiment the electronic device comprises a board. The chip is arranged on said board. The contact pad is also arranged on said board. Advantageously, the bond wire provides an electrical connection between the semiconductor chip and the board of the electronic device.

In an embodiment of the electronic device, the contact pad is arranged on a second semiconductor chip. Advantageously, the bond wire serves to connect the two semiconductor chips directly to each other, allowing for a high bandwidth connection. Advantageously, the direct connection between the semiconductor chips may eliminate layers of chip level wiring,

substrate level wiring and board level wiring and allow for a routing with higher flexibility.

In an embodiment of the electronic device, said layer of electrically insulating material comprises a resist. Advantageously, this allows for an easy and cost-efficient arrangement of the layer of electrically insulating material on the surface of the semiconductor chip.

In an embodiment of the electronic device, said layer of insulating material comprises a thickness of less than 1 µm. Advantageously, a layer with such a thickness provides a sufficient electrical insulation.

In an embodiment of the electronic device, a thickness of said layer of insulating material is smaller or equal to a thickness of said bond pad. Advantageously, this allows for the bond wire to run from the bond pad to the contact pad in a low-profile loop.

In an embodiment of the electronic device, a thickness of said layer of insulating material differs from a thickness of said bond pad by less than 20 %. Advantageously, this ensures that the layer of insulating material prevents an electric short between the bond wire and the surface of the semiconductor chip.

In an embodiment of the electronic device, the bond wire extends less than 100 µm above said bond pad. Advantageously, this results in a low height profile of the electronic device.

In an embodiment of the electronic device, the bond wire comprises gold. Advantageously, bond wires comprising gold provide good mechanical and electrical properties.

In an embodiment of the electronic device, the semiconductor chip is an optoelectronic semiconductor chip. In this embodi-

ment the electronic device is an optoelectronic device. The optoelectronic semiconductor chip may for example be a light emitting diode chip, a semiconductor laser chip or a chip comprising a photovoltaic solar cell.

A method for producing an electronic device comprises steps of providing a semiconductor chip comprising a surface, wherein a bond pad is arranged on said surface, of arranging a layer of electrically insulating material on said surface in a section of said surface, wherein the section is arranged between said bond pad and an edge of said surface, and of arranging a bond wire between said bond pad and a contact pad. Advantageously, this method allows for producing an electronic device with a low height profile. The bond wire of the electronic device is advantageously secured against shorting to the surface of the semiconductor chip by the layer of electrically insulating material arranged on the surface of the semiconductor chip. This may decrease a yield loss due to wire shorts. The method allows for using very short bond wires which enables providing more interconnections per unit area and allows for using small semiconductor chips with small bond pads.

In an embodiment of the method, the bond wire is arranged using a ball stitch on ball bonding sequence. Advantageously, this allow for arranging the bond wire with a wire loop with a low height profiles.

In an embodiment of the method, the bond wire is bonded from the contact pad to the bond pad. Advantageously, this allows for connecting the bond wire to the bond pad at a low angle, allowing for a low overall height profile.

The accompanying drawings are included in order to provide a further understanding of the present invention and are incorporated into and constitute a part of this specification. The drawings illustrate embodiments of the present invention and together with the description serve to explain the principles

of the invention. Other embodiments of the present invention and many of the intended advantages of the present invention will be readily appreciated as they will be better understood by reference to the following detailed description. The elements of the drawings are not to scale with regard to each other.

Figure 1 shows a schematic sectional representation of a part of an electronic device; and

Figure 2 shows a schematic flow diagram of a method for producing an electronic device.

Figure 1 shows a schematic sectional drawing of a part of an electronic device 100. The electronic device 100 my be an optoelectronic device or another kind of electronic device. The electronic device 100 may for example be a light-emitting diode (LED) device, a laser device or a photovoltaic device.

The electronic device 100 comprises a semiconductor chip 200. The semiconductor chip 200 may be an optoelectronic semiconductor chip or another kind of semiconductor chip. The semiconductor chip 200 may for example be a light-emitting diode chip, a semiconductor laser chip or a chip comprising a photovoltaic cell. The semiconductor chip 200 may also be referred to as a die.

The semiconductor chip 200 comprises an upper surface 210 and a lower surface 220 on the opposite side of the upper surface 210. The upper surface 210 may be provided for a passage of electromagnetic radiation, for example a passage of visible light.

A bond pad 230 is arranged on the upper surface 210 of the semiconductor chip 200. The bond pad 230 is provided for electrically connecting the semiconductor chip 200. Further electric contacts of the semiconductor chip 200 may be ar-

ranged on the upper surface 210 or the lower surface 220 of the semiconductor chip 200.

The electronic device 100 further comprises a board 300. The board 300 serves as a carrier for the semiconductor chip 200. The semiconductor chip 200 is arranged on an upper side 310 of the board 300. The lower surface 220 of the semiconductor chip 200 faces the upper side 310 of the board 300. The lower surface 220 of the semiconductor chip 200 may for example be soldered or glued onto the upper side 310 of the board 300.

The board 300 of the electronic device 100 also serves to provide an electrical connection to the semiconductor chip 200. A contact pad 330 is arranged on the upper side 310 of the board 300 nearby the semiconductor chip 200. A bond wire 110 runs from the contact pad 330 on the upper side 310 of the board 300 to the bond pad 230 on the upper surface 210 of the semiconductor chip 200 and electrically connects the contact pad 330 to the bond pad 230. The bond wire 110 comprises an electrically conducting material. The bond wire 110 may for example comprise gold. The bond wire 110 may for example comprise a diameter of 30 µm or 38 µm.

Between the bond pad 230 of the semiconductor chip 200 and the contact pad 330 of the board 300, the bond wire 110 forms a loop with a low height profile. Between the bond pad 230 and the contact pad 330, the bond wire 110 reaches a bond wire height 140 above the upper surface 210 of the semiconductor chip 200. The bond wire height 130 is preferably below 100 µm, in particular below 90 µm.

The bond wire 110 may be arranged between the bond pad 230 and the contact pad 330 using a ball stitch on ball bonding (BSOB) sequence. In this case, the bond wire 110 is connected to the bond pad 230 on the upper surface 210 of the semiconductor chip 200 by a stitch bond 120 and to the contact pad 330 on the upper side 310 of the board 300 by a ball bond 130. An acute angle between the bond wire 110 and the bond

pad 230 at the location of the stitch bond 120 may support a low-profile loop of the bond wire 110. The ball bond 130 may be created before the stitch bond 120. The bond wire 110 may be bonded from the contact pad 330 to the bond pad 230.

Due to the low height profile of the loop of the bond wire 110 between the bond pad 230 and the contact pad 330, the bond wire 110 runs in close proximity to the upper surface 210 of the semiconductor chip 200. In order to prevent a short between the bond wire 110 and the semiconductor chip 200, the bond wire 110 should remain electrically insulated from the upper surface 210 of the semiconductor chip 200. To this end, an insulating layer 240 is arranged in a section 211 on the upper surface 210 of the semiconductor chip 200. The section 211 is located between the bond pad 230 and an outer edge 215 of the upper surface 210. The bond wire 110 extends over the section 211 of the upper surface 210 and thus over the insulating layer 240 arranged in that section 211.

The insulating layer 240 comprises an electrically insulating material. The insulating layer 240 may for example comprise a resist.

The lateral dimensions of the insulating layer 240 are large enough to prevent the bond wire 110 from touching the upper surface 210 of the semiconductor chip 200 even if the bond wire 110 sways or sags. The lateral dimensions of the insulating layer 240 may for example be as large as the lateral dimensions of the bond pad 230 or larger than the lateral dimensions of the bond pad 230.

In a direction perpendicular to the upper surface 210, the bond bad 230 comprises a bond pad thickness 235. The insulating layer 240 comprises an insulating layer thickness 245 in the direction perpendicular to the upper surface 210. The bond pad thickness 235 may be below 1 µm. The bond pad thickness 235 may for example be 900 nm. The thickness 235 of the

bond pad 230 is preferably about the same as the thickness 235 of the bond pad 230 or less than the thickness 235 of the bond pad 230. The thickness 245 of the insulating layer 240 and the thickness 235 of the bond pad 230 preferably differ by less than 20 %. The thickness 245 of the insulating layer 240 is preferably less than 1 µm.

In an alternative embodiment of the electronic device, the contact pad 330 is not arranged on the board 300 but is a bond pad of a further semiconductor chip. In this embodiment, the bond wire 110 consequently serves to electrically connect the bond pad 230 of the semiconductor chip 200 to the bond pad of the further semiconductor chip. The board 300 may be omitted in this embodiment.

Figure 2 shows a schematic flow diagram of a method 400 for producing the electronic device 100.

In a first step 410, the semiconductor chip 200 is provided. The semiconductor chip 200 comprises the upper surface 210 with the bond pad 230 arranged on the upper surface 210.

In a second step 420, the insulating layer 240 is arranged on the upper surface 210. The insulating layer 240 is arranged in the section 211 which is located between the bond pad 230 and the edge 215 of the upper surface 210. The insulating layer 240 comprises an electrically insulating material, for example a resist. The insulating layer 240 may for example be arranged on the upper surface 210 in a last production step during a front-end assembly before polishing the semiconductor chip 200.

In a third step 430, the bond wire 110 is arranged between the bond pad 230 and the contact pad 330. The bond wire 110 may for example be arranged using a ball stitch on ball bonding sequence. The bond wire 110 may be bonded from the contact pad 330 to the bond pad 230.

While the invention has been described in detail with reference to specific embodiments thereof, it will be apparent to one of ordinary skill in the art that various changes and modifications can be made therein without departing from the spirit and scope thereof. Accordingly, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

Reference numbers

100	electronic device
110	bond wire
120	stitch bond
130	ball bond
140	bond wire height
200	semiconductor chip
210	upper surface
211	section
215	edge
220	lower surface
230	bond pad
235	bond pad thickness
240	insulating layer
245	insulating layer thickness
300	board
310	upper side
330	contact pad
400	production method
410	first step
420	second step
430	third step

Claims

1. An electronic device (100)
comprising a semiconductor chip (200) with a surface (210),
wherein a bond pad (230) is arranged on said surface (210),
wherein a layer (240) of electrically insulating material is arranged on said surface (210) in a section (211) of said surface (210),
wherein the section (211) is arranged between said bond pad (230) and an edge (215) of said surface (210);
wherein a bond wire (110) is arranged between said bond pad (230) and a contact pad (330).

2. The electronic device (100) as claimed in claim 1,
wherein the electronic device (100) comprises a board (300),
wherein the chip (200) is arranged on said board (300),
wherein the contact pad (330) is arranged on said board (300).

3. The electronic device (100) as claimed in claim 1,
wherein the contact pad (330) is arranged on a second semiconductor chip.

4. The electronic device (100) as claimed in any one of the preceding claims,
wherein said layer (240) of electrically insulating material comprises a resist.

5. The electronic device (100) as claimed in any one of the preceding claims,
wherein said layer (240) of insulating material comprises a thickness (245) of less than 1 µm.

6. The electronic device (100) as claimed in any one of the preceding claims,

wherein a thickness (245) of said layer (240) of insulating material is smaller or equal to a thickness (235) of said bond pad (230).

7. The electronic device (100) as claimed in any one of the preceding claims,
wherein a thickness (245) of said layer (240) of insulating material differs from a thickness (235) of said bond (230) pad by less than 20 %.

8. The electronic device (100) as claimed in any one of the preceding claims,
wherein the bond wire (110) extends less than 100 µm above said bond pad (230).

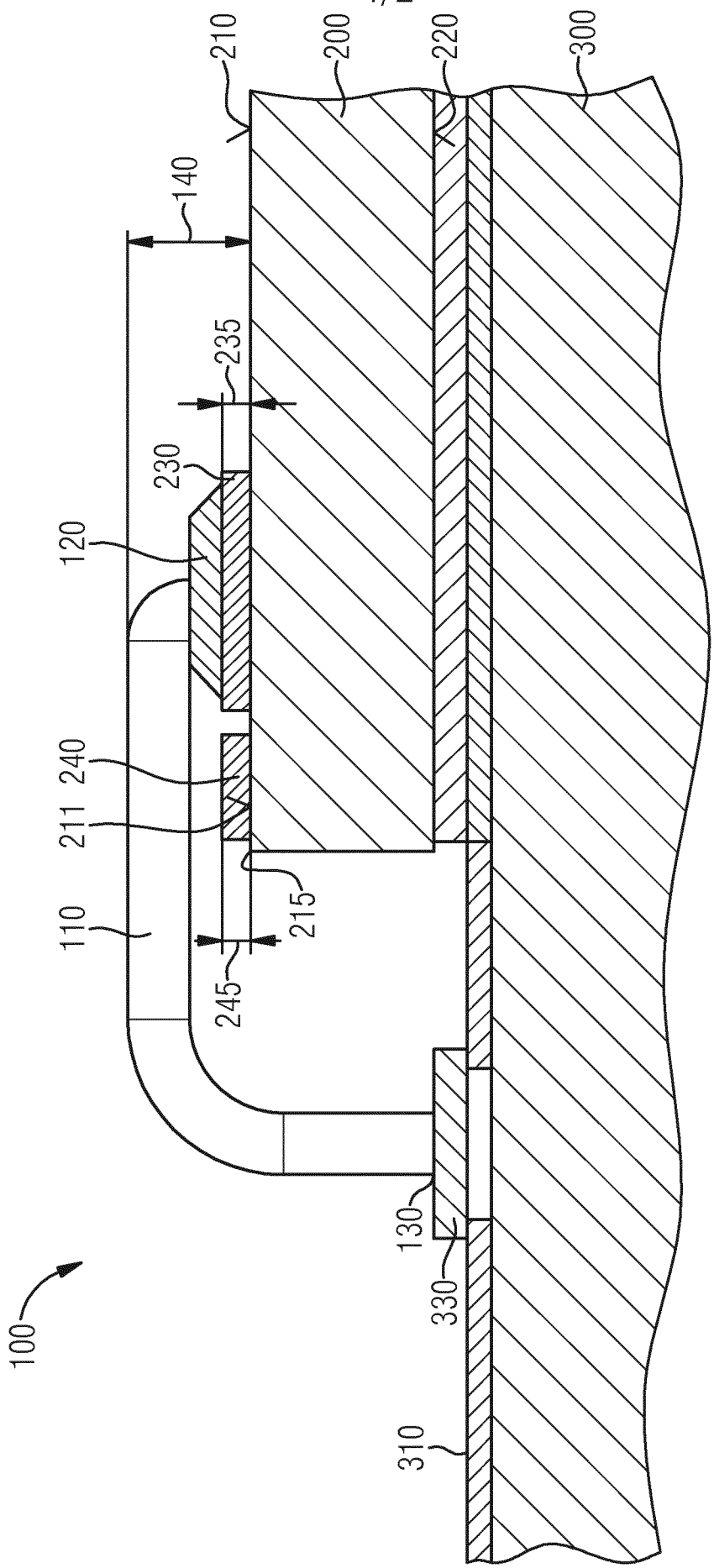
9. The electronic device (100) as claimed in any one of the preceding claims,
wherein the bond wire (110) comprises gold.

10. The electronic device (100) as claimed in any one of the preceding claims,
wherein the semiconductor chip (200) is an optoelectronic semiconductor chip.

11. A method for producing an electronic device (100) comprising the following steps:
- providing a semiconductor chip (200) comprising a surface (210), wherein a bond pad (230) is arranged on said surface (210);
- arranging a layer (240) of electrically insulating material on said surface (210) in a section (211) of said surface (210), wherein the section (211) is arranged between said bond pad (230) and an edge (215) of said surface (210);
- arranging a bond wire (110) between said bond pad (230) and a contact pad (330).

12. The method as claimed in claim 11, wherein the bond wire (110) is arranged using a ball stitch on ball bonding sequence.

13. The method as claimed in any one of claims 11 and 12, wherein the bond wire (110) is bonded from the contact pad (330) to the bond pad (230).


100
110
120
130
140
200
210
211
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220
230
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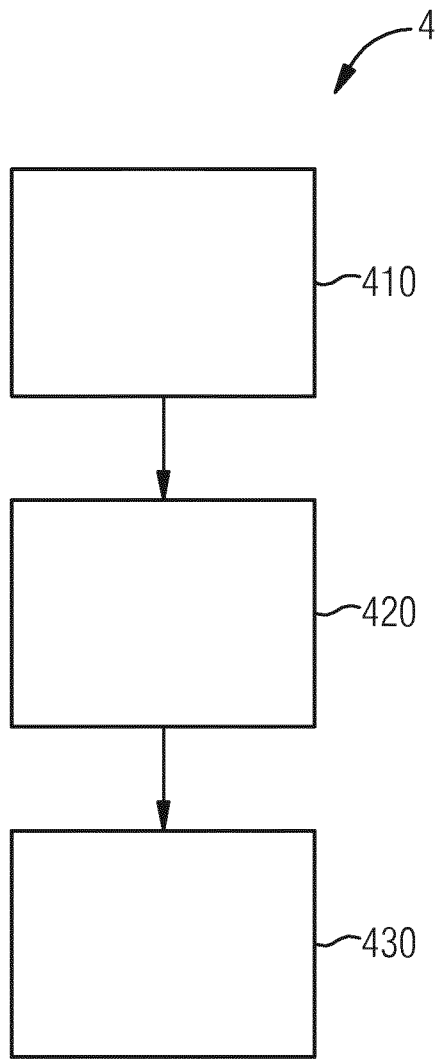
240
245
300
310
330

FIG 1

FIG 2



INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2013/057698

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L23/49 H01L21/60 H01L33/62 H01L31/02 H01S5/042
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2006 165521 A (NIPPON SHEET GLASS CO LTD) 22 June 2006 (2006-06-22) paragraphs [0015], [0018], [0027] - [0029], [0039], [0041]; figures 7b,8,16,17A-17D	1,2,9-13
X	US 2005/161792 A1 (UCHIDA YASUFUMI [JP]) 28 July 2005 (2005-07-28) paragraphs [0007], [0021], [0039] - [0047]; figures 1-5	1,3,11, 13
X	US 2011/006418 A1 (WATANABE MITSUHISA [JP] ET AL) 13 January 2011 (2011-01-13) paragraphs [0007], [0034] - [0038], [0049] - [0073]; figures 2,4A-4C	1,2,9, 11-13

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
7 August 2013	16/08/2013

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Ahlstedt, Mattias

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Form PCT/ISA/210 (second sheet) (April 2005)

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP S58 54646 A (NIPPON ELECTRIC CO) 31 March 1983 (1983-03-31) abstract; figure 3	1,3,11, 13
X	JP H07 335682 A (TOSHIBA ELETRONIC IWATE; TOSHIBA CORP) 22 December 1995 (1995-12-22) paragraphs [0006], [0014], [0017], [0020], [0022], [0027], [0042], [0044], [0046]; claim 3; figures 1,2,3,5,6b	1,8,9, 11-13
X	US 6 864 166 B1 (YIN LENG NAM [SG] ET AL) 8 March 2005 (2005-03-08) column 3, line 48 - column 5, line 32; figure 4 column 6, line 35 - line 55	1,2,8,9, 11,13
X	JP 2011 124487 A (RENESAS ELECTRONICS CORP) 23 June 2011 (2011-06-23)	1,3,9, 11-13
A	paragraphs [0063], [0107], [0108]; figure 25	8
X	EP 1 343 109 A2 (FUJITSU LTD [JP]) 10 September 2003 (2003-09-10) paragraphs [0004], [0018], [0019]; figures 3,4	1,2,8,9
A	EP 0 753 891 A2 (TEXAS INSTRUMENTS INC [US]) 15 January 1997 (1997-01-15) column 2, line 8 - line 13 column 3, line 20 - line 27; figure 3	1,8,9, 11-13

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/EP2013/057698

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☒ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

1-3, 8-13

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☒ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-3, 9-13

   directed to that the contact pad is arranged on a second semiconductor chip

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2. claim: 4

   direct to that said layer of electrically insulating material comprises a resist

   ---

3. claim: 5

   directed to that the layer of insulating material comprises a thickness of less than 1 micron

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4. claim: 6

   directed to that thickness of said layer of insulating material is smaller or equal to a thickness of said bond pad.

   ---

5. claim: 7

   directed to that a thickness of said layer of insulating material differs from a thickness of said bond pad by less than 20 %.

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6. claim: 8

   directed to that the bond wire extends less than 100 microns above said bond pad.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2013/057698

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