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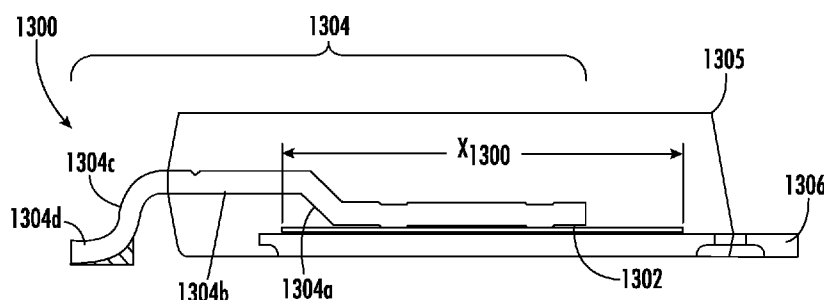


FIG. 13

(57) Abstract: A semiconductor device includes a housing, a die disposed in the housing and having first and second surfaces, a first single-member conductive lead electrically coupled to the first surface and extending through the housing, and a second single-member conductive lead electrically coupled to the second surface and extending through the housing. As compared to prior semiconductor devices, such a semiconductor device can be easier, cheaper, and/or faster to manufacture, and/or, for a given device footprint, can accommodate a larger semiconductor die.



SEMICONDUCTOR DEVICE HAVING SINGLE-MEMBER CONDUCTIVE LEADS COUPLED TO BOTH SIDES OF A DIE, AND METHOD FOR FORMING, AND SYSTEM INCORPORATING, THE SEMICONDUCTOR DEVICE

TECHNICAL FIELD

[0001] The disclosure relates to semiconductor devices, and more specifically to an improved arrangement of a chip having a die with leads attached to both surfaces of the die and extending from the housing that encapsulates the die.

BACKGROUND

[0002] In the manufacture of known transistor chips, leads are attached to both surfaces of a die. The attachment of the leads to the die's conductive pad on the bottom surface can be accomplished by placing a first lead over a conductive pad of the die and forming a conductive connection, for example by soldering. This can be done with multiple leads and per die or dies simultaneously prior to the leads/die(s) being separated from the lead frame. Connection of one or leads to the conductive pad on a second (top) surface of the die is then carried out individually (*i.e.*, typically not at the same time as other second leads are placed and attached) and in a more complex manner as compared to the placing and attaching of the first lead. The second leads may also be multipart.

[0003] An improvement in this type of assembly is needed to improve manufacturability as well as reduce the chance of defects.

SUMMARY

[0004] In an embodiment, a semiconductor device is provided including a housing, a die disposed in the housing and having first and second surfaces, a first single-member conductive lead electrically coupled to the first surface and extending through the housing, and a second single-member conductive lead electrically coupled to the second surface and extending through the housing. As compared to prior semiconductor devices, such as semiconductor device can be less expensive to manufacture and/or, for a given device footprint, can accommodate a larger die.

[0005] In another embodiment, a system is provided that incorporates a controller and one or more such semiconductor devices.

[0006] In yet another embodiment, a method for manufacturing one or more semiconductor devices is provided that includes attaching a first side of each of at least one die to a respective paddle of a lead-frame strip, and attaching a second side of each of the at least one die to a respective paddle of a clip-

frame strip. As compared to prior methods for manufacturing a given number of semiconductor devices, such a method can be less expensive, less complex, and/or faster, and/or can yield a higher percentage of useable semiconductor devices.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] A more detailed understanding may be had from the following description, given by way of example in conjunction with the accompanying drawings, wherein like reference numerals in the figures indicate like elements, and wherein:

[0008] FIG. 1A is a view of an NMOS power transistor, according to an embodiment;

[0009] FIG. 1B is a schematic symbol of the NMOS power transistor of FIG. 1A;

[0010] FIG. 2 is a cross-sectional transparent side view of a conventional NMOS power transistor;

[0011] FIG. 3 is a cross-sectional transparent side view of an NMOS power transistor, according to an embodiment;

[0012] FIGS. 4A-4C are respective plan views of a lead-frame (LF) strip, a clip-frame (CF) strip, and the CF strip disposed over, and in alignment with, the LF strip, according to an embodiment;

[0013] FIG. 5 is a plan view of an LF strip, according to an embodiment;

[0014] FIG. 6 is a plan view of the LF strip of FIG. 5 with solder formed over the surfaces of the die paddles, according to an embodiment;

[0015] FIG. 7 is a plan view of the LF strip of FIG. 6 with dies disposed over the pre-soldered die paddles, according to an embodiment;

[0016] FIG. 8 is a plan view of the LF strip of FIG. 7 with solder formed over the exposed surfaces of the dies, according to an embodiment;

[0017] FIG. 9 is a plan view of a CF strip aligned with, and disposed over, the LF strip of FIG. 8, and paddles of the CF strip each disposed over an exposed surface of a respective die, according to an embodiment;

[0018] FIG. 10 is the CF strip and LF strip of FIG. 9 with the dies and portions of the leads encapsulated (housings formed), according to an embodiment;

[0019] FIG. 11 is a flow diagram of a method for forming a semiconductor device such as the transistor of FIGS. 1A, 3, and 12, according to an embodiment;

[0020] FIG. 12 is a cross-sectional transparent side view of a conventional NMOS power transistor having a given footprint with an indication of a maximum allowable die size;

[0021] FIG. 13 is a cross-sectional transparent side view of a packaged NMOS power transistor having the same given footprint as the transistor of FIG. 12 and with an indication of a maximum allowable die size, according to an embodiment; and

[0022] FIG. 14 is a schematic diagram of a system that includes one or more of the semiconductor devices of FIGS 1A, 3, and 12, according to an embodiment.

DETAILED DESCRIPTION

[0023] Certain terminology is used in the following description for convenience only and is not limiting. The words "inwardly" and "outwardly" refer to directions toward and away from the parts referenced in the drawings. The terms "top" and "bottom" refer to directions on the articles as shown in the drawings. A reference to a list of items that are cited as, for example, "at least one of a or b" (where a and b represent the items being listed) means any single one of the items a or b, or a combination of a and b thereof. This would also apply to lists of three or more items in like manner so that individual ones of the items or combinations thereof are included. The terms "about" and "approximately" encompass + or – 10% of an indicated value unless otherwise noted. The terminology includes the words specifically noted above, derivatives thereof and words of similar import.

[0024] FIG. 1A is an isometric view of packaged semiconductor device, here an NMOS power transistor 100 having a package 102, according to an embodiment. The power transistor 100 is suitable for many applications such as being one of the output transistors of a switching power supply (not shown in FIG. 1A). The package 102 includes an optional drain pad 104, which also can be configured as a heat sink, drain leads 106 coupled to the drain pad 104, source leads 108, a gate lead 110, and a housing 112. At their ends opposite to the optional drain pad 104, the drain leads 106 may be electrically tied together. Alternately, in an embodiment where the drain pad 104 is omitted, each drain lead 106 can extend into the housing and be electrically coupled to a pad on a surface of a die (not shown in FIG. 1A) within the housing 112. As described below in conjunction with FIG. 1B, the transistor 100 can be configured to have an inherent body diode (not shown in FIG. 1A) by virtue of the transistor's source (not shown in FIG. 1A) being coupled to the transistor's body region (not shown in FIG. 1A) inside of the housing 112. In an embodiment, the transistor 100 is a vertical enhancement-mode NMOS power transistor.

[0025] FIG. 1B shows a schematic symbol 120 of the NMOS power transistor 100 of FIG. 1A in an embodiment where the transistor is an enhancement-mode transistor. Per the schematic symbol 120, the transistor 100 includes a gate (G) 122, an N-type drain (D) 124, an N-type source (S) 126, a P-type body 128, and an inherent PN-junction diode (typically called an "inherent body diode" or a "body diode") 130.

[0026] While the gate-to-source voltage V_{GS} is less than a threshold voltage $V_{GS(th)}$, the NMOS transistor 100 operates in its cut-off region during which the drain-to-source current I_{DS} is relatively small (e.g., a few to tens of microamperes (μA), and is often approximated as = 0 Amperes (A)).

[0027] While V_{GS} is greater than $V_{GS(th)}$ and the drain-to-source voltage V_{DS} is less than $V_{GS} - V_{GS(th)}$, the NMOS transistor 100 operates in its linear or “triode” region, during which the value of I_{DS} is proportional to $V_{GS} - V_{GS(th)}$ for a given value of V_{DS} .

[0028] And while V_{GS} is greater than $V_{GS(th)}$ and V_{DS} is greater than $V_{GS} - V_{GS(th)}$, the NMOS transistor 100 operates in its saturation region, during which the value of I_{DS} is proportional to $(V_{GS} - V_{GS(th)})^2$ (many applications of the NMOS transistor call for configuring circuitry that includes the NMOS transistor such that the NMOS transistor operates in its saturation region).

[0029] If the drain voltage V_D goes below the source voltage V_S while the NMOS transistor 100 is operating in, or near, its cut-off mode, then the inherent body diode 130 may conduct a source-to-drain current if the source-to-drain voltage V_{SD} is greater than the body diode's threshold, or “turn-on,” voltage V_{th} . For example, the body diode 130 may conduct a source-to-drain current I_{SD} for a relatively brief period during a discharge of a phase inductor of a switching power supply such as a buck converter.

[0030] FIG. 2 is a cross-sectional transparent side view of a conventional NMOS power transistor 200, which includes a die 202, a lead-frame paddle 204, a first lead 206, a second lead 208 having an internal portion 210 and an external portion 212, and a housing 214.

[0031] During manufacture of the transistor 200, the first lead 206 is attached to (e.g., integral with) a lead frame that includes the paddle 204 and that facilitates placement of the first lead over a conductive pad (not shown in FIG. 2) on a first side (here a bottom) of the die 202 and attachment (typically by soldering) of the first lead to the conductive pad. It is only after attachment of the first lead 206 to the die's conductive pad that the first lead is separated from the lead frame. Furthermore, because other first leads also are attached to the lead frame, multiple first leads can be placed over, and attached to, respective conductive pads on the first side of the die at the same time.

[0032] In contrast, the second lead 208 is placed over, and attached to, a conductive pad (not shown in FIG. 2) on a second side (here a top) of the die 202 individually (*i.e.*, typically not at the same time as other second leads are placed and attached) and in a more complex manner as compared to the placing and attaching of the first lead 206.

[0033] First, the internal portion 210 of the second lead 208 is attached (typically soldered) to a conductive pad on the upper side of the die 202. But if the die 202 and internal portion 210 are rotated relative to one another in a plane parallel to the die 202, or are otherwise misaligned, even by a relatively small amount, during the placing and attaching process, the resulting transistor 200 can be rendered unsuitable for use, and, therefore, can be discarded or “failed.” After the internal portion 210 is attached to the conductive pad on the upper surface of the die 202, the external portion 212 of the second lead 208 is placed and attached, by soldering or welding, to the internal portion, thus forming an attachment joint 216. But if the internal portion 210 and the external portion 212 are rotated relative to one another

in a plane parallel to the die 202, or are otherwise misaligned, even by a relatively small amount, during the placing and attaching process, the resulting transistor 200 can be rendered unsuitable for use, and, therefore, can be discarded or “failed.” Furthermore, the attachment joint 216 is an additional point of potential failure. In addition, placing and attaching second leads 208 individually is time consuming and, therefore, reduces the throughput (*i.e.*, the number of semiconductor devices per unit time) of a process for manufacturing the transistor 200. Moreover, the volume occupied by the attachment joint 216 reduces, within the housing 214, the area available for the die 202 and, therefore, limits the maximum size of a die that the housing can accommodate for a given footprint of the transistor 200.

[0034] Consequently, there is a need for a semiconductor device with more reliably placeable leads and that can accommodate a larger die for a given device footprint, and/or for a semiconductor manufacturing process that is more reliable, less expensive, and/or higher throughput than existing processes.

[0035] FIG. 3 is a cross-sectional transparent side view of an NMOS power transistor 300, which includes a die 302, a lead-frame paddle 304, a first lead 306, a second lead 308, and a housing 314, according to an embodiment.

[0036] During manufacture of the transistor 300, the first lead 306 is attached to (*e.g.*, integral with) a lead frame (not shown in FIG. 3), which facilitates placement of the first lead over a conductive pad (not shown in FIG. 3) on a first side (here a bottom) of the die 302 and attachment (typically by soldering) of the first lead to the conductive pad. It is only after placing and attaching the first lead 306 to the conductive pad on the first side of the die that the first lead is separated from the lead frame. Furthermore, because other first leads also are attached to the lead frame, multiple first leads can be attached to respective conductive pads on the first side of the die at the same time.

[0037] Similarly, during manufacture of the transistor 300, the second lead 308, which, unlike the second lead 208 of FIG. 2, is a single piece (a single member) attached to a clip frame (not shown in FIG. 3), which facilitates placement of the second lead over a conductive pad (not shown in FIG. 3) on a second side (here a top) of the die 302 and attachment (typically by soldering) of the second lead to a conductive pad (not shown in FIG. 3) on the second side of the die. It is only after placing and attaching of the second lead 308 to the conductive pad on the second side of the die that the second lead is separated from the clip frame. Furthermore, because other second leads also are attached to the clip frame, multiple second leads can be attached to respective conductive pads on the second side of the die at the same time.

[0038] As discussed in the following, because the second lead 308 is a single member, it can be less prone to causing errors than the multi-member lead 208 of FIG. 2. Furthermore, because the second lead 308 is attached to a clip frame during placing and attaching the second lead to the top side of the die, there can be fewer rotational and other misalignment errors, at least one fewer potential failure point

(e.g., because there is no attachment joint such as the joint 216 of FIG. 2), the housing 314 can accommodate a larger die 302 than the housing 214 (FIG. 2), and the process for manufacturing the transistor 300 can be more reliable than the process for manufacturing the transistor 200 of FIG. 2. In addition, because multiple second leads 308 can be attached to the die 302 at the same time, the process for manufacturing the transistor 300 can be faster (*i.e.*, higher throughput), less expensive, and/or less complex than a process for manufacturing the transistor 200 of FIG. 2.

[0039] In FIG. 3, the first lead 306 extends from a plane at or near a top (non-mounting) side 307 of the housing 314, bends (upwardly in FIG. 3) at a first bend 306a, has a directed (upwardly in FIG. 3) extension portion 306b, prior to bending outwardly to form a contact area 306c, which is generally aligned with a bottom (mounting) side 309 of the housing 314. The second lead 308a, which extends out of an opposite side of the housing 314 from the first lead 306, also includes a first bend 308a (an upward bend in FIG. 3) to extend (upwardly in FIG. 3) from a surface of the die 302 opposite to the lead-frame paddle 304, which first bend transitions into an outwardly directed extension portion 308b, which extends through the side of the housing, prior to a second bend 308c (an upward bend in FIG. 3), which transitions to an extension portion 308d (an upward extension in FIG. 3), which, via a third bend 308e, transitions to a contact area 308f, which is generally aligned with the bottom (mounting) side 309 of the housing.

[0040] FIG. 4A is a plan view of a lead-frame strip 400, according to an embodiment.

[0041] FIG. 4B is a plan view of a clip-frame strip 402, according to an embodiment.

[0042] FIG. 4C is a plan view of the clip-frame strip 402 disposed over, and aligned with, the lead-frame strip 400, according to an embodiment.

[0043] Referring to FIGS. 4A – 4C, dies (not shown in FIGS. 4A – 4C) are placed on paddles 406 of the lead frame 400, and conductive pads on the bottoms of the dies are conductively coupled (*e.g.*, by soldering) to leads 408 of the lead-frame strip. The coupling agent (*e.g.*, adhesive solder) may secure each die to a corresponding pad, or a separate adhesive or other attaching agent may be used instead of, or in addition to, the coupling agent.

[0044] Then, the clip-frame strip 402 is placed over the die-populated lead-frame strip 400 and is aligned with the lead-frame strip using alignment holes or other alignment markings 410. The lead-frame strip 400 and the clip-frame strip 402 are moved toward one another such that the lead-frame strip and the clip-frame strip “sandwich” the dies.

[0045] Next, paddles 412 of the clip-frame strip 402 contact the tops of the dies (not shown in FIGS. 4A-4C) such that conductive pads on the tops of the dies are conductively coupled (*e.g.*, by soldering) to leads 414 of the clip-frame strip.

[0046] Then, the dies and portions of the leads 408 and 414 are encapsulated in a housing (not shown in FIGS. 4A-4C, but similar to the housings 1000 of FIG. 10) made from a suitable material, such as epoxy or ceramic, to form semiconductor chips.

[0047] Next, the semiconductor chips are separated from the lead- and clip-frame strips 400 and 402.

[0048] Still referring to FIGS. 4A-4C, because the lead-frame and clip-frame strips permit multiple semiconductor chips to be formed simultaneously, the cost, complexity, and/or manufacturing time per chip can be reduced relative to a process in which the leads 208 (FIG. 2) are individually placed and coupled to pads on a semiconductor die. For example, although the lead-frame and clip-frame strips 400 and 402 are shown as accommodating twenty-four dies, the lead-frame and clip-frame strips can be configured to accommodate any suitable number of dies, such as thirty two, sixty four, two hundred fifty six, or five hundred twelve. In addition, the alignment holes and alignment markings 410 can reduce the severity and occurrence of alignment errors, and thus increase the process yield, relative to a process in which the leads 414 are individually placed and coupled to pads on the die like the leads 208 of FIG. 2.

[0049] FIG. 5 is a plan view of a lead-frame strip 500 having paddles 502, leads 504, and alignment holes and markings 506, according to an embodiment. Although the lead-frame strip 500 is shown as including twenty four paddles 502 configured to accommodate, respectively, twenty four dies (not shown in FIG. 5), the lead-frame strip can include any suitable number (e.g., twelve, sixteen, thirty two, forty eight, sixty four, seventy two, ninety six, one hundred twenty, one hundred twenty eight, one hundred forty four, one hundred sixty eight, one hundred ninety two, two hundred sixteen, two hundred forty, and two hundred fifty six) of paddles configured to accommodate any suitable number (e.g., twelve, sixteen, thirty two, forty eight, sixty four, seventy two, ninety six, one hundred twenty, one hundred twenty eight, one hundred forty four, one hundred sixty eight, one hundred ninety two, two hundred sixteen, two hundred forty, and two hundred fifty six) of dies.

[0050] FIG. 6 is a plan view of the lead-frame strip 500 of FIG. 5 with solder 600 formed over the surfaces of the die paddles 502, according to an embodiment.

[0051] FIG. 7 is a plan view of the lead-frame strip 500 of FIG. 6 with dies 700 disposed over the pre-soldered die paddles 502, according to an embodiment.

[0052] FIG. 8 is a plan view of the lead-frame strip 500 of FIG. 7 with solder 800 formed over the exposed surfaces of the dies 700, according to an embodiment.

[0053] FIG. 9 is a plan view of a clip-frame strip 900 having die paddles 902, leads 904, and alignment holes and markings 906, disposed over the lead-frame strip 500 of FIG. 8 such that the alignment holes and markings are aligned with the corresponding alignment holes and markings 506 (see FIG. 5) of the lead-frame strip 500 and such that the clip-frame-strip paddles 902 each are disposed over an exposed surface of a respective die 700 and each include conductive pads (not shown in FIG. 9) conductively

coupled (such as by solder) to corresponding conductive pads on the die surface, according to an embodiment. And the conductive pads of the clip-frame-strip paddles 902 are conductively coupled (such as by solder) to the leads 904.

[0054] FIG. 10 is a plan view of the resulting structure 1002 from the clip-frame strip 900 and the lead-frame strip 500 (not visible in FIG. 10) of FIG. 9 with the dies 700 (not visible in FIG. 10) of FIG. 9 and portions of the leads 504 and 904 being encapsulated in corresponding housings 1000, according to an embodiment.

[0055] FIG. 11 is a flow diagram 1100 of a method (sometimes called a “semiconductor process” or a “semiconductor manufacturing process”) for forming a semiconductor device such as the transistor 100 of FIG. 1A, the transistor 300 of FIG. 3, or the transistor 1300 of FIG. 13, according to an embodiment.

[0056] Referring to FIGS. 5 – 11, a semiconductor process for manufacturing a semiconductor device or chip, such as the transistor 100 of FIG. 1A, the transistor 300 of FIG. 3, or the transistor 1300 of FIG. 13, is described according to an embodiment.

[0057] Referring to FIGS. 5 and 11, the unpopulated lead-frame strip 500 is introduced to the processing line.

[0058] Referring to FIGS. 6 and 11, at 1102, solder 600 is formed on the die paddles 502 of the lead-frame strip 500. For example, the solder may be printed on conductive pads (not shown in FIG. 6) that are disposed on the paddles 502 and that are respectively coupled to the leads 504. And the solder 600 also can act as an adhesive to secure dies (see FIG. 7) to the paddles 502; alternatively, an adhesive separate from the solder can be formed, for example by printing, on portions of the paddles other than the conductive pads. In an embodiment, solder printing is a suitable solder-forming technique because it can offer precise control of the volume of solder being deposited onto the paddles 502.

[0059] Referring to FIGS. 7 and 11, at 1104 the dies 700 are attached to the die paddles 502 of the lead-frame strip 500. The dies 700 are attached to the paddles 502 such that solder 600 (FIG. 6) electrically couples conductive pads (not shown in FIG. 7) on the bottom surfaces of the dies to corresponding conductive pads (not shown in FIG. 7) on the die-facing surfaces of the paddles 502, where these paddle conductive pads are electrically coupled to respective sets of the leads 504. For example, the item 1104 can include a solder reflow. Consequently, after completion of the item 1104, circuitry on each of the dies 700 is coupled to a respective set of the leads 504 via the conductive pads of the paddles 502, solder, and the conductive pads of the dies 700. And, as stated above in conjunction with FIGS. 6 and 11, the dies 700 can be secured to the paddles 502 by the solder 600 (e.g., adhesive solder) or by a separate adhesive.

[0060] Referring to FIGS. 8 and 11, at 1106, solder 800 is formed on the exposed surfaces (upper surfaces in FIG. 8) of the dies 700. For example, the solder 800 may be printed on conductive pads (not

shown in FIG. 8) that are disposed on the exposed surfaces of the dies 700 and that are respectively coupled to respective circuitry on the dies. And the solder 800 also can act as an adhesive to secure the dies 700 to paddles 902 of the clip-frame strip 900 as described below in conjunction with FIG. 9; alternatively, an adhesive separate from the solder can be formed, for example by printing, on portions of the dies' upper surfaces other than the conductive pads. In an embodiment, solder printing is a suitable solder-forming technique because it can offer precise control of the volume of solder being deposited onto the dies 700.

[0061] Referring to FIGS. 9 and 11, at 1108, the clip-frame strip 900 is aligned with the lead-frame strip 500. For example, the strips 500 and 900 are aligned by using one or more alignment tools (not shown in FIG. 9) to align the alignment holes or marks 506 with the corresponding alignment holes or marks 906. As a result of such an alignment of the clip-frame strip 900 with the lead-frame strip 500, each of the paddles 902 of the clip-frame strip is aligned with a corresponding one of the paddles 502 (see FIG. 5) of the lead-frame strip 500 and, therefore, is aligned with a corresponding one of the dies 700. Said another way, as a result of the alignment of the lead-frame strip 500 with the clip-frame strip 900, each of the dies 700 is effectively "sandwiched" between a corresponding pair of the paddles 502 and 902.

[0062] Still referring to FIGS. 9 and 11, at 1110 the clip-frame strip 900 is moved toward the lead-frame strip 500 while alignment is obtained to attach the paddles 902 of the clip-frame strip to the dies 700. The paddles 902 are attached to the dies 700 such that the solder 800 (FIG. 8) electrically couples conductive pads (not shown in FIG. 9) on the exposed surfaces (the top surfaces in FIG. 9) of the dies to corresponding conductive pads (not shown in FIG. 9) on the die-facing surfaces of the paddles 902, where these paddle conductive pads are electrically coupled to respective sets of the leads 904. For example, the item 1110 can include a solder reflow. Consequently, after completion of the item 1110, circuitry on each of the dies 700 is coupled to a respective set of the leads 904 via the conductive pads of the paddles 902, solder, and the conductive pads on the top surfaces (the surfaces facing the paddles 902) of the dies 700. And, as stated above in conjunction with FIGS. 8 and 11, the paddles 902 can be secured to the dies 700 by the solder 800 (e.g., adhesive solder) or by a separate adhesive.

[0063] Referring to FIGS. 10 and 11, at 1112 the dies 700 of FIG. 9 (dies not visible in FIG. 10) and portions of the leads 504 and 904 extending from the dies (see e.g., FIGS. 7 and 9) are encapsulated with a suitable material to form housings 1000. For example, an epoxy or other plastic may be molded (e.g., injection or another type of molding) around the dies 700 to form the housings 1000. Or the housings may be formed by a ceramic or may be hermetically sealed. And, in another example, the encapsulated dies 700 may each be formed to include a respective conductive plate such as a ground plate or the drain plate 104 of FIG. 1A.

[0064] Referring to FIG. 11, at 1114, the resulting structure 1002 of FIG. 10 is processed post-encapsulating. For example, the structure 1002 is de-junked or otherwise cleaned, the exposed portions of the leads 504 and 904 are plated (for example, with tin (Sn)), and the housings 1000 are laser marked (for example with the part number and provider).

[0065] Next, at 1116, the housed semiconductor components, devices, or chips are separated from the lead-frame and clip-frame strips 500 and 900, and, referring to FIG. 3, the exposed portions of the leads 504 and 904 remaining after component separation are shaped to form external leads such as the leads 306 and 308. Alternatively, each set of leads 504 or 904 may be coupled together or may be one solid piece, and may be shaped in a same manner as if the leads are separated from one another.

[0066] Then, at 1118, the separated semiconductor components, devices, or chips, are tested. For example, the components may be subject to electrical-signal tests such as a JTAG boundary scan or electrical- and heat-stressing tests.

[0067] Next, at 1120, the semiconductor components, devices, or chips are sorted based on the results of the tests at item 1118.

[0068] Referring again to FIGS. 5-11, the semiconductor process described in conjunction with the flow diagram 1100 can yield semiconductor components, devices, or chips (sometimes called "ICs" or "Integrated Circuits") that are, on a per-chip basis, up to about 40% less expensive to manufacture than counterpart chips manufactured by other processes, and can increase the yield of acceptable ICs by up to about 1.5%.

[0069] FIG. 12 is a cross-sectional transparent side view of a conventional NMOS power transistor 1200 having a die 1202 and manufactured according to an individual-lead-placement process that is similar to the process described above in conjunction with FIG. 2 and that utilizes two-member leads 1204 (indicated along with the overall length), which are similar to the two-member leads 208 of FIG. 2.

[0070] FIG. 13 is a cross-sectional transparent side view of an NMOS power transistor 1300 having a die 1302 and manufactured according to the process that is described above in conjunction with FIGS. 5-11 and that utilizes single-member leads 1304 (one such lead shown in FIG. 13 and indicated along with the overall length), which are similar to the single-member leads 306 and 308 of FIG. 3. In FIG. 13, the single member lead 1304 rises upwardly at a first bend 1304a from the top surface of the die 1302, then transitions to an extension portion 1304b, which extends outwardly beyond a housing 1305, and then bends downwardly at a second bend 1304c prior to extending further outwardly at a connection area 1304d, which is generally at about a same level as the lead 1306, which is connected to the bottom surface of the die 1302. Thus, the leads 1304 and 1306 provide the same functionality as the lead 1204 and a lead 1206 of the conventional transistor 1200 of FIG. 12.

[0071] Referring to FIGS. 12 and 13, the power transistor 1300 can have a maximum die dimension X_{1300} , which is up to about 30% wider than a maximum die dimension X_{1200} , which the power transistor 1200 can have. That is, the manufacturing process described above in conjunction with FIGS. 5-11 can yield a semiconductor-chip package that allows a maximum die dimension of up to about 30% larger than a maximum die dimension allowed by a package manufactured by process that employs the individual-lead-placement process using two-member leads 1204 as described above in conjunction with FIGS. 2 and 12. For example, $X_{1200} = 3.7$ millimeters (mm) as compared to $X_{1300} = 4.41$ mm.

[0072] FIG. 14 is a schematic diagram of a system 1400, which incorporates one or more of the NMOS transistors 100, 300, or 1300 of FIGS. 1, 3, and 13, according to an embodiment. For purposes of explanation, the system 1400 is described as including two NMOS transistors 1300, although it is understood that the system 1400 would be configured and would function similarly if one or both of the transistors were replaced with an NMOS transistor 100 or 300.

[0073] In an embodiment, the system 1400 is a single-phase buck-converter power supply, which includes a power-supply controller 1402, a switching circuit 1404, and a filter circuit 1406, and which is configured to provide a regulated output voltage V_{out} to a load 1408.

[0074] The controller 1402 can be a conventional power-supply controller, and is configured to receive, as a feedback signal, V_{out} (or a derivative thereof), and also may be configured to receive, as another feedback signal, V_{drive} (or a derivative thereof), depending on the control mode in which the power supply system 1400 is configured to operate. For example, if the controller 1402 employs current-mode control, then the controller may form a current-control loop that receives, as an input, the voltage V_{drive} . The controller 1402 is also coupled between V_{in} , which powers the controller, and circuit ground.

[0075] The switching circuit 1404 includes a high-side NMOS transistor 1410 and a low-side NMOS transistor 1412, which are both the same as, or similar to, the NMOS transistor 1300 of FIG. 13. The high-side transistor 1410 has its drain coupled to an input voltage V_{in} , its gate coupled to receive a control signal Control_Highside from the controller 1402, and its source coupled to an input node 1414 of the filter circuit 1406. The low-side transistor 1412 has its drain coupled to the input node 1414 of the filter circuit 1406, its gate coupled to receive a control signal Control_Lowside from the controller 1402, and its source coupled to circuit ground.

[0076] The filter circuit 1406 includes an inductor 1416 coupled between the input and output nodes 1414 and 1418 of the filter circuit 1406, and includes a capacitor 1420 coupled between the output node 1418 of the filter circuit and circuit ground.

[0077] The load 1408 can be any suitable load, such as a microprocessor, microcontroller, or other integrated circuit.

[0078] In operation, the power-supply controller 1402 generates Control_Highside having a level that turns the transistor 1410 “on” and generates Control_Lowside having a level that turns the transistor 1412 “off.”

[0079] A linearly increasing current I_{inductor} flows from V_{in} , through the drain-source junction of the “on” transistor 1410, and through the inductor 1416, to the capacitor 1420 and load 1408. Respective components of this linearly increasing current I_{inductor} power the load 1408 and charge the capacitor 1420.

[0080] After a period of time, the power-supply controller 1402 generates Control_Highside having a level that turns the transistor 1410 “off” and generates Control_Lowside having a level that turns the transistor 1412 “on.”

[0081] After this switching transition, a linearly decreasing current I_{inductor} flows from circuit ground, through the source-drain junction of the “on” transistor 1412, and through the inductor 1416, to the capacitor 1420 and load 1408. Respective components of this linearly decreasing current I_{inductor} power the load 1408 and charge the capacitor 1420. Depending on the timing of the turning “off” of the transistor 1410 relative to the turning “on” of the transistor 1412, the inherent body diode (see FIG. 1B) of the transistor 1412 may be forward biased and conduct I_{inductor} for a period of time before the transistor 1412 is fully “on.”

[0082] The power-supply controller 1402 thereafter repeats this switching cycle, adjusting the duty cycle of the transistor 1410 in a manner that regulates V_{out} to a value, such as 1.1 Volts (V), for which the controller 1402 and power supply system 1400 are configured.

[0083] Further details regarding the structure and operation of the power supply system 1400 and similar power supplies are known.

[0084] Referring to FIGS. 1A-1B, 3-11, and 13-14, alternate embodiments are contemplated. For example, although the process for packaging an NMOS transistor is described, other semiconductor components, devices, chips, and/or ICs, such as a PMOS transistor, a bipolar transistor, a BiCMOS transistor, a microcontroller, and/or a microprocessor, can be packaged according to the above-described semiconductor-packaging process. Furthermore, the system 1400 can be a power supply other than a single-phase buck converter, for example, a multi-phase buck converter with or without coupled inductors, a boost converter, a buck-boost converter, and/or a flyback converter, can be a current regulator instead of, and/or in addition to, a voltage regulator, and/or can be a system other than a power supply.

[0085] Although the features and elements of the disclosed subject matter are described in embodiments in particular combinations, each feature or element may be used alone without the other features and elements of the embodiments or in various combinations with or without other features and elements of the disclosed subject matter.

[0086] While features and elements are described above in particular combinations, one of ordinary skill in the art will appreciate that each feature or element can be used alone or in any combination with the other features and elements.

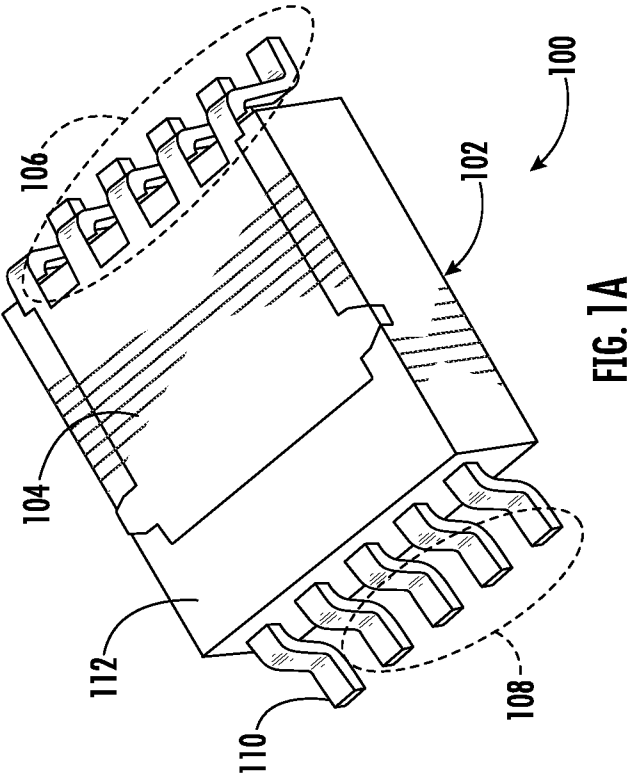
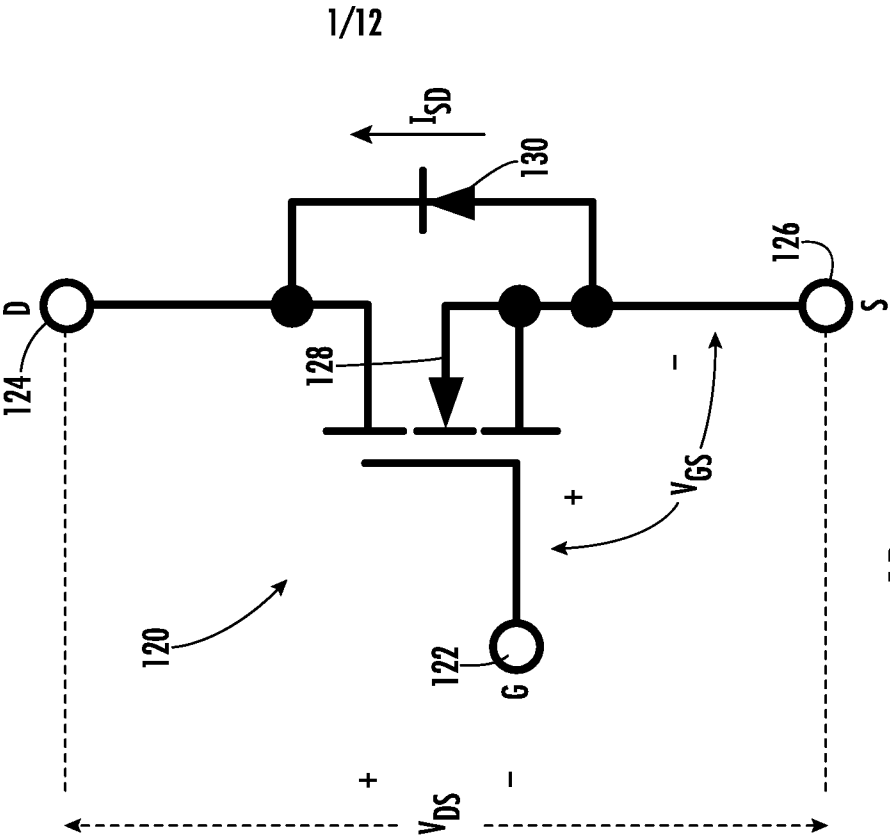
CLAIMS

What is Claimed:

1. A semiconductor device, comprising:
a housing;
a die disposed in the housing and having first and second surfaces;
a first single-member conductive lead electrically coupled to the first surface and extending through the housing; and
a second single-member conductive lead electrically coupled to the second surface and extending through the housing.
2. The semiconductor device of claim 1, further comprising:
multiple single-member conductive leads, including the first single-member conductive lead, electrically coupled to the first surface and extending through the housing; and
multiple other single-member conductive leads, including the second single-member conductive lead, electrically coupled to the second surface and extending through the housing.
3. The semiconductor device of claim 1, further comprising:
multiple single-member conductive leads, including the first single-member conductive lead, electrically coupled to the first surface and to one another and extending through the housing; and
multiple other single-member conductive leads, including the second single-member conductive lead, electrically coupled to the second surface and to one another and extending through the housing.
4. The semiconductor device of claim 1, further comprising one or more transistors disposed on the die.
5. The semiconductor device of claim 1, further comprising:
a transistor disposed on the die and having a drain and a source;
multiple single-member conductive leads, including the first single-member conductive lead, electrically coupled to one of the drain and source; and
multiple other single-member conductive leads, including the second single-member conductive lead, electrically coupled to the other of the drain and source.
6. The semiconductor device of claim 1, further comprising:
a conductive plate disposed over an outside of the housing;
multiple single-member conductive leads, including the first single-member conductive lead, electrically coupled to the first surface and to the conductive plate; and
multiple other single-member conductive leads, including the second single-member conductive lead, electrically coupled to the second surface.

7. The semiconductor device of claim 1, further comprising:
 - a conductive plate disposed over an outside of the housing;
 - a transistor disposed on the die and having a drain and a source;
 - multiple single-member conductive leads, including the first single-member conductive lead, electrically coupled to the conductive plate and to one of the drain and source; and
 - multiple other single-member conductive leads, including the second single-member conductive lead, electrically coupled to the other of the drain and source.
8. A method, comprising:
 - attaching a first side of each of at least one die to a respective paddle of a lead-frame strip; and
 - attaching a second side of each of the at least one die to a respective paddle of a clip-frame strip.
9. The method of claim 8 wherein:
 - the attaching of the first side includes soldering the first side of each of the at least one die to a respective paddle of the lead-frame strip; and
 - the attaching of the second side includes soldering the second side of each of the at least one die to a respective paddle of the clip-frame strip.
10. The method of claim 8, further comprising:
 - forming solder on each paddle of the lead-frame strip before attaching the first side of each of the at least one die to the respective paddle of the lead-frame strip; and
 - forming solder on each paddle of the clip-frame strip before attaching the second side of each of the at least one die to the respective paddle of the clip-frame strip.
11. The method of claim 8, further comprising aligning the clip-frame strip with the lead-frame strip before attaching the respective paddle of the clip-frame strip to the second side of each of the at least one die.
12. The method of claim 8, further comprising aligning alignment marks of the clip-frame strip with corresponding alignment marks of the lead-frame strip before attaching the respective paddle of the clip-frame strip to the second side of each of the at least one die.
13. The method of claim 8, further comprising encapsulating each of the dies to form chips.
14. The method of claim 13, further comprising testing the chips before separating the chips from the lead-frame and the clip-frame strips.
15. The method of claim 13, further comprising de-junking the chips, the lead-frame strip, and the clip-frame strip before separating the chips from the lead-frame and the clip-frame strips.
16. The method of claim 13, further comprising plating exposed leads of the chips before separating the chips from the lead-frame and the clip-frame strips.

17. The method of claim 13, further comprising marking housings formed by the encapsulating of the chips before separating the chips from the lead-frame and clip-frame strips.
18. The method of claim 13, further comprising separating the chips from the lead-frame and the clip-frame strips.
19. The method of claim 18, further comprising shaping exposed leads of the chips after separating the chips from the lead-frame and the clip-frame strips.
20. A system, comprising:
a controller;
a filter network; and
a switching circuit configured to drive the filter network to generate a regulated output signal in response to the controller, the switching circuit having one or more semiconductor devices each including:
a housing;
a die disposed in the housing and having first and second surfaces;
a first single-member conductive lead electrically coupled to the first surface and extending through the housing; and
a second single-member conductive lead electrically coupled to the second surface and extending through the housing.
21. The system of claim 20 wherein at least one of the one or more semiconductor devices includes a MOS transistor.



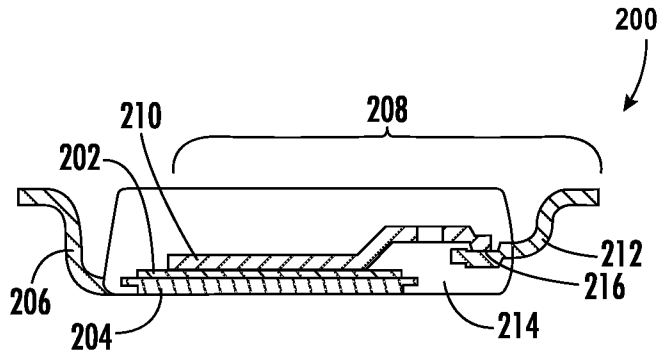


FIG. 2
(PRIOR ART)

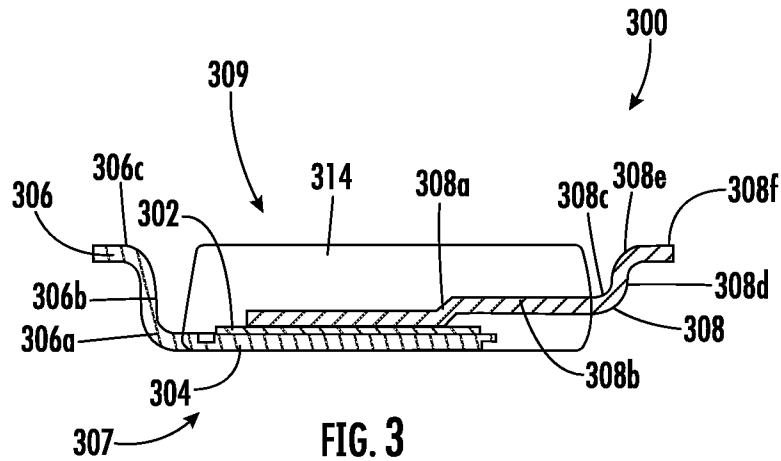
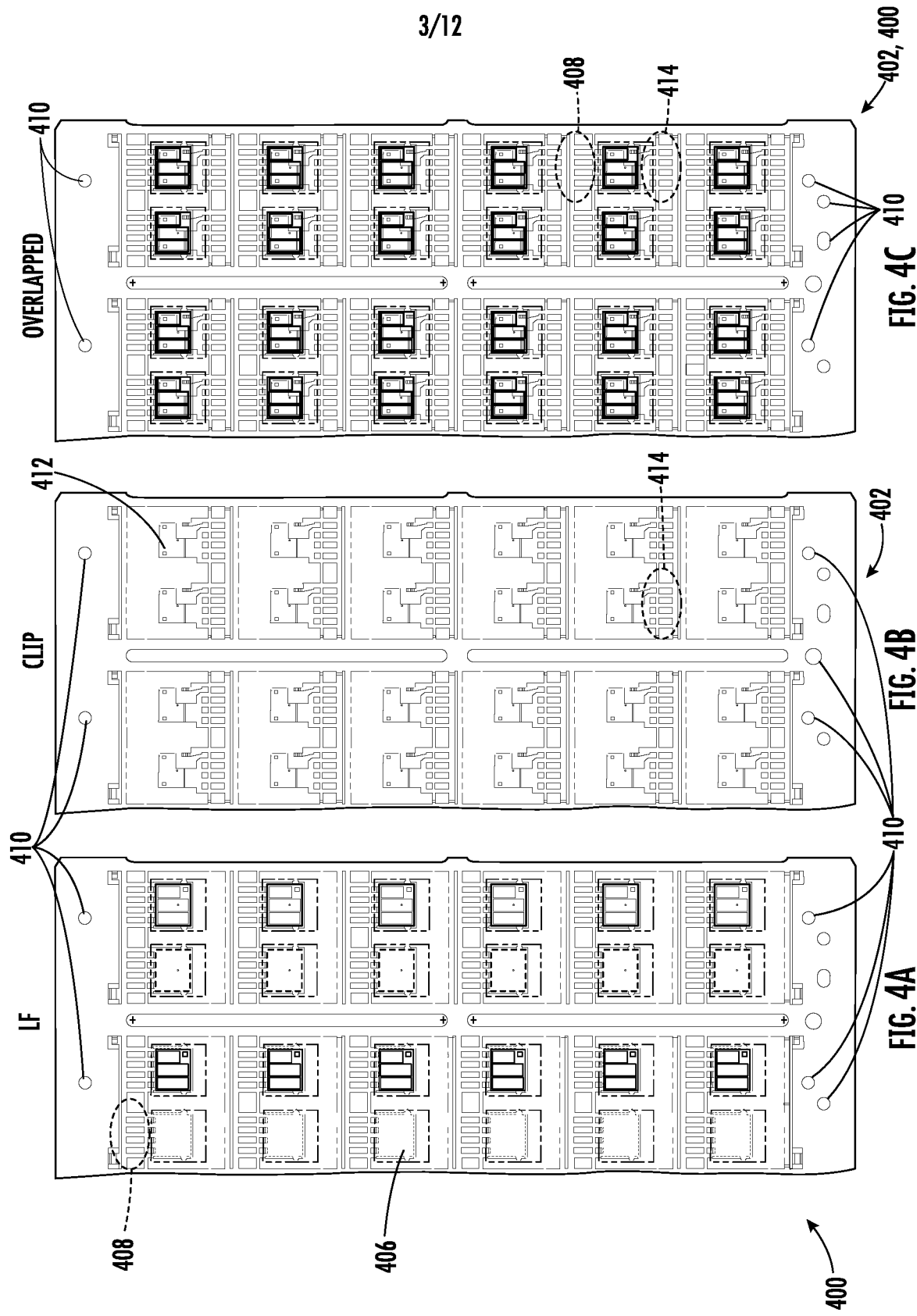


FIG. 3



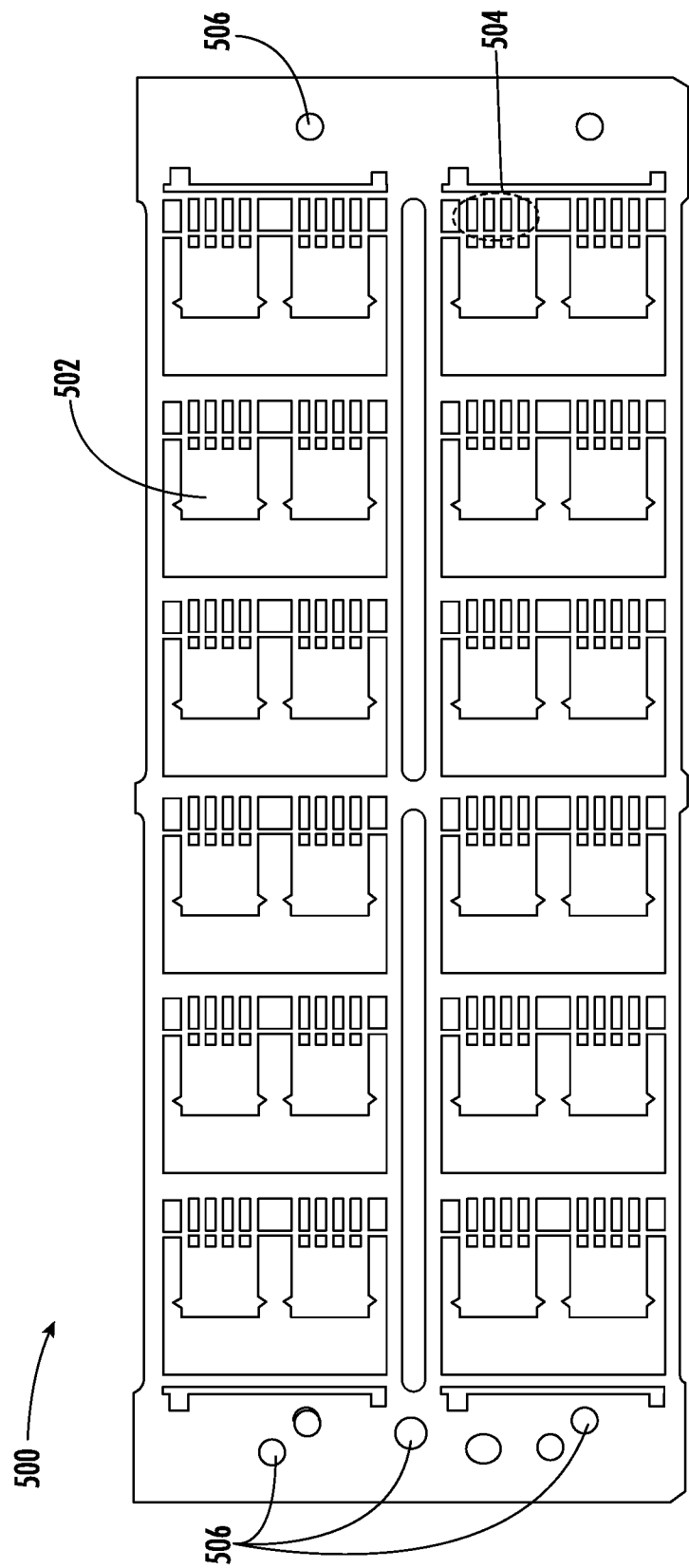


FIG. 5

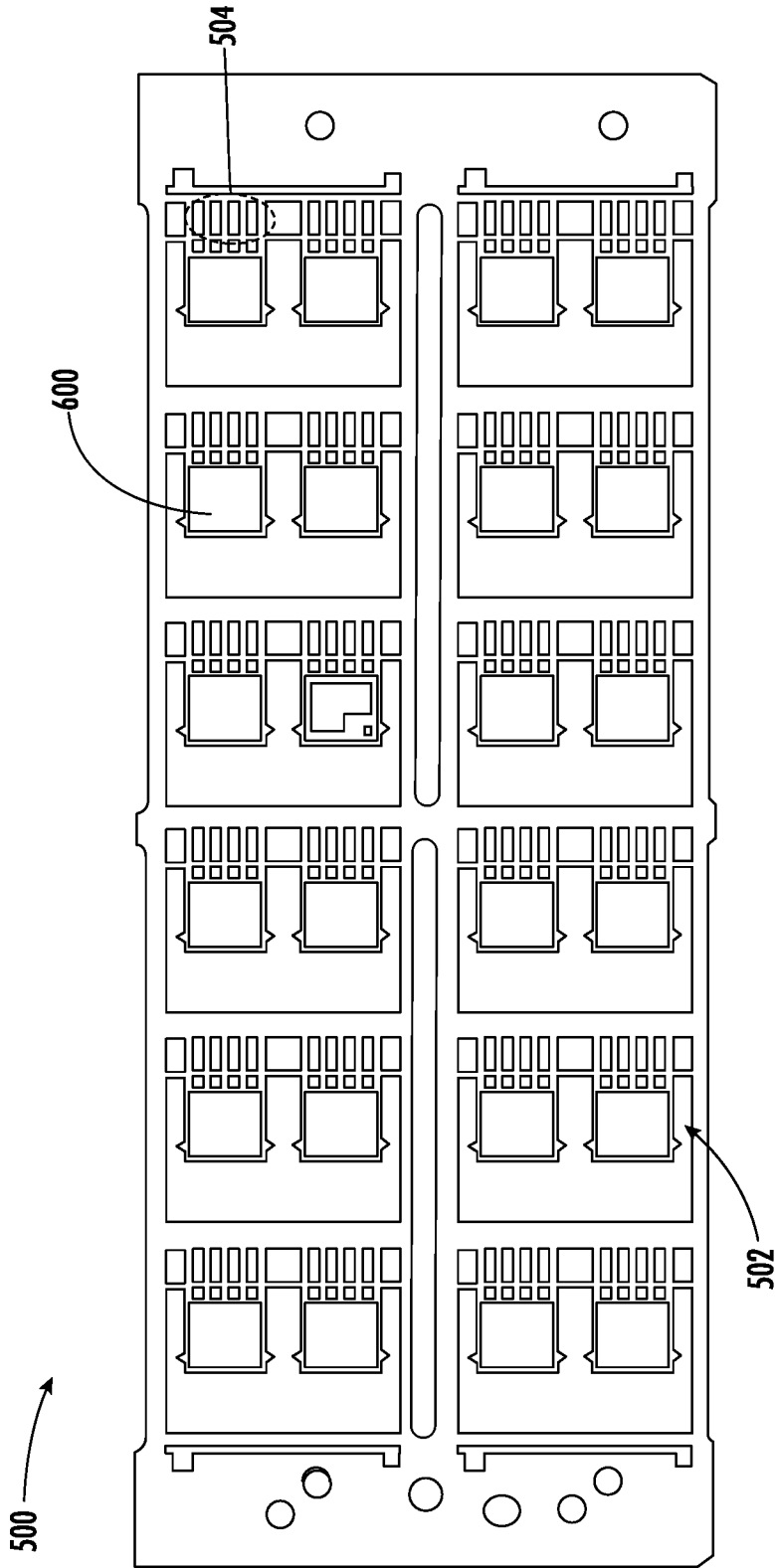


FIG. 6

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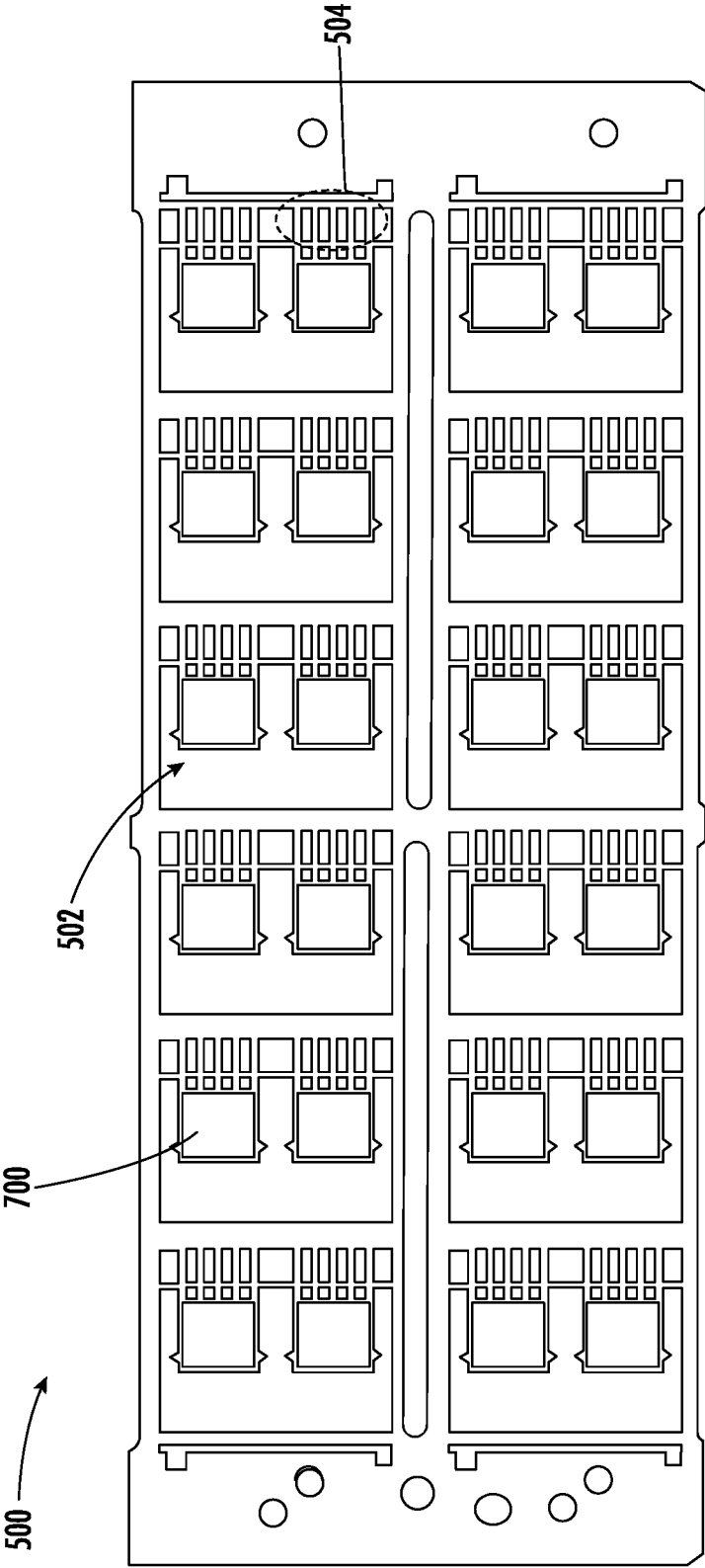


FIG. 7

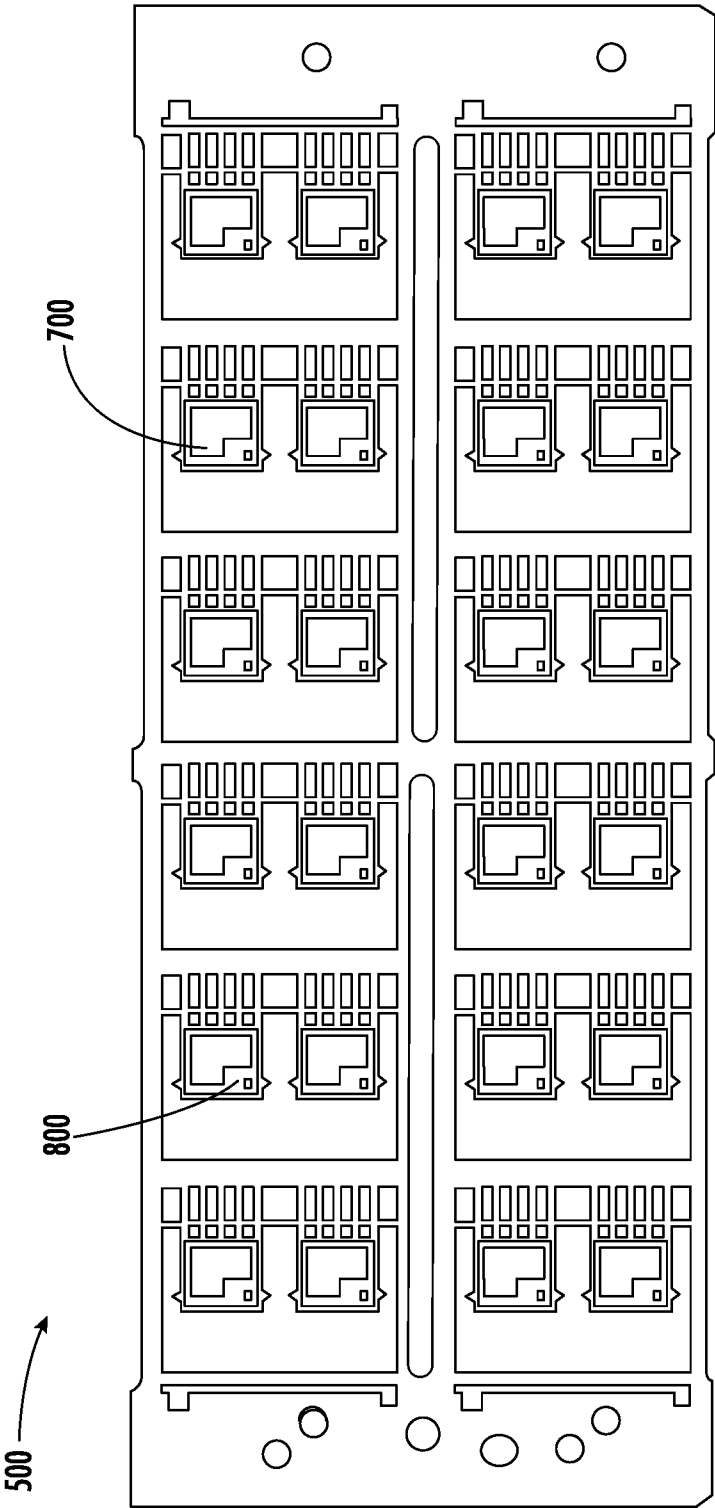
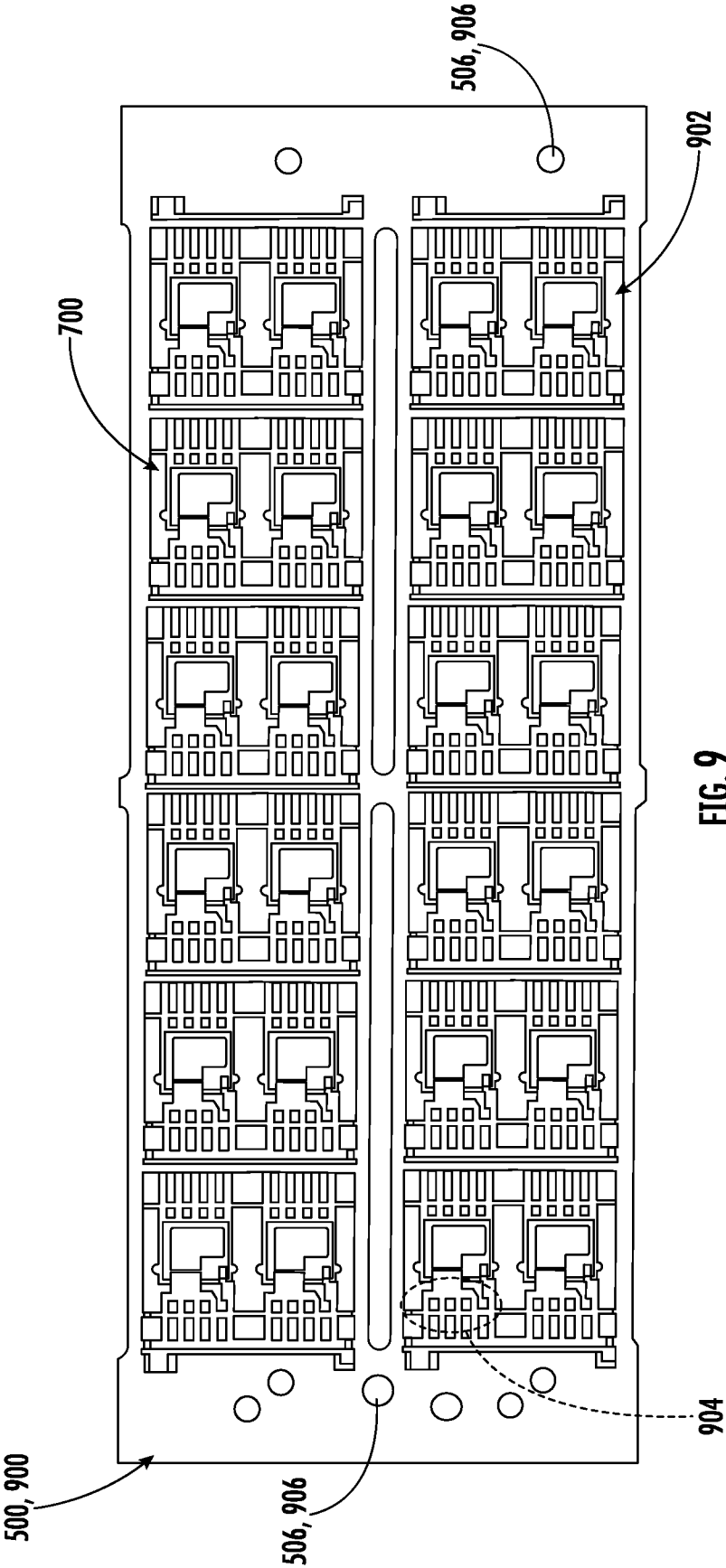


FIG. 8

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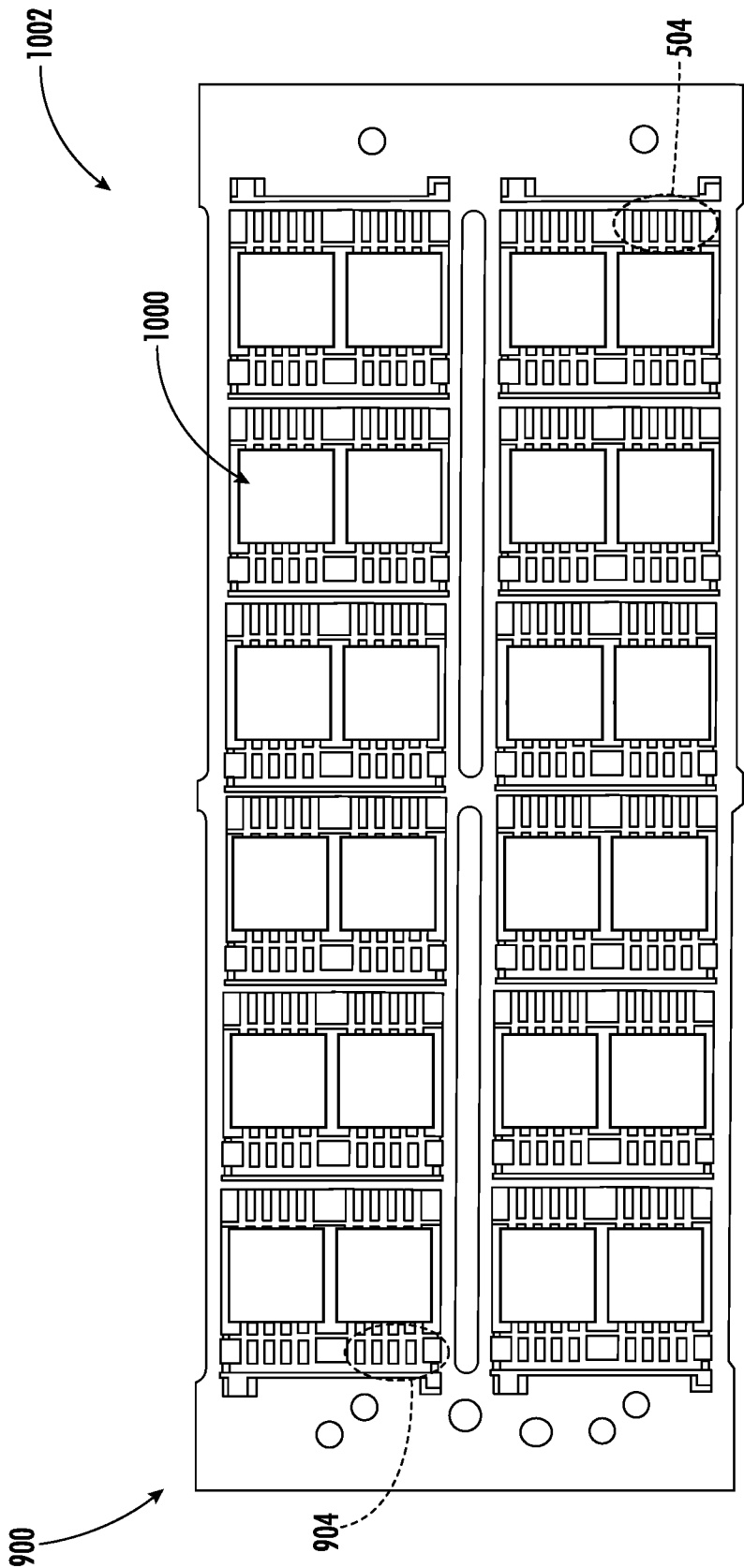


FIG. 10

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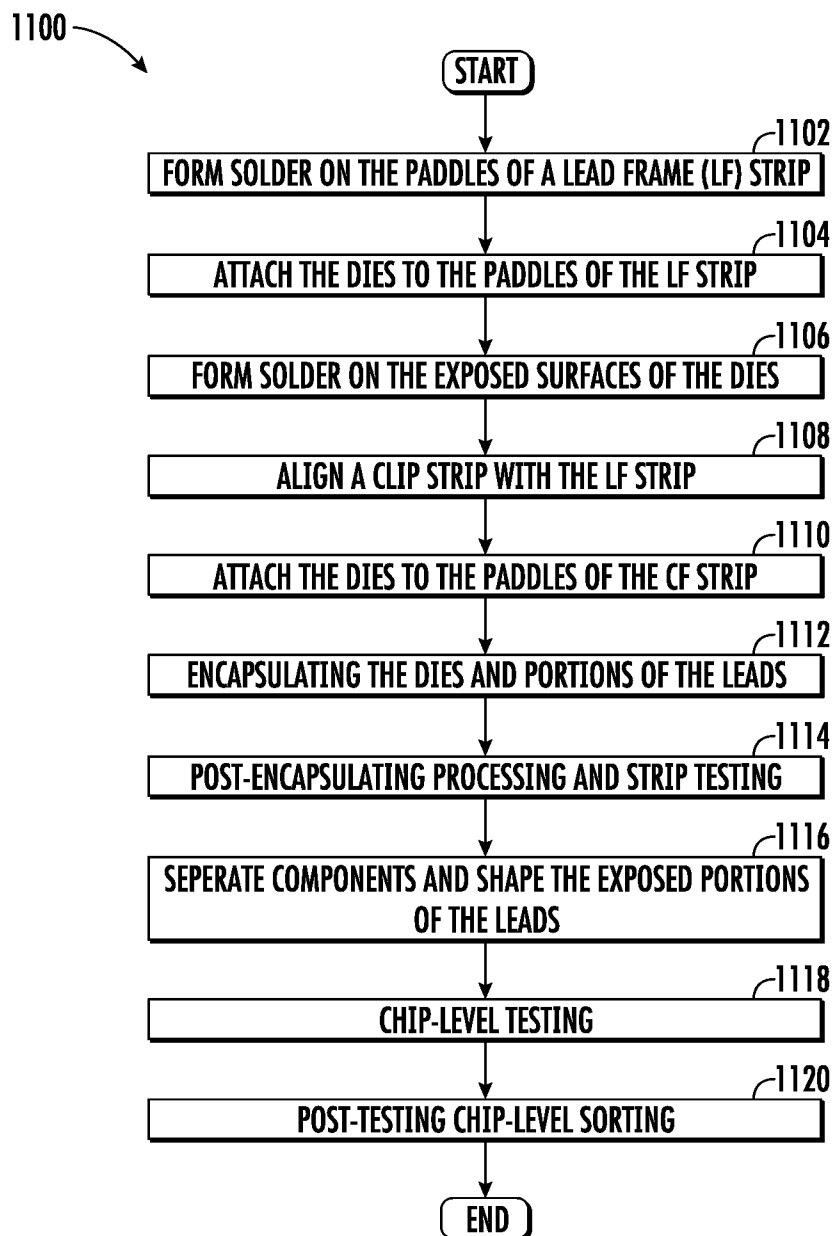


FIG. 11

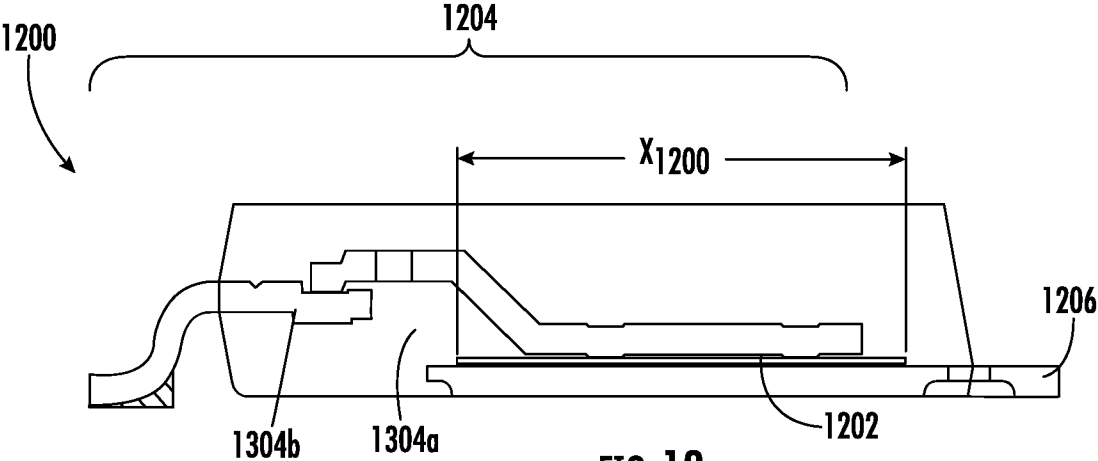


FIG. 12
(PRIOR ART)

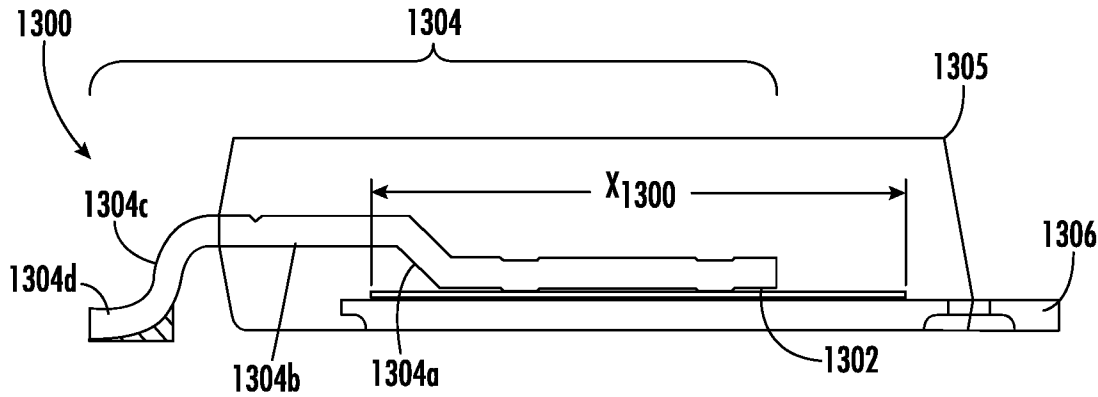


FIG. 13

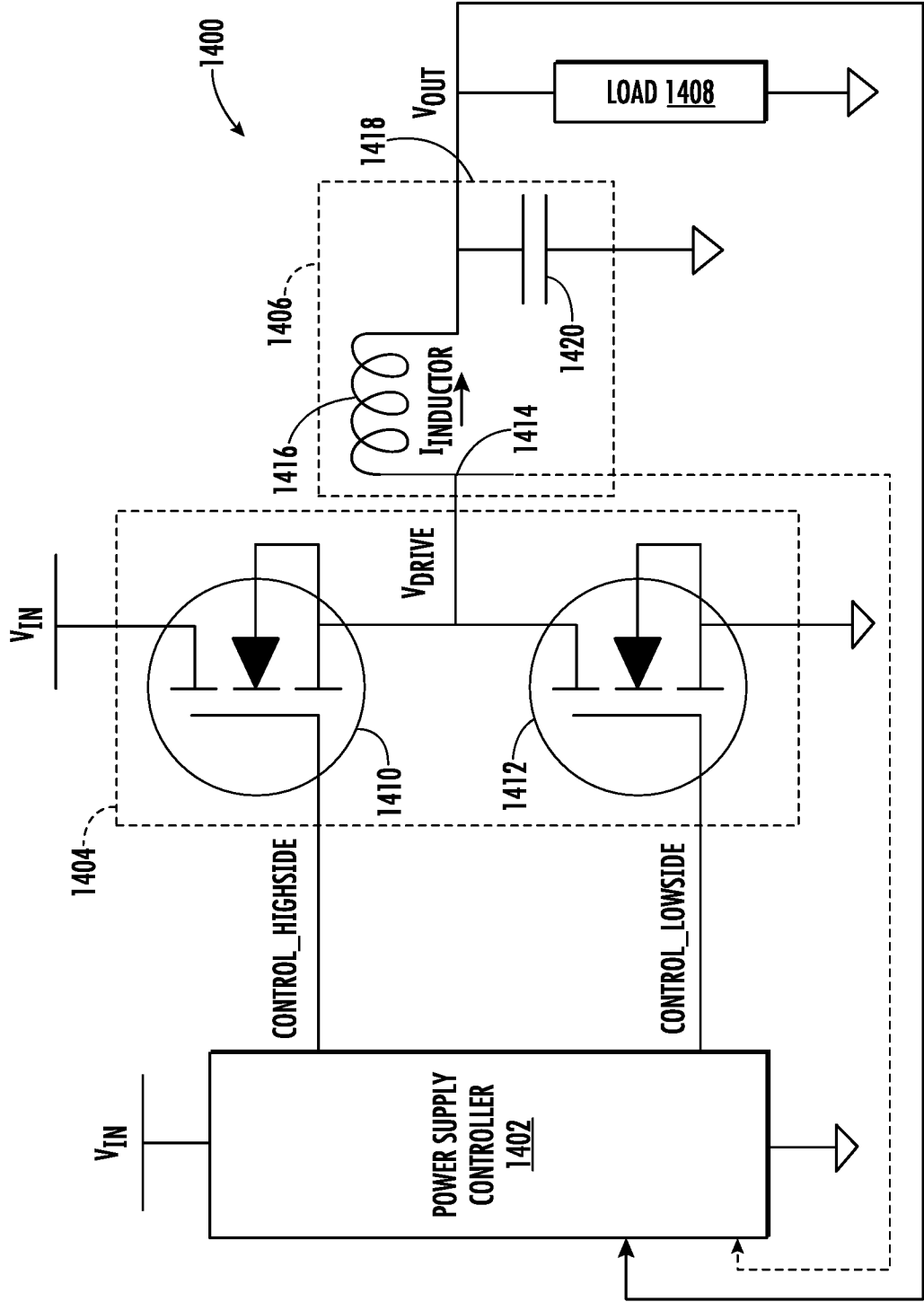


FIG. 14

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2023/024511

A. CLASSIFICATION OF SUBJECT MATTER H01L 23/495(2006.01)i; H01L 23/04(2006.01)i; H01L 23/544(2006.01)i; H01L 21/66(2006.01)i; H01L 29/78(2006.01)i; H01L 23/31(2006.01)i; H01L 23/00(2006.01)i; H01L 21/78(2006.01)i According to International Patent Classification (IPC) or to both national classification and IPC				
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H01L 23/495(2006.01); H01L 21/56(2006.01); H01L 21/60(2006.01); H01L 23/48(2006.01); H01L 23/52(2006.01); H01L 29/78(2006.01) Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Korean utility models and applications for utility models Japanese utility models and applications for utility models Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) eKOMPASS(KIPO internal) & Keywords: die, chip, housing, lead, frame				
C. DOCUMENTS CONSIDERED TO BE RELEVANT				
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.		
X Y	EP 2306515 A2 (SILICONIX INCORPORATED) 06 April 2011 (2011-04-06) See paragraphs [0028]-[0033], [0044]-[0050] and figures 2A-2D, 4A-4B.	1-10,13,18-19 11-12,14-17,20-21		
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A	US 6040626 A (CHUAN CHEAH et al.) 21 March 2000 (2000-03-21) See column 3, line 30 - column 4, line 8 and figure 3.	1-21		
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.				
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Date of the actual completion of the international search 15 February 2024		Date of mailing of the international search report 15 February 2024		
Name and mailing address of the ISA/KR Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon 35208, Republic of Korea Facsimile No. +82-42-481-8578		Authorized officer LEE Kang Ha Telephone No. +82-42-481-5003		

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/US2023/024511

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