



## INTEGRATED CURRENT CONTROLLER FOR MAINTAINING HOLDING CURRENT OF A DIMMER CIRCUIT

### CLAIM OF PRIORITY

**[0001]** This application claims priority under Article 8 of the Patent Cooperation Treaty (PCT) to U.S. Provisional Application No. 61/777,339, filed March 12, 2013.

### TECHNICAL FIELD

**[0002]** Embodiments of the present invention relate generally to power supplies. More specifically, examples of the present invention are related to control circuits for use with power supplies that include dimming circuitry.

### BACKGROUND

**[0003]** Electronic devices use power to operate. Power is generally delivered through a wall socket as high voltage alternating current (ac). A device typically referred to as a power supply or as a power converter can be utilized in lighting systems to convert the high voltage ac input into a well regulated direct current (dc) output through an energy transfer element. Switched mode power converters are commonly used due to their high efficiency, small size, and low weight to power many of today's electronics. During operation, a switch included in a driver circuit of the power converter is utilized to provide the desired output by varying the duty cycle (typically the ratio of the on time of the switch to the total switching period), varying the switching frequency or varying the number of pulses per unit time of the switch in a power converter. Typically, the switching frequency of a switched mode power converter is much greater than the line frequency of the high voltage ac input. In fact, the switching frequency may be orders of magnitudes greater than the line frequency.

**[0004]** In one type of dimming for lighting applications, a TRIAC dimmer circuit, or a thyristor dimmer circuit, removes a portion of the ac input voltage to

limit the amount of voltage and current supplied to an incandescent lamp. This is known as phase dimming because it is often convenient to designate the position of the missing voltage in terms of a fraction of the period of the ac input voltage measured in degrees. In general, the ac input voltage is a sinusoidal waveform and the period of the ac input voltage is referred to as a full line cycle. As such, half the period of the ac input voltage is referred to as a half line cycle. An entire period has 360 degrees, and a half line cycle has 180 degrees. Typically, the phase angle is a measure of how many degrees (from a reference of zero degrees) of each half line cycle the dimmer circuit removes. As such, removal of half the ac input voltage in a half line cycle by a TRIAC dimmer circuit corresponds to a phase angle of 90 degrees. In another example, removal of a quarter of the ac input voltage in a half line cycle may correspond to a phase angle of 45 degrees.

**[0005]** Although phase angle dimming works well with incandescent lamps that receive the altered ac line voltage directly, phase angle dimming typically creates problems for light emitting diode (LED) lamps driven by a switched mode power converter. Conventional regulated switched mode power converters are typically designed to ignore distortions of the ac input voltage and deliver a constant regulated output until a low input voltage causes them to shut off. As such, conventional regulated switched mode power converters cannot dim LED lamps. Unless a power converter for an LED lamp is specially designed to recognize and respond to the voltage from a TRIAC dimmer circuit in a desirable way, the dimmer circuit can produce unacceptable results such as flickering of the LED lamp.

**[0006]** Another difficulty in using TRIAC dimmer circuits with LED lamps comes from a characteristic of the dimmer circuit itself. For instance, a TRIAC dimmer circuit is a semiconductor component that behaves as a controlled ac switch. In other words, it behaves as an open switch to an ac voltage until it receives a trigger signal at a control terminal, which causes the switch to close. The switch remains closed as long as the current through the switch is above a value referred to as the holding current. Most incandescent lamps use more than enough current from the ac power source to allow reliable and consistent operation of a

TRIAC dimmer circuit. However, the low current used by efficient power converters to drive LED lamps may not draw sufficient current to keep the dimmer circuit conducting for the expected portion of the ac line period.

### SUMMARY

**[0007]** In one example, a control circuit for use in a power converter that has a dimmer circuit coupled to an input of the power converter includes a current controller and a main controller. The current controller controls a current through an energy transfer element of the power converter by cycling between a first and second states. The main controller controls the current controller in a first mode where the first state of the current controller is an ON state and the second state is an OFF state such that an output of the power converter is regulated. The main controller controls the current controller in a second mode where the first state is the ON state but the second state is a non-zero minimum current state to maintain an input current of the power converter that is equal to or greater than a holding current threshold of the dimmer circuit.

**[0008]** In another example, a power converter includes an energy transfer element and an integrated control circuit. The integrated control circuit includes a current controller and a main controller. The current controller controls a current through an energy transfer element of the power converter by cycling between a first and second states. The main controller controls the current controller in a first mode where the first state of the current controller is an ON state and the second state is an OFF state such that an output of the power converter is regulated. The main controller controls the current controller in a second mode where the first state is the ON state but the second state is a non-zero minimum current state to maintain an input current of the power converter that is equal to or greater than a holding current threshold of the dimmer circuit.

**[0009]** In yet another example, a main controller for use in a power converter includes a drive circuit, a phase detection circuit, and a linear control circuit. The drive circuit generates a drive signal in response to a feedback signal

representative of the output of the power converter. The drive signal controls a power switch of a current controller of the power converter in either a first mode or in a second mode. The phase detection circuit receives an input sense signal and generates a phase angle signal in response thereto. The phase angle signal is representative of a phase angle of an input voltage of the power converter. The linear control circuit generates a linear control signal which controls a controlled current source of the current controller of the power converter in response to the phase angle signal. The linear control signal controls the controlled current source when in the second mode of operation. The current controller is controlled in the first mode when the phase angle is less than a phase angle threshold and wherein the current controller is controlled in the second mode when the phase angle is greater than the phase angle threshold.

#### **BRIEF DESCRIPTION OF DRAWINGS**

**[0010]** Non-limiting and non-exhaustive embodiments of the present invention are provided in the following figures, wherein like reference numerals refer to like parts throughout the various views unless otherwise specified.

**[0011]** FIG. 1A is an example schematic diagram illustrating a power converter having a main controller coupled to receive an input sense signal representative of an input current of the power converter, in accordance with the teachings of the present disclosure.

**[0012]** FIG. 1B is an example schematic diagram illustrating a power converter having a main controller coupled to receive an input sense signal representative of a dimmer output voltage of the power converter, in accordance with the teachings of the present disclosure.

**[0013]** FIG. 1C is an example schematic diagram illustrating a power converter having a main controller coupled to receive an input sense signal representative of rectified input voltage of the power converter, in accordance with the teachings of the present disclosure.

[0014] FIG. 1D is an example schematic diagram illustrating a power converter having a main controller coupled to receive an input sense signal representative of an output current of the power converter, in accordance with the teachings of the present disclosure.

[0015] FIG. 1E is an example schematic diagram illustrating a power converter having a main controller coupled to receive an input sense signal representative of an current through the energy transfer element of the power converter, in accordance with the teachings of the present disclosure.

[0016] FIGS. 2A-2C illustrate example waveforms of an ac voltage, a dimmer output voltage, and a rectified input voltage, in accordance with the teachings of the present disclosure.

[0017] FIGS. 3A-3D illustrate various example waveforms of the input current with respect to a phase angle of the input voltage operating in a first mode and a second mode, in accordance with the teachings of the present disclosure.

[0018] FIG. 4A illustrates a drain current of a current controller operating in a first mode of operation, in accordance with the teachings of the present disclosure.

[0019] FIG. 4B illustrates a drain current of a current controller operating in a second mode of operation, in accordance with the teachings of the present disclosure.

[0020] FIG. 4C illustrates drain current of a current controller operating in a third mode of operation, in accordance with the teachings of the present disclosure.

[0021] FIG. 5 is an example schematic diagram illustrating a power converter having a control circuit that includes a main controller and a current controller, in accordance with the teachings of the present disclosure.

[0022] FIG. 6 is an example functional block diagram illustrating a main controller, in accordance with the teachings of the present disclosure.

[0023] FIG. 7 is an example schematic diagram illustrating a power converter having a control circuit that includes a main controller and a current controller, in accordance with the teachings of the present disclosure.

[0024] FIG. 8 is an example functional block diagram illustrating a main controller, in accordance with the teachings of the present disclosure.

[0025] FIG. 9 is an example schematic diagram illustrating an isolated power converter, in accordance with the teachings of the present disclosure.

[0026] Corresponding reference characters indicate corresponding components throughout the several views of the drawings. Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help to improve understanding of various embodiments of the present invention. Also, common but well-understood elements that are useful or necessary in a commercially feasible embodiment are often not depicted in order to facilitate a less obstructed view of these various embodiments of the present invention.

#### DETAILED DESCRIPTION

[0027] In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one having ordinary skill in the art that the specific detail need not be employed to practice the present invention. In other instances, well-known materials or methods have not been described in detail in order to avoid obscuring the present invention.

[0028] Reference throughout this specification to "one embodiment", "an embodiment", "one example" or "an example" means that a particular feature, structure or characteristic described in connection with the embodiment or example is included in at least one embodiment of the present invention. Thus, appearances of the phrases "in one embodiment", "in an embodiment", "one example" or "an example" in various places throughout this specification are not necessarily all referring to the same embodiment or example. Furthermore, the particular features, structures or characteristics may be combined in any suitable combinations and/or subcombinations in one or more embodiments or examples. Particular features,

structures or characteristics may be included in an integrated circuit, an electronic circuit, a combinational logic circuit, or other suitable components that provide the described functionality. In addition, it is appreciated that the figures provided herewith are for explanation purposes to persons ordinarily skilled in the art and that the drawings are not necessarily drawn to scale.

[0029] As mentioned above, a TRIAC dimmer circuit is one example of a dimming circuit included in power supplies utilized in lighting applications. The dimming circuit removes a portion of the ac input voltage to limit the amount of voltage and current supplied to a load (e.g., an incandescent lamp). However, if the load that is driven by a power converter includes an LED lamp, unless the power converter is specially designed to recognize and respond in a desirable way to a voltage having removed portions, the TRIAC dimmer circuit can produce unacceptable results such as flickering of the LED lamp. In addition, since LED lamps generally draw less current than incandescent lamps, the low current drawn by efficient power converters that drive LED lamps from the ac power source may not be enough current (*i.e.*, the holding current) to keep a TRIAC dimmer circuit conducting for the expected portion of the ac line period. Furthermore, the high frequency transition of the sharply increasing input voltage that occurs when the dimmer circuit fires during each half line cycle causes inrush input current ringing, which may drop below holding current.

[0030] Therefore, power converter controller designs usually rely on including a dummy load within the power converter to take enough extra current from the input of the power converter to keep the TRIAC dimmer circuit conducting. In addition, or instead, a bleeder circuit may be utilized to keep the current through the TRIAC dimmer circuit above the holding current. Conventional bleeder circuits may include a series damping resistor, which is coupled between the TRIAC dimmer circuit and the input of the power converter. However, the series damping resistance conducts current (and therefore dissipates power) while a voltage is present. As such, use of a series damping resistance affects the efficiency of the overall power conversion system.

**[0031]** Accordingly, examples of power converters used in lighting systems with dimming circuitry may include a current controller that is coupled to control current through an energy transfer element of the power converter in order to regulate an output of the power converter. Embodiments discussed herein control the current controller to operate in multiple modes of operation. In a first mode, the current controller may be controlled to cycle between an ON state and an OFF state. In response to detecting that the input current of the power converter will soon fall below a holding current threshold, the current controller may then be operated in a second mode of operation, where the current controller cycles between the ON state and a non-zero minimum current state. The non-zero minimum current state of the current controller maintains the input current of the power converter to be equal to or greater than the holding current threshold of the dimmer circuit.

**[0032]** To illustrate, FIG. 1A is an example schematic diagram illustrating a power converter 100 having a main controller 118 coupled to receive an input sense signal 140 that is representative of an input current  $I_{IN}$  130 of the power converter 100, in accordance with the teachings of the present disclosure. The illustrated example of power converter 100 includes a current controller 106, an input capacitor  $C_{IN}$  109, a diode D1 110, an energy transfer element L1 108, and an output capacitor  $C_O$  112. Also shown in FIG. 1A are a dimmer circuit 102, a rectifier 104, a load 114, and a sense circuit 116. The illustrated example of current controller 106 includes a switch 120 (e.g., a power switch) and a current source 122. Although FIG. 1A illustrates power converter 100 configured as a buck converter, various other types of power converter topologies may be implemented in accordance with the teachings herein. For example, power converter 100 may be configured as any switch mode power converter topology including, for example, flyback, forward, boost, buck, half bridge, and full bridge, among many others including resonant types.

**[0033]** In operation, power converter 100 provides power to load 114 from an unregulated input voltage. In one embodiment, the input voltage is an ac input voltage  $V_{AC}$  124. As shown, dimmer circuit 102 receives ac input voltage  $V_{AC}$  124

to produce dimmer output voltage  $V_{DO}$  126. The dimmer output voltage  $V_{DO}$  126 is received by the rectifier 104 to produce a rectified input voltage  $V_{IN}$  128. In one example, rectifier 104 includes a full-wave rectifier circuit.

[0034] FIGS. 2A-2C illustrate example waveforms of an ac input voltage 224, a dimmer output voltage 226, and a rectified input voltage 228, in accordance with the teachings of the present disclosure. Ac input voltage 224, dimmer output voltage 226, and rectified input voltage 228 are possible representations of ac input voltage 124, dimmer output voltage 126, and rectified input voltage 128, respectively, of FIG. 1A.

[0035] As shown in FIG. 2A, ac input voltage  $V_{AC}$  224 is generally a sinusoidal waveform with a period denoted as a full line cycle  $T_{AC}$  248. A full line cycle  $T_{AC}$  248 of ac input voltage  $V_{AC}$  224 is denoted as the length of time between every other zero-crossing. When expressed as an angular displacement instead of time, a full line cycle spans 360 degrees, with 180 degrees between zero crossings.

[0036] Now referring to dimmer output voltage 226 of FIG. 2B, the half line cycle 250 of the ac input voltage  $V_{AC}$  224 is denoted as the length of time between consecutive zero-crossings. The phase angle  $\Phi$  252 is measured as how many degrees (from a reference of zero degrees) the dimmer circuit 102 disconnects the input voltage  $V_{AC}$  224. For leading edge dimming, dimmer circuit 102 disconnects the ac input voltage  $V_{AC}$  224 from power converter 100 when the ac input voltage  $V_{AC}$  224 substantially crosses zero voltage. After a given amount of time, the dimmer circuit 102 reconnects ac input voltage  $V_{AC}$  224 with power converter 100 and the dimmer output voltage  $V_{DO}$  226 substantially follows the ac input voltage  $V_{AC}$  224. In other words, the dimmer circuit 102 removes a portion of the ac input voltage 224 to provide the dimmer output voltage  $V_{DO}$  226 thus limiting the amount of power supplied to a load (such as an LED lamp).

[0037] FIG. 2C illustrates that at the beginning of each half line cycle 250, rectified input voltage  $V_{IN}$  228 is substantially equal to zero, corresponding to the time that the dimmer circuit 102 disconnects the ac input voltage  $V_{AC}$  224 from the power converter. When the dimmer circuit 102 reconnects the ac input voltage  $V_{AC}$

224 to the power converter, the rectified input voltage  $V_{IN}$  228 substantially follows the positive magnitude of the dimmer output voltage  $V_{DO}$  226 and the ac input voltage  $V_{AC}$  224 (i.e.,  $V_{IN} = |V_{DO}|$ ). As shown, dimmer output voltage  $V_{DO}$  226 sharply changes from zero to substantially follow the ac input voltage  $V_{AC}$  224 when dimmer circuit 102 reconnects the ac input voltage 224.

**[0038]** Referring now back to FIG. 1A, the illustrated embodiment of current controller 106 includes switch 120 and controlled current source 122. Current controller 106 is coupled to the cathode of the diode D1 110 and to one terminal of energy transfer element L1 108. Energy transfer element L1 108 is further coupled to an output capacitor  $C_O$  112. The output capacitor  $C_O$  112 is coupled to the output return 111 to provide an output voltage  $V_O$  132 across the output capacitor 112. The load 114 is coupled to the output capacitor  $C_O$  112. The anode of diode D1 110, output capacitor  $C_O$  112, and the load 114 are coupled to the output return 111. Current controller 106 is also coupled to input capacitor  $C_{IN}$  109. In the example shown, the input capacitor  $C_{IN}$  109 is coupled to the rectifier 104 such that the voltage across the input capacitor  $C_{IN}$  109 is the rectified input voltage  $V_{IN}$  128. Rectifier 104 is further coupled to dimmer circuit 102, which in one example may include a triac dimmer circuit 113. Dimmer circuit 102 is coupled to receive the ac input voltage  $V_{AC}$  124.

**[0039]** In operation, when switch 120 is closed (i.e., ON state), switch current  $I_{SW}$  may pass through the switch 120 to energy transfer element L1 108, thereby charging output capacitor  $C_O$  112 and providing power to load 114. When switch 120 is open (i.e., OFF state), inductor current  $I_P$  continues through the energy transfer element L1 108, capacitor  $C_O$  112, and load 114. The inductor current  $I_P$  then returns through diode D1 110, thereby ramping down while energy stored in energy transfer element 108 discharges.

**[0040]** Main controller 118 includes terminals for receiving and/or providing the input sense signal 140, switch current sense signal 142, switch drive signal  $U_D$  144, linear control signal  $U_{LC}$  146, and feedback signal  $U_{FB}$  138. In the example of FIG. 1A, input sense 140 is representative of the input current  $I_{IN}$  130. In one

embodiment, switch current sense signal 142, received by main controller 118, is representative of the switch current  $I_{SW}$  through switch 120. Switch drive signal  $U_D$  144 is provided to control the switching of switch 120. Main controller 118 is configured to output a linear control signal  $U_{LC}$  146 for controlling current source 122. As shown in FIG. 1A, main controller 118 is also coupled to receive a feedback signal  $U_{FB}$  138, which, in this example, is received from sense circuit 116. In one embodiment, feedback signal  $U_{FB}$  138 is representative of the output of power converter 100. For example, sense circuit 116 may be coupled to receive an output quantity signal  $U_O$  136 that is representative of the output of the power converter 100, which may be output voltage  $V_O$  132, output current  $I_O$  134, or a combination of the two.

**[0041]** Main controller 118 may maintain the minimum holding current for the triac 113 to operate properly and regulate output power supplied to load 114. Main controller 118 also regulates power to load 114 by controlling current controller 106 based on the feedback signal 138. Switch 120 is controlled in response to the switch drive signal  $U_D$  144. Main controller 118 controls the operation of the power converter 100 with switch drive signal 144 to regulate the power delivered to load 114. In addition, the main controller 118 utilizes the current controller 106 to provide current such that the input current does not fall below the minimum holding current of dimmer circuit 102. Main controller 118 receives input sense signal 140 and determines whether the input current  $I_{IN}$  130 may be close to falling below the holding current threshold. In one example, if a magnitude of input sense signal 140 falls below a threshold, main controller 118 provides the linear control signal 146 which enables the controlled current source 122. As illustrated, input current  $I_{IN}$  130 is substantially equal to the sum of the linear current  $I_{LNR}$  and the switch current  $I_{SW}$ . In response to the linear control signal 146, controlled current source 122 provides additional current  $I_{LNR}$  which then increases the input current  $I_{IN}$  above the holding current. In one example, when a magnitude of input sense signal 140 falls below the threshold, controlled current source 122 provides a constant linear current  $I_{LNR}$ . In another example, controlled current source 122

provides a variable linear current  $I_{LNR}$  that changes with changes in the input sense signal 140. For example, current source 122 may provide a linear current  $I_{LNR}$  that is inversely proportional to the magnitude of the input sense signal 140.

**[0042]** Main controller 118 may control current controller 106 in multiple modes of operation. In one embodiment, a first mode includes cycling switch 120 between an ON state and an OFF state while controlled current source 122 is disabled, such that the controlled current source 122 does not provide additional current. In this embodiment, when in the first mode of operation, the drain current  $I_D$ , may return to zero each time switch 120 turns off (i.e., OFF state).

**[0043]** If the main controller 118 detects that input current  $I_{IN}$  130 will soon fall below a minimum threshold level (e.g., below a holding current threshold of dimmer circuit 102), main controller 118 may change to controlling current controller 106 in a second mode of operation. In one example, the second mode of operation includes cycling switch 120 between the ON state and the OFF state while current source 122 is enabled to provide the linear current  $I_{LNR}$ . While in the second mode of operation current source 122 is enabled to provide linear current  $I_{LNR}$ , such that the input current  $I_{IN}$  130 is maintained at least above the holding current threshold of dimmer circuit 102. In this example, when in the second mode of operation, the drain current  $I_D$  is equal to the switch current  $I_{SW}$  plus the linear current  $I_{LNR}$ .

**[0044]** As mentioned above, main controller 118 may control current controller 106 in multiple modes of operation. Thus, in one embodiment, current controller 106 may include a third mode of operation in addition to the first and second modes discussed above. In this example, main controller 118 may control the current controller 106 in the third mode of operation in response to a light load at the output of the power converter. The input voltage may be low or the load may be small such that there may be little to no benefit in using the switching element. In the third mode of operation, switch 120 is held in the OFF state and current source 122 is driven in a linear mode to provide enough holding current at the input

of power converter 100. In this example, the drain current  $I_D$ , is simply equal to the linear current  $I_{LNR}$ .

**[0045]** FIG. 1B is an example schematic diagram illustrating a power converter 101 having a main controller 118 coupled to receive input sense signal 140. Power converter 101 couples and operates similar to power converter 100 discussed above. In the power converter 100 of FIG. 1A, main controller 118 was coupled to receive an input sense signal 140 that is representative of the input current  $I_{IN}$  130 and main controller 118 determines the mode of operation of current controller 106 based on a magnitude of the input current  $I_{IN}$ . However, in the embodiment of FIG. 1B, input sense signal 140 is representative of dimmer output voltage  $V_{DO}$  126. Thus, main controller 118 of FIG. 1B may determine the mode of operation based on the dimmer output voltage  $V_{DO}$  126. In one embodiment, main controller 118 includes a phase detection circuit to determine the phase angle of the dimmer output voltage  $V_{DO}$  126. Main controller 118 of FIG. 1B, may then compare the determined phase angle against a phase angle threshold in order to determine the mode of operation. In one embodiment, a measured phase angle below the phase angle threshold corresponds to the first mode of operation, while a phase angle at or above the phase angle threshold corresponds to the second mode of operation.

**[0046]** FIG. 1C is an example schematic diagram illustrating a power converter 103 having main controller 118 coupled to receive input sense signal 140, in this embodiment, that is representative of rectified input voltage  $V_{IN}$  128. Power converter 103 couples and operates similar to power converter 100 discussed above. In the embodiment of FIG. 1C, input sense signal 140 is representative of rectified input voltage  $V_{IN}$  128. Thus, main controller 118 of FIG. 1C may determine the mode of operation based on rectified input voltage  $V_{IN}$  128. In one embodiment, main controller 118 includes a phase detection circuit to determine the phase angle of the rectified input voltage  $V_{IN}$  128. Main controller 118 of FIG. 1C, may then compare the determined phase angle against a phase angle threshold in order to determine the mode of operation. In one embodiment, a measured phase angle

below the phase angle threshold corresponds to the first mode of operation, while a phase angle at or above the phase angle threshold corresponds to the second mode of operation.

**[0047]** FIG. 1D is an example schematic diagram illustrating a power converter 105 having a main controller 118 coupled to receive input sense signal 140, which in this embodiment is representative of an output current  $I_O$  134 of the power converter 105. Power converter 105 couples and operates similar to power converter 100 discussed above. In the embodiment of FIG. 1D, input sense signal 140 is representative of output current  $I_O$  134. Thus, main controller 118 of FIG. 1D may determine the mode of operation based on a magnitude of output current  $I_O$  134. In one embodiment, output current  $I_O$  is taken as the current through diode D1 110. In this example, the current through diode D1 110 may be representative of an input (e.g., input current  $I_{IN}$  130) when switch 120 is not conducting (i.e., in the OFF state).

**[0048]** FIG. 1E is an example schematic diagram illustrating a power converter 107 having main controller 118 coupled to receive input sense signal 140, which in this example is representative of an inductor current  $I_P$  through energy transfer element L1 108. Power converter 107 couples and operates similar to power converter 100 discussed above. In the embodiment of FIG. 1E, input sense signal 140 is representative of inductor current  $I_P$ . Thus, main controller 118 of FIG. 1D may determine the mode of operation based on a magnitude of inductor current  $I_P$ . In this example, inductor current  $I_P$  through energy transfer element L1 108 may be representative of an input (e.g., input current  $I_{IN}$  130) when switch 120 is conducting (i.e., in the ON state).

**[0049]** FIGS. 3A-3D illustrate various example waveforms of the input current  $I_{IN}$  with respect to a phase angle of the input voltage operating in a first, second, and an optional third mode of operation, in accordance with embodiments of the present disclosure. For example, FIG. 3A illustrates waveforms of the input current  $I_{IN}$  330 in a first and second mode of the current controller (e.g., current controller 106). The vertical axis represents input current  $I_{IN}$  330, while the

horizontal axis represents the phase angle 352. As mentioned above, the phase angle 352 is a measure of how many degrees (from a reference of zero degrees) of each half line cycle the dimmer circuit removes the ac input voltage 124 from the power converter. A first phase threshold is represented by  $\Phi_H$  360. In addition, FIG. 3A illustrates a thin dashed line representative of the switch current  $I_{SW}$  and a thin solid line representative of the linear current  $I_{LNR}$ . At certain phase angles, the average input current may fall below the minimum holding current. As such, the main controller may sense the phase angle of the triac to indirectly sense the input current. The thick solid line is representative of the resultant input current  $I_N$  330.

**[0050]** As the phase angle of the dimmer circuit 102 increases due to dimming control, switch current  $I_{SW}$  decreases due to the drop in available energy from dimmer circuit 102. For a first range of the phase angle, the current controller may operate in a first mode. In the first mode of operation, the input current is substantially equal to the switch current (shown as a dashed line) since the current controller is cycling between an ON state and an OFF state while the controlled current source is disabled such that the controlled current source is not providing additional current. As such, in the first mode of operation, the input current 330 is shown as substantially following the switch current. As illustrated, the average input current decreases with an increasing phase angle.

**[0051]** Illustrated in FIG. 3A is a phase threshold 360 which is representative of the phase angle which the average input current may fall below the holding current  $I_{HOLD}$  358. When the phase angle 352 is greater than phase threshold 360, the current controller may switch to operating in a second mode of operation. In the second mode of operation, the current controller cycles between the ON state and a non-zero minimum current state, such that the input current is substantially equal to the sum of the switch current  $I_{SW}$  and the linear current  $I_{LNR}$ . For the example of FIG. 3A, the main controller controls the controlled current source such that the linear current increases  $I_{LNR}$  as the phase angle increases. In the example shown, the switch current  $I_{SW}$  decreases at the same rate at which the linear

current is increased, such that the resultant input current  $I_{IN}$  is a constant value while the current controller in the second mode.

**[0052]** FIG. 3B illustrates waveforms of the input current  $I_{IN}$  330 in a first and second mode of the current controller, in accordance with another embodiment of the present disclosure. In the embodiment of FIG. 3B, the main controller controls the controlled current source such that the linear current  $I_{LNR}$  is substantially constant with an increasing phase angle. As such, when the current controller is operating in the second mode, the input current 330 increases by the value of the linear current  $I_{LNR}$  and then decreases at the same rate as the switch current decreases. Or in other words, the linear current  $I_{LNR}$  provides a fixed offset in the second mode of operation for the example shown in FIG. 3B. Further, in this example of the second mode, the value of the linear current  $I_{LNR}$  is substantially equal to the holding current  $I_{HOLD}$  of the dimmer circuit.

**[0053]** FIG. 3C illustrates waveforms of the input current  $I_{IN}$  330 in a first, second, and an optional third mode of the current controller, in accordance with another embodiment of the present disclosure. The third mode of operation occurs in response to a light load. When phase angle 352 reaches the first phase threshold  $\Phi_1$  360, the current controller transitions from the first mode of operation to the second mode of operation. While in the second mode, as the switch current  $I_{SW}$  decreases, current source 356 of the current controller 106 provides a linear current  $I_{LNR}$  to the input current  $I_{IN}$ . As shown in FIG. 3C, the linear current  $I_{LNR}$  is increased in response to increases in phase angle 352. In response to phase angle 352 reaching a second phase threshold  $\Phi_2$  368, the current controller transitions to a third mode of operation. In the third mode of operation, Switch 120 is open (i.e., OFF state). The input current is substantially equal to linear current  $I_{LNR}$ , which is still increased in response to increases in phase angle 352. This indicates the current source is driven in linear mode to provide enough holding current to input current  $I_{IN}$  330.

**[0054]** FIG. 3D illustrates waveforms of the input current  $I_{IN}$  330 in a first, second, and optional third mode of the current controller. However, the main

controller controls the current source in the second and third modes of operation such that the linear current  $I_{LNR}$  is substantially constant with an increasing phase angle 352. As such, when the current controller is operating in the second and third modes, the linear current  $I_{LNR}$  provides a fixed offset for the example shown in FIG. 3D.

**[0055]** FIG. 4A illustrates a drain current  $I_D$  407 of a current controller operating in a first mode of operation, in accordance with the teachings of the present disclosure. Drain current  $I_D$  407 is one possible representation of drain current  $I_D$  of FIGS. 1A-1E. In the example of FIG. 4A, the main controller is operating in discontinuous conduction mode (DCM). The vertical axis denotes the drain current  $I_D$  407 while the horizontal axis represents time. The switching period of each waveform is denoted by  $T_S$  470. The on time period (i.e., the time that current controller 106 is in the ON state each switching period  $T_S$ ) is denoted by  $T_{ON}$  472. The off time period (i.e., the time that current controller 106 is in the OFF state each switching period  $T_S$ ) is denoted  $T_{OFF}$  474. In a first mode of operation, switch 120 is cycled on and off while current source 122 is disabled, such that current source 122 does not provide additional current. Thus, in the first mode of operation the drain current  $I_D$  is equal to the switch current  $I_{SW}$ . As shown in FIG. 4A, when switch 120 is turned on, the switch current  $I_{SW}$  increases. Once switch 120 is turned off, switch current  $I_{SW}$  decreases and substantially falls to zero.

**[0056]** FIG. 4B illustrates the drain current  $I_D$  of a current controller operating in a second mode of operation, in accordance with the teachings of the present disclosure. In this example, while in the second mode, the main controller controls current source 122 to provide a constant current  $I_{LNR}$  423, while switch is cycled on and off. Thus, in the second mode of operation, the current controller 106 includes an ON state that is maintained for an on time period  $T_{ON}$  472. During the on time period  $T_{ON}$  472, the drain current  $I_D$  is substantially equal to the switch current  $I_{SW}$  plus the linear current  $I_{LNR}$  423. As shown in FIG. 4B, current controller 106 also includes a non-zero minimum current state that is maintained for a minimum current time period  $T_{MIN\_I}$  474. During the minimum current time period

$T_{MIN\_I}$  the drain current  $I_D$  is still equal to the switch current  $I_{SW}$  plus the linear current  $I_{LNR}$  423, but since the switch is off, the switch current  $I_{SW}$  is substantially zero, thereby resulting in a drain current  $I_D$  that is equal to the linear current  $I_{LNR}$  423. As described above, the linear current  $I_{LNR}$  423 is added during the second mode of operation maintain the input current  $I_{IN}$  of the power converter at or above a holding current of the dimmer circuit. In one embodiment, the magnitude of the linear current  $I_{LNR}$  423 is substantially equal to or greater than the minimum holding current requirements of the dimmer circuit (e.g., dimmer circuit 102).

[0057] FIG. 4C illustrates drain current  $I_D$  of the current controller operating in a third mode of operation, in accordance with the teachings of the present disclosure. In one embodiment, the third mode of operation includes main controller 118 disabling switch 120, such that switch 120 is kept open and switch current  $I_{SW}$  is substantially equal to zero. However, to keep a triac of the dimmer circuit functioning properly, main controller 118 enables current source 122 such that current controller 106 provides a current  $I_{LNR}$  423 that is equal to or greater than a minimum holding current requirement of the triac.

[0058] FIG. 5 is an example schematic diagram illustrating a power converter 500 having a control circuit 501 that includes a main controller 518 and a current controller 506, in accordance with the teachings of the present disclosure. Power converter 500 couples and operates similar to power converter 100 discussed above. In the power converter 100 of FIG. 1A, main controller 118 provides separate control signals to switch 120 and controller current source 122. However, in the embodiment of FIG. 5 main controller 518 provides a single combined drive signal  $U_D/U_{LC}$  545 to current controller 506. Also, current controller 506 includes a metal oxide semiconductor field effect transistor (MOSFET) that functions as both a switch and a controlled current source. In one embodiment, when in the first mode of operation, main controller 518 generates combined drive signal  $U_D/U_{LC}$  to cycle the MOSFET between an OFF state and an ON state, where the ON state includes driving the MOSFET to be fully on (e.g., in a saturation region of the MOSFET). When in the second mode of operation, main controller 518 generates combined

drive signal  $U_D/U_{LC}$  to cycle the MOSFET between the ON state and a non-zero minimum current state, where the non-zero minimum current state includes driving the MOSFET to be partially on (e.g., in a linear region of the MOSFET). Input sense signal 540 can be represented by any of the embodiments mentioned previously with regards to FIGS. 1A-1E. As shown in the example of FIG. 5, main controller 518 and current controller 506 may be combined onto a single integrated circuit 501.

**[0059]** FIG. 6 is an example functional block diagram illustrating a main controller 618, in accordance with the teachings of the present disclosure. Main controller 618 is one possible implementation of main controller 518 of FIG. 5. As shown, the illustrated example of main controller 618 includes a phase detection 676, reference generator 678, error amplifier 684, linear control circuit 680, and drive circuit 686. Main controller 618 includes terminals for the input sense signal 640, switch current sense signal 642, switch drive signal  $U_D$  645, and feedback signal  $U_{FB}$  638.

**[0060]** Phase detection 676 is coupled to receive the input sense signal 640. The phase detection circuit 676 determines the phase angle from the input sense signal 640 and outputs a phase angle signal 652. In one embodiment the phase angle signal 652 is representative of the phase angle of the dimmer circuit at the input of the power converter. Reference generator 678 and linear control circuit 680 are coupled to receive the phase angle signal 652. The reference generator output signal changes with respect to changes in the phase angle. Reference generator 678 is coupled to the inverting terminal of the error amplifier 684. In particular, the output of reference generator 678 is coupled to be received by the inverting terminal of the error amplifier 684. In one embodiment, error amplifier 684 may be a comparator that compares the reference signal 682 with the feedback signal 638. The non-inverting terminal of the error amplifier 684 is coupled to receive the feedback signal  $U_{FB}$  638. The output of the error amplifier 684 is coupled to the drive circuit 686. Drive circuit 686 is coupled to receive both the switch current sense 642 signal and the linear control circuit signal 646. Drive circuit 686

generates a drive signal 645 in response to the output of error amplifier 684, linear control signal 646, and switch current sense signal 642. Linear control circuit 680 is coupled to receive the phase angle signal 652. Optionally, linear control circuit 680 may also receive the feedback signal  $U_{FB}$  638 to compare in conjunction with phase angle 652.

[0061] The linear control signal 646 sets the value at which to drive the switch to maintain the minimum input holding current based on phase angle 652. Linear control circuit 680 can also control the output current  $I_O$  by keeping it proportional to the phase dimming angle based on the feedback signal  $U_{FB}$  638.

[0062] Phase detection 676 determines the phase angle from the input sense signal 640 and provides the phase angle signal 652 for the reference generator 678 and linear control circuit 680. Reference generator 678 generates a reference voltage  $U_{REF}$  682 based on the phase angle provided by the phase angle signal 652. Error amplifier 684 outputs an error voltage from the reference generator and feedback signal  $U_{FB}$  638. Based on the error voltage, the drive circuit 686 varies the drive signal  $U_D$  645 to regulate the output. The changes in drive signal  $U_D$  645 may include but not limited to, the on/off time, frequency, and duty cycle.

[0063] FIG. 7 is an example schematic diagram illustrating a power converter 700 having a control circuit 701 that includes a main controller 718 and a current controller 706, in accordance with the teachings of the present disclosure. Power converter 700 couples and operates similar to power converter 100 discussed above. As shown in FIG. 7, this example of current controller 706 includes a MOSFET switch 720 and a controlled current source (i.e., MOSFET 790 and JFET 788). In one embodiment, JFET 788 is coupled to MOSFET 790, where the JFET includes a control terminal coupled to the common reference of the current controller.

[0064] The JFET 788 is an example of a current source to power converter 700. The JFET 788 is one embodiment that provides the minimum holding current for the triac. In one embodiment, the linear current may be a constant value. In another embodiment, the linear current is proportional to changes in the phase angle.

[0065] The embodiment of FIG. 7 may reduce the dependence of an external bleeder circuit to take enough extra current from the input of the power supply to keep the triac conducting. An external bleeder circuit may be undesirable because the bleeder circuit would dissipate energy (in the form of heat) and require the use of extra components with associated penalties in cost and efficiency. Thus, aspects of the present invention discussed herein reduce the overall amount of components required. Accordingly, embodiments of the present disclosure provide the required amount of current, as needed, to maintain proper operation of the triac, while also regulating the output of the power converter, without the need for external components, such as a bleeder circuit.

[0066] FIG. 8 is an example functional block diagram illustrating a main controller 818, in accordance with the teachings of the present disclosure. Main controller 818 is one possible implementation of main controller 718 of FIG. 7. Main controller 818 operates and couples similar to main controller 618, discussed above, except that main controller 818 generates a drive signal 844 that is separate and distinct from a generated linear control signal 846.

[0067] Phase detection 876 is coupled to receive the input sense signal 840. Reference generator 878 and linear control circuit 880 are coupled to receive the phase angle signal 852. Reference generator 878 is coupled to the inverting terminal of the error amplifier 884. The non-inverting terminal of the error amplifier 884 is coupled to receive the feedback signal  $U_{FB}$  838. The output of the error amplifier 884 is coupled to the drive circuit 886. Drive circuit 886 is also coupled to receive the switch current sense 842 signal and linear control circuit signal 846. Drive circuit 886 generates a drive signal 844. Linear control circuit 880 receives the feedback signal  $U_{FB}$  838.

[0068] FIG. 9 is an example schematic diagram illustrating an isolated power converter 900, in accordance with the teaching of the present disclosure. As mentioned above, various types of power converter topologies may be implemented in accordance with the teachings herein. Thus, FIG. 9 illustrates an embodiment of main controller 918 and current controller 906 incorporated into a power converter

900 having flyback power converter topology. This illustrated example of power converter 900 includes current controller 906, energy transfer element 908, input return 911, output capacitor C1 912, output diode D1 915, sense circuit 916, output return 917, main controller 918, and clamp 919. Energy transfer element 908 is shown as including a primary winding 909 and a secondary winding 913. Current controller 906 is shown as including a switch 920 and a controlled current source 922. Also shown in FIG. 9 is load 914 coupled to the output of power converter 900. In one embodiment, load 914 includes one or more light emitting diodes (LEDs).

**[0069]** The power converter 900 utilizes the energy transfer element T1 908 to transfer voltage between the primary 909 and the secondary 913 windings. The clamp circuit 919 is coupled to the primary winding 909 to limit the maximum voltage. Switch 920 is opened and closed in response to the drive signal 944. It is generally understood that a switch that is closed may conduct current and is considered on, while a switch that is open cannot conduct current and is considered off. In one example, the switch S1 920 may be a transistor such as a metal-oxide-semiconductor field-effect transistor (MOSFET). In another example, main controller 918 may be implemented as a monolithic integrated circuit or may be implemented with discrete electrical components or a combination of discrete and integrated components. In operation, the switching of the switch 920 produces a pulsating current at the rectifier D1 915. The current in the rectifier D1 915 is filtered by the output capacitor C1 912 to produce a substantially constant output voltage  $V_O$  932, output current  $I_O$  934, or a combination of the two at the load 914.

**[0070]** The power converter 100 further comprises circuitry to regulate the output which is exemplified as output quantity  $U_O$  936. In one example, the sense circuit 916 may sense the output quantity  $U_O$  936 from an additional winding (not shown) included in the energy transfer element T1 908. In another example, there may be a galvanic isolation (not shown) between the main controller 918 and the sense circuit 916. The galvanic isolation could be implemented by using devices such as an opto-coupler, a capacitor or a magnetic coupling.

**[0071]** The sense circuit 916 senses the output quantity  $U_O$  934 of the power converter 900 to provide the feedback signal  $U_{FB}$  938 to the main controller 918. The feedback signal  $U_{FB}$  938 may be a voltage signal or a current signal and provides information regarding the output quantity  $U_O$  936 to the main controller 918. In addition, the main controller 918 receives the switch current sense input signal 942 which relays the switch current  $I_{SW}$  in the switch 920. In addition, the main controller 918 may receive the input sense signal 940. Input sense signal 940 can be represented by any of the embodiments mentioned previously with regards to FIGS. 1A-1E.

**[0072]** Main controller 918 may maintain the minimum holding current for the triac to operate properly and regulate output power supplied to load 914. Main controller 918 controls current controller 906 in a similar manner as described in FIGS. 1A-1E.

### CLAIMS

What is claimed is:

1. A control circuit for use in a power converter, the control circuit comprising:  
a current controller to be coupled to control a current through an energy transfer element of the power converter, wherein the current controller cycles between a first state and a second state; and  
a main controller coupled to generate at least one signal to control a mode of operation of the current controller, wherein the main controller controls the current controller in a first mode of operation where the first state of the current controller is an ON state and the second state is an OFF state such that an output of the power converter is regulated, and wherein the main controller controls the current controller in a second mode of operation where the first state of the current controller is an ON state and the second state is a non-zero minimum current state such that an input current of the power converter is maintained to be equal to or greater than a holding current threshold of a dimmer circuit that is coupled to an input of the power converter.
2. The control circuit of claim 1, wherein the main controller is coupled to receive an input current of the power converter and controls the current controller in the first mode when the input current is greater than the holding current threshold and controls the current controller in the second mode when the input current is less than the holding current threshold.
3. The control circuit of claim 1, wherein the main controller is coupled to receive a dimmer output voltage of the power converter and controls the current controller in the first mode when a phase angle of the dimmer output voltage is less than a phase angle threshold and controls the current controller in the second mode when the phase angle of the dimmer output voltage is greater than the phase angle threshold.

4. The control circuit of claim 1, wherein the main controller is coupled to receive a rectified input voltage of the power converter and controls the current controller in the first mode when a phase angle of the rectified input voltage is less than a phase angle threshold and controls the current controller in the second mode when the phase angle of the rectified input voltage is greater than the phase angle threshold.

5. The control circuit of claim 1, wherein the main controller is coupled to receive an output current of the power converter and controls the current controller in the first mode when the output current is greater than the holding current threshold and controls the current controller in the second mode when the output current is less than the holding current threshold.

6. The control circuit of claim 1, wherein the current controller comprises:

a power switch having first and second terminals and coupled to conduct a switch current through the power switch; and

a controlled current source having first and second terminals and coupled to provide a controlled current, wherein the first terminal of the controlled current source is coupled to the first terminal of the power switch and wherein the second terminal of the controlled current source is coupled to the second terminal of the power switch, such that a drain current of the current controller is equal to the switch current added to the controlled current when the current controller is in the second mode.

7. The control circuit of claim 6, wherein the drain current is equal to the switch current when the current controller is in the first mode.

8. The control circuit of claim 6, wherein the at least one signal includes a first signal to selectively disable the controlled current source when operating the current controller in the first mode and to selectively enable the controlled current source when operating the current controller in the second mode.

9. The control circuit of claim 8, wherein the at least one signal includes a second signal to control the power switch such that

the power switch is enabled to allow the switch current to flow through the power switch when the current controller is in the ON state,

the power switch is disabled to substantially prevent the switch current from flowing through the power switch when the current controller is in the OFF state, and

the power switch is disabled to substantially prevent the switch current from flowing through the power switch when the current controller is in the non-zero minimum current state.

10. The control circuit of claim 9, wherein the main controller comprises:

a drive circuit coupled to generate the second signal to enable and disable the power switch in response to a feedback signal representative of the output of the power converter;

a phase detection circuit coupled to receive a input sense signal and to generate a phase angle signal in response thereto, wherein the phase angle signal is representative of a phase angle of an input voltage of the power converter; and

a linear control circuit coupled to generate the first signal to enable and disable the controlled current source in response to the phase angle signal.

11. The control circuit of claim 10, when the linear control circuit enables the controlled current source, the controlled current is variable responsive to the phase angle of the input voltage.

12. The control circuit of claim 11, wherein the controlled current increases with increases in the phase angle, such that the input current of the power converter is substantially constant.

13. The control circuit of claim 6, wherein the controlled current source comprises a constant current source and a control switch coupled to selectively enable and disable the constant current source in response to the first signal.

14. The control circuit of claim 13, wherein the control switch comprises a metal oxide semiconductor field effect transistor (MOSFET), and wherein the constant current source comprises a junction field effect transistor (JFET) having a base coupled to a common reference of the control circuit.

15. The control circuit of claim 13, wherein the power switch comprises a metal oxide field effect transistor (MOSFET) and wherein the constant current source comprises a junction field effect transistor (JFET).

16. The control circuit of claim 1, wherein the current controller comprises a transistor that, in response to the at least one signal, turns on to put the current controller in the ON state, turns off to put the current controller in the OFF state, and operates in a linear mode of operation to put the current controller in the non-zero minimum current state.

17. The control circuit of claim 16, wherein the main controller comprises:

- a drive circuit coupled to generate the at least one signal to turn on and turn off the transistor in response to a feedback signal representative of the output of the power converter;

- a phase detection circuit coupled to receive a input sense signal and to generate a phase angle signal in response thereto, wherein the phase angle signal is representative of a phase angle of an input voltage of the power converter; and

- a linear control circuit coupled to provide the drive circuit with a linear control signal to control the transistor in the linear mode of operation in response to the phase angle signal.

18. The control circuit of claim 16, wherein the transistor is configured to provide a constant non-zero current in response to the at least one signal when current controller is in the non-zero minimum current state.

19. The control circuit of claim 16, wherein the variable current increases with increases in the phase angle, such that an input current of the power converter is substantially constant.

20. A power converter, comprising:

- an energy transfer element; and

- an integrated control circuit, including:

- a current controller coupled to control a current through the energy transfer element, wherein the current controller cycles between a first state and a second state; and

- a main controller coupled to generate at least one signal to control a mode of operation of the current controller, wherein the main controller controls the current controller in a first mode of operation where the first state of the current controller is an ON state and the second state is an OFF state such that an output of the power converter is regulated, and wherein the main controller controls the current controller in a second mode of operation where the first state of the current controller is an ON state and the second state is a non-zero minimum current state such that an input current of the power converter is maintained to be equal to or greater than a holding current threshold of a dimmer circuit that is coupled to an input of the power converter.

21. The power converter of claim 20, wherein the main controller is coupled to receive an input current of the power converter and controls the current controller in the first mode when the input current is greater than the holding current threshold and controls the current controller in the second mode when the input current is less than the holding current threshold.

22. The power converter of claim 20, wherein the main controller is coupled to receive a dimmer output voltage of the power converter and controls the current controller in the first mode when a phase angle of the dimmer output voltage is less than a phase angle threshold and controls the current controller in the second mode when the phase angle of the dimmer output voltage is greater than the phase angle threshold.

23. The power converter of claim 20, wherein the main controller is coupled to receive a rectified input voltage of the power converter and controls the current controller in the first mode when a phase angle of the rectified input voltage is less than a phase angle threshold and controls the current controller in the second mode when the phase angle of the rectified input voltage is greater than the phase angle threshold.

24. The power converter of claim 20, wherein the main controller is coupled to receive an output current of the power converter and controls the current controller in the first mode when the output current is greater than the holding current threshold and controls the current controller in the second mode when the output current is less than the holding current threshold.

25. The power converter of claim 20, wherein the current controller comprises:

- a power switch having first and second terminals and coupled to conduct a switch current through the power switch; and

- a controlled current source having first and second terminals and coupled to provide a controlled current, wherein the first terminal of the controlled current source is coupled to the first terminal of the power switch and wherein the second terminal of the controlled current source is coupled to the second terminal of the power switch, such that a drain current of the current controller is equal to the

switch current added to the controlled current when the current controller is in the second mode.

26. The power converter of claim 25, wherein the drain current is equal to the switch current when the current controller is in the first mode.

27. The power converter of claim 25, wherein the at least one signal includes a first signal to selectively disable the controlled current source when operating the current controller in the first mode and to selectively enable the controlled current source when operating the current controller in the second mode.

28. The power converter of claim 27, wherein the at least one signal includes a second signal to control the power switch such that

the power switch is enabled to allow the switch current to flow through the power switch when the current controller is in the ON state,

the power switch is disabled to substantially prevent the switch current from flowing through the power switch when the current controller is in the OFF state, and

the power switch is disabled to substantially prevent the switch current from flowing through the power switch when the current controller is in the non-zero minimum current state.

29. The power converter of claim 28, wherein the main controller comprises:

a drive circuit coupled to generate the second signal to enable and disable the power switch in response to a feedback signal representative of the output of the power converter;

a phase detection circuit coupled to receive a input sense signal and to generate a phase angle signal in response thereto, wherein the phase angle signal is representative of a phase angle of an input voltage of the power converter; and

a linear control circuit coupled to generate the first signal to enable and disable the controlled current source in response to the phase angle signal.

30. The power converter of claim 29, when the linear control circuit enables the controlled current source, the controlled current is variable responsive to the phase angle of the input voltage.

31. The power converter of claim 30, wherein the controlled current increases with increases in the phase angle, such that the input current of the power converter is substantially constant.

32. The power converter of claim 25, wherein the controlled current source comprises a constant current source and a control switch coupled to selectively enable and disable the constant current source in response to the first signal.

33. The power converter of claim 32, wherein the control switch comprises a metal oxide semiconductor field effect transistor (MOSFET), and wherein the constant current source comprises a junction field effect transistor (JFET) having a base coupled to a common reference of the control circuit.

34. The power converter of claim 32, wherein the power switch comprises a metal oxide field effect transistor (MOSFET), and wherein the constant current source comprises a junction field effect transistor (JFET).

35. The power converter of claim 20, wherein the current controller comprises a transistor that, in response to the at least one signal, turns on to put the current controller in the ON state, turns off to put the current controller in the OFF state, and operates in a linear mode of operation to put the current controller in the non-zero minimum current state.

36. The power converter of claim 35, wherein the main controller comprises:
- a drive circuit coupled to generate the at least one signal to turn on and turn off the transistor in response to a feedback signal representative of the output of the power converter;
  - a phase detection circuit coupled to receive a input sense signal and to generate a phase angle signal in response thereto, wherein the phase angle signal is representative of a phase angle of an input voltage of the power converter; and
  - a linear control circuit coupled to provide the drive circuit with a linear control signal to control the transistor in the linear mode of operation in response to the phase angle signal.
37. The power converter of claim 35, wherein the transistor is configured to provide a constant non-zero current in response to the at least one signal when current controller is in the non-zero minimum current state.
38. The power converter of claim 35, wherein the transistor is configured to provide a variable current that is responsive to the phase angle of the input voltage when the current controller is in the non-zero minimum current state.
39. A main controller for use in a power converter, the main controller comprising:
- a drive circuit coupled to generate a drive signal in response to a feedback signal representative of the output of the power converter, the drive signal to be provided to control a power switch of a current controller of the power converter in a first mode and a second mode;
  - a phase detection circuit coupled to receive an input sense signal and to generate a phase angle signal in response thereto, wherein the phase angle signal is representative of a phase angle of an input voltage of the power converter; and
  - a linear control circuit coupled to generate a linear control signal which controls a controlled current source of the current controller of the power converter in response to the phase angle signal, wherein the linear control signal controls the

controlled current source in the second mode of operation, wherein the current controller is controlled in the first mode when the phase angle is less than a phase angle threshold and wherein the current controller is controlled in the second mode when the phase angle is greater than the phase angle threshold.

40. The main controller of claim 39, wherein the current controller is controlled in a first state and a second state, wherein the drive signal controls the power switch such that the first state the current controller is in an ON state and the second state the current controller is in an OFF state in the first mode of operation.

41. The main controller of claim 39, wherein the current controller is controlled in a first state and a second state, wherein the drive signal controls the power switch and the linear control circuit controls the controlled current source such that the first state the current controller is an ON state and the second state the power switch is a non-zero minimum current state in the second mode of operation.

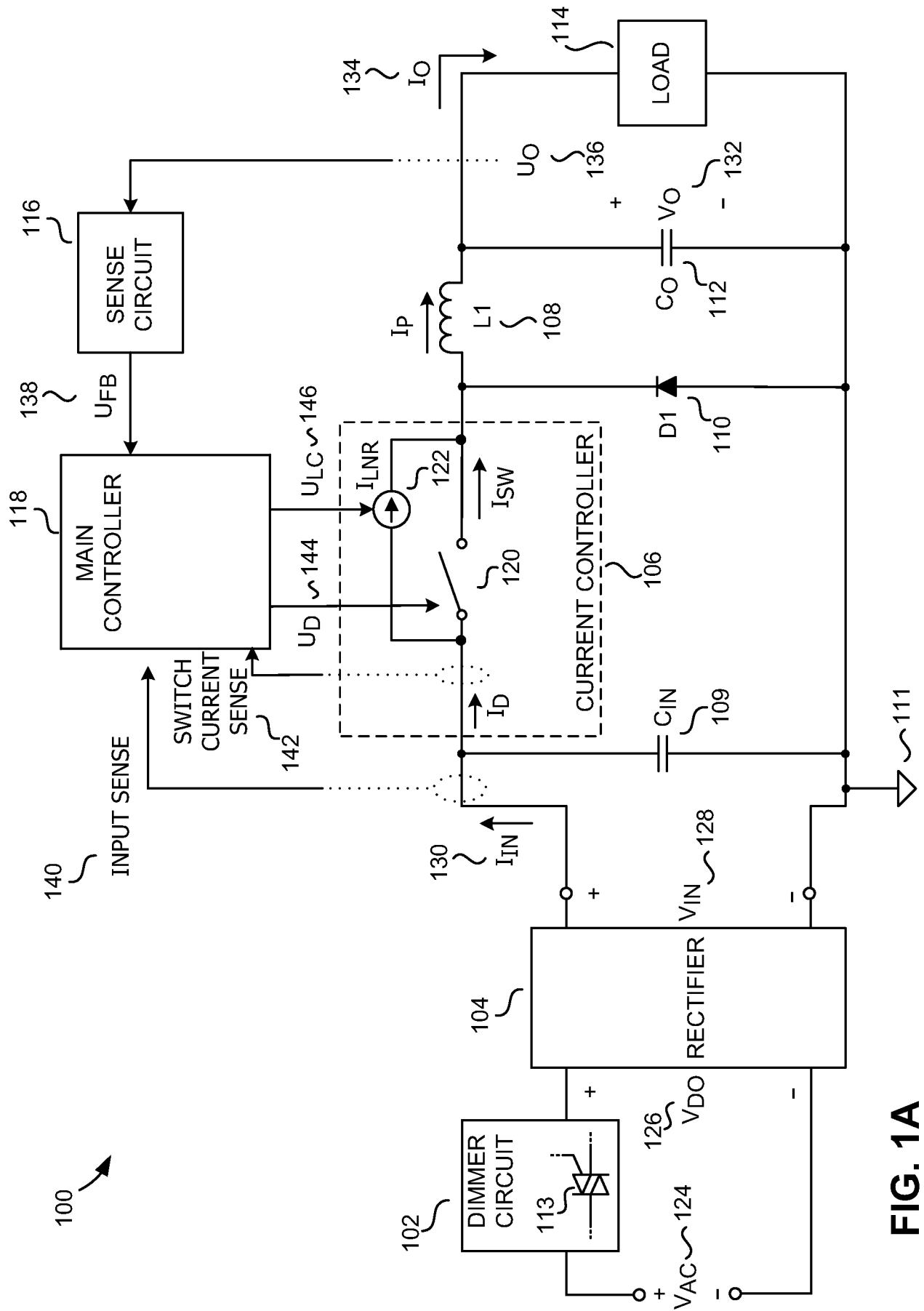


**FIG. 1A**

2/14

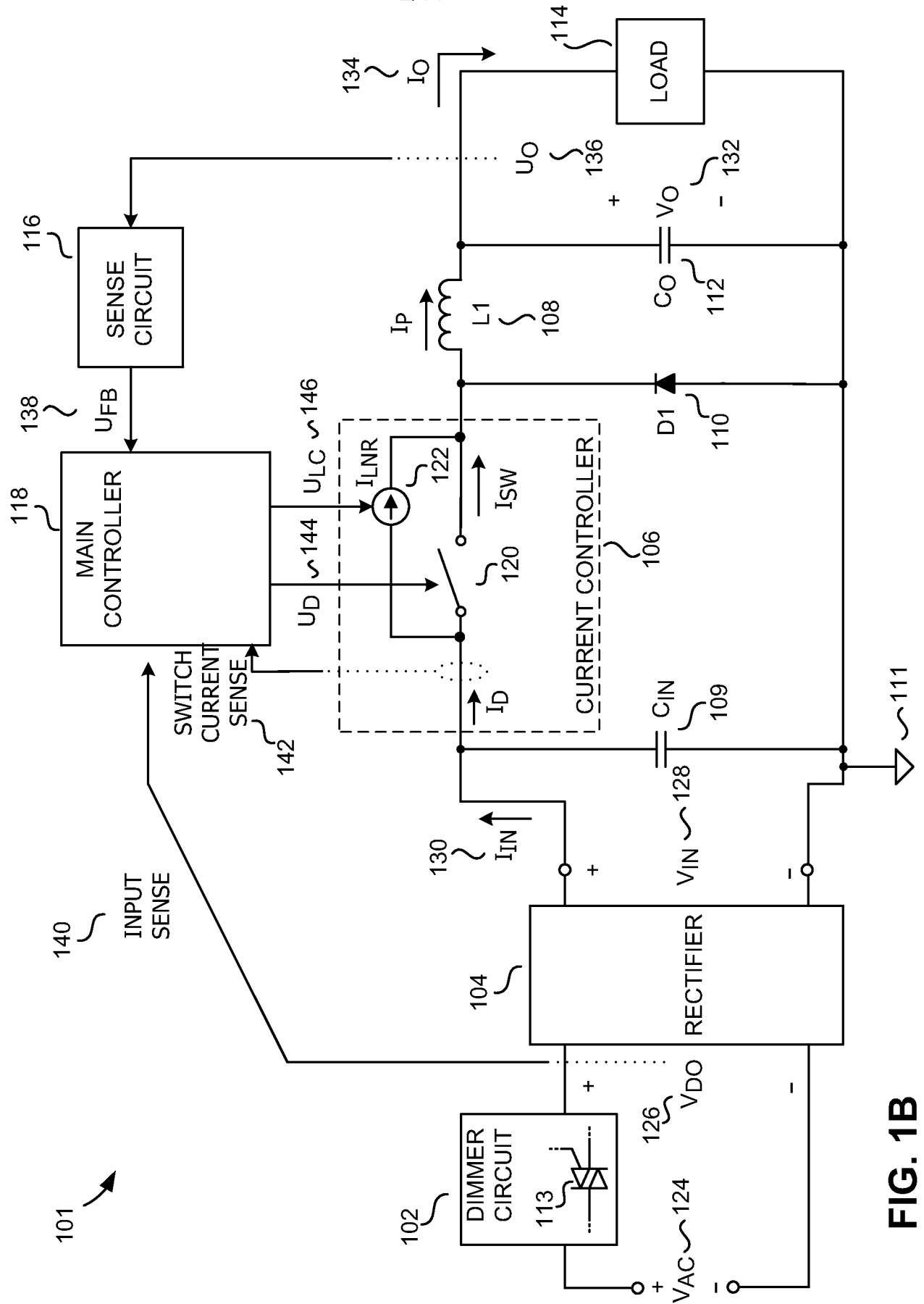


FIG. 1B

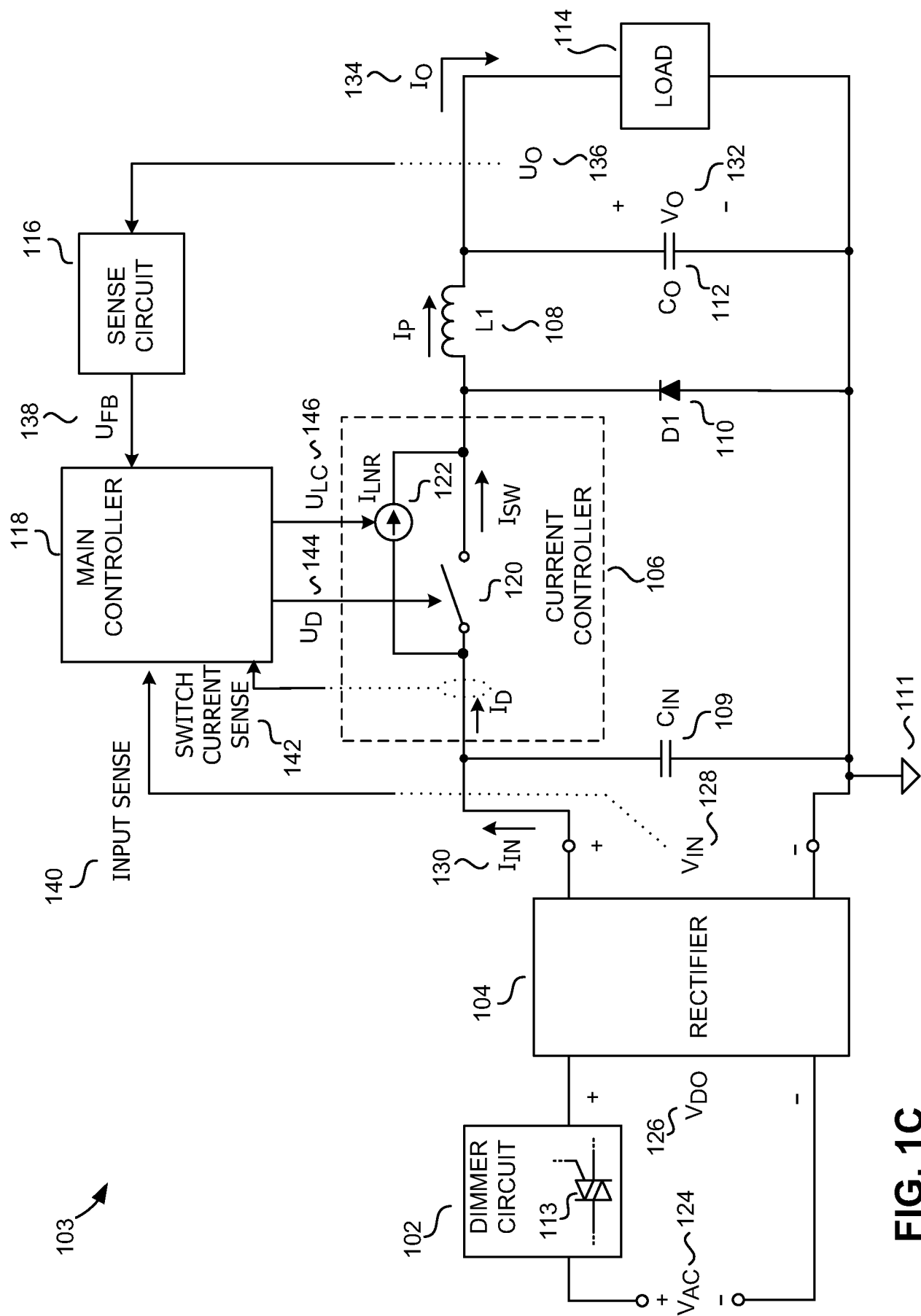


FIG. 1C

4/14

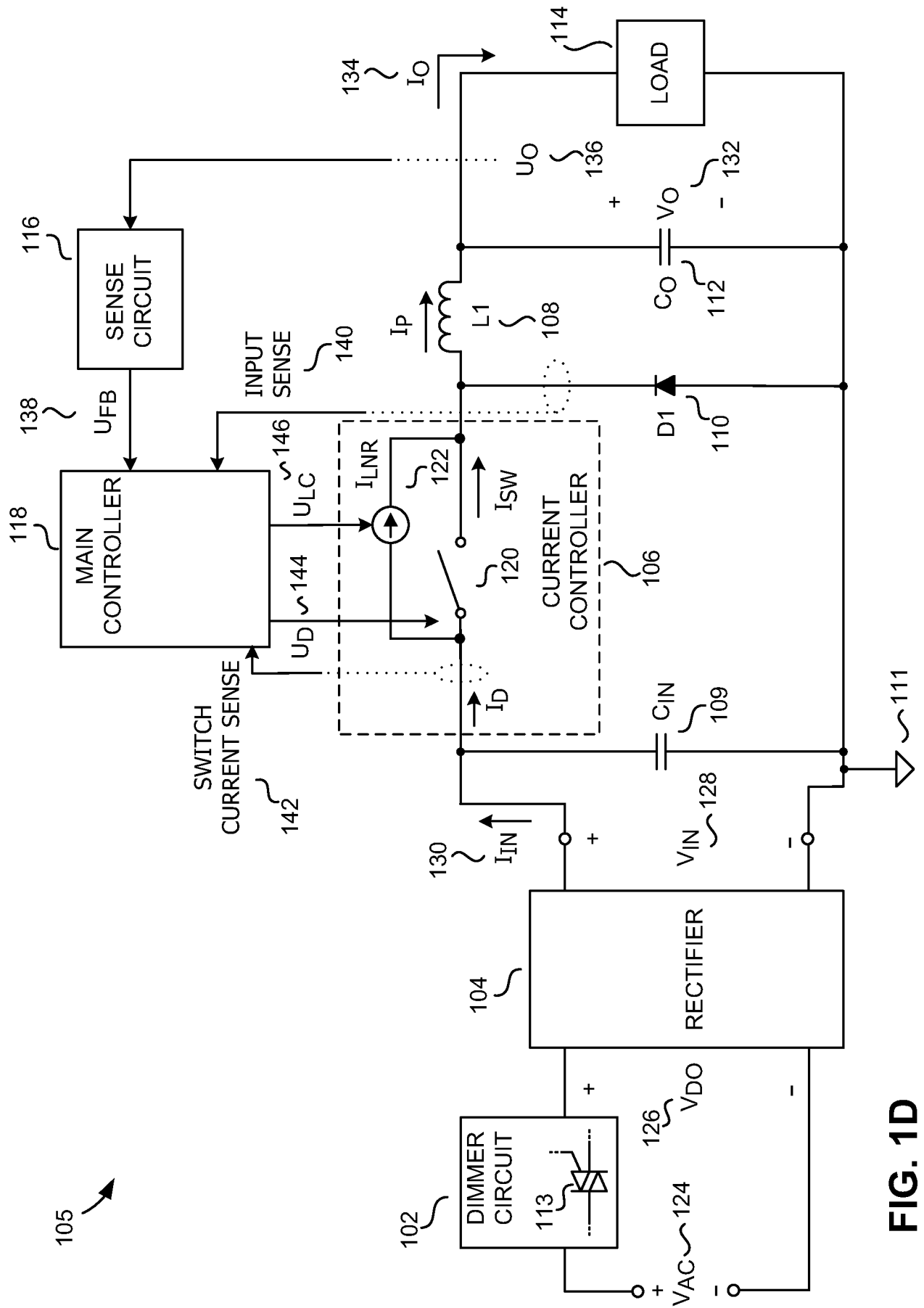


FIG. 1D

5/14

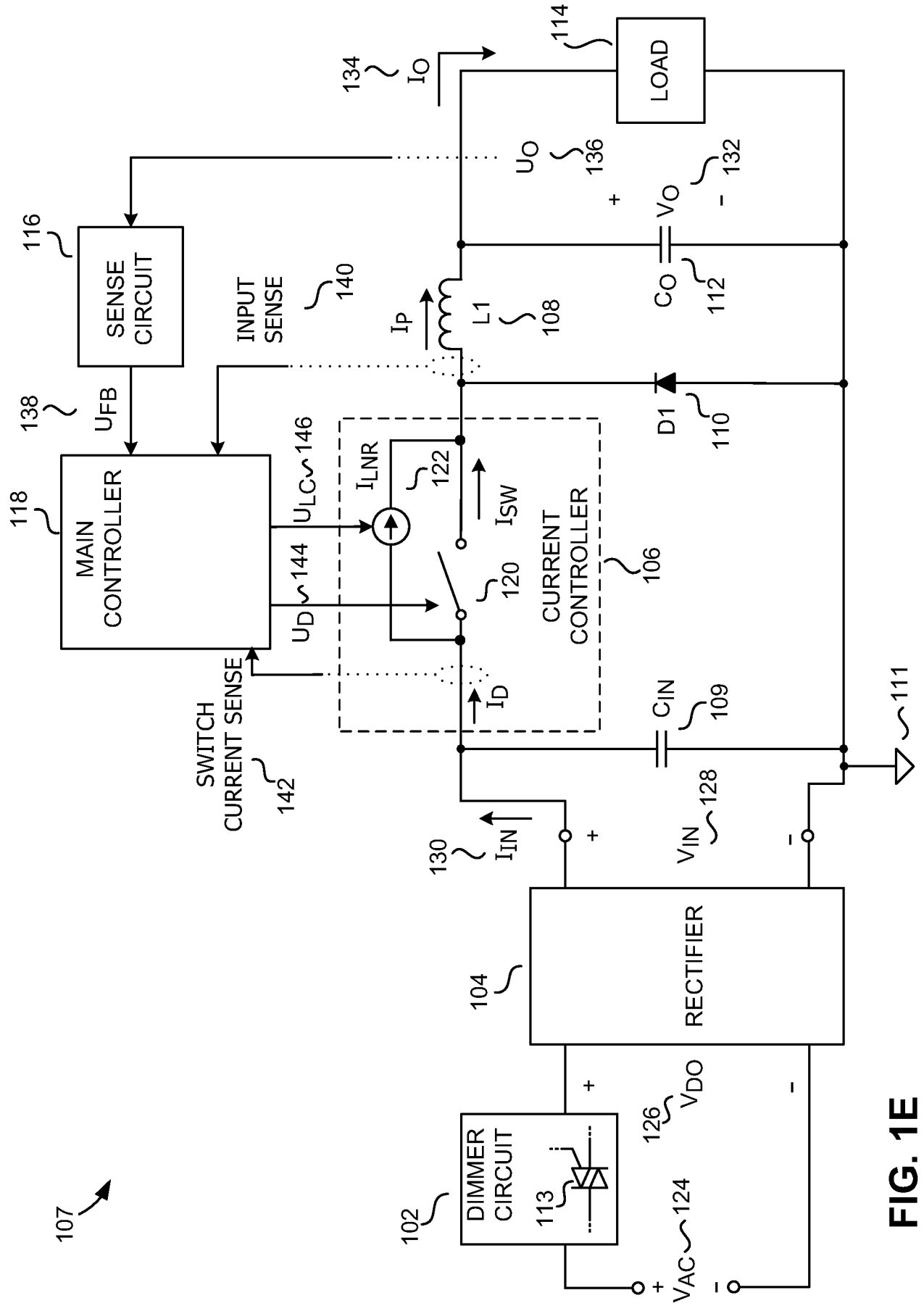


FIG. 1E

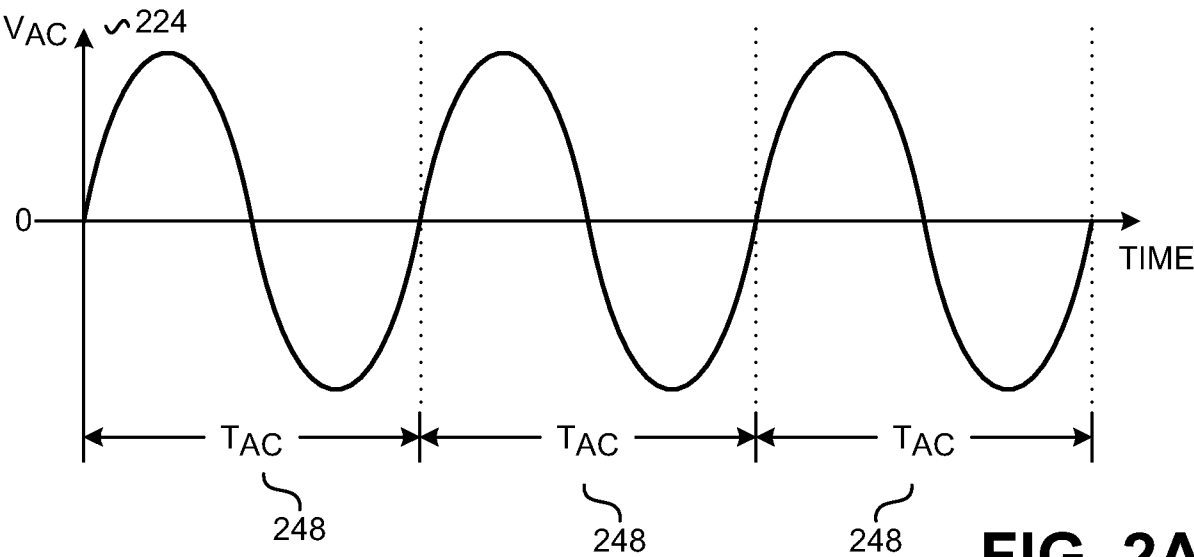


FIG. 2A

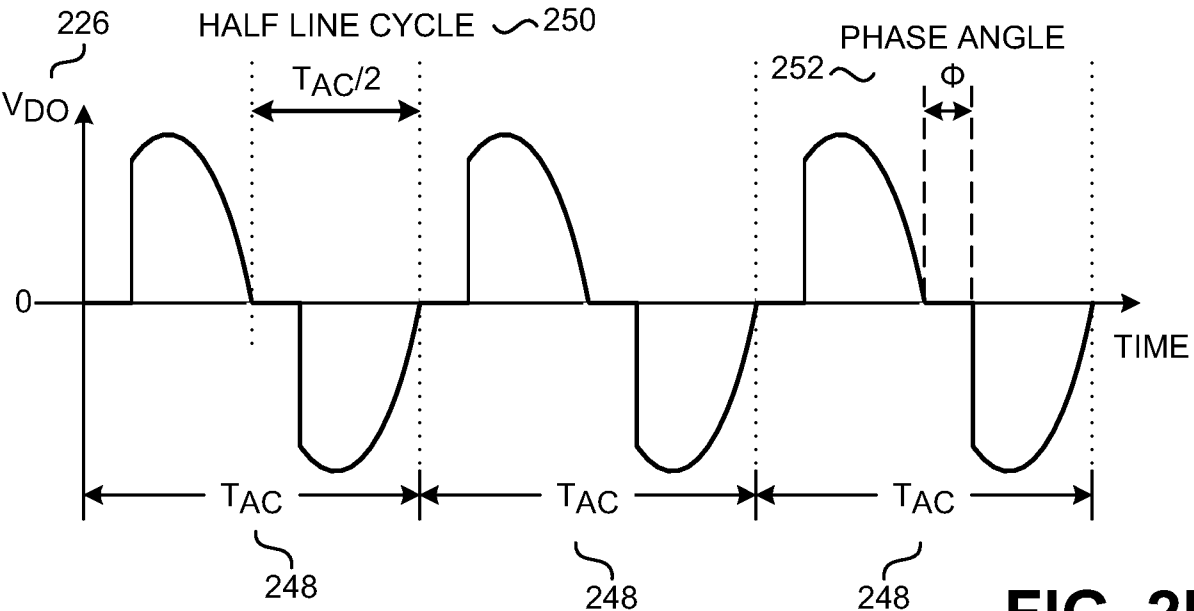


FIG. 2B

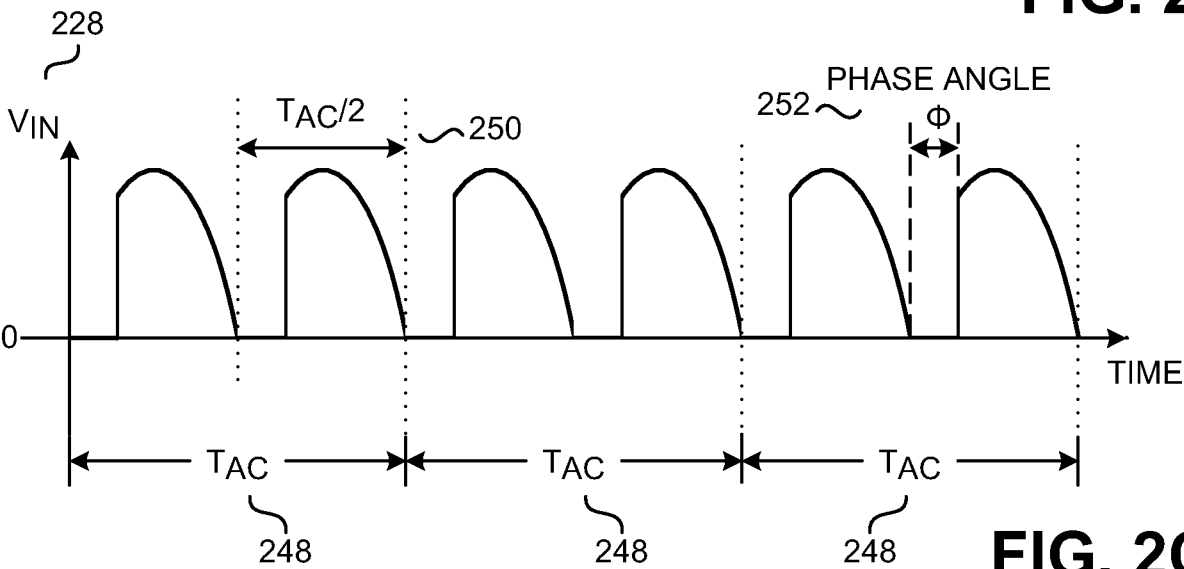


FIG. 2C

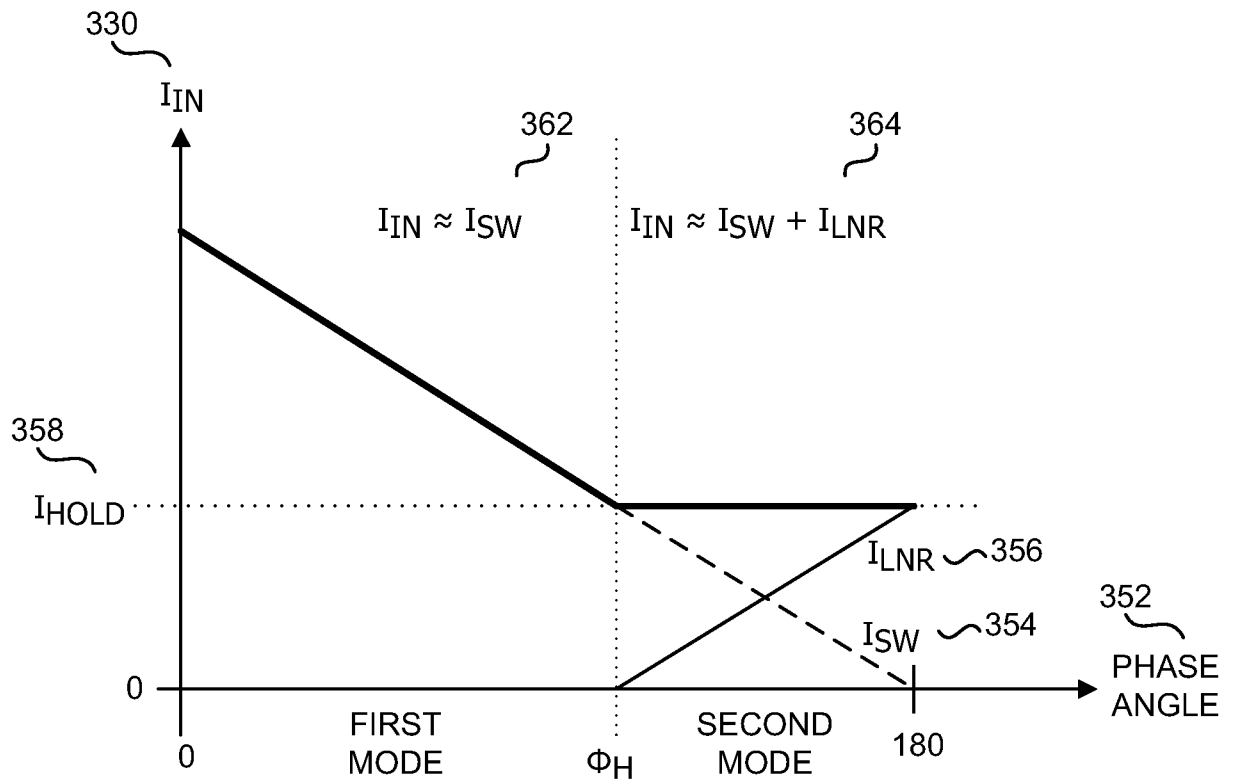


**FIG. 3A**

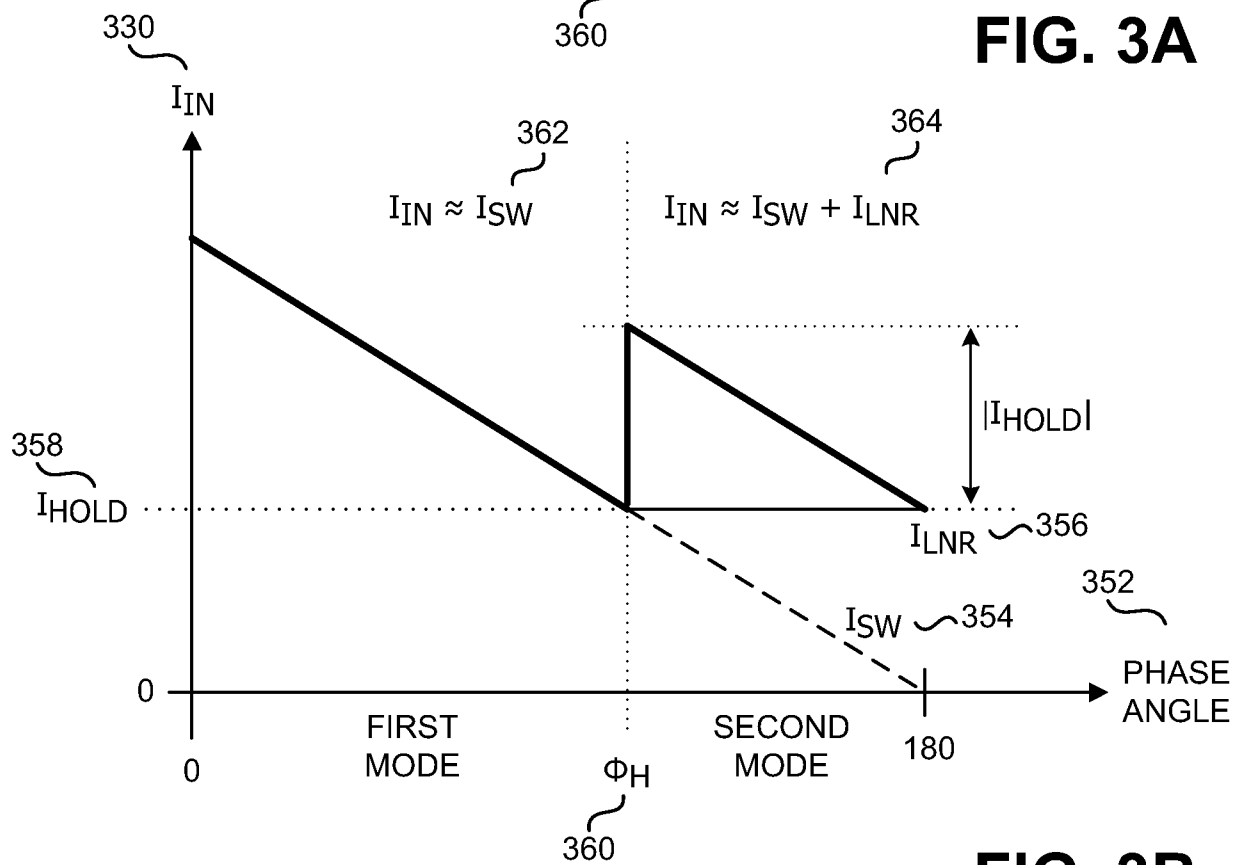
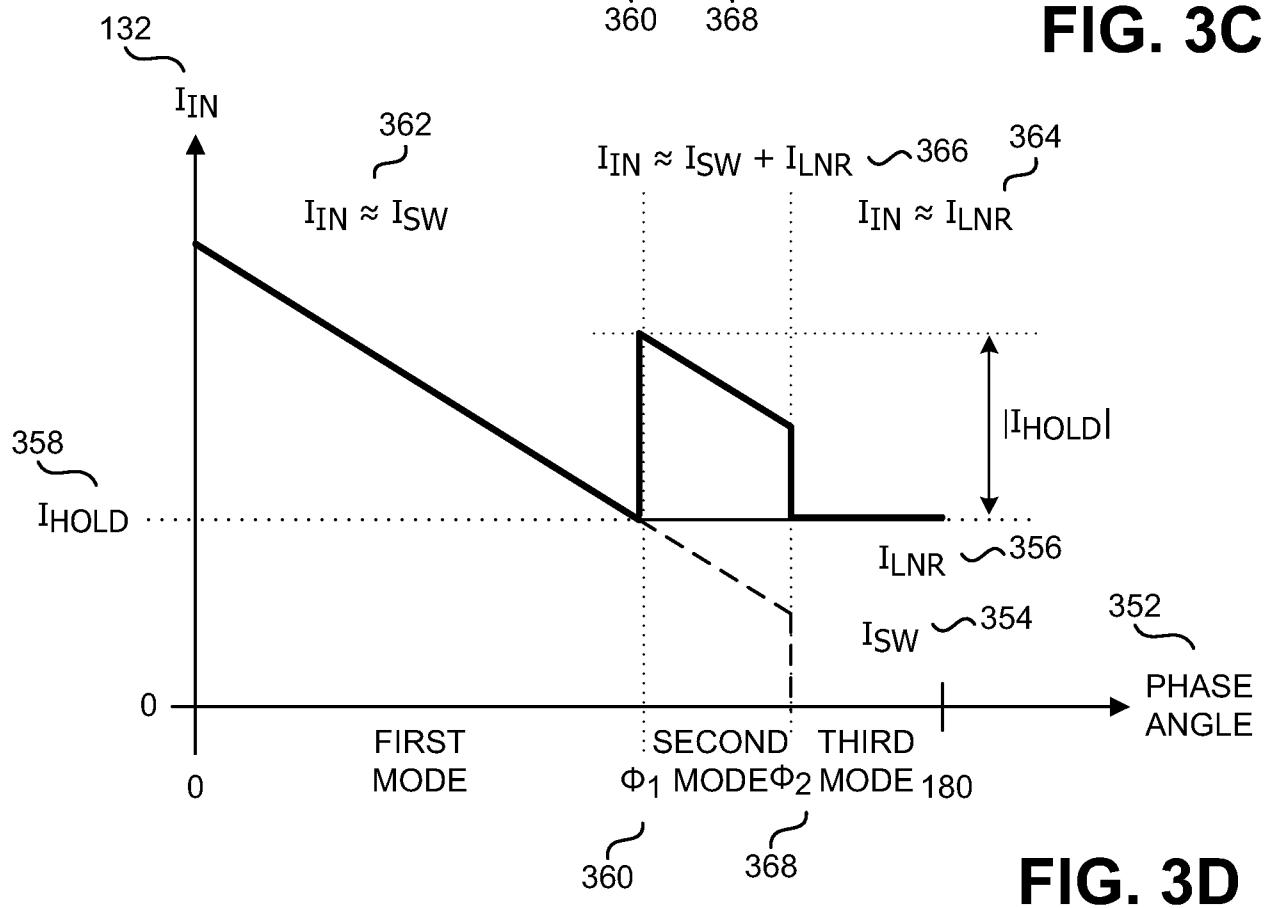
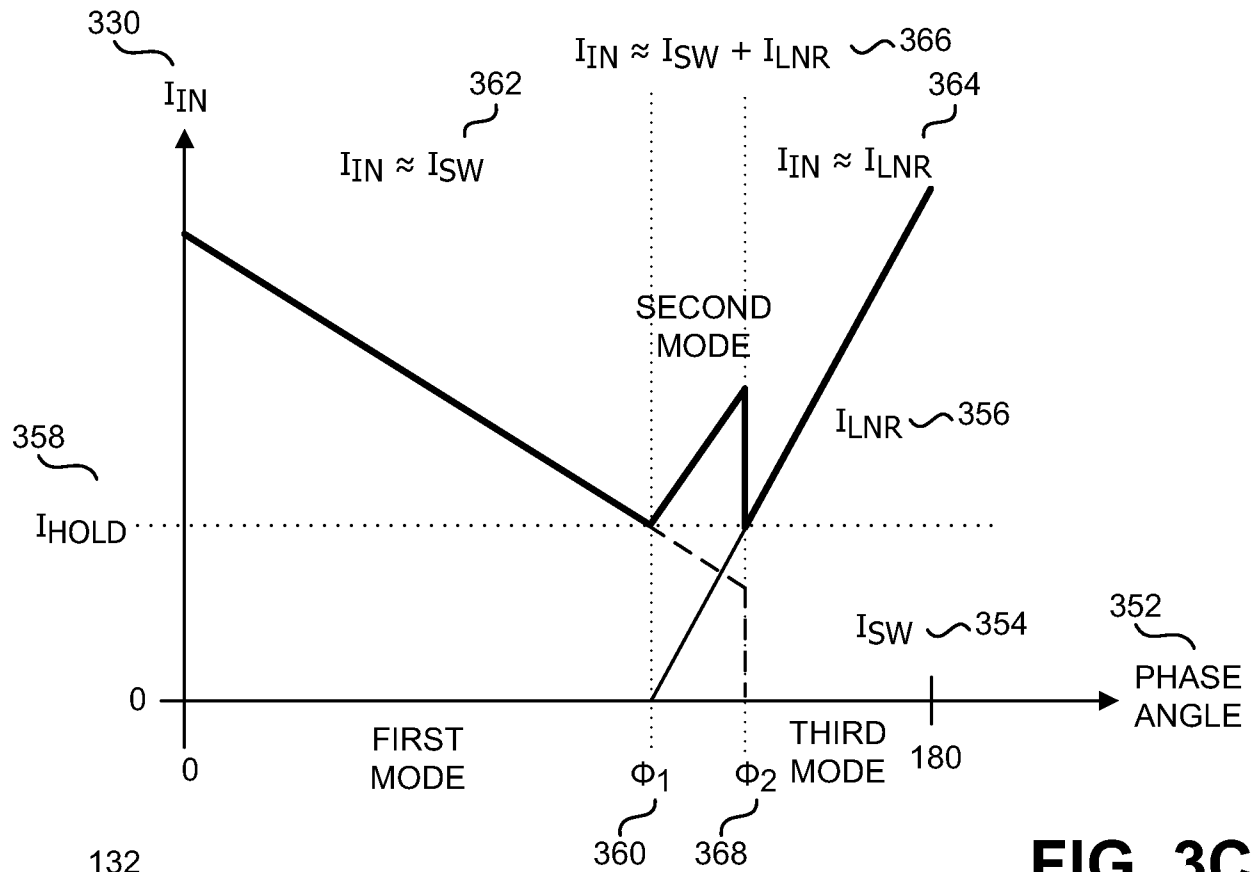
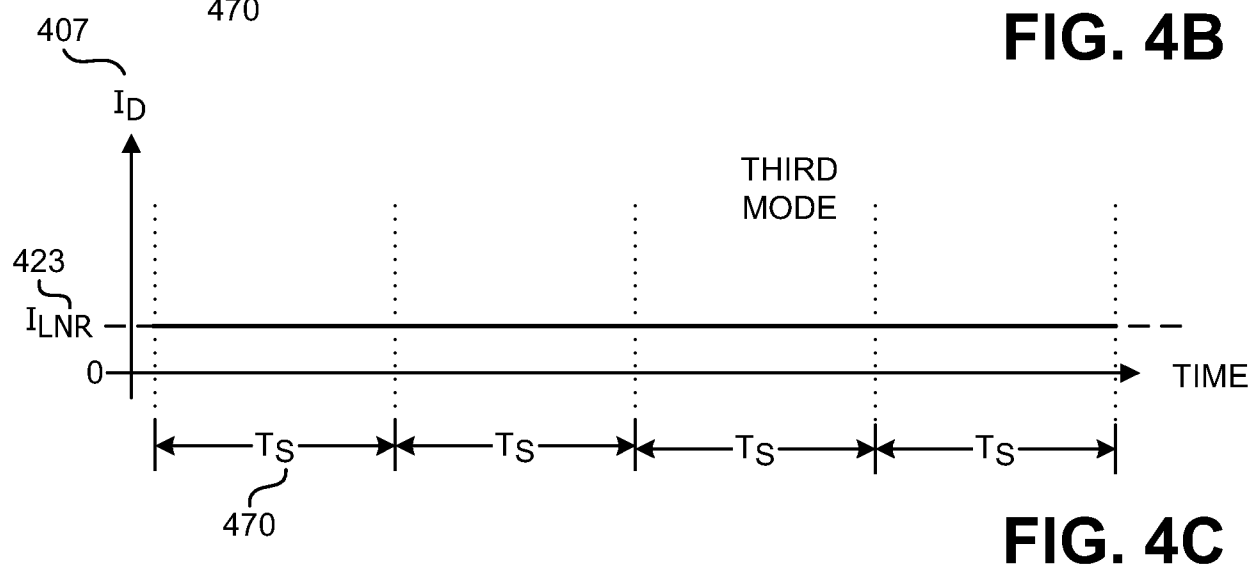
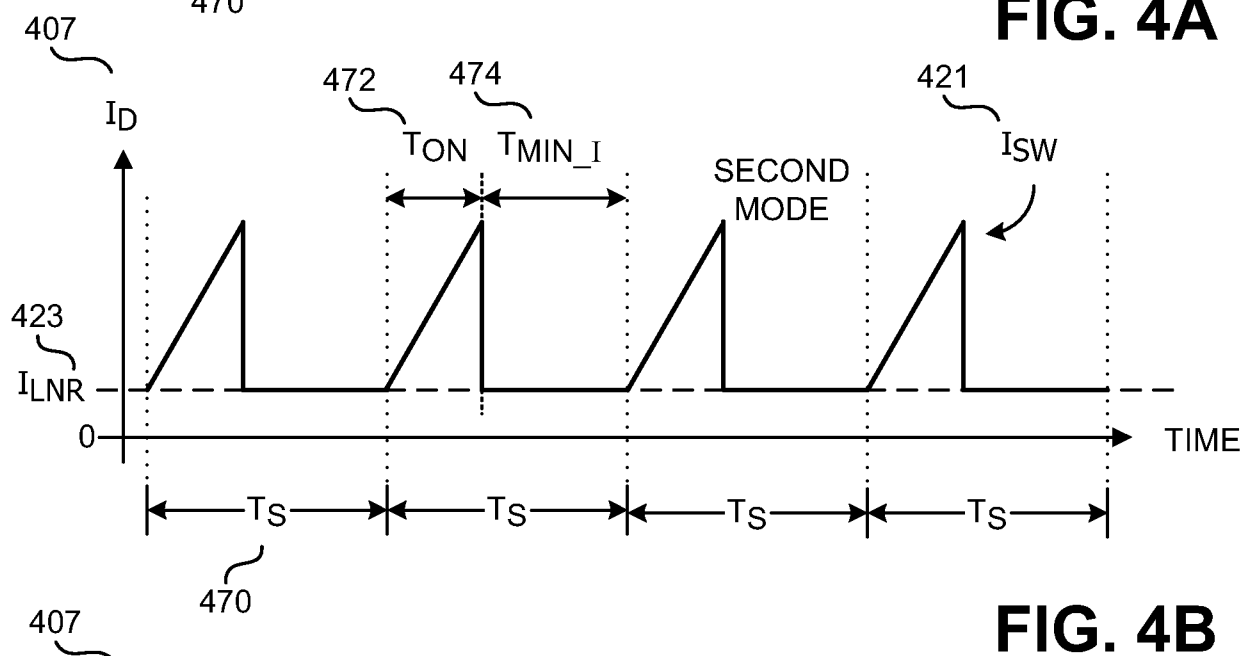
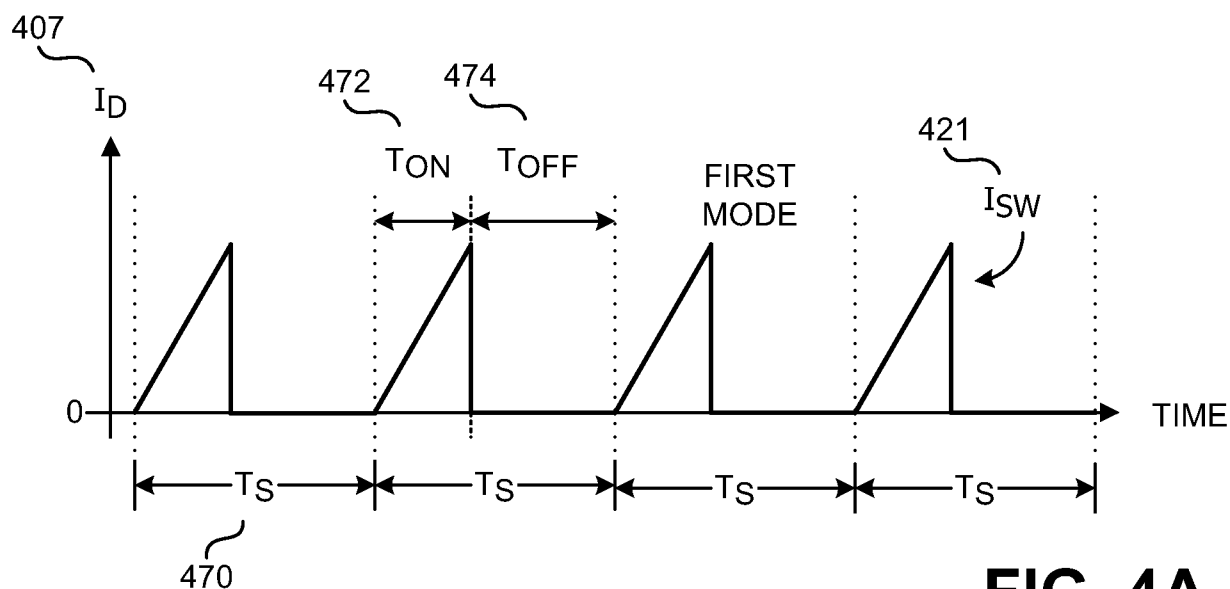


**FIG. 3B**





10/14

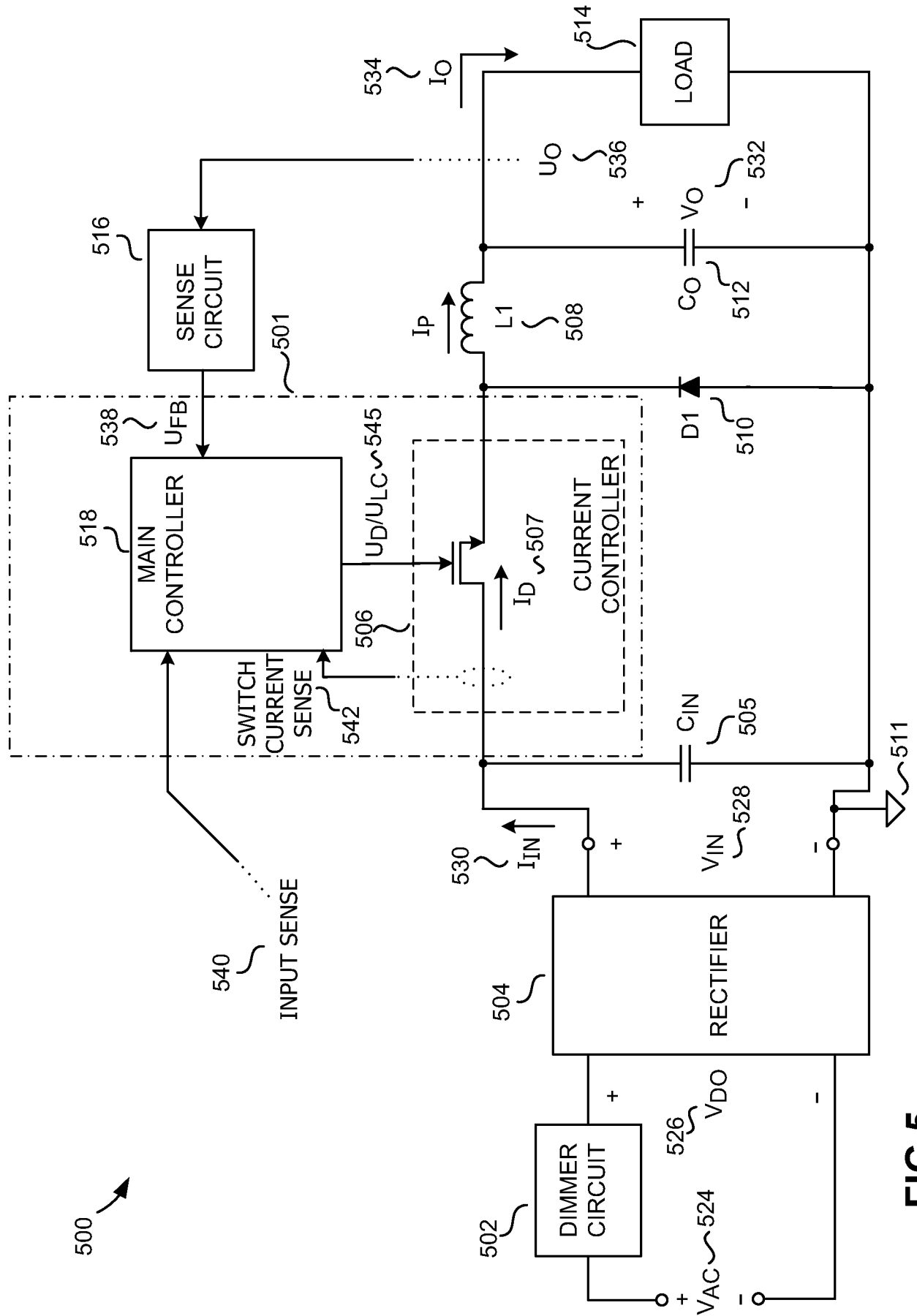


FIG.5

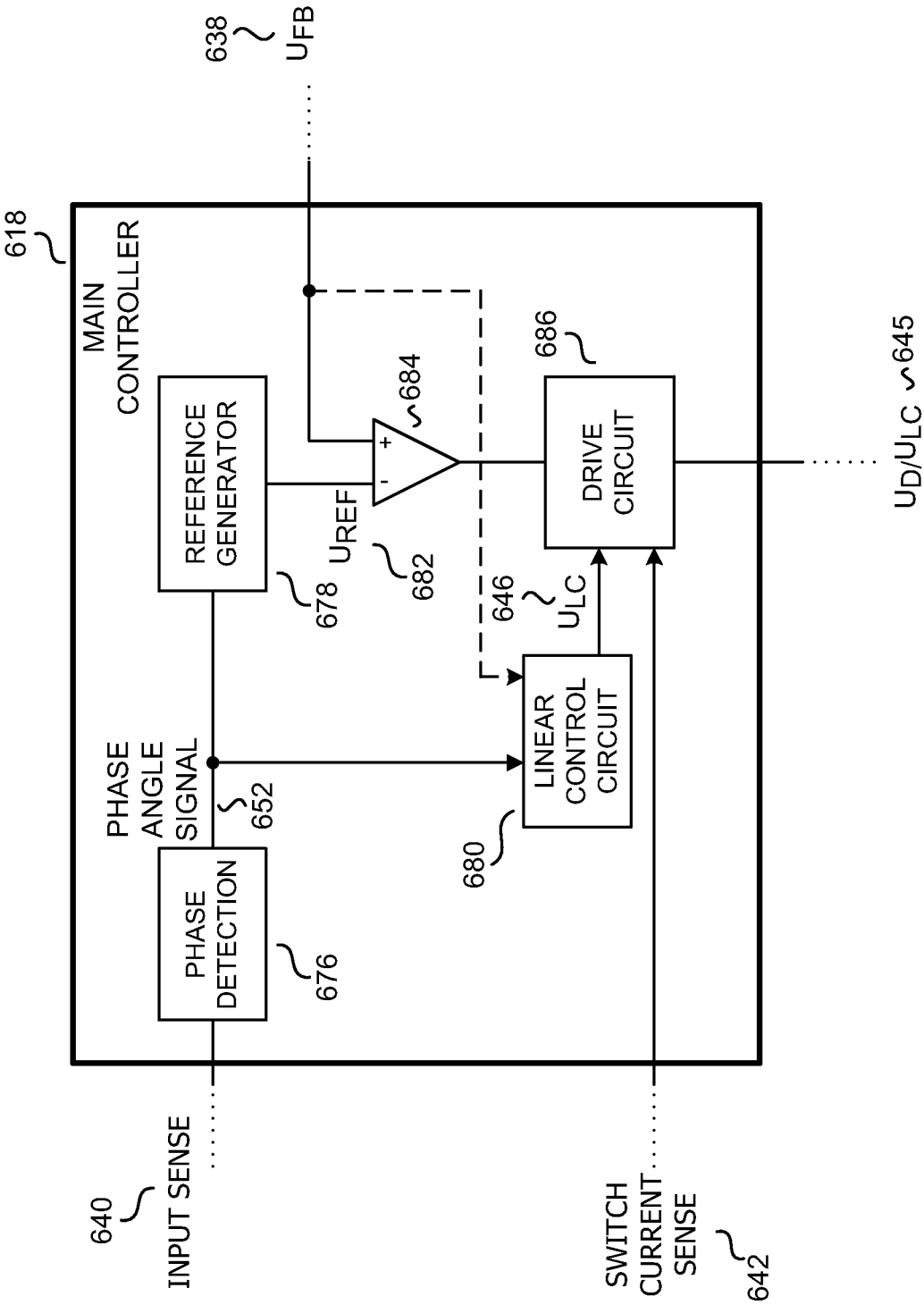


FIG.6

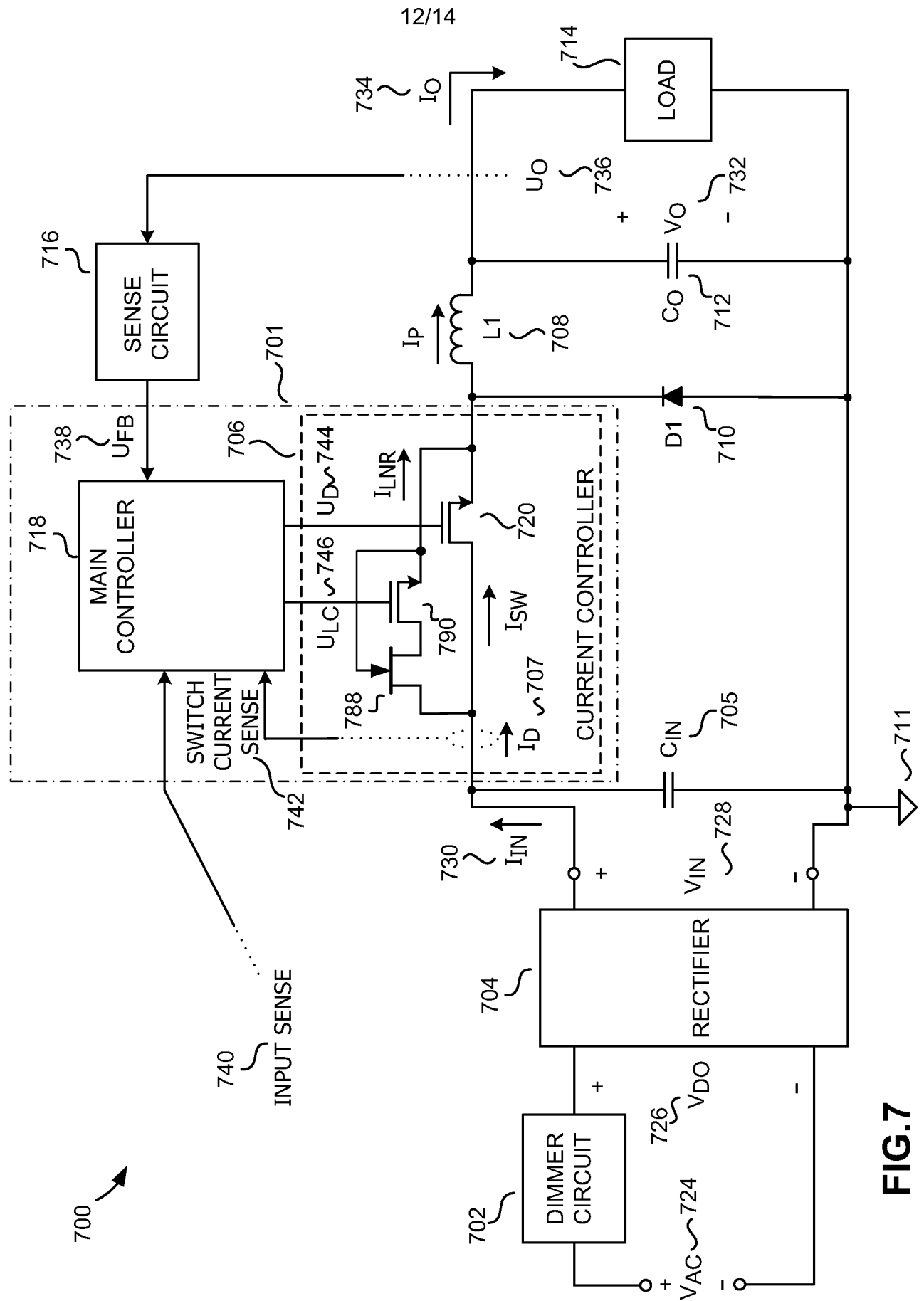


**FIG. 7**

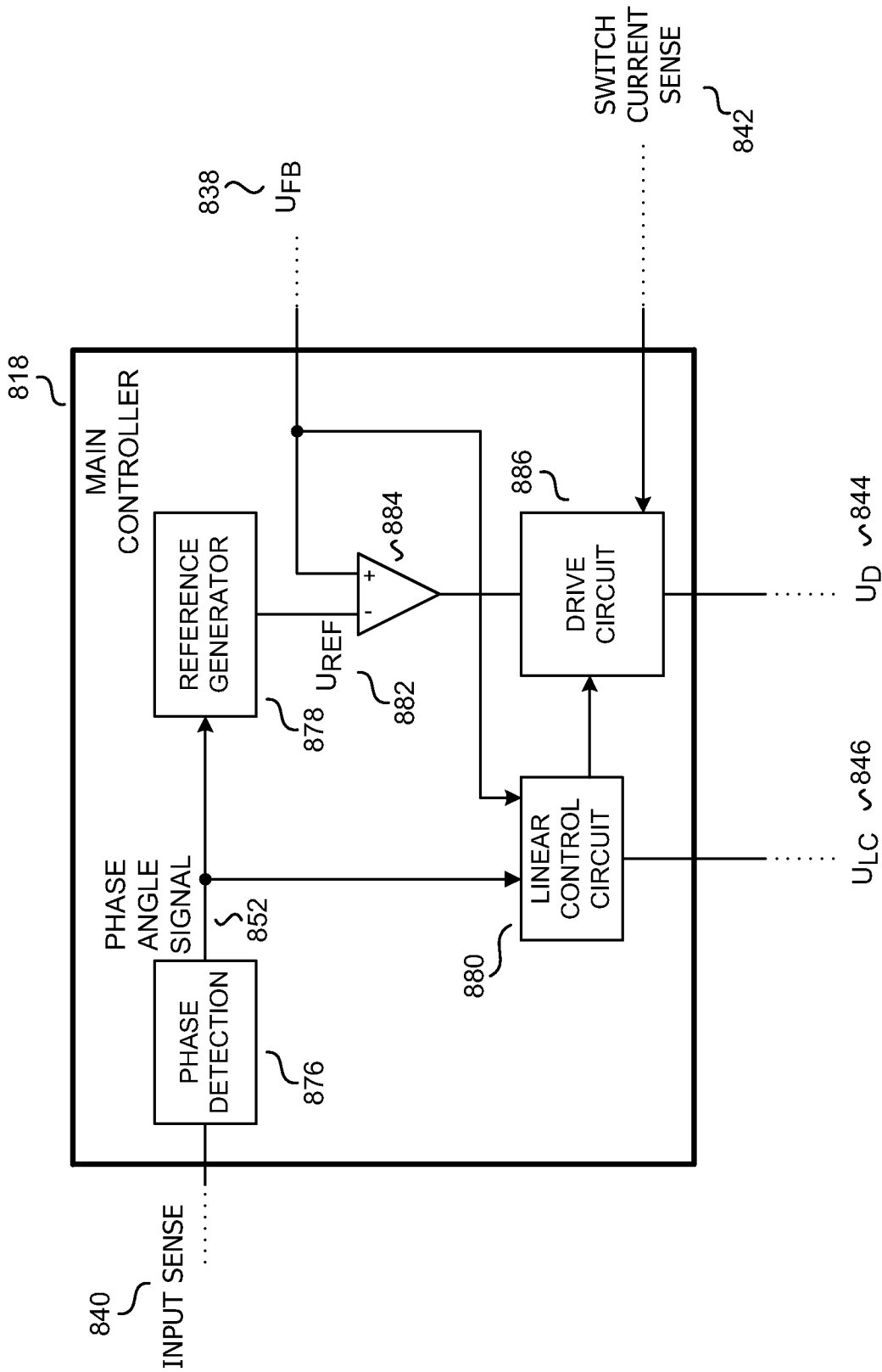


FIG.8

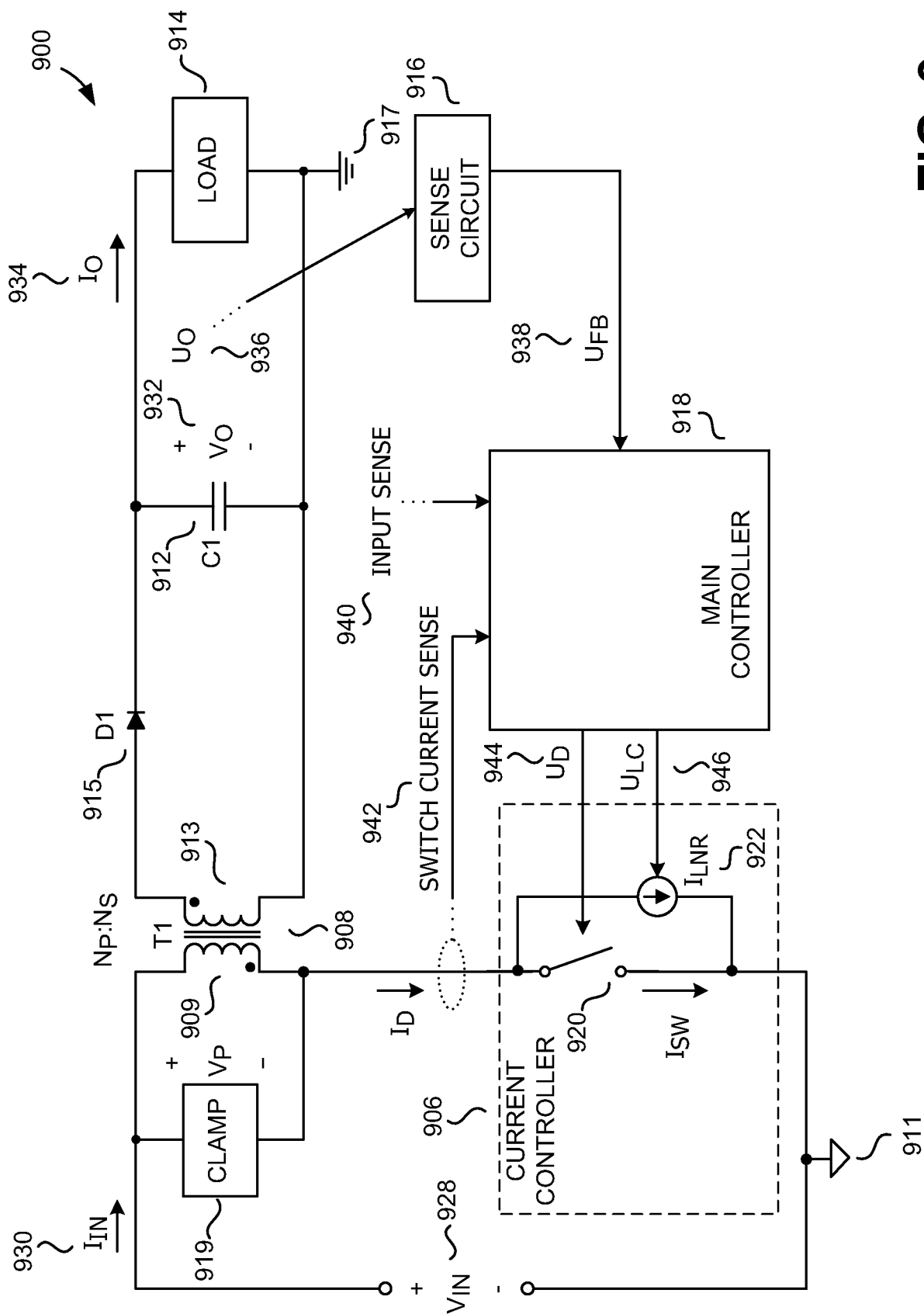


FIG. 9

## INTERNATIONAL SEARCH REPORT

International application No.  
**PCT/US2014/023741****A. CLASSIFICATION OF SUBJECT MATTER****H05B 37/02(2006.01)i, H05B 33/08(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

H05B 37/02; H05B 39/04; H05B 41/16; H05B 33/08

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) &amp; Keywords: converter, mode, dimmer, current, controller

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                                                                            | Relevant to claim No. |
|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| Y         | US 2012-0280629 A1 (YURY GAKNOKI et al.) 08 November 2012<br>See paragraphs [0006], [0027], [0029], [0033]-[0036], [0042], [0051]-[0053], [0062]; claims 1, 18; and figure 1. | 1-41                  |
| Y         | WO 2011-042510 A2 (LEMNIS LIGHTING PATENT HOLDING B.V.) 14 April 2011<br>See paragraphs [0012], [0049], [0054], [0061], [0064]; and figure 3.                                 | 1-41                  |
| A         | US 2011-0241557 A1 (MIROSLAW MAREK GROTKOWSKI et al.) 06 October 2011<br>See paragraphs [0003], [0009], [0063]; and figure 1A.                                                | 1-41                  |
| A         | US 2008-0018261 A1 (MARK ALLEN KASTNER) 24 January 2008<br>See paragraphs [0003], [0009], [0013]; and figure 4.                                                               | 1-41                  |
| A         | US 2013-0049622 A1 (CHRISTIAN PURA ANGELES) 28 February 2013<br>See paragraphs [0002], [0004]; and figure 1.                                                                  | 1-41                  |



Further documents are listed in the continuation of Box C.



See patent family annex.

\* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&amp;" document member of the same patent family

Date of the actual completion of the international search

26 May 2014 (26.05.2014)

Date of mailing of the international search report

**26 May 2014 (26.05.2014)**

Name and mailing address of the ISA/KR

International Application Division  
Korean Intellectual Property Office  
189 Cheongsu-ro, Seo-gu, Daejeon Metropolitan City, 302-701,  
Republic of Korea

Facsimile No. +82-42-472-7140

Authorized officer

JEONG, So Yeon

Telephone No. +82-42-481-5656



**INTERNATIONAL SEARCH REPORT**

Information on patent family members

International application No.

**PCT/US2014/023741**

| Patent document<br>cited in search report | Publication<br>date | Patent family<br>member(s)                                                                                                                             | Publication<br>date                                                                                          |
|-------------------------------------------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------|
| US 2012-0280629 A1                        | 08/11/2012          | CN 102291871 A<br>EP 2381742 A2<br>EP 2381742 A3<br>JP 2011-228305 A<br>US 2011-254525 A1<br>US 2014-049241 A1<br>US 8242766 B2<br>US 8593129 B2       | 21/12/2011<br>26/10/2011<br>16/11/2011<br>10/11/2011<br>20/10/2011<br>20/02/2014<br>14/08/2012<br>26/11/2013 |
| WO 2011-042510 A2                         | 14/04/2011          | CN 102648664 A<br>EP 2486776 A2<br>GB 201016908 D0<br>GB 2475127 A<br>JP 2013-507729 A<br>KR 10-2012-0082912 A<br>TW 2011-29253 A<br>WO 2011-042510 A3 | 22/08/2012<br>15/08/2012<br>24/11/2010<br>11/05/2011<br>04/03/2013<br>24/07/2012<br>16/08/2011<br>02/02/2012 |
| US 2011-0241557 A1                        | 06/10/2011          | CN 102577624 A<br>EP 2494851 A1<br>US 2011-266974 A1<br>US 8283875 B2<br>US 8339066 B2<br>WO 2011-050453 A1                                            | 11/07/2012<br>05/09/2012<br>03/11/2011<br>09/10/2012<br>25/12/2012<br>05/05/2011                             |
| US 2008-0018261 A1                        | 24/01/2008          | None                                                                                                                                                   |                                                                                                              |
| US 2013-0049622 A1                        | 28/02/2013          | None                                                                                                                                                   |                                                                                                              |