



(51) International Patent Classification:

H01L 21/8238 (2006.01) *H01L 29/66* (2006.01)
H01L 29/417 (2006.01)

(21) International Application Number:

PCT/US2017/027218

(22) International Filing Date:

12 April 2017 (12.04.2017)

(25) Filing Language:

English

(26) Publication Language:

English

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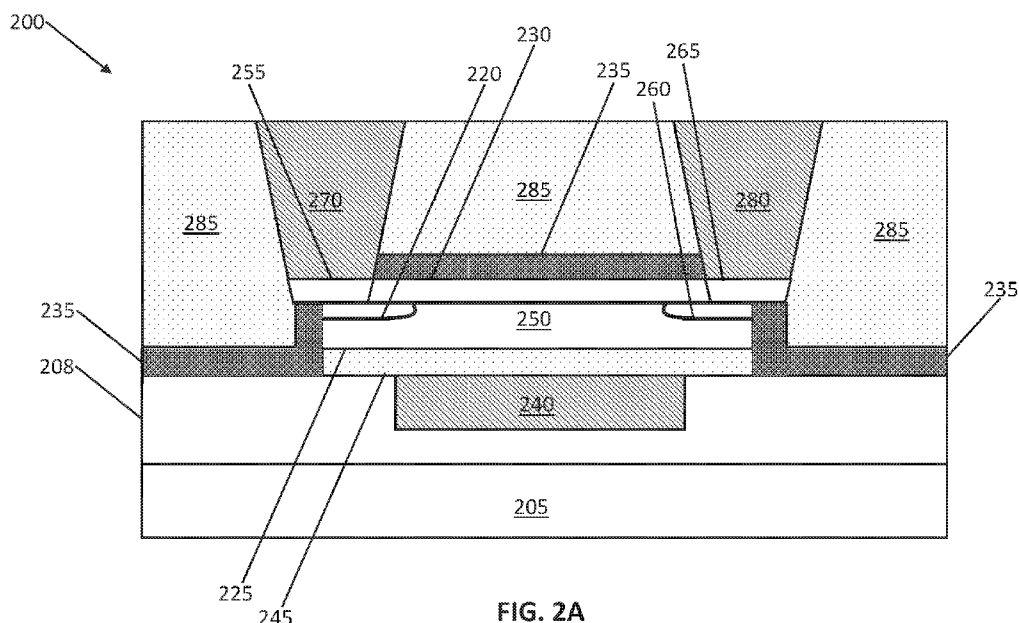
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(81) Designated States (*unless otherwise indicated, for every
kind of national protection available*): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ,
CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO,
DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN,
HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KH, KN, KP, KR,
KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG,
MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM,
PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC,

(54) Title: SEMICONDUCTING OXIDE DEVICE SOURCE AND DRAIN CONTACTS



(57) Abstract: Techniques are disclosed for forming semiconductor integrated circuits including interface layers between a conductive contact and doped semiconducting oxide source and drain regions that reduce contact resistance between the conductive contact and the doped semiconducting oxide source and drain regions. The interface layers include a material non-reactive with the semiconducting oxide, or an oxygen-gettering material to create oxygen-deficient defects in the doped semiconducting oxide source and drain regions that pin the Fermi level and reduce the Schottky barrier height, thereby reducing contact resistance. The semiconducting oxide channel can be formed of at least two semiconducting oxides, and the interface layers can include a layer between the conductive contact and the oxygen-gettering material, the layer comprising a segregation material that forms an alloy with metal of the semiconducting oxide of the at least two semiconducting oxides having a highest energy conduction band, further reducing the Schottky barrier height.

SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR,
TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

SEMICONDUCTING OXIDE DEVICE SOURCE AND DRAIN CONTACTS**BACKGROUND**

Increased performance of circuit devices including transistors, diodes, resistors, capacitors, and other passive and active electronic devices formed on a semiconductor substrate is typically a major factor considered during design, manufacture, and operation of those devices. For example, during design and manufacture or forming of metal oxide semiconductor (MOS) transistor semiconductor devices, such as those used in a complementary metal oxide semiconductor (CMOS), it is often desired to increase movement of electrons in N-type MOS device (NMOS) and P-type MOS device (PMOS) and contact regions. Such increased mobility can be achieved by reducing contact resistance.

At the contact regions of the source and drain, a conductive material is deposited on the doped surface, providing contacts. The interaction between the conductive material and the doped surface produces a semiconductor junction. The resulting semiconductor junction is characterized by a Schottky barrier height between the conduction band and the Fermi level. Conduction of electrons through the Schottky barrier is limited by the barrier height and results in contact resistance.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagram illustrating resistance components of a standard MOS device.

FIG. 2A illustrates a semiconducting oxide device including interface layers non-reactive with the semiconducting oxide layer between the source and drain metal contacts and the source and drain regions, respectively, according to an embodiment of this disclosure.

FIG. 2B illustrates a semiconducting oxide device including interface layers non-reactive with the semiconducting oxide layer between the source and drain metal contacts and the source and drain regions, respectively, according to another embodiment of this disclosure.

FIG. 3A illustrates a semiconducting oxide device including oxygen-gettering interface layers between the source and drain metal contacts and the source and drain regions, respectively, according to another embodiment of this disclosure.

FIG. 3B illustrates a semiconducting oxide device including oxygen-gettering interface layers and optional segregation interface layers between the source and drain metal contacts and

the source and drain regions, respectively, according to yet another embodiment of this disclosure.

FIG. 3C illustrates a semiconducting oxide device including the oxygen-gettering interface layers and optional segregation interface layers between the source and drain metal contacts and the source and drain regions, respectively, according to still another embodiment of this disclosure.

FIG. 4A is a method for forming a semiconducting oxide device including interface layers non-reactive with the semiconducting oxide layer, according to an embodiment of this disclosure.

FIG. 4B is a method for forming a semiconducting oxide device including oxygen-gettering interface layers, according to another embodiment of this disclosure.

FIGS. 5A to 5F illustrate structures that are formed when carrying out the method of FIG. 4A or FIG. 4B, in accordance to embodiments of this disclosure.

FIGS. 5G-1 and 5H-1 illustrate structures that are formed when carrying out the method of FIG. 4A, in accordance to an embodiment of this disclosure.

FIGS. 5G-2A, 5G-2B, and 5H-2 illustrate structures that are formed when carrying out the method of FIG. 4B, in accordance to an embodiment of this disclosure.

FIG. 6 illustrates methods for forming a semiconducting oxide device including interface layers non-reactive with the semiconducting oxide layer or oxygen-gettering interface layers, but with a top-gate configuration, according to another embodiment of this disclosure.

FIGS. 7A to 7D illustrate structures that are formed when carrying out the method of FIG. 6, in accordance to an embodiment of this disclosure.

FIG. 8A is a graph of carbide to oxide reaction energy (kJ/mol) as a function of carbide work function (WF).

FIG. 8B is a graph of free energy of oxidation (kJ/mol) as a function of work function (eV).

FIGS. 8C(a)-(d) are illustrations of changes in bandgap of semiconducting oxides in accordance to an embodiment of this disclosure.

FIG. 8D is a plot of bandgap energy (eV) and charge neutrality level (eV) for several semiconducting oxides and silicon.

FIG. 9 is a depiction of a computing system configured according to an embodiment of this disclosure.

FIG. 10A is a phase diagram of temperature as a function of atomic % of cobalt (Co) and indium (In).

FIG. 10B is a phase diagram of temperature as a function of atomic % of cobalt (Co) and gallium (Ga).

The figures depict various embodiments of the present disclosure for purposes of illustration only. In the drawings, each identical or nearly identical component that is illustrated in various figures may be represented by a like numeral. For purposes of clarity, not every component may be labeled in every drawing. As will be appreciated, the figures are not necessarily drawn to scale or intended to limit the present disclosure to the specific configurations shown. For instance, while some figures generally indicate straight lines, right angles, and smooth surfaces, an actual implementation of a transistor structure may have less than perfect straight lines, right angles, and some features may have surface topology or otherwise be non-smooth, given real world limitations of the processing equipment and techniques used. In short, the figures are provided merely to show example structures. Numerous variations, configurations, and other embodiments will be apparent from the following detailed discussion.

DETAILED DESCRIPTION

Techniques are disclosed for forming semiconductor integrated circuits including interface layers between a conductive contact and doped semiconducting oxide source and drain regions that reduce contact resistance between the conductive contact and the doped semiconducting oxide source and drain regions. In some embodiments of the present disclosure, this reduction in contact resistance is accomplished by an interface layer comprising a material non-reactive with the semiconducting oxide, between the source/drain contact and the corresponding source/drain region. In other embodiments of the present disclosure, this reduction in contact resistance is accomplished by an interface layer comprising an oxygen-gettering material that creates oxygen-deficient defects in the doped semiconducting oxide source and drain regions that pin the Fermi level near a charge neutrality level and reduce the Schottky barrier height, thereby reducing contact resistance. In some such embodiments, the semiconducting oxide channel can be formed of two or more semiconducting oxides, and the interface layers can optionally include a segregation layer between the conductive source and drain contacts and the oxygen-gettering material. In such cases, the segregation layer comprises a material that forms an alloy with metal of the semiconducting oxide of the two or more semiconducting oxides having a highest energy conduction band, thereby further reducing the

Schottky barrier height. Numerous structural variations can employ the techniques provided herein, including configurations where the source/drain regions are on the same side of the semiconducting oxide layer that the gate stack is located (top-gate configuration), as well as configurations where source/drain regions are on the side of the semiconducting oxide layer that is opposite the side on which the gate stack is located (bottom-gate configuration). As will be further appreciated, the disclosed techniques may provide various advantages over standard MOSFETs, such as reduced contact resistance in scaled devices that may enable overall devices to run at lower power and in some applications with lower current. As will be further appreciated, such embodiments may expand circuit design options available in product development cycles, and also open up options for longer battery life products to expand to applications beyond the central processing unit market.

General Overview

As shown in FIG. 1, a semiconducting oxide transistor 100 formed on a substrate 105 includes a source contact 110, a doped source region 120 in a semiconducting oxide layer 125, a gate spacer 130 between the source contact 110 and gate stack (including gate dielectric 145 and electrode 140), a channel region 150 formed from semiconducting oxide layer 125 under the gate dielectric layer 145, a doped drain region 160 in the semiconducting oxide layer 125, a drain contact 170, and a gate spacer 180 between the drain contact 170 and the gate stack. The overall resistance of the semiconducting oxide transistor 100 includes contributions from contact resistance, R_{contact} , spacer resistance, R_{spacer} , and channel resistance, R_{channel} . Due to technology scaling that continues to reduce all dimensions of the device, as the length of the channel region continues to be reduced, the contribution of the channel resistance to the overall resistance decreases, and the contribution of the contact resistance is likely to rise as a percentage of the total device resistance, and may become larger than the channel resistance. Existing contact strategies to semiconducting oxides suffer from high contact resistance. Embodiments of the present disclosure recognize this problem and are configured to help to mitigate or otherwise reduce contact resistance, as will be appreciated.

Semiconducting Oxide Devices with Interface Layers Between Contacts and Source and Drain Regions

In an embodiment according to this disclosure, shown in FIG. 2A, a semiconducting oxide transistor 200 is formed on a semiconductor substrate 205. The semiconductor substrate 205 may be implemented, for example, with a bulk silicon or a silicon-on-insulator substrate

configuration. In some implementations, the semiconductor substrate 205 may be formed using crystalline silicon. In other implementations, the semiconductor substrate 205 may be formed using alternate materials, which may or may not be combined with silicon, such as germanium, silicon germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, indium gallium arsenide (*e.g.*, $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$), gallium arsenide, or gallium antimonide. In a more general sense, any material that may serve as a foundation upon which a semiconductor device may be built or otherwise formed can be used for substrate 205 in accordance with various embodiments of the present disclosure.

As can be further seen, the example embodiment of FIG. 2A illustrates a semiconductor-on-insulator configuration that includes an insulator layer 208 on semiconductor substrate 205, although bulk substrates and other suitable configurations can be used as well. Insulator layer 208 can be formed from any suitable insulator material, such as, for example, silicon dioxide. In this example embodiment, the gate stack is a bottom-gate configuration and includes a gate dielectric 245 (which may be high-k gate dielectric material) and a gate electrode 240.

Examples of high-k gate dielectric materials include, for instance, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some specific example embodiments of the present disclosure, the high-k gate dielectric layer may be between around 5 Å to around 200 Å thick (*e.g.*, 20 Å to 50 Å), although other suitable dimension can be used. In some specific embodiments of the present disclosure, the gate electrode 240 material is polysilicon or a metal layer (*e.g.*, tungsten, titanium, copper, aluminum tungsten, titanium nitride, tantalum, and tantalum nitride, or a combination of such materials), although other suitable gate electrode materials can be used as well. The gate electrode 240 material, which may be a sacrificial material that is later removed for a replacement metal gate (RMG) process, has a thickness in the range of 50 Å to 500 Å (*e.g.*, 100 Å), in some example embodiments, although other suitable dimension can be used. In one specific example case, the gate stack includes a silicon dioxide gate dielectric 245 and a polysilicon or tungsten gate electrode 240. In still other embodiments of the present disclosure, the gate dielectric 245 includes multiple components such as a first layer of silicon dioxide on the channel region 250, and a second layer of hafnium oxide on the silicon dioxide layer. Likewise, the gate electrode 240 may include multiple components in some embodiments, such as work function metals and/or barrier materials surrounding a metal core or plug. Any number of gate stack configurations can be used, whether high-k or not, as will be appreciated.

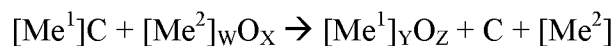
FIG. 2A further illustrates the channel region 250 over the gate dielectric 245. The channel region 250 is formed of a layer 225 of semiconducting oxide, such as, for example, titanium oxide (TiO_2), tungsten oxide (WO_3), tin(II) oxide (SnO), strontium titanate (SrTiO_3), gallium oxide (Ga_2O_3), copper(I) oxide (Cu_2O), and copper(II) oxide (CuO), or combinations thereof, to name a few examples. The channel region 250 may be undoped or lightly doped, as the case may be. FIG. 2A further illustrates the doped source region 220 and doped drain region 260 formed in the semiconducting oxide layer 225. Any number of source and drain layer configurations can be used here, with respect to dopant type and concentration (*e.g.*, boron, arsenic, phosphorous, or other suitable dopant, at a concentration of $1\text{E}20\text{ cm}^{-3}$ or higher), and dimension (*e.g.*, vertical thickness of source and drain regions may range, for instance, from 50 to 500 nm, as may the horizontal width).

FIG. 2A further illustrates a capping layer 230 over the semiconducting oxide layer 225. Examples of suitable capping layer materials include, but are not limited to, oxides of silicon (*e.g.*, silicon dioxide (SiO_2)), doped oxides of silicon, fluorinated oxides of silicon, carbon doped oxides of silicon, various low-k dielectric materials known in the arts, and combinations thereof. FIG. 2A further illustrates an optional sealing layer 235, which in some embodiments can be used to hermetically seal the semiconducting oxide layer 225. Suitable materials for the optional sealing layer 235 include dense insulating materials, such as, for example, oxides of silicon (*e.g.*, silicon dioxide (SiO_2)), nitrides of silicon (*e.g.*, silicon nitride (Si_3N_4)), hafnium dioxide (HfO_2), titanium dioxide (TiO_2), and alumina (Al_2O_3).

FIG. 2A further illustrates a source contact 270 and a drain contact 280 formed over the doped source and drain regions 220 and 260, respectively. The contacts 270 and 280 are formed of a conductive material, such as a metal species. The metal species may be a pure metal, such as titanium, tungsten, or tantalum, or may be an alloy such as a metal-metal alloy or a metal-semiconductor alloy (*e.g.*, such as a silicide material). As used herein, the term metal includes alloys, stacks, and other combinations of multiple metals. In still other embodiments, the contacts 270 and 280 have multiple components, such as a barrier or liner layer, work function metals, and plug metals. In a more general sense, any number of contact structures may be used for contacts 270 and 280.

FIG. 2A further illustrates an interlayer dielectric (ILD) material layer 285. Examples of suitable dielectric materials for ILD material layer 285 include, but are not limited to, oxides of silicon (*e.g.*, silicon dioxide (SiO_2)), doped oxides of silicon, fluorinated oxides of silicon, carbon doped oxides of silicon, various low-k dielectric materials known in the arts, and combinations thereof.

FIG. 2A further illustrates a first layer 255, also referred to herein as a first interface layer 255, between the source region 220 and the source metal contact 270, the first layer 255 comprising a first material non-reactive with the semiconducting oxide layer 225, and a second layer 265, also referred to herein as a second interface layer 265, between the drain region 260 and the drain metal contact 280, the second layer 265 comprising a second material non-reactive with the semiconducting oxide layer 225. The interface layers 255 and 265 prevent oxidation of the metal of the contacts 270 and 280 by preventing a reaction with the semiconducting oxide layer 225 from forming a metal oxide insulator at the interface between the contact and the semiconducting oxide. As will be appreciated in light of this disclosure, formation of such a metal oxide insulator is undesirable, in that it causes increased contact resistance. Example non-reactive materials that can be used for the interface layers 255 and 265 include a carbide, a nitride, a silicide, a germanide, or a tin (Sn) alloy of the metal of the respective source and drain contacts 270 and 280. For example, in an embodiment having titanium (Ti) contacts 270 and 280, the interface layers 255 and 265 comprise titanium carbide (TiC), titanium nitride (TiN), titanium silicide (TiSi), titanium germanide (TiGe), a titanium-tin alloy, or combinations thereof. A carbide interface layer 255 and 265 is particularly preferred for n-type contacts 270 and 280 having a carbide work-function (WF) of about 5 eV or less, as shown in FIG. 8A, including metals such as molybdenum (Mo), tungsten (W), vanadium (V), titanium (Ti), niobium (Nb), tantalum (Ta), zirconium (Zr), hafnium (Hf), lanthanum (La), yttrium (Y), scandium (Sc), or combinations thereof. Those carbides have a relatively low carbide to oxide reaction, as shown in FIG. 8A, disfavoring the reaction



and therefore preventing the semiconducting oxide ($[\text{Me}^2]_w\text{O}_x$) from losing oxygen atoms to the carbide interface layer ($[\text{Me}^1]\text{C}$). A carbide interface layer 255 and 265 has the additional benefit that carbon is a shallow donor in most semiconducting oxide materials. Therefore, if the semiconducting oxide becomes contaminated with carbon, the additional doping of the semiconducting oxide will increase the n-type conductivity of the semiconducting oxide region underneath the contact, further increasing mobility and lowering contact resistance.

FIG. 2B illustrates a semiconducting oxide device 201 including interface layers non-reactive with the semiconducting oxide layer between the source and drain metal contacts and the source and drain regions, respectively, according to another embodiment of this disclosure. This embodiment is similar to the embodiment shown in FIG. 2A, in that it also includes non-reactive interface layers 255 and 265 to prevent oxidation of the metal of the contacts 270 and 280 by preventing a reaction with the semiconducting oxide layer 225 from forming a metal

oxide insulator at the interface between the contact and the semiconducting oxide. To this end, the relevant discussion equally applies here. However, there are some structural differences. In particular, the embodiment in FIG. 2B employs a top-gate configuration 241, rather than a bottom-gate configuration 240. So, there is no insulator layer 208 on semiconductor substrate 205. Nor is there a capping layer 230, or a sealing layer 235. There is, however, a gate spacer 271 between the source contact 270 and interface layer 255 and the gate stack (including gate dielectric 245 and gate electrode 241), and a gate spacer 281 between the drain contact 280 and interface layer 265 and the gate stack.

In another embodiment according to this disclosure, shown in FIG. 3A, a semiconducting oxide transistor 300 is formed on a semiconductor substrate 305. As can be seen, FIG. 3A illustrates a semiconductor-on-insulator configuration that includes an insulator layer 308 on semiconductor substrate 305. In this example embodiment, the gate stack is a bottom-gate configuration, similar to that shown in Figure 2A. The gate stack includes a gate dielectric layer 345 (which may be high-k gate dielectric material) and a gate electrode 340. The previous relevant discussion with respect to the substrate 205, insulator layer 208, gate dielectric layer 245, and gate electrode 240 is equally applicable here as will be appreciated, and not all details and variations are repeated for sake of brevity.

FIG. 3A further illustrates the channel region 350 formed on the gate dielectric layer 345. The channel region 350 is formed of a layer 325 of semiconducting oxide, such as, for example, cadmium oxide (CdO_2), indium oxide (In_2O_3), tin(IV) oxide (SnO_2), zinc oxide (ZnO), iron(III) oxide (Fe_2O_3), and combinations thereof, to name a few examples. The channel region 350 may be undoped or lightly doped, as the case may be. FIG. 3A further illustrates the doped source region 320 and doped drain region 360 formed in the semiconducting oxide layer 325, and source contact 370 and a drain contact 380 formed over the doped source and drain regions 320 and 360, respectively. FIG. 3A further illustrates a capping layer 330 over the semiconducting oxide layer 325, and an optional sealing layer 335 that hermetically seals the semiconducting oxide layer 325. The previous relevant discussion with respect to the doped source region 220, doped drain region 260, source contact 270, drain contact 280, capping layer 230, and optional sealing layer 235 is equally applicable here as will be appreciated, and not all details and variations are repeated for sake of brevity.

FIG. 3A further illustrates a first layer 356, also referred to herein as a first oxygen-gettering interface layer 356, between the source region 320 and the source metal contact 370, the first layer 356 comprising a first oxygen-gettering material, and a second layer 366, also referred to herein as a second oxygen-gettering interface layer 366, between the drain region 360

and the drain metal contact 380, the second layer 366 comprising a second oxygen-gettering material. Suitable materials for the oxygen-gettering layers 356 and 366 include gadolinium (Gd), hafnium (Hf), lanthanum (La), and zirconium (Zr). These oxygen-gettering materials have a higher affinity for oxygen than the semiconducting oxide materials, because they have a lower free energy of oxidation than, for example, indium (In), as shown in FIG. 8B, and therefore these n-type work-function metals (*i.e.*, metals having a work-function of less than about 5 eV) react, as illustrated in FIG. 8C(a), with the semiconducting oxide material and create oxide layers 357 and 367 at the interface between the layers 356 and 366 and the source and drain regions 320 and 360, respectively. The oxygen-gettering interface layers 356 and 366 need to be sufficiently thin, in a range of between 1 and 5 atomic layers, to allow tunneling of electrons through them, as an insulator layer of oxide otherwise increases contact resistance as discussed above. However, the resulting defects in the semiconducting oxide underneath the oxygen-gettering layers 356 and 366 caused by oxygen vacancies are believed to pin the Fermi level (indicated by dashed lines in FIGS. 8C(a)-(d)) of the semiconducting oxide near the so-called charge neutrality level (CNL) of the semiconducting oxide. For semiconducting oxides whose conduction band is close in energy (eV) to the charge neutrality level (indicated by a dashed line in FIG. 8D), such as cadmium oxide (CdO_2), indium oxide (In_2O_3), tin(IV) oxide (SnO_2), zinc oxide (ZnO), and iron(III) oxide (Fe_2O_3), this shift in the Fermi level closer to the conduction band reduces the Schottky barrier height, increasing mobility and lowering contact resistance, as illustrated in FIG. 8C(b).

If the semiconducting oxide layer 325 includes at least two semiconducting oxides, then, as shown in FIG. 3B, the semiconducting oxide transistor 300 further includes a third layer 358, also referred to herein as a first segregation layer 358, between the source region 320 and the source metal contact 370, and a fourth layer 368, also referred to herein as a second segregation layer 368, between the drain region 360 and the drain metal contact 380, the first and second segregation layers 358 and 368 comprising a material that forms an alloy with metal of the semiconducting oxide of the at least two semiconducting oxides having the highest energy conduction band among the at least two semiconducting oxides, as illustrated in FIG. 8C(c). In an example embodiment, in a semiconducting oxide layer 325 formed of an alloy of indium oxide (In_2O_3) and gallium oxide (Ga_2O_3), where Ga_2O_3 has a higher energy conduction band than In_2O_3 , as shown in FIG. 8B, segregation layers 358 and 368 can include cobalt (Co), because, as shown in phase diagrams for cobalt and indium, and cobalt and gallium (see FIGS. 10A, and 10B, respectively), cobalt alloys with gallium but not with indium, and thereby depletes interfaces 357 and 367 of the semiconducting oxide having the higher energy

conduction band and produces indium-rich interfaces 357 and 367, creating a modified stoichiometry gradient that has an overall increased electron affinity near the interfaces 357 and 367, thereby creating a gradient in the Schottky barrier height that effectively further reduces the barrier height and corresponding contact resistance, as illustrated in FIG. 8C(d). Additional examples of semiconducting alloys and corresponding suitable segregation layer metals are listed in Table I.

Table I.

Oxide Alloy Metals	Indium, Gallium (IGO)	Indium, Zinc (IZO)	Indium, Gallium (IGZO)	Indium, Tin (ITO)
Segregation Options	Manganese, Copper, Cobalt, Iron	Copper, Cobalt	Manganese, Copper, Cobalt, Iron	Manganese, Copper, Cobalt, Iron, Molybdenum

The segregation layers 358 and 368 are not required in all embodiments of the present disclosure wherein the semiconducting oxide layer 325 includes at least two semiconducting oxides. For example, if the source and drain metal contacts 370 and 380 include titanium, and the semiconducting oxide layer 325 includes an alloy of In_2O_3 , Ga_2O_3 , and ZnO , titanium will preferentially react (through the thin oxygen-gettering interface layers 356 and 366) with In_2O_3 , because titanium has the lowest free energy of oxidation as compared to the metals of this semiconducting oxide alloy (In, Ga, and Zn), and In has the highest free energy of oxidation from among these same metals, as shown in FIG. 8B, thereby maximizing the free energy of reaction. The reaction between titanium and In_2O_3 will produce indium-rich interfaces 357 and 367, creating a modified stoichiometry gradient that has an overall increased electron affinity near the interfaces 357 and 367, without including segregation layers 358 and 368.

FIG. 3C illustrates a semiconducting oxide device 301 including the oxygen-gettering interface layers and optional segregation interface layers between the source and drain metal contacts and the source and drain regions, respectively, according to yet another embodiment of this disclosure. This embodiment is similar to the embodiments shown in FIGs. 3A and 3B, in that it also includes oxygen-gettering interface layers 356 and 366 and the optional segregation layers 358 and 368. To this end, the relevant discussion equally applies here. However, there are some structural differences. In particular, the embodiment in FIG. 3C employs a top-gate configuration, rather than a bottom-gate configuration. So, there is no insulator layer 308 on semiconductor substrate 205. Nor is there a capping layer 330, or a sealing layer 335. There is,

however, a gate spacer 371 between the source contact 370 and interface layer 355 and the gate stack (including gate dielectric 345 and gate electrode 341), and a gate spacer 381 between the drain contact 380 and interface layer 365 and the gate stack.

Methodology and Architecture

FIG. 4A is a method for forming a semiconductor integrated circuit including interface layers between a conductive contact and doped semiconducting oxide source and drain regions, the interface layers including a material non-reactive with the semiconducting oxide, in accordance with an embodiment of the present disclosure. FIGS. 5A through 5H-1 illustrate example structures that are formed as the method is carried out, and in accordance with some embodiments.

As can be seen, the method includes providing 410 a semiconductor substrate including an insulator layer on the substrate. FIG. 5A illustrates an insulator layer 508 on semiconductor substrate 505. The previous relevant discussion with respect to the substrate 205 and insulator layer 208 is equally applicable here as will be appreciated, and not all details and variations are repeated for the sake of brevity. With further reference to FIG. 4A, the method further includes forming 420 a gate electrode in the insulator layer, as shown in FIG. 5B. The gate electrode 540 can be formed as typically done or using any suitable standard or custom techniques. In some embodiments of the present disclosure, the gate electrode 540 may be formed by depositing and then patterning a gate electrode layer. The previous relevant discussion with respect to the gate electrode 240 is equally applicable here as will be appreciated, and not all details and variations are repeated for the sake of brevity.

With further reference to FIG. 4A, the method further includes forming 430 a stack including a gate dielectric layer 545, a semiconducting oxide layer 525, and a capping layer 530, as shown in FIG. 5C. The layers 545, 525, and 530 may be blanket deposited onto the insulator layer 508 and gate electrode 540 using standard deposition processes such as chemical vapor deposition (CVD), atomic layer deposition (ALD), spin-on deposition (SOD), or physical vapor deposition (PVD). Alternate deposition techniques may be used as well, for instance, the gate dielectric layer 545 may be thermally grown. The previous relevant discussion with respect to the gate dielectric layer 245, semiconducting oxide layer 225, and capping layer 230 is equally applicable here as will be appreciated, and not all details and variations are repeated for the sake of brevity. Recall the channel region is in the semiconducting oxide layer 525, and may be undoped or lightly doped. With further reference to FIG. 4A, the method further includes patterning 440 the stack including the gate dielectric layer 545, the semiconducting oxide layer

525, and the capping layer 530 over the gate electrode 540, as shown in FIG. 5D. A standard patterning process may be carried out to etch away portions of the gate dielectric layer 545, the semiconducting oxide layer 525, and the capping layer 530 to form the stack shown in FIG. 5D. A hardmask can be used to protect the stack while the extra materials are etched away or otherwise removed, as will be appreciated.

With further reference to FIG. 4A, the method optionally further includes depositing 450 a hermetic sealing material layer 535 over the stack formed at 440 and over the insulator layer 508, followed by depositing 460 an interlayer dielectric material layer (ILD) 585 over the optional layer 535, as shown in FIG. 5E. The layers 535 and 585 may be blanket deposited onto the semiconductor substrate using standard deposition processes such as CVD, ALD, SOD, or PVD. The previous relevant discussion with respect to the hermetic sealing material layer 235 and ILD material layer 285 is equally applicable here as will be appreciated, and not all details and variations are repeated for the sake of brevity. With further reference to FIG. 4A, the method further includes forming 470 source and drain contact trenches 571 and 581, as shown in FIG. 5F. Any etching process suitable for anisotropically etching the ILD material 585, optional hermetic sealing layer 535, and capping layer 530 described above selectively over the semiconducting oxide layer 525 can be used to form source contact trench 571 and drain contact trench 581.

With further reference to FIG. 4A, the method further includes defining 480 source and drain regions 520 and 560 in semiconducting oxide 525, as shown in FIG. 5F. Ion implantation can be used to provide the source/drain regions in the semiconducting oxide, as may an etch and replace process where epitaxial source drain regions are grown in recesses formed in the semiconducting oxide. Any number of source and drain layer configurations can be used here, with respect to dopant type and concentration (*e.g.*, boron, arsenic, phosphorous, or other suitable dopant, at a concentration of $1\text{E}20\text{ cm}^{-3}$ or higher), and dimension (*e.g.*, vertical thickness of source and drain regions may range, for instance, from 50 to 500 nm, as may the horizontal width). With further reference to FIG. 4A, the method further includes forming 481 non-reactive interface layers 555 and 565 in source and drain contact trenches 571 and 581, as shown in FIG. 5G-1. The interface layers 555 and 565 can be formed by deposition of the carbide, nitride, silicide, germanide, or tin (Sn) alloy of the metal of the respective source and drain contacts, using deposition processes suitable for the respective non-reactive material, such as CVD, ALD, PVD, plasma enhanced ALD (PEALD), or plasma enhanced CVD (PECVD). PEALD and PECVD including a hydrogen plasma can be used to deposit carbides from metalorganic precursors. For example, molybdenum (Mo) and tungsten (W) carbides can be

deposited from imido-amido complexes of Mo or W. For PECVD, carbon can be deposited using a precursor such as a gaseous hydrocarbon (*e.g.*, methane (CH₄), ethane (C₂H₆), propane (C₃H₈), or butane (C₄H₁₀)). Alternatively, in the case of carbide interface layers 555 and 565, amorphous carbon can be deposited into source and drain contact trenches 571 and 581, by, for example, CVD, followed by deposition of the contact metal by, for example PVD, whereby a carbide is formed due to the energy deposited during PVD atom impingement, and, additionally or alternatively, annealing at a temperature suitable to form carbide interface layers 555 and 565.

With further reference to FIG. 4A, the method further includes forming 490 source and drain metal contacts 570 and 580 in source and drain contact trenches 571 and 581, respectively, over the interface layers 555 and 565, as shown in FIG. 5H-1. The metal contacts 570 and 580 can be formed using any number of standard deposition processes. In some cases, source/drain contact structures are provided that include multiple components, such as a liner or barrier layer, resistance reducing metal, work function metals, and a plug. The previous relevant discussion with respect to the source and drain metal contacts 270 and 280 is equally applicable here as will be appreciated, and not all details and variations are repeated for the sake of brevity.

FIG. 4B is a method for forming a semiconductor integrated circuit including interface layers between a conductive contact and doped semiconducting oxide source and drain regions, the interface layers including an oxygen-gettering material that creates oxygen-deficient defects in the doped semiconducting oxide source and drain regions, in accordance with another embodiment of the present disclosure. The method steps 410 to 480 are the same as described above with reference to FIGS. 5A to 5F, and therefore are not repeated. With further reference to FIG. 4B, the method further includes forming 482 oxygen-gettering interface layers 556 and 566, as shown in FIG. 5G-2A. Any process suitable for depositing, for example, 1 to 5 atomic layers of an oxygen-gettering material, such as, for example, ALD, can be used to form oxygen-gettering interface layers 556 and 566. The previous relevant discussion with respect to the oxygen-gettering interface layers 356 and 366 is equally applicable here as will be appreciated, and not all details and variations are repeated for the sake of brevity.

With further reference to FIG. 4B, the method further includes forming 485 optional segregation material layers 558 and 568 over the oxygen-gettering interface layers 556 and 566, as shown in FIG. 5G-2B, using deposition processes such as CVD, ALD, or PVD. The previous relevant discussion with respect to the segregation material layers 358 and 368 is equally applicable here as will be appreciated, and not all details and variations are repeated for the sake of brevity.

With further reference to FIG. 4B, the method further includes forming 490 source and drain metal contacts 570 and 580 in source and drain contact trenches 571 and 581, respectively, over the oxygen-gettering interface layers 556 and 566, and optional segregation material layers 558 and 568, as shown in FIG. 5H-2. The previous relevant discussion with respect to step 490 is equally applicable here as will be appreciated, and not all details and variations are repeated for the sake of brevity.

FIG. 6 illustrates methods for forming a semiconducting oxide device including interface layers non-reactive with the semiconducting oxide layer or oxygen-gettering interface layers, but with a top-gate configuration, according to another embodiment of this disclosure. As will be appreciated, some of the method is the same as provided with the methodologies of FIGs. 4A and 4B, but here are some differences, as will be appreciated. The previous relevant discussion is equally applicable here, with respect to example materials for forming techniques for the various structural features shown.

With reference to FIG. 6, the method includes depositing 601 a semiconducting oxide layer 725 on a substrate 705, using standard deposition processes such as CVD, ALD, SOD, or PVD. The channel is provided in the semiconducting oxide layer 725. Assuming a gate-last process, the method continues with forming 603 a dummy gate stack over the channel region, the gate stack including one or more dummy gate materials (e.g., polysilicon gate), followed by forming gate spacers 741 on the sides of the dummy gate stack. The dummy gate stack and spacers 741 can be formed as normally done, such as via a blanket deposition and etch process to provide dummy gate stack, followed by deposition and etch process to provide the gate spacers 741. In other embodiments using a gate-first approach, the final gate structure can be provided at this time, as will be explained at 609. The resulting structure is shown in FIG. 7A, which presumes a gate-last process flow.

Once the dummy gate is formed, the method may continue in a number of ways, but generally includes forming 605 one or more interface layers over the semiconducting oxide 725. In one example case, the forming at 605 includes forming non-reactive interface layers 755 and 765 over the semiconducting oxide layer 725 and gate stack (such as described with reference to Figure 4A). Alternatively, the forming at 605 includes forming oxygen-gettering interface layers 756 and 766 over the semiconducting oxide layer 725 and gate stack (such as described with reference to Figure 4B). In some such embodiments, the forming at 605 may further include depositing segregation layers 758 and 768 on the oxygen-gettering interface layers 756 and 766. In any such cases, excess interface layer materials can be removed from the gate stack to provide the structure shown in Figure 7B.

The method continues with depositing 607 an insulator fill material over the structure and planarizing down to the top of the gate stack, to provide the structure shown in Figure 7C. The method of this example embodiment continues with forming 609 the final gate structure, by removing the dummy gate stack from between the gate spacers 741, and depositing the desired gate dielectric 745 (e.g., high-k dielectric, such as hafnium or a bi-layer structure of silicon dioxide and hafnium oxide) and gate electrode 740 (e.g., tungsten, or a tungsten plug and work function metals such as titanium nitride). An example resulting structure is shown in Figure 7C. Note in the example embodiment shown that the gate dielectric 745 covers both the semiconducting oxide layer 725 over the channel region as well as the sides of the gate spacers 741. Other embodiments may just have the gate dielectric 745 on the semiconducting oxide layer 725. In such gate-last process flows, note that the channel region can be exposed during removal of the dummy gate. In some cases, the underlying semiconducting oxide layer 725 is a fin-like body or wire-shape. In such cases, the gate structure may cover multiple sides of the channel, or wrap all the way around the channel. In gate-all-around embodiments, the etch to remove dummy gate could be further configured to remove underlying substrate material to liberate the semiconducting oxide layer 725 in the channel region, so as to allow the subsequently deposited gate dielectric and gate electrode materials to wrap around the channel. Etch chemistry selective to the semiconducting oxide layer 725 material (but not the substrate material) can be used in such cases, as will be appreciated. In other embodiments, this final gate structure is formed at 603, as part of a gate-first process flow. As will be appreciated, the method may now continue as previously described with respect to 470 (form source/drain contact trenches in the insulator fill material), followed by 480 (define the source/drain regions 720/760 in the semiconductor oxide layer 725, followed by 490 (form the source/drain metal contacts 770/780 in the contact trenches). An example resulting structure is shown in Figure 7D.

Numerous variations will be apparent in light of this disclosure. Note that the techniques provided herein can be used in any number of process flows, including gate-last, gate-first, bottom-gate, and top-gate process flows. Thus, a given gate electrode may be, for example, under the channel region, or over the channel region, or both under and over the channel region such as in the case of a nanowire channel.

Use of the techniques and structures provided herein may be detectable using tools such as: electron microscopy including scanning/transmission electron microscopy (SEM/TEM), scanning transmission electron microscopy (STEM), and reflection electron microscopy (REM); composition mapping; x-ray crystallography or diffraction (XRD); energy-dispersive x-ray spectroscopy (EDS); secondary ion mass spectrometry (SIMS); time-of-flight SIMS (ToF-

SIMS); atom probe imaging or tomography; local electrode atom probe (LEAP) techniques; 3D tomography; or high resolution physical or chemical analysis, to name a few suitable example analytical tools. In particular, in some embodiments of the present disclosure, such tools may indicate the presence of interface layers between a conductive contact and doped

5 semiconducting oxide source and drain regions that reduce contact resistance between the conductive contact and the doped semiconducting oxide source and drain regions as variously described herein.

Example System

10 FIG. 9 is an example computing system implemented with one or more of the integrated circuit structures as disclosed herein, in accordance with some embodiments of the present disclosure. As can be seen, the computing system 900 houses a motherboard 902. The motherboard 902 may include a number of components, including, but not limited to, a processor 904 and at least one communication chip 906, each of which can be physically and
15 electrically coupled to the motherboard 902, or otherwise integrated therein. As will be appreciated, the motherboard 902 may be, for example, any printed circuit board, whether a main board, a daughterboard mounted on a main board, or the only board of system 900, *etc.*

Depending on its applications, computing system 900 may include one or more other components that may or may not be physically and electrically coupled to the motherboard 902.

20 These other components may include, but are not limited to, volatile memory (*e.g.*, DRAM), non-volatile memory (*e.g.*, read only memory (ROM)), a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a
25 camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth). Any of the components included in computing system 900 may include one or more integrated circuit structures or devices configured in accordance with an example embodiment (*e.g.*, to include one or more interface layers between a conductive contact and doped semiconducting oxide source and drain regions that reduce contact resistance between
30 the conductive contact and the doped semiconducting oxide source and drain regions, as variously provided herein). In some embodiments, multiple functions can be integrated into one or more chips (*e.g.*, for instance, note that the communication chip 906 can be part of or otherwise integrated into the processor 904).

The communication chip 906 enables wireless communications for the transfer of data to and from the computing system 900. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, *etc.*, that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 906 may implement any of a number of wireless standards or protocols, including, but not limited to, Wi-Fi (Institute of Electrical and Electronics Engineers (IEEE) 802.11 family), worldwide interoperability for microwave access (WiMAX) (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), 1x evolution-data optimized (Ev-DO), high speed packet access (HSPA+), high speed downlink packet access (HSDPA+), high speed uplink packet access (HSUPA+), enhanced data rates for GSM evolution (EDGE), global system for mobile communication (GSM), general packet radio service (GPRS), code division multiple access (CDMA), time division multiple access (TDMA), digital enhanced cordless telecommunications (DECT), Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing system 900 may include a plurality of communication chips 906. For instance, a first communication chip 906 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 906 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others. In some embodiments, communication chip 906 may include one or more transistor structures including interface layers between a conductive contact and doped semiconducting oxide source and drain regions that reduce contact resistance between the conductive contact and the doped semiconducting oxide source and drain regions as variously described herein.

The processor 904 of the computing system 900 includes an integrated circuit die packaged within the processor 904. In some embodiments, the integrated circuit die of the processor includes onboard circuitry that is implemented with one or more integrated circuit structures or devices as variously described herein. The term “processor” may refer to any device or portion of a device that processes, for instance, electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 906 also may include an integrated circuit die packaged within the communication chip 906. In accordance with some such example embodiments, the integrated circuit die of the communication chip includes one or more integrated circuit structures or devices as variously described herein. As will be appreciated in light of this

disclosure, note that multi-standard wireless capability may be integrated directly into the processor 904 (*e.g.*, where functionality of any chips 906 is integrated into processor 904, rather than having separate communication chips). Further note that processor 904 may be a chip set having such wireless capability. In short, any number of processor 904 and/or communication chips 906 can be used. Likewise, any one chip or chip set can have multiple functions integrated therein.

In various implementations, the computing system 900 may be a laptop, a netbook, a notebook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra-mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, a digital video recorder, or any other electronic device that processes data or employs one or more integrated circuit structures or devices formed using the disclosed techniques, as variously described herein.

Further Example Embodiments

The following examples pertain to further embodiments, from which numerous permutations and configurations will be apparent.

Example 1 is a semiconductor integrated circuit, comprising: a channel region, the channel region including a semiconducting oxide; a gate electrode under the channel region; a gate dielectric layer between the gate electrode and the channel region; a source region adjacent to the channel region; a source metal contact over the source region; a first layer between the source region and the source metal contact, the first layer comprising a first material non-reactive with the semiconducting oxide; a drain region adjacent to the channel region; a drain metal contact over the drain region; and a second layer between the drain region and the drain metal contact, the second layer comprising a second material non-reactive with the semiconducting oxide.

Example 2 includes the subject matter of Example 1, wherein the semiconducting oxide includes at least one of titanium oxide (TiO₂), tungsten oxide (WO₃), tin(II) oxide (SnO),

strontium titanate (SrTiO_3), gallium oxide (Ga_2O_3), copper(I) oxide (Cu_2O), and copper(II) oxide (CuO).

Example 3 includes the subject matter of Example 1 or Example 2, wherein semiconducting oxide includes oxygen and at least one of titanium, tungsten, tin, strontium,
5 gallium, and copper.

Example 4 includes the subject matter of any of Examples 1 to 3, wherein the first material includes at least one of a carbide, a nitride, a silicide, and a germanide.

Example 5 includes the subject matter of any of Examples 1 to 4, wherein the second material includes at least one of a carbide, a nitride, a silicide, and a germanide.

10 Example 6 includes the subject matter of any of Examples 1 to 5, wherein the gate electrode includes at least one of titanium (Ti), tungsten (W), copper (Cu), and aluminum (Al)

Example 7 includes a computing device that includes the subject matter of any of Examples 1 to 6.

Example 8 includes a method for forming a semiconductor integrated circuit, the method
15 comprising: forming a channel region, the channel region including a semiconducting oxide;
forming a gate electrode under the channel region; forming a gate dielectric layer between the
gate electrode and the channel region; forming a source region adjacent to the channel region;
forming a source metal contact over the source region; forming a first layer between the source
region and the source metal contact, the first layer comprising a first material non-reactive with
20 the semiconducting oxide; forming a drain region adjacent to the channel region; forming a drain
metal contact over the drain region; and forming a second layer between the drain region and the
drain metal contact, the second layer comprising a second material non-reactive with the
semiconducting oxide.

Example 9 includes the subject matter of Example 8, wherein the semiconducting oxide
25 includes at least one of titanium oxide (TiO_2), tungsten oxide (WO_3), tin(II) oxide (SnO),

strontium titanate (SrTiO_3), gallium oxide (Ga_2O_3), copper(I) oxide (Cu_2O), and copper(II) oxide (CuO).

Example 10 includes the subject matter of either of Examples 8 or 9, wherein the semiconducting oxide includes oxygen and at least one of titanium, tungsten, tin, strontium,
5 gallium, and copper.

Example 11 includes the subject matter of any of Examples 8 to 10, wherein the first material includes at least one of a carbide, a nitride, a silicide, and a germanide.

Example 12 includes the subject matter of any of Examples 8 to 11, wherein the second material includes at least one of a carbide, a nitride, a silicide, and a germanide.

10 Example 13 includes the subject matter of any of Examples 8 to 12, wherein the gate electrode includes at least one of titanium (Ti), tungsten (W), copper (Cu), and aluminum (Al).

Example 14 is a semiconductor integrated circuit, comprising: a channel region, the channel region including at least one semiconducting oxide; a gate electrode under the channel region; a gate dielectric layer between the gate electrode and the channel region; a source region
15 adjacent to the channel region; a source metal contact over the source region; a first layer between the source region and the source metal contact, the first layer comprising a first oxygen-gettering material; a drain region adjacent to the channel region; a drain metal contact over the drain region; and

a second layer between the drain region and the drain metal contact, the second layer comprising
20 a second oxygen-gettering material.

Example 15 includes the subject matter of Example 14, wherein the semiconducting oxide includes oxygen and at least one of cadmium, indium, tin, zinc, and iron.

Example 16 includes the subject matter of Example 14 or Example 15, wherein the semiconducting oxide includes indium and oxygen.

Example 17 includes the subject matter of any of Examples 14 to 16, wherein the semiconducting oxide includes at least one of cadmium oxide (CdO_2), indium oxide (In_2O_3), tin(IV) oxide (SnO_2), zinc oxide (ZnO), and iron(III) oxide (Fe_2O_3).

Example 18 includes the subject matter of any of Examples 14 to 17, wherein the
5 semiconducting oxide includes indium oxide (In_2O_3).

Example 19 includes the subject matter of any of Examples 14 to 18, wherein the first oxygen-gettering material includes at least one of gadolinium (Gd), hafnium (Hf), lanthanum (La), and zirconium (Zr).

Example 20 includes the subject matter of any of Examples 14 to 19, wherein the second
10 oxygen-gettering material includes at least one of gadolinium (Gd), hafnium (Hf), lanthanum (La), and zirconium (Zr).

Example 21 includes the subject matter of any of Examples 14 to 20, wherein the at least one semiconducting oxide includes at least two semiconducting oxides.

Example 22 includes the subject matter of any of Examples 14 to 21, further including a
15 third layer between the source metal contact and the first layer, the third layer comprising a segregation material that forms an alloy with metal of the semiconducting oxide of the at least two semiconducting oxides having a highest energy conduction band.

Example 23 includes the subject matter of any of Examples 14 to 22, further including a fourth layer between the drain metal contact and the second layer, the fourth layer comprising a
20 segregation material that forms an alloy with metal of the semiconducting oxide of the at least two semiconducting oxides having a highest energy conduction band.

Example 24 includes the subject matter of any of Examples 14 to 23, wherein the gate electrode includes at least one of titanium (Ti), tungsten (W), copper (Cu), and aluminum (Al).

Example 25 includes a computing device that includes the subject matter of any of
25 Examples 14 to 24.

Example 26 includes a method for forming a semiconductor integrated circuit, the method comprising: forming a channel region, the channel region including at least one semiconducting oxide; forming a gate electrode under the channel region; forming a gate dielectric layer between the gate electrode and the channel region; forming a source region adjacent to the channel region; forming a source metal contact over the source region; forming a first layer between the source region and the source metal contact, the first layer comprising a first oxygen-gettering material; forming a drain region adjacent to the channel region; forming a drain metal contact over the drain region; and forming a second layer between the drain region and the drain metal contact, the second layer comprising a second oxygen-gettering material.

Example 27 includes the subject matter of Example 26, wherein the semiconducting oxide includes oxygen and at least one of cadmium, indium, tin, zinc, and iron.

Example 28 includes the subject matter of Example 26 or Example 27, wherein the semiconducting oxide includes indium and oxygen.

Example 29 includes the subject matter of any of Examples 26 to 28, wherein the semiconducting oxide includes at least one of cadmium oxide (CdO_2), indium oxide (In_2O_3), tin(IV) oxide (SnO_2), zinc oxide (ZnO), and iron(III) oxide (Fe_2O_3).

Example 30 includes the subject matter of any of Examples 26 to 29, wherein the semiconducting oxide includes indium oxide (In_2O_3).

Example 31 includes the subject matter of any of Examples 26 to 30, wherein the first oxygen-gettering material includes at least one of gadolinium (Gd), hafnium (Hf), lanthanum (La), and zirconium (Zr).

Example 32 includes the subject matter of any of Examples 26 to 31, wherein the second oxygen-gettering material includes at least one of gadolinium (Gd), hafnium (Hf), lanthanum (La), and zirconium (Zr).

Example 33 includes the subject matter of any of Examples 26 to 32, wherein the at least one semiconducting oxide includes at least two semiconducting oxides.

Example 34 includes the subject matter of any of Examples 26 to 33, further including a third layer between the source metal contact and the first layer, the third layer comprising a segregation material that forms an alloy with metal of the semiconducting oxide of the at least two semiconducting oxides having a highest energy conduction band.

5 Example 35 includes the subject matter of any of Examples 26 to 34, further including a fourth layer between the drain metal contact and the second layer, the fourth layer comprising a segregation material that forms an alloy with metal of the semiconducting oxide of the at least two semiconducting oxides having a highest energy conduction band.

 Example 36 includes the subject matter of any of Examples 26 to 35, wherein the gate
10 electrode includes at least one of titanium (Ti), tungsten (W), copper (Cu), and aluminum (Al).

 The foregoing description of example embodiments has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the present disclosure to the precise forms disclosed. Many modifications and variations are possible in light of this disclosure. It is intended that the scope of the present disclosure be limited not by
15 this detailed description, but rather by the claims appended hereto. Future filed applications claiming priority to this application may claim the disclosed subject matter in a different manner, and may generally include any set of one or more limitations as variously disclosed or otherwise demonstrated herein.

What is claimed is:

1. A semiconductor integrated circuit, comprising:
 - a channel region, the channel region including a semiconducting oxide;
 - a gate electrode under the channel region;
 - 5 a gate dielectric layer between the gate electrode and the channel region;
 - a source region adjacent to the channel region;
 - a source metal contact over the source region;
 - a first layer between the source region and the source metal contact, the first layer comprising a first material non-reactive with the semiconducting oxide;
 - 10 a drain region adjacent to the channel region;
 - a drain metal contact over the drain region; and
 - a second layer between the drain region and the drain metal contact, the second layer comprising a second material non-reactive with the semiconducting oxide.
- 15 2. The semiconductor integrated circuit of claim 1, wherein the semiconducting oxide includes at least one of titanium oxide (TiO_2), tungsten oxide (WO_3), tin(II) oxide (SnO), strontium titanate (SrTiO_3), gallium oxide (Ga_2O_3), copper(I) oxide (Cu_2O), and copper(II) oxide (CuO).
- 20 3. The semiconductor integrated circuit of claim 1, wherein the first material includes at least one of a carbide, a nitride, a silicide, and a germanide.
4. The semiconductor integrated circuit of any one of claims 1-3, wherein the second material includes at least one of a carbide, a nitride, a silicide, and a germanide.
- 25 5. A method for forming a semiconductor integrated circuit, the method comprising:
 - forming a channel region, the channel region including a semiconducting oxide;
 - forming a gate electrode under the channel region;
 - forming a gate dielectric layer between the gate electrode and the channel region;
 - 30 forming a source region adjacent to the channel region;
 - forming a source metal contact over the source region;

forming a first layer between the source region and the source metal contact, the first layer comprising a first material non-reactive with the semiconducting oxide; forming a drain region adjacent to the channel region; forming a drain metal contact over the drain region; and forming a second layer between the drain region and the drain metal contact, the second layer comprising a second material non-reactive with the semiconducting oxide.

6. The method for forming a semiconductor integrated circuit of claim 5, wherein the semiconducting oxide includes at least one of titanium oxide (TiO_2), tungsten oxide (WO_3), tin(II) oxide (SnO), strontium titanate (SrTiO_3), gallium oxide (Ga_2O_3), copper(I) oxide (Cu_2O), and copper(II) oxide (CuO).
7. The method for forming a semiconductor integrated circuit of claim 5, wherein the first material includes at least one of a carbide, a nitride, a silicide, and a germanide.
8. The method for forming a semiconductor integrated circuit of any one of claims 5-7, wherein the second material includes at least one of a carbide, a nitride, a silicide, and a germanide.
9. A semiconductor integrated circuit, comprising:
 - a channel region, the channel region including at least one semiconducting oxide;
 - a gate electrode under the channel region;
 - a gate dielectric layer between the gate electrode and the channel region;
 - a source region adjacent to the channel region;
 - a source metal contact over the source region;
 - a first layer between the source region and the source metal contact, the first layer comprising a first oxygen-gettering material;
 - a drain region adjacent to the channel region;
 - a drain metal contact over the drain region; and
 - a second layer between the drain region and the drain metal contact, the second layer comprising a second oxygen-gettering material.

10. The semiconductor integrated circuit of claim 9, wherein the semiconducting oxide includes at least one of cadmium oxide (CdO_2), indium oxide (In_2O_3), tin(IV) oxide (SnO_2), zinc oxide (ZnO), and iron(III) oxide (Fe_2O_3).

5 11. The semiconductor integrated circuit of claim 10, wherein the semiconducting oxide includes indium oxide (In_2O_3).

10 12. The semiconductor integrated circuit of claim 11, wherein the first oxygen-gettering material includes at least one of gadolinium (Gd), hafnium (Hf), lanthanum (La), and zirconium (Zr).

13. The semiconductor integrated circuit of any one of claims 9-12, wherein the second oxygen-gettering material includes at least one of gadolinium (Gd), hafnium (Hf), lanthanum (La), and zirconium (Zr).

15 14. The semiconductor integrated circuit of claim 9, wherein the at least one semiconducting oxide includes at least two semiconducting oxides.

20 15. The semiconductor integrated circuit of claim 14, further including a third layer between the source metal contact and the first layer, the third layer comprising a segregation material that forms an alloy with metal of the semiconducting oxide of the at least two semiconducting oxides having a highest energy conduction band.

25 16. The semiconductor integrated circuit of claim 14, further including a fourth layer between the drain metal contact and the second layer, the fourth layer comprising a segregation material that forms an alloy with metal of the semiconducting oxide of the at least two semiconducting oxides having a highest energy conduction band.

30 17. A method for forming a semiconductor integrated circuit, the method comprising: forming a channel region, the channel region including at least one semiconducting oxide;

forming a gate electrode under the channel region;
forming a gate dielectric layer between the gate electrode and the channel region;
forming a source region adjacent to the channel region;
forming a source metal contact over the source region;
5 forming a first layer between the source region and the source metal contact, the first
layer comprising a first oxygen-gettering material;
forming a drain region adjacent to the channel region;
forming a drain metal contact over the drain region; and
forming a second layer between the drain region and the drain metal contact, the
10 second layer comprising a second oxygen-gettering material.

18. The method for forming a semiconductor integrated circuit of claim 17, wherein
the semiconducting oxide includes at least one of cadmium oxide (CdO_2), indium
oxide (In_2O_3), tin(IV) oxide (SnO_2), zinc oxide (ZnO), and iron(III) oxide
15 (Fe_2O_3).
19. The method for forming a semiconductor integrated circuit of claim 18, wherein
the semiconducting oxide includes indium oxide (In_2O_3).
20. The method for forming a semiconductor integrated circuit of claim 19, wherein
20 the first oxygen-gettering material includes at least one of gadolinium (Gd),
hafnium (Hf), lanthanum (La), and zirconium (Zr).
21. The method for forming a semiconductor integrated circuit of any one of claims
25 17-20, wherein the second oxygen-gettering material includes at least one of
gadolinium (Gd), hafnium (Hf), lanthanum (La), and zirconium (Zr).
22. The method for forming a semiconductor integrated circuit of claim 17, wherein
the at least one semiconducting oxide includes at least two semiconducting
30 oxides.
23. The method for forming a semiconductor integrated circuit of claim 22, further
including a third layer between the source metal contact and the first layer, the
third layer comprising a segregation material that forms an alloy with metal of the

semiconducting oxide of the at least two semiconducting oxides having a highest energy conduction band.

- 5 24. The method for forming a semiconductor integrated circuit of claim 22, further including a fourth layer between the drain metal contact and the second layer, the fourth layer comprising a segregation material that forms an alloy with metal of the semiconducting oxide of the at least two semiconducting oxides having a highest energy conduction band.

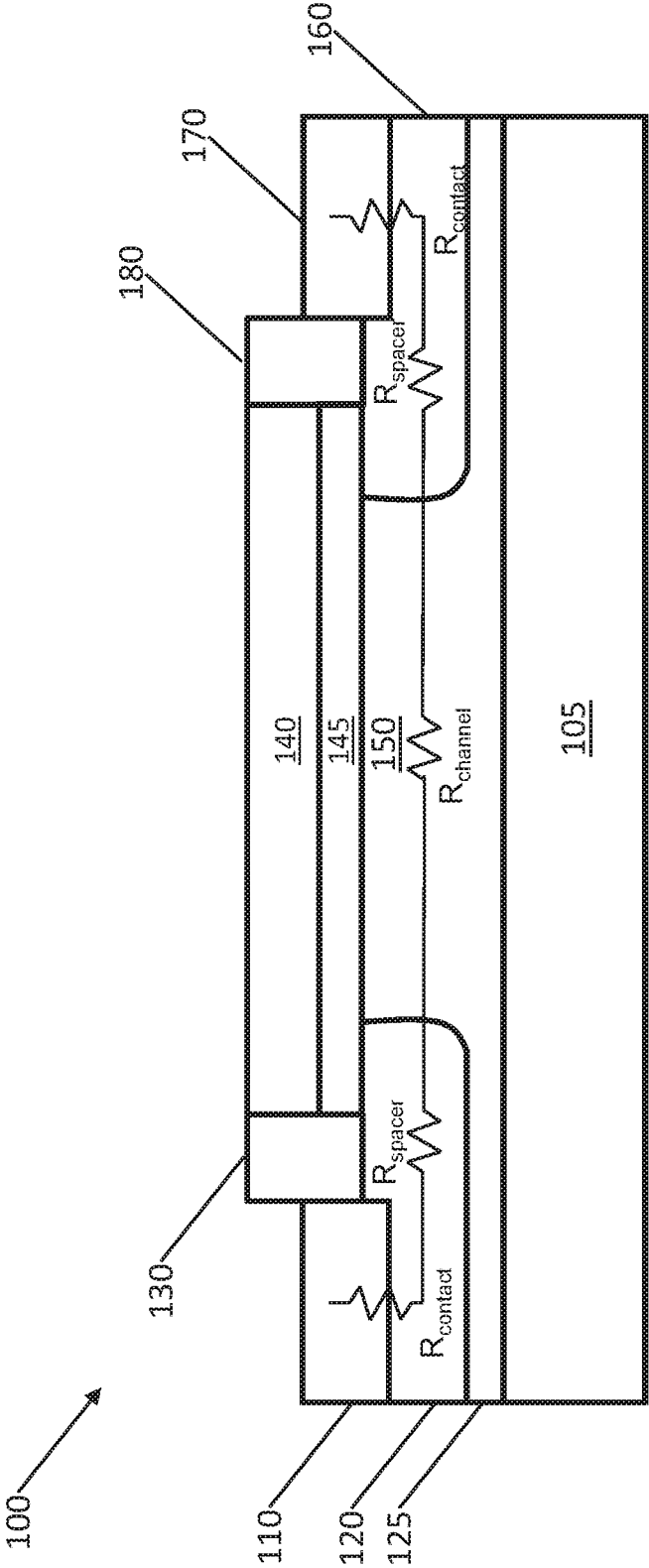


FIG. 1

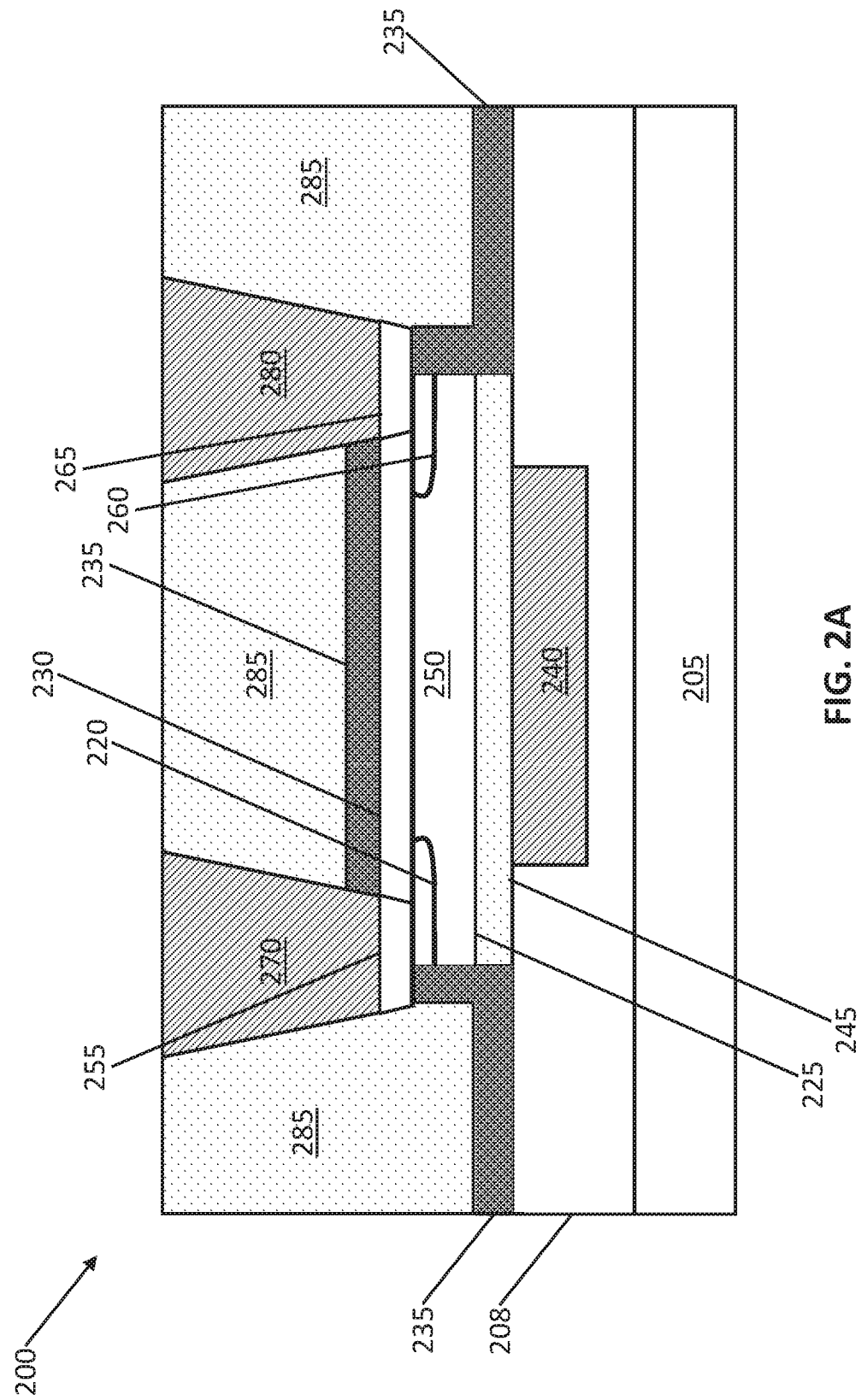


FIG. 2A

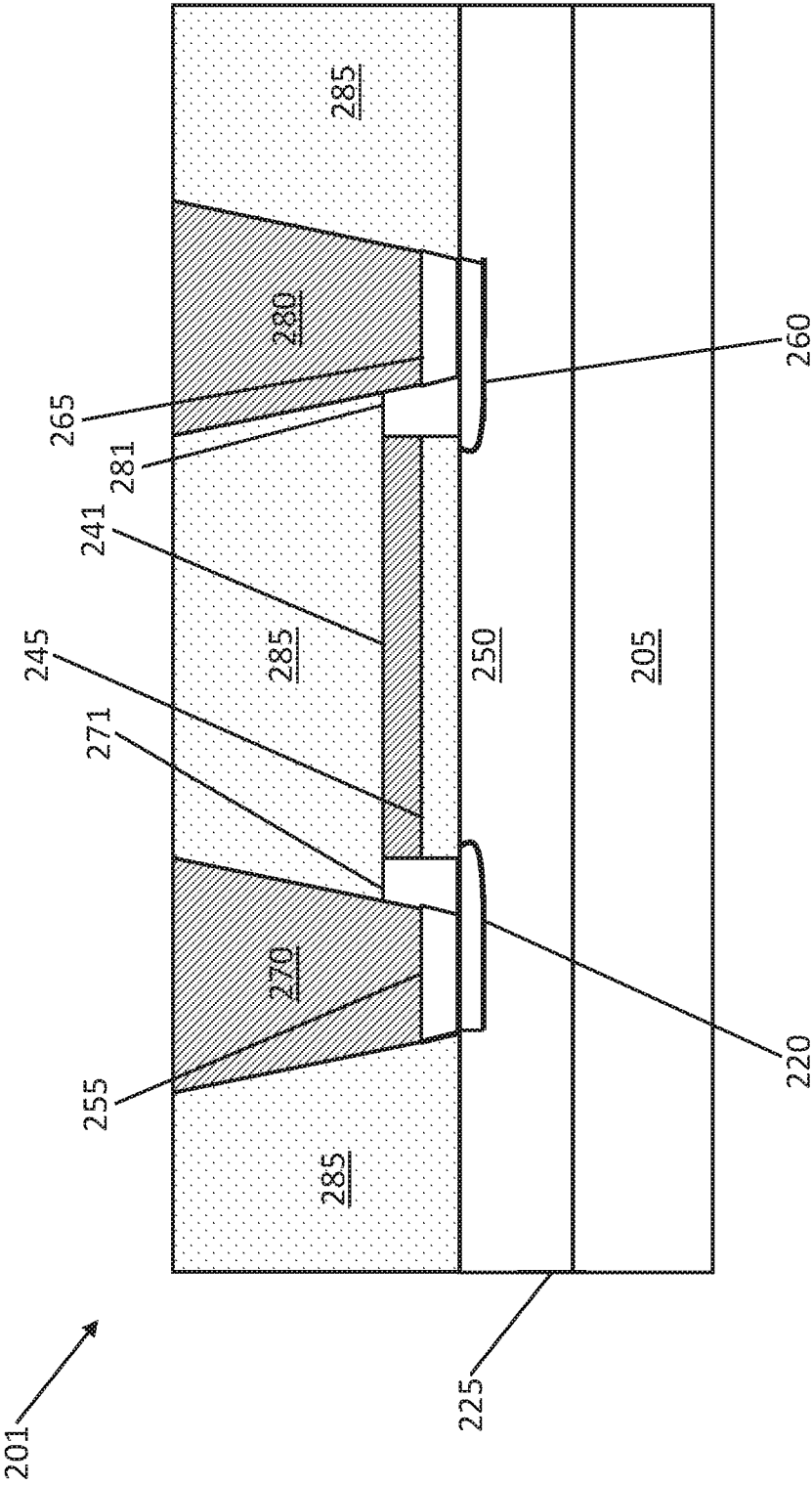


FIG. 2B

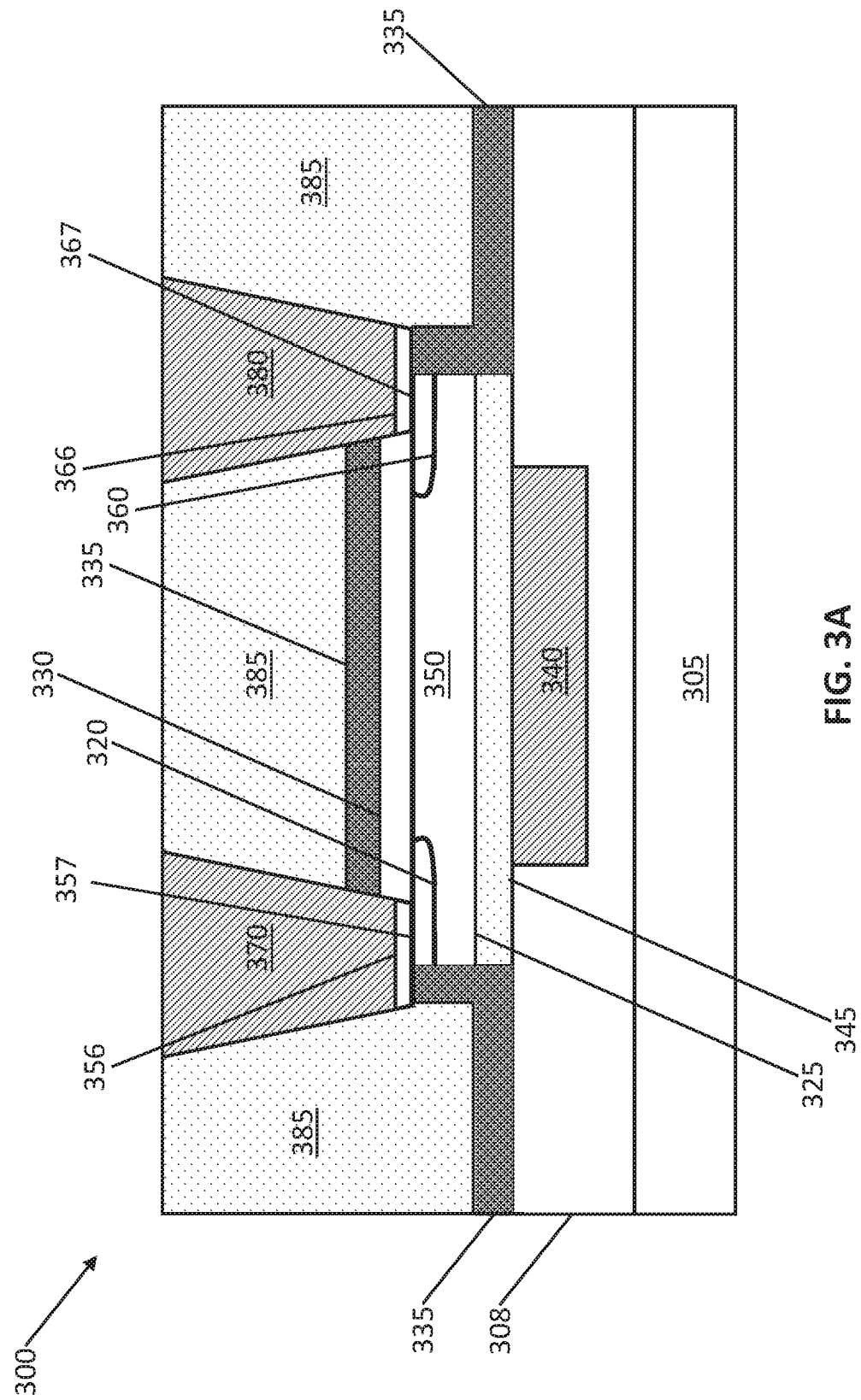
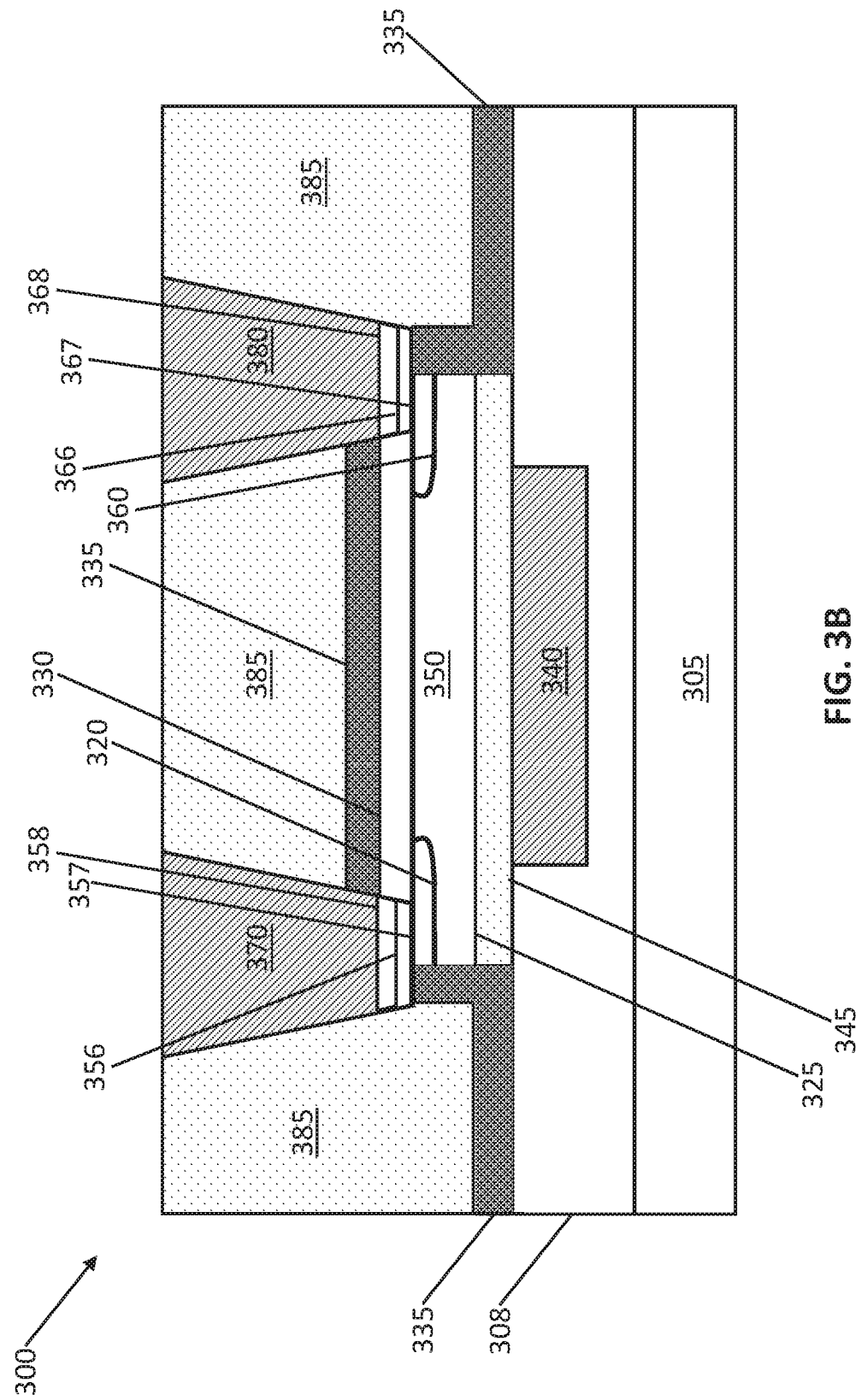


FIG. 3A



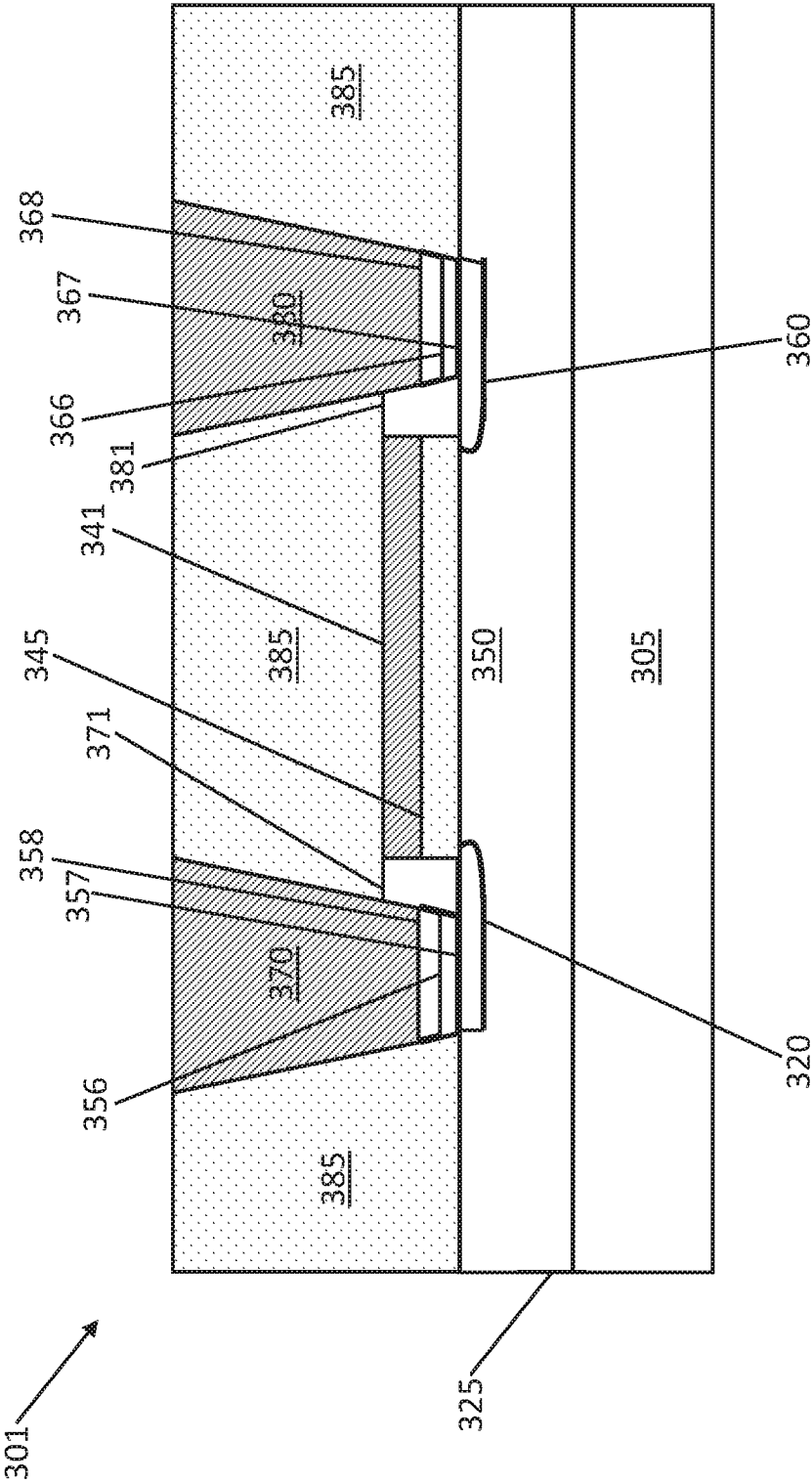
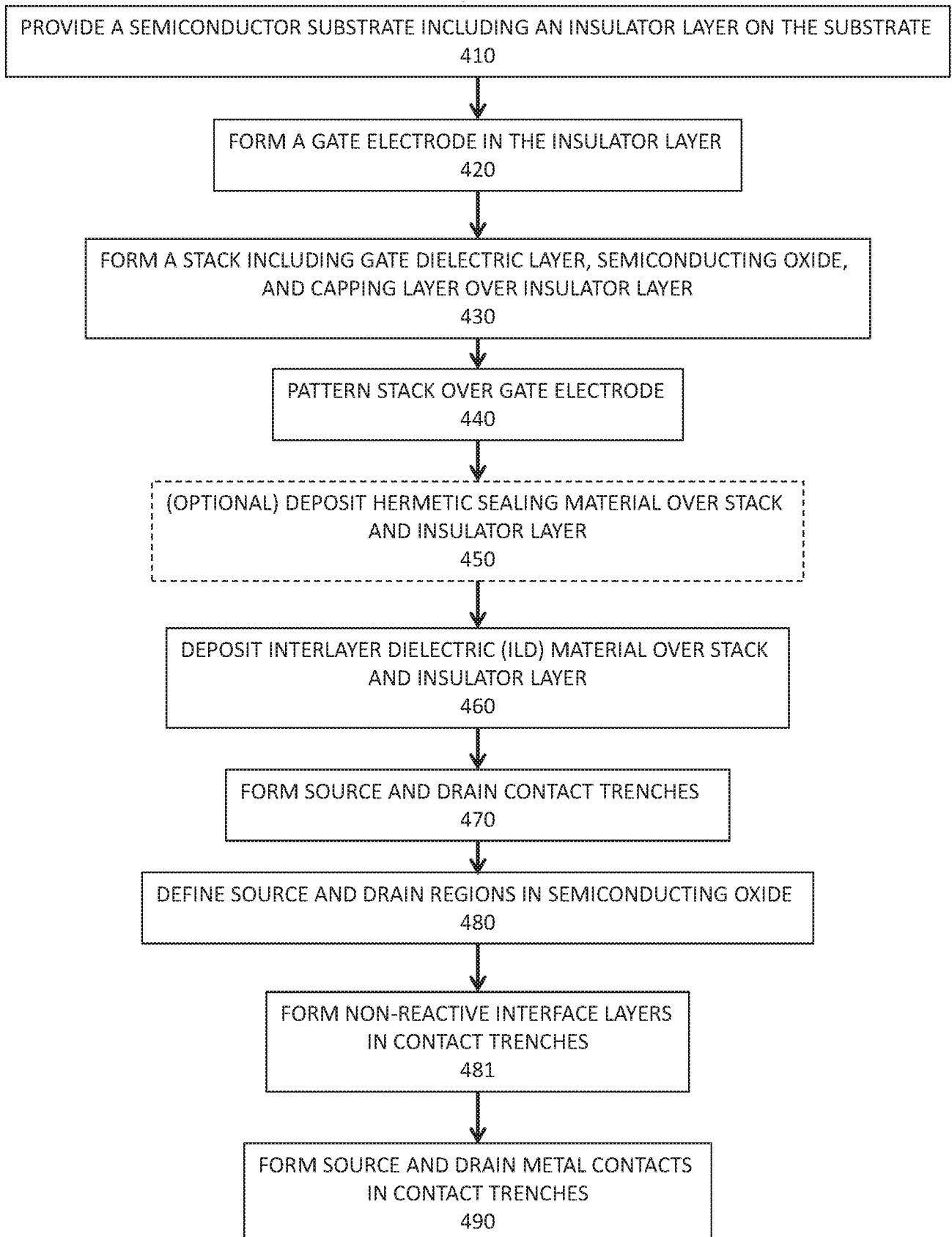


FIG. 3C

**FIG. 4A**

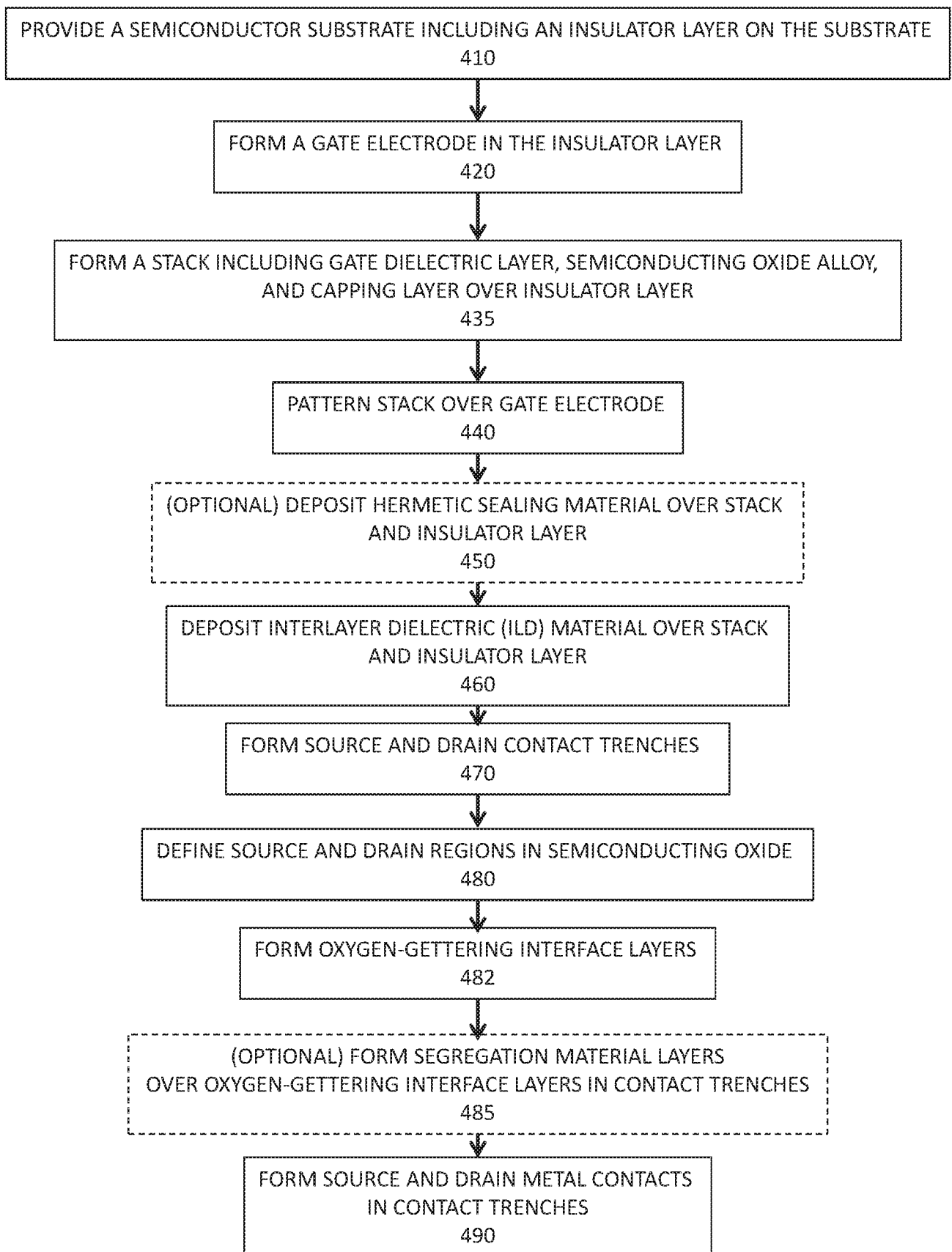


FIG. 4B

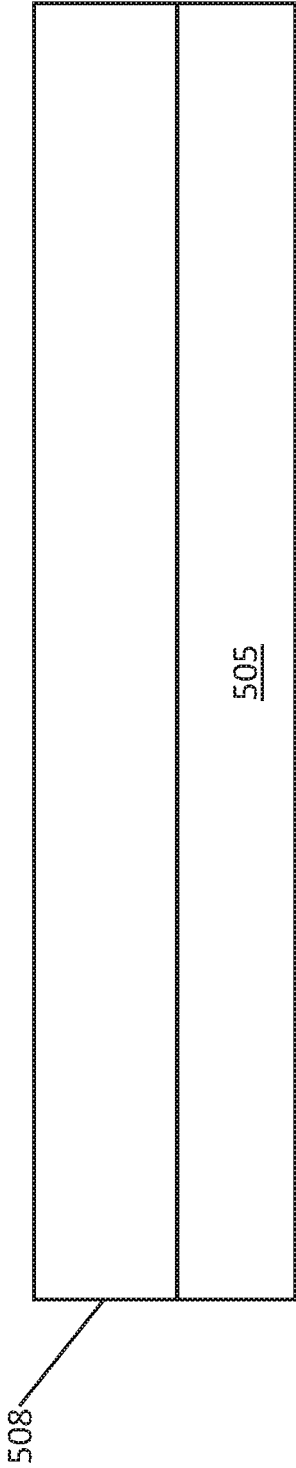


FIG. 5A

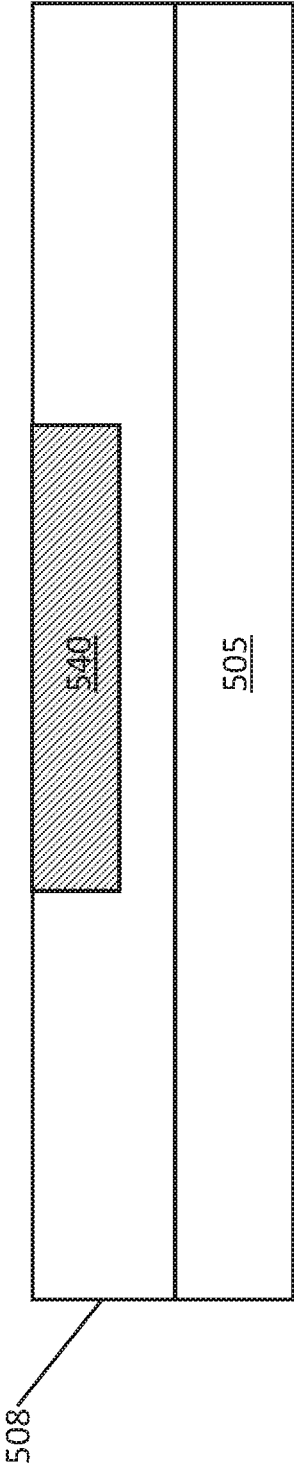


FIG. 5B

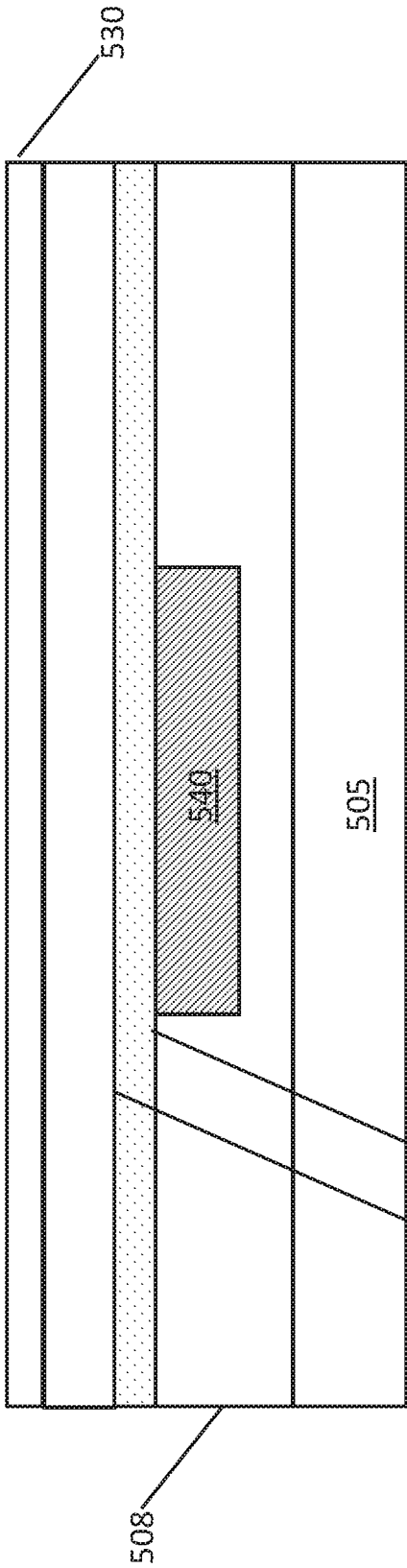


FIG. 5C

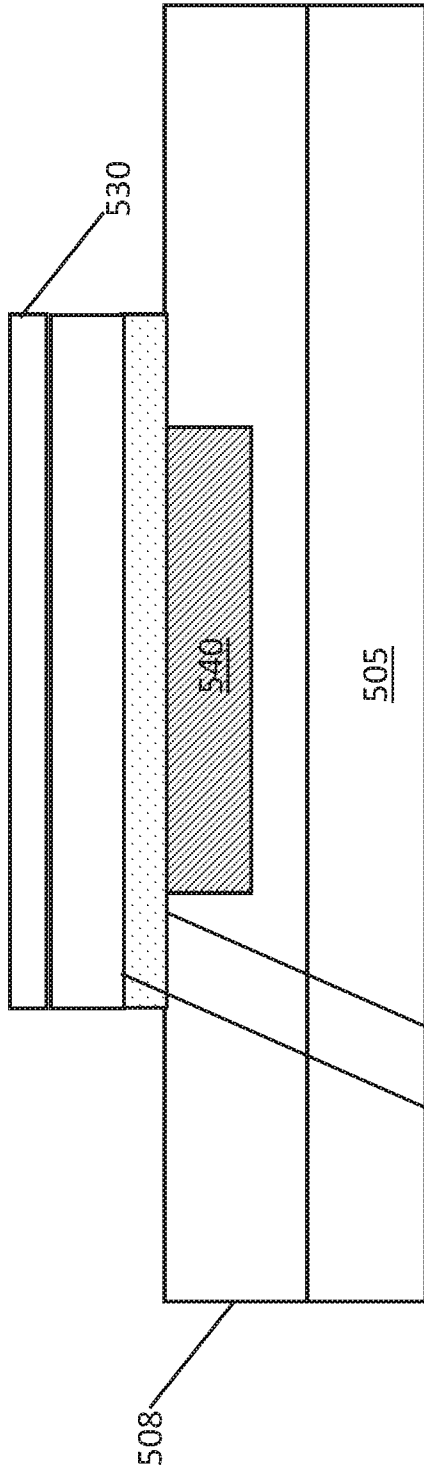


FIG. 5D

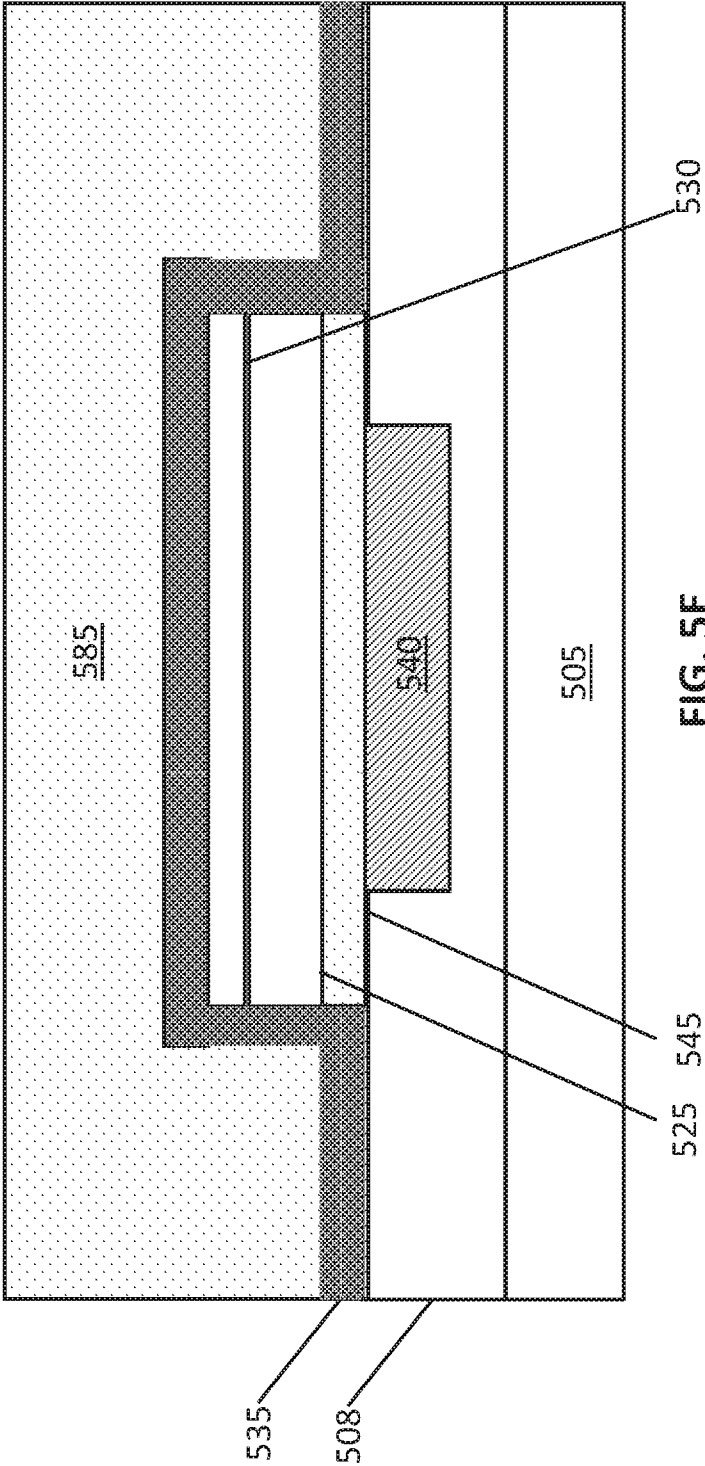
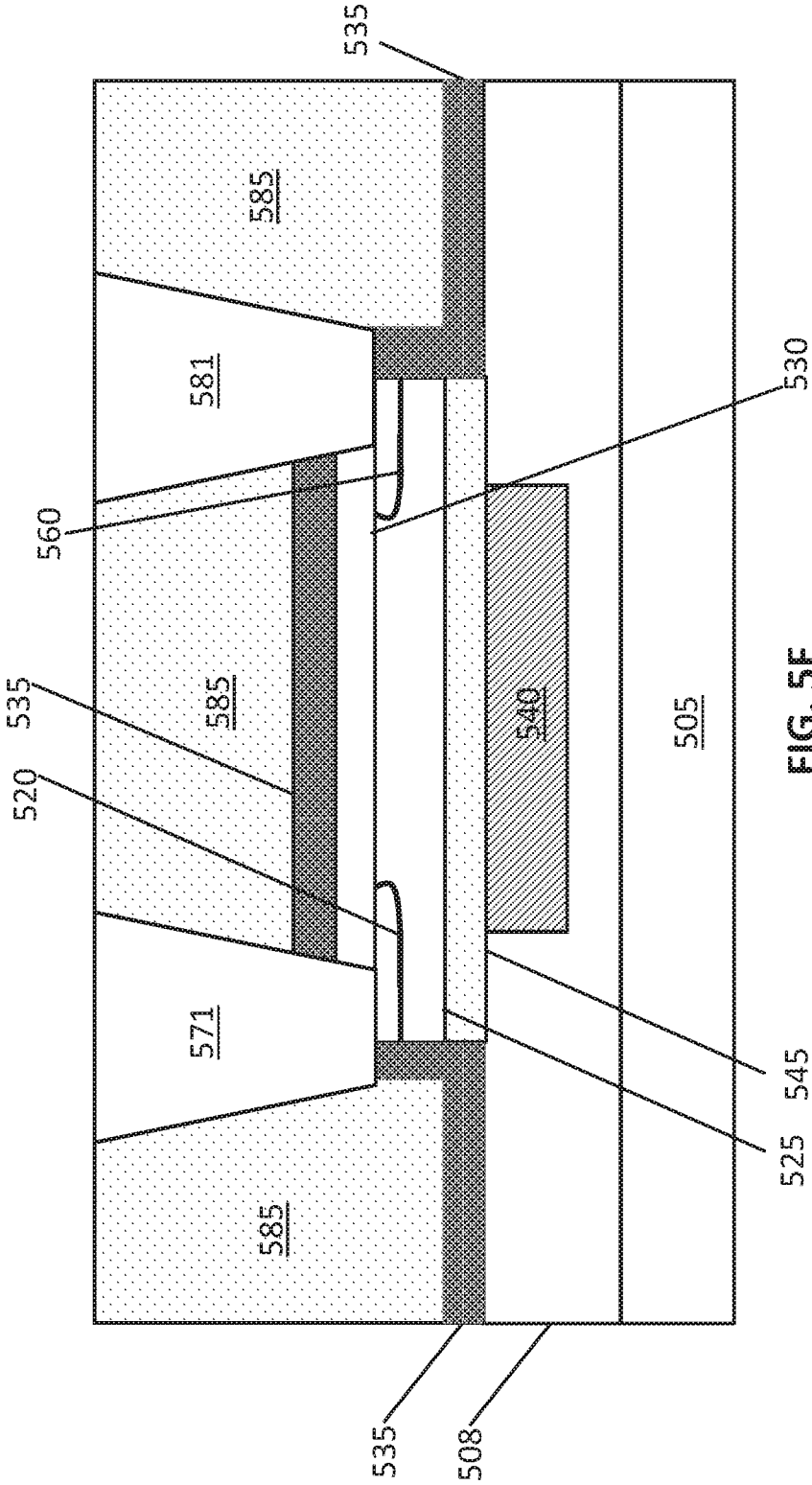


FIG. 5E



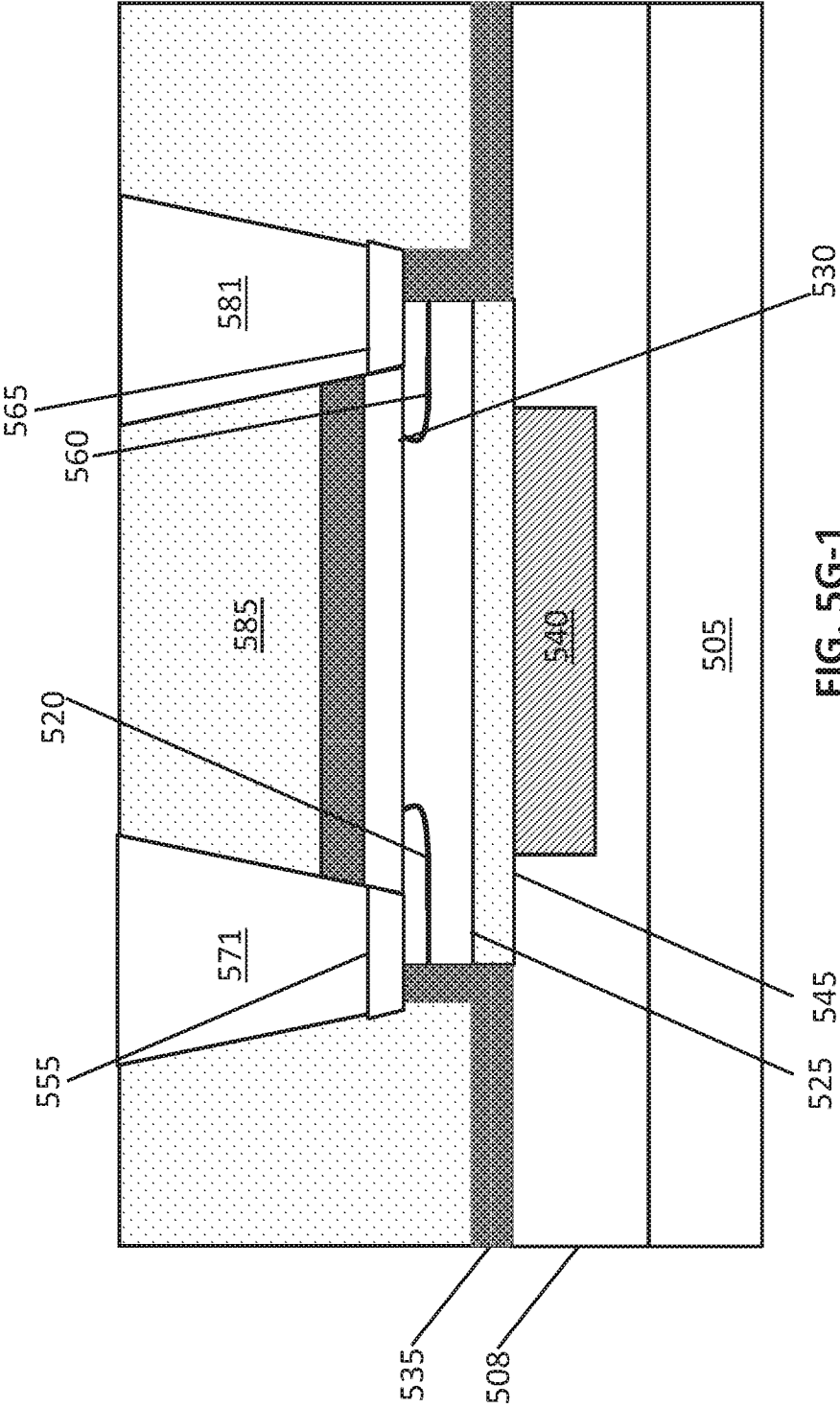


FIG. 5G-1

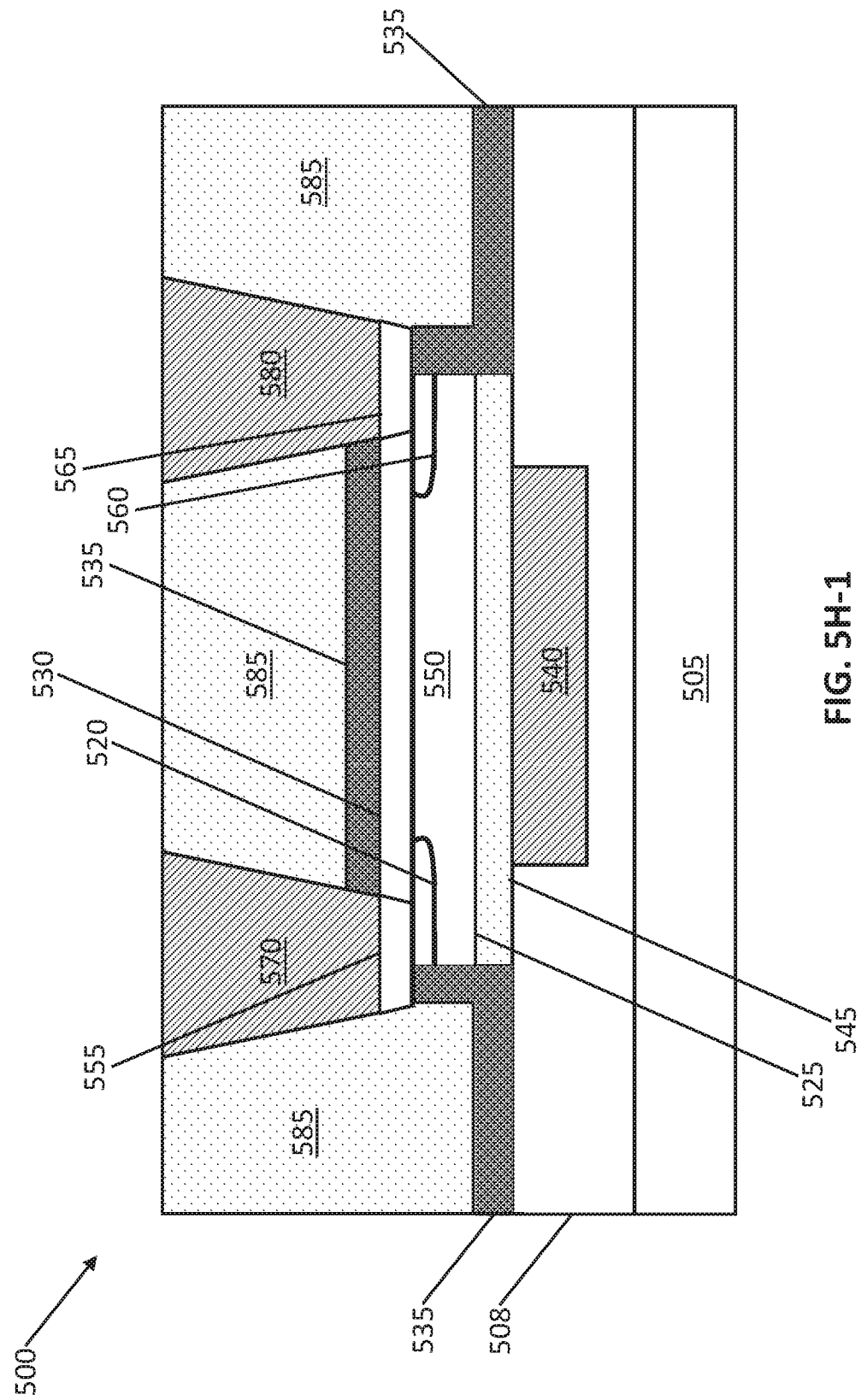


FIG. 5H-1

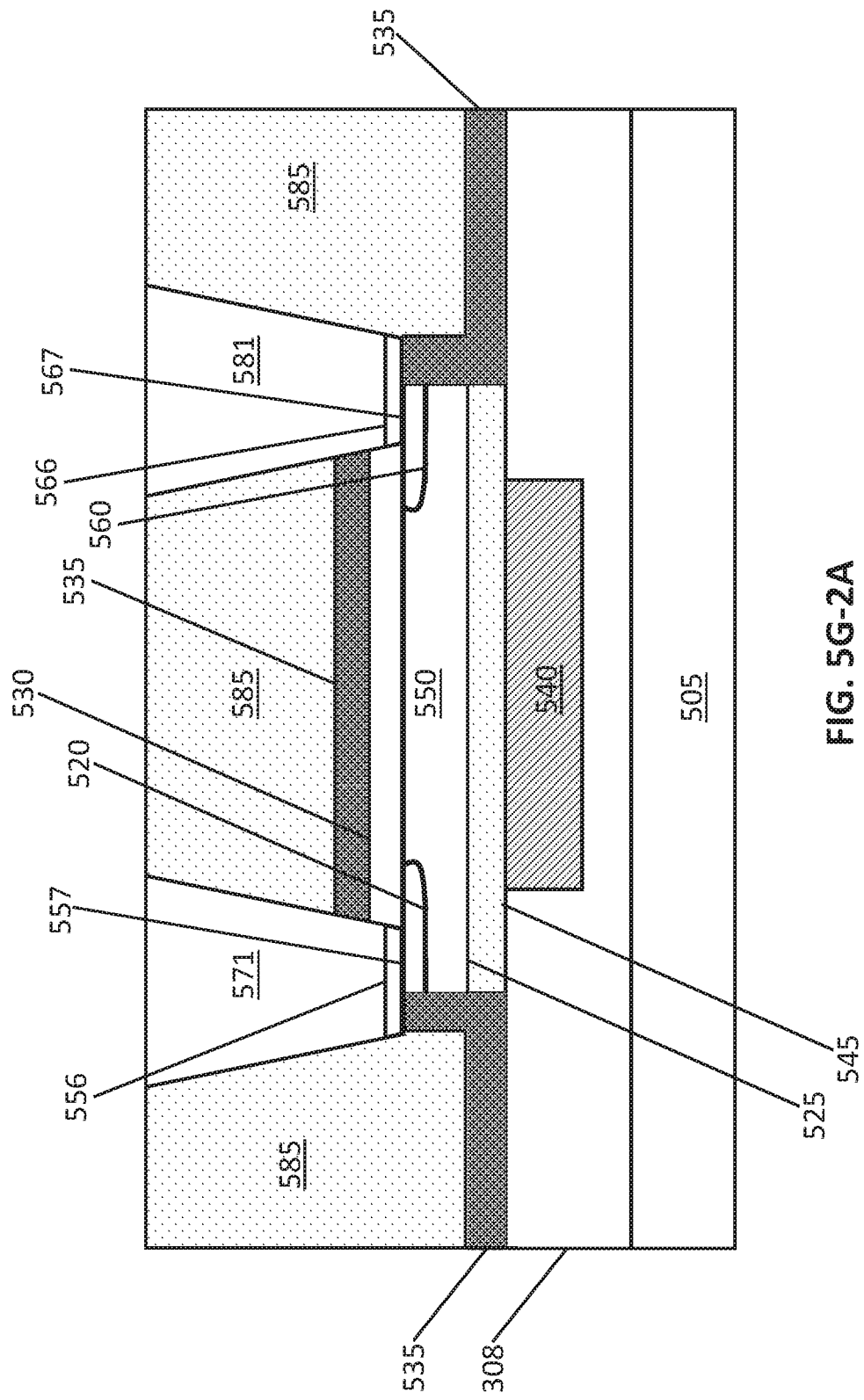


FIG. 5G-2A

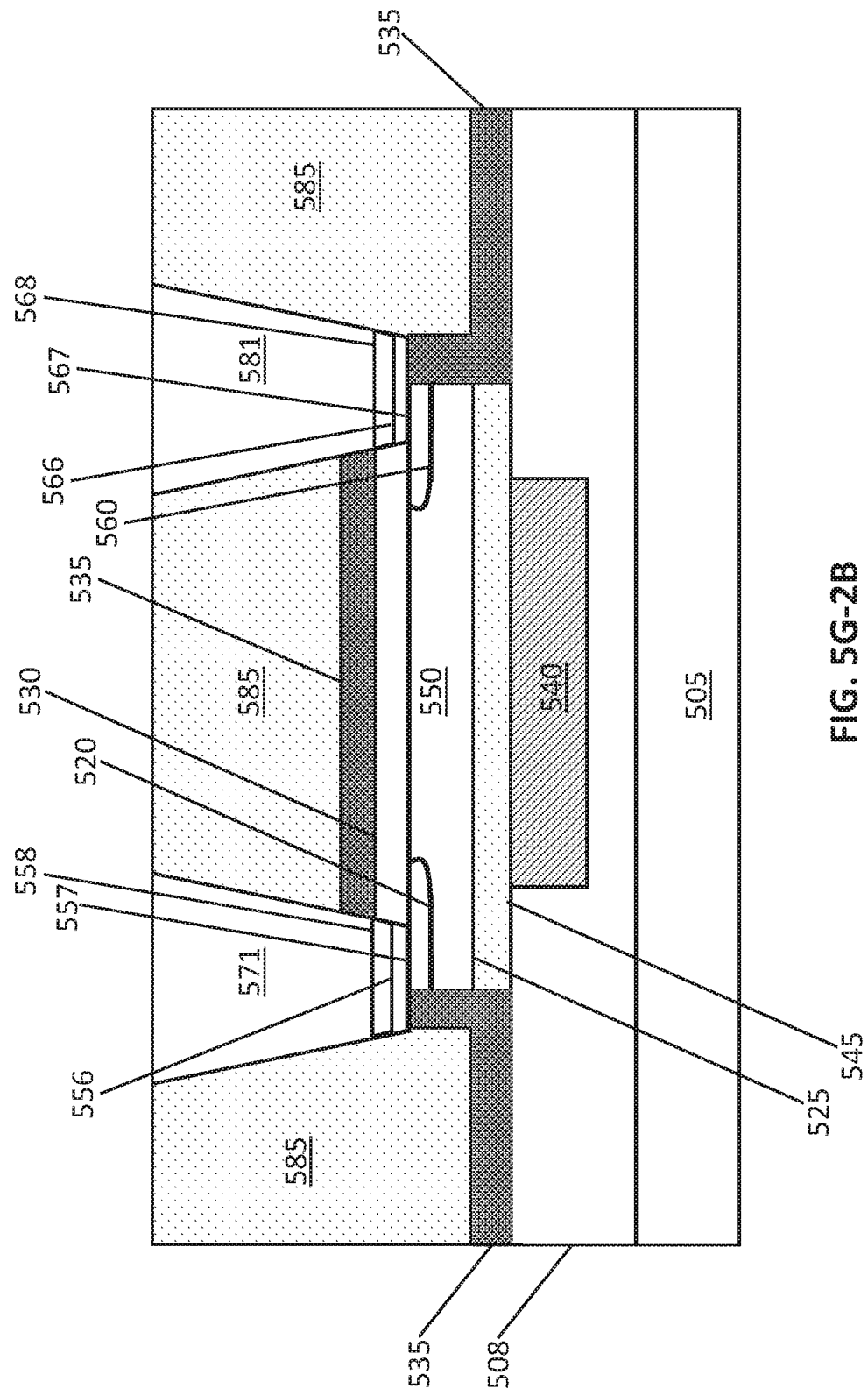


FIG. 5G-2B

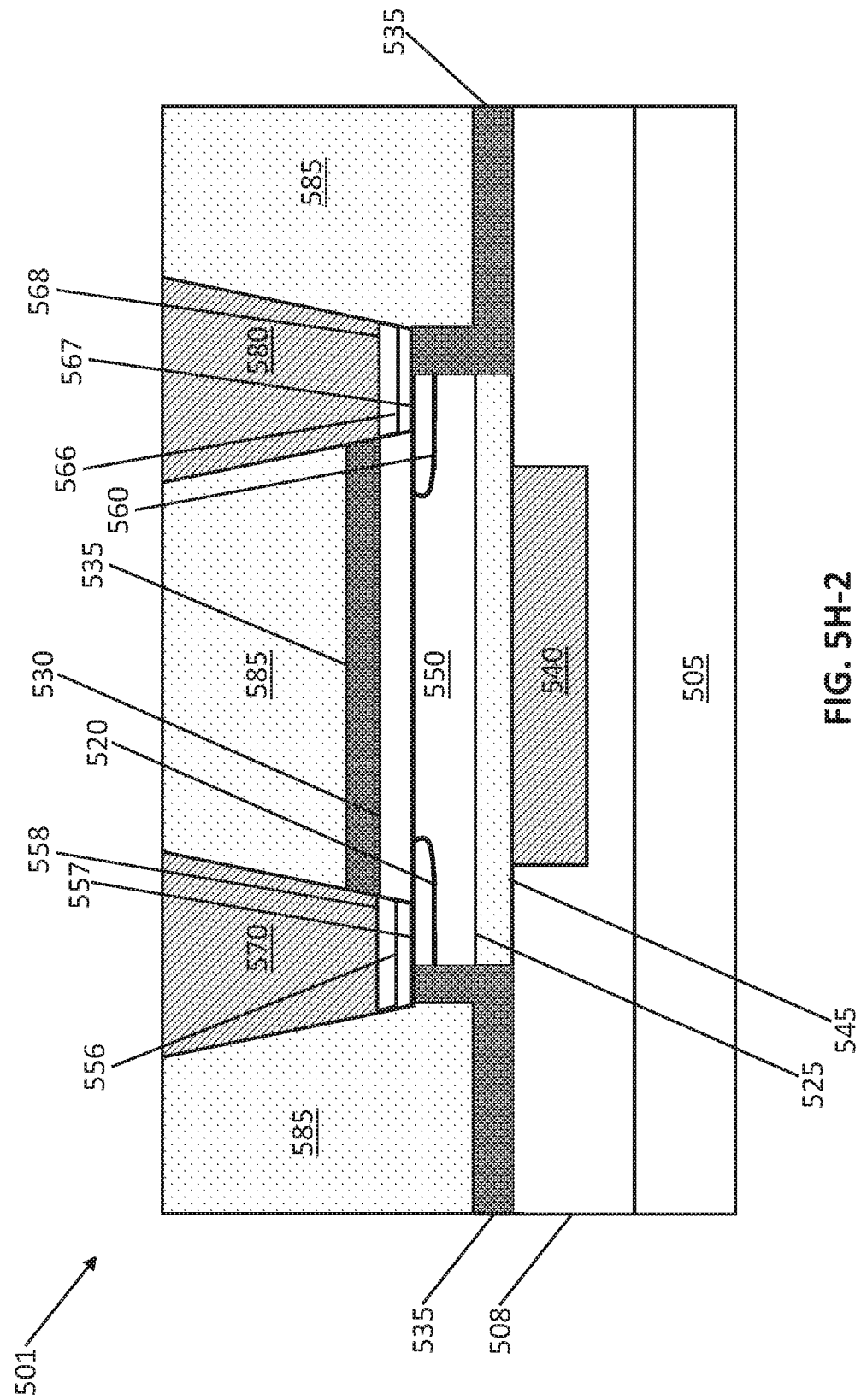
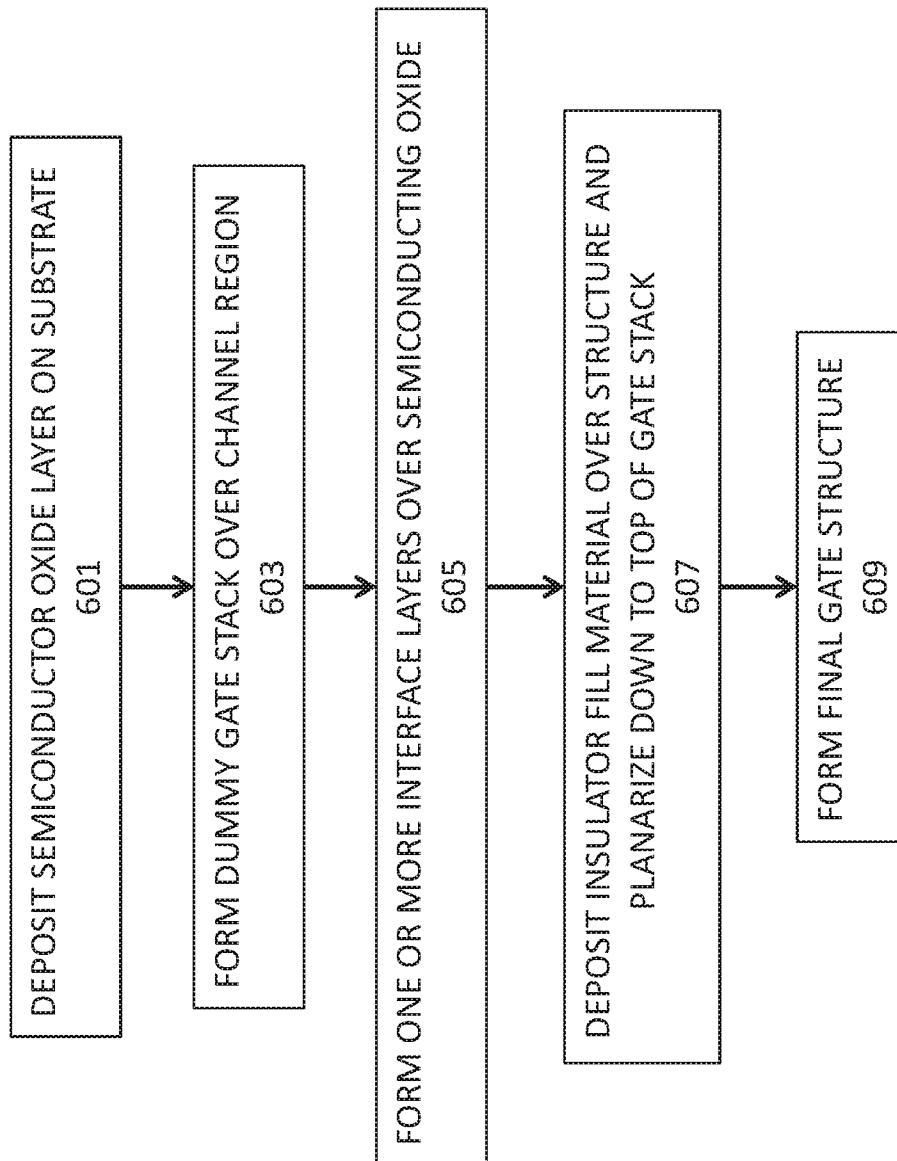


FIG. 5H-2

**FIG. 6**

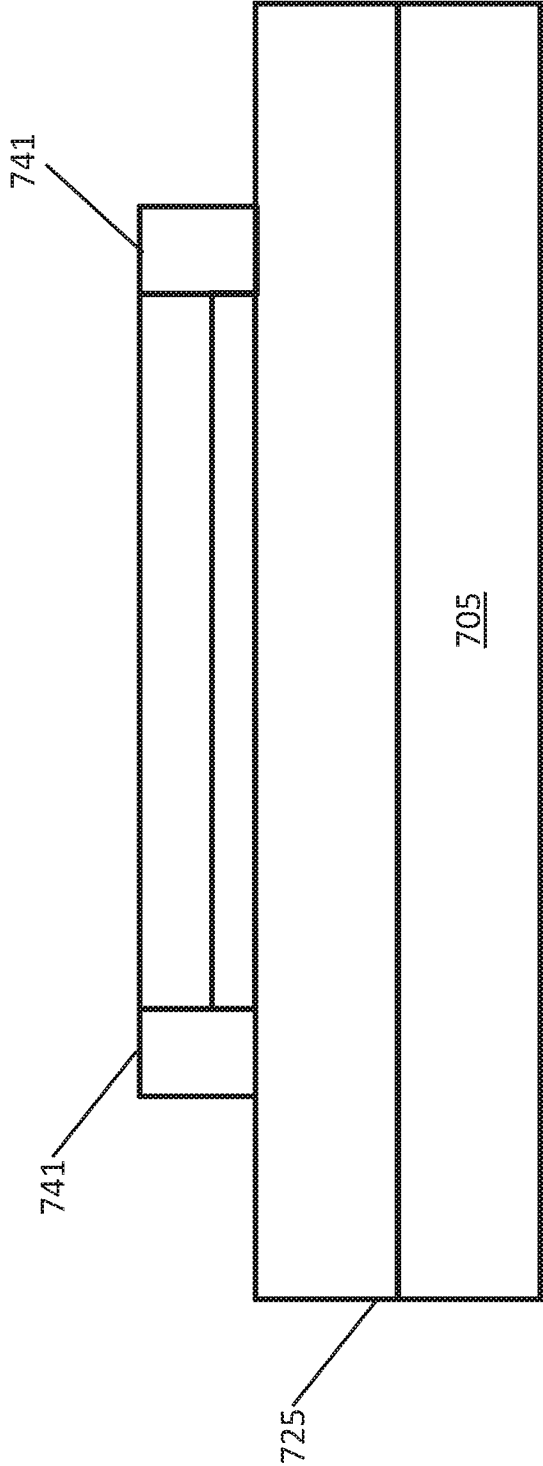


FIG. 7A

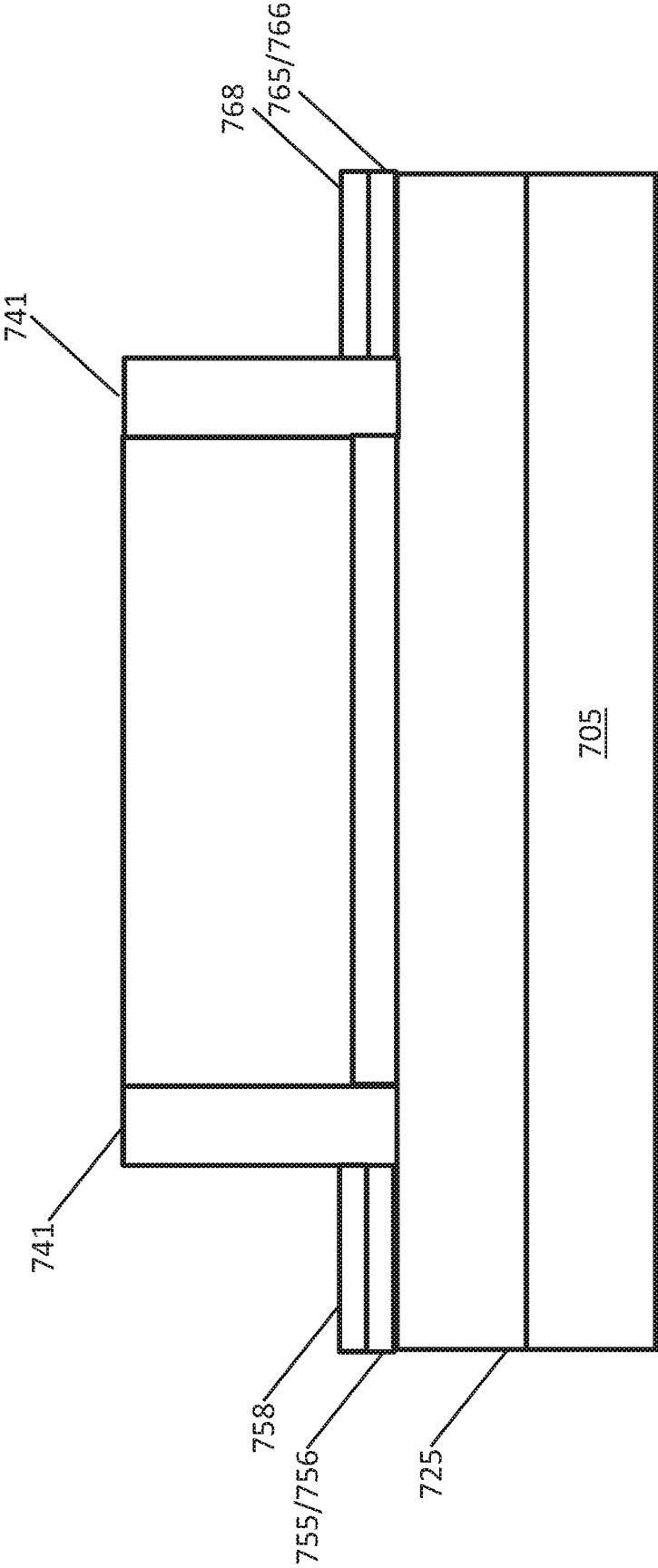


FIG. 7B

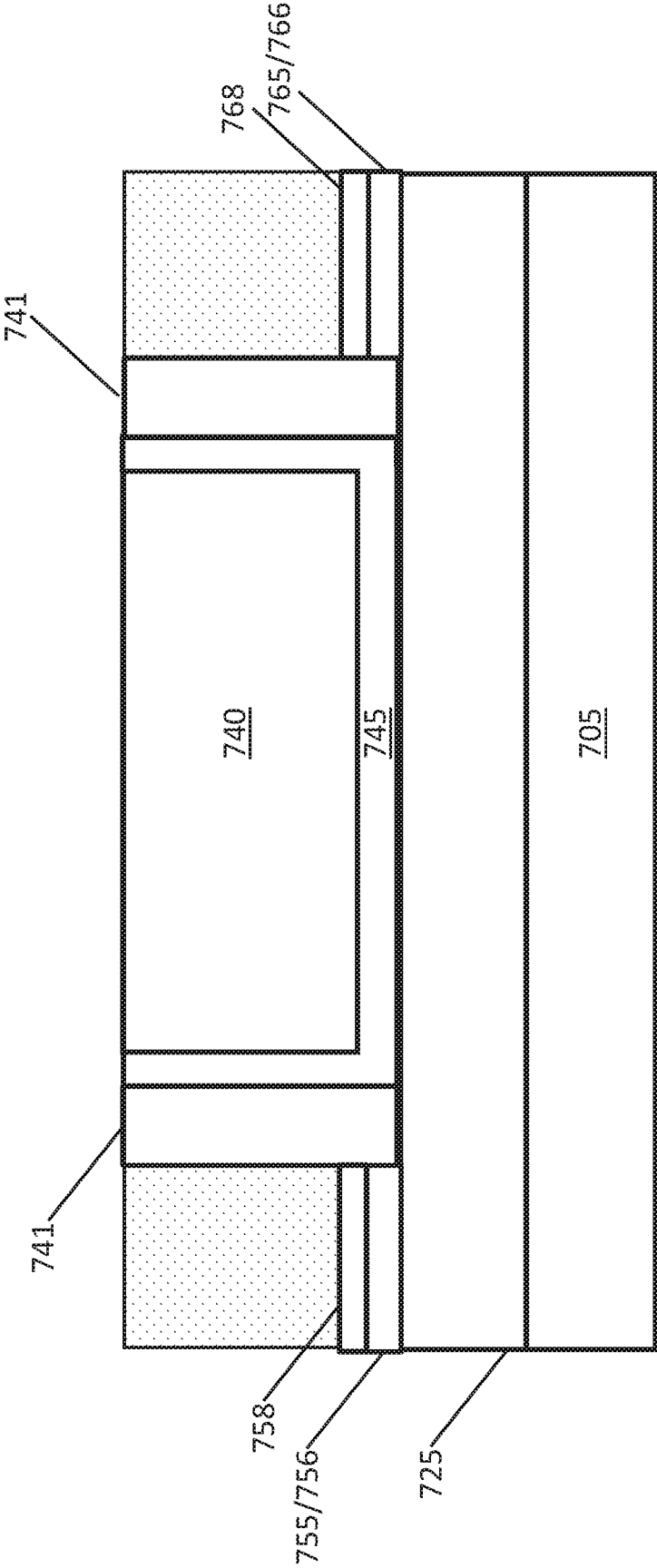


FIG. 7C

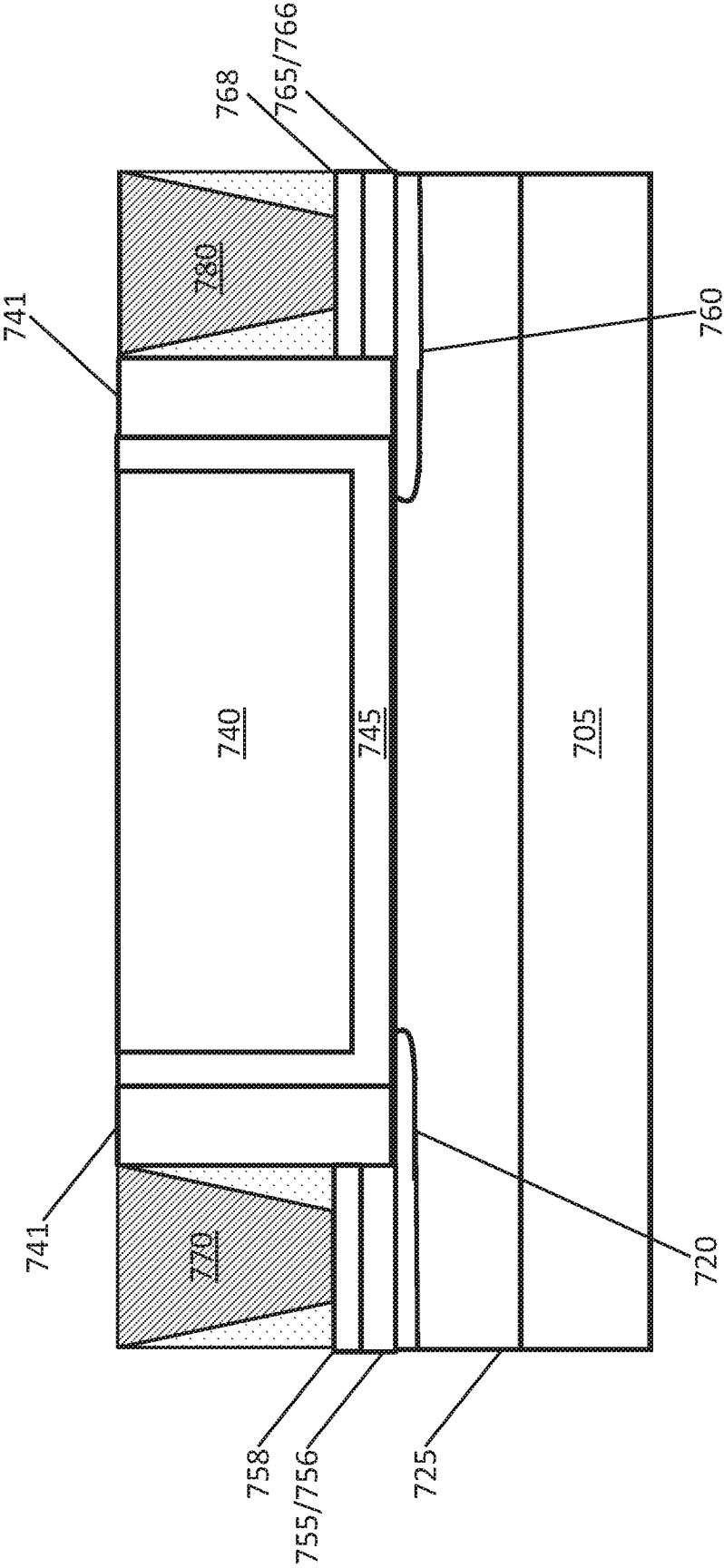


FIG. 7D

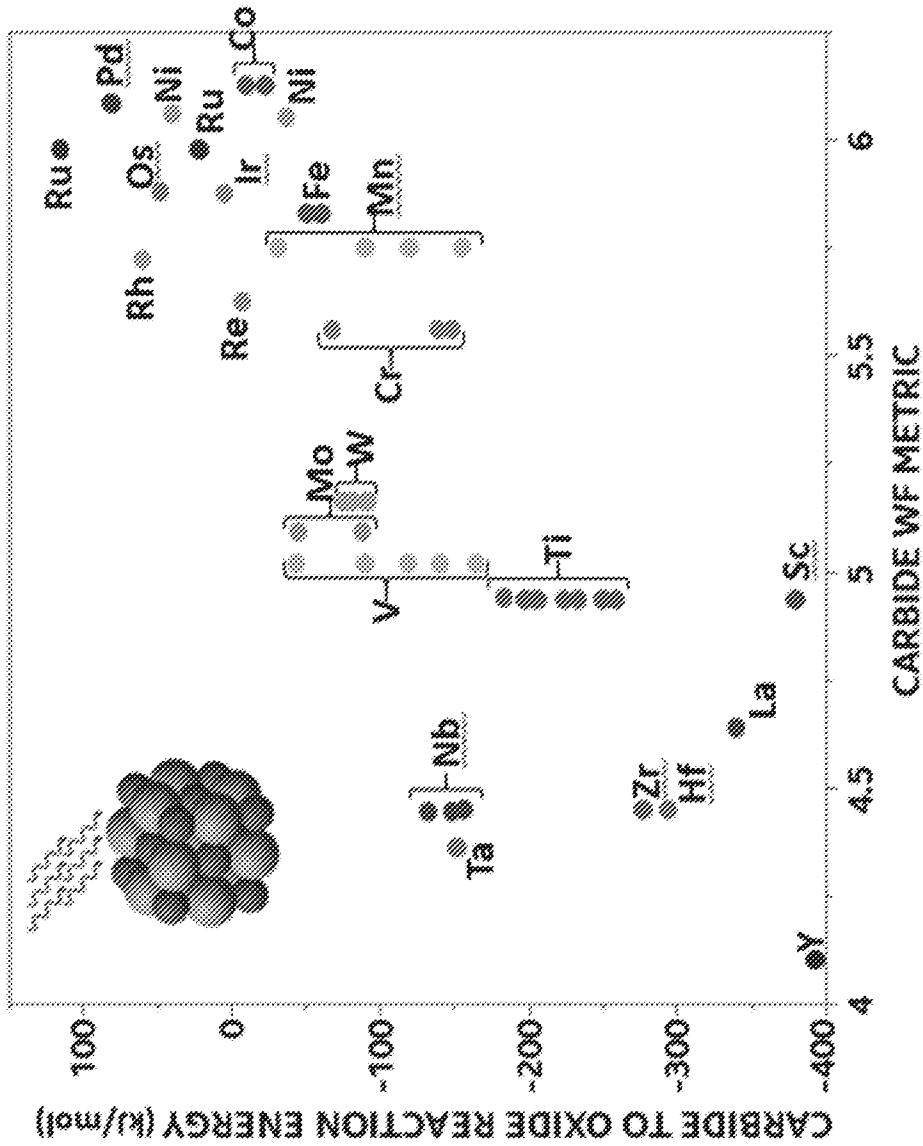


FIG. 8A

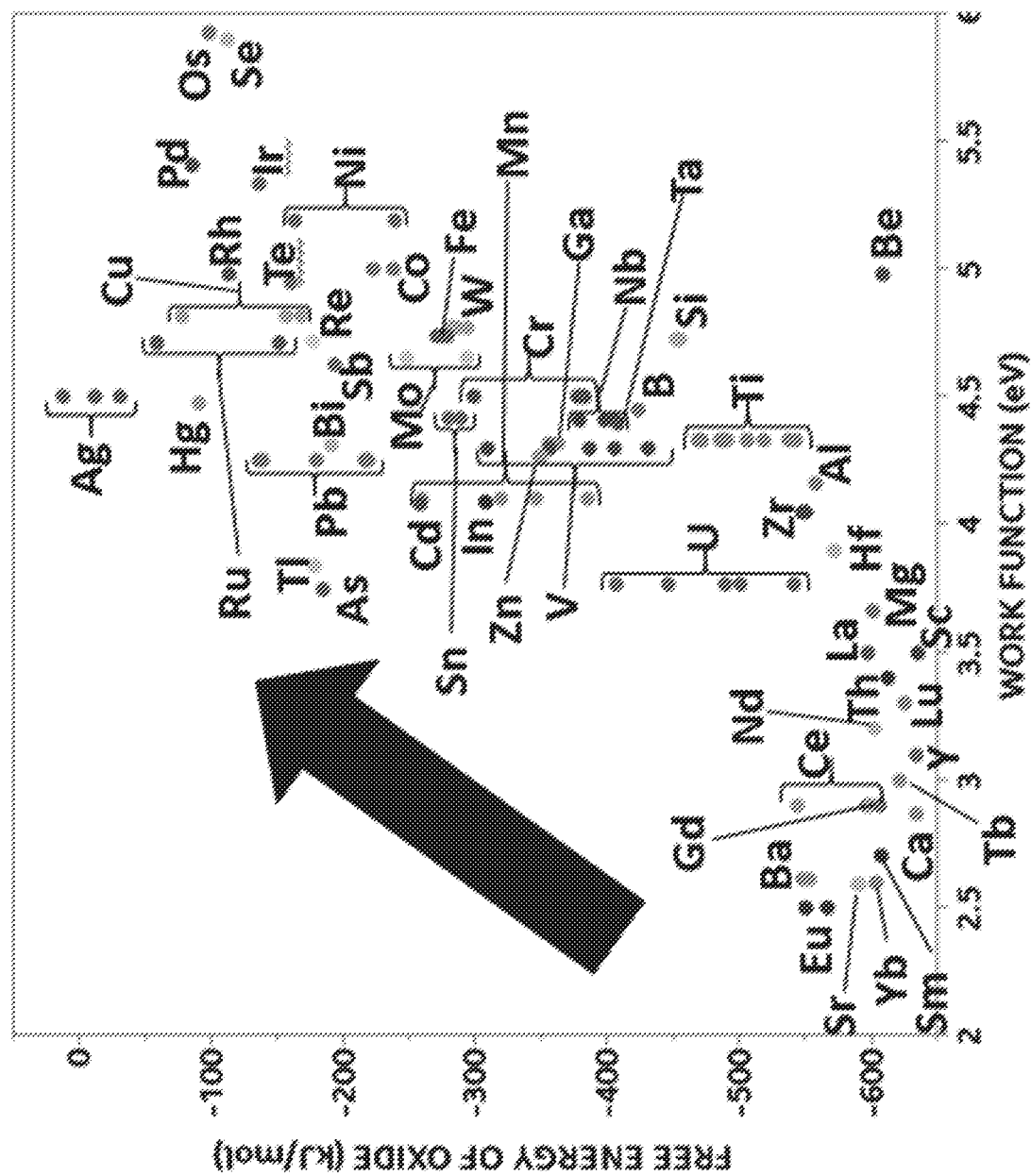


FIG. 8B

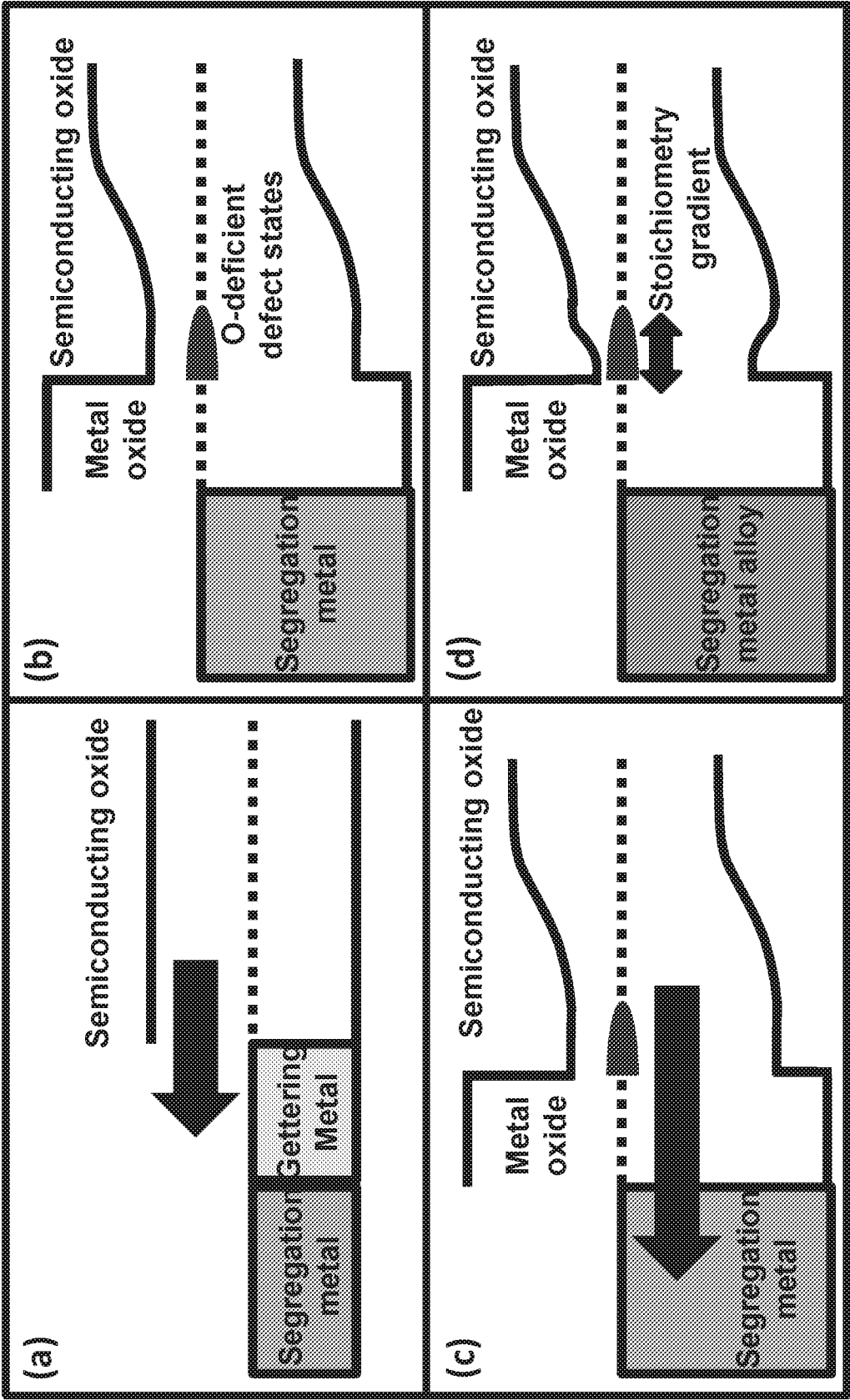


FIG. 8C

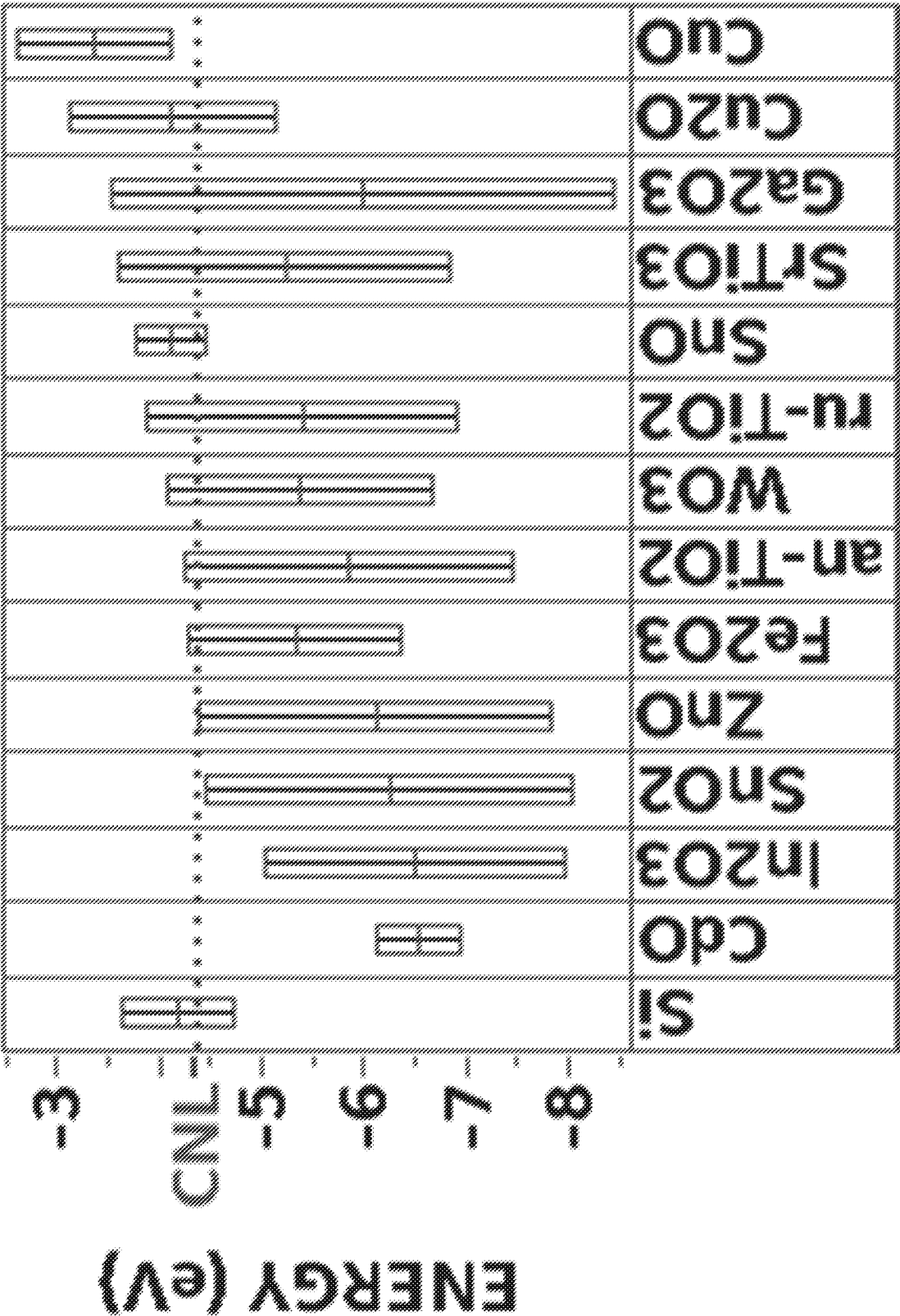
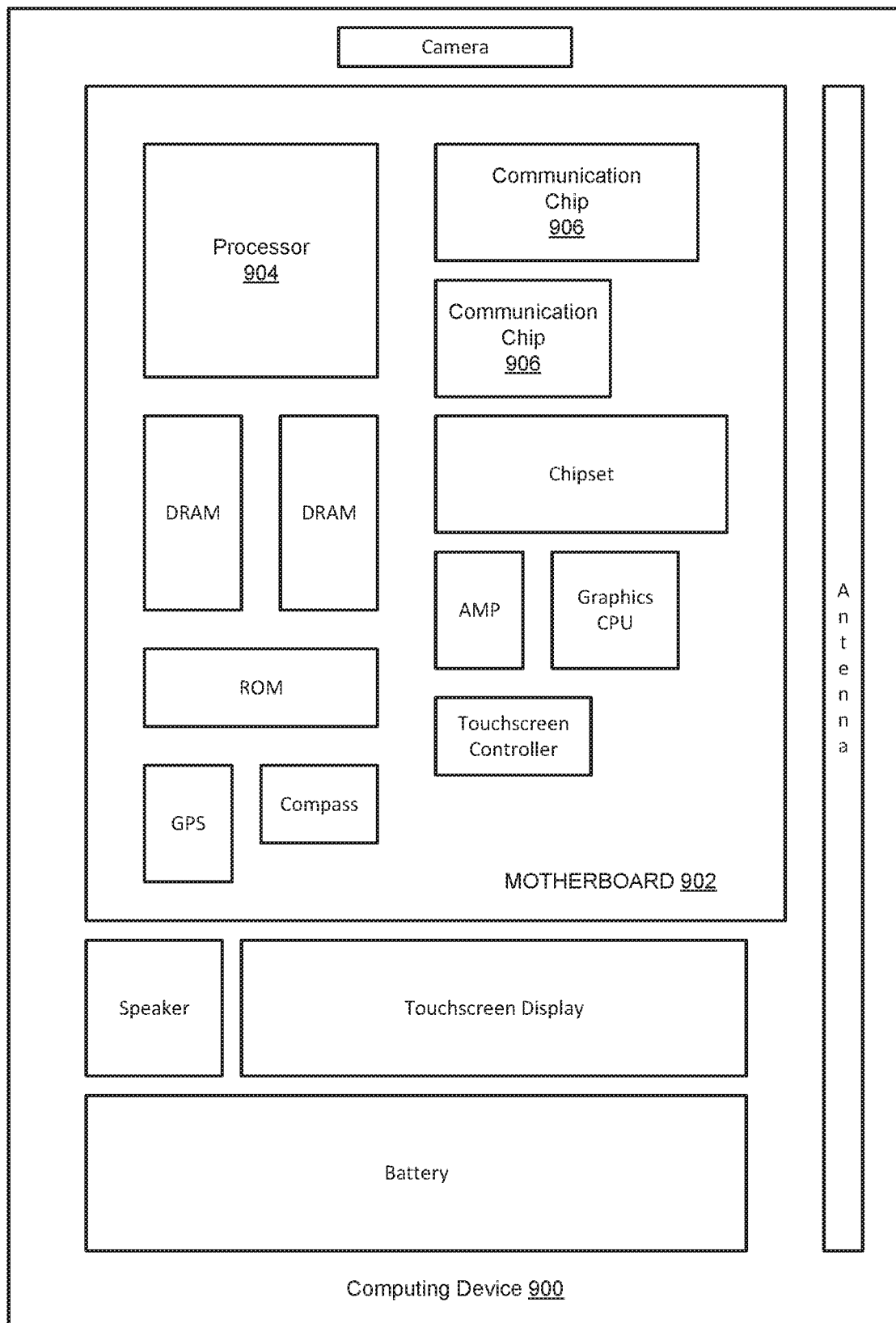


FIG. 8D

**FIG. 9**

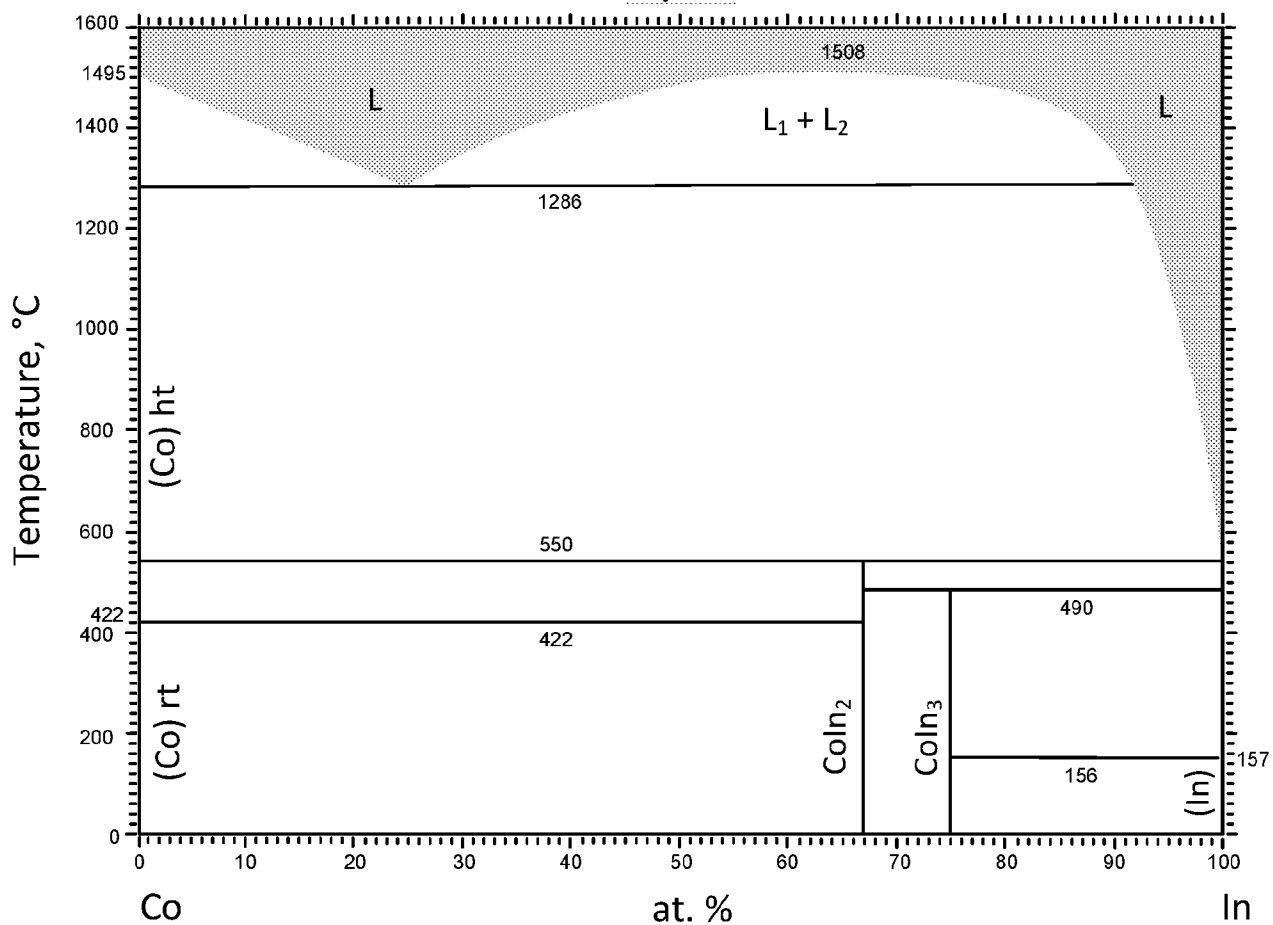


FIG. 10A

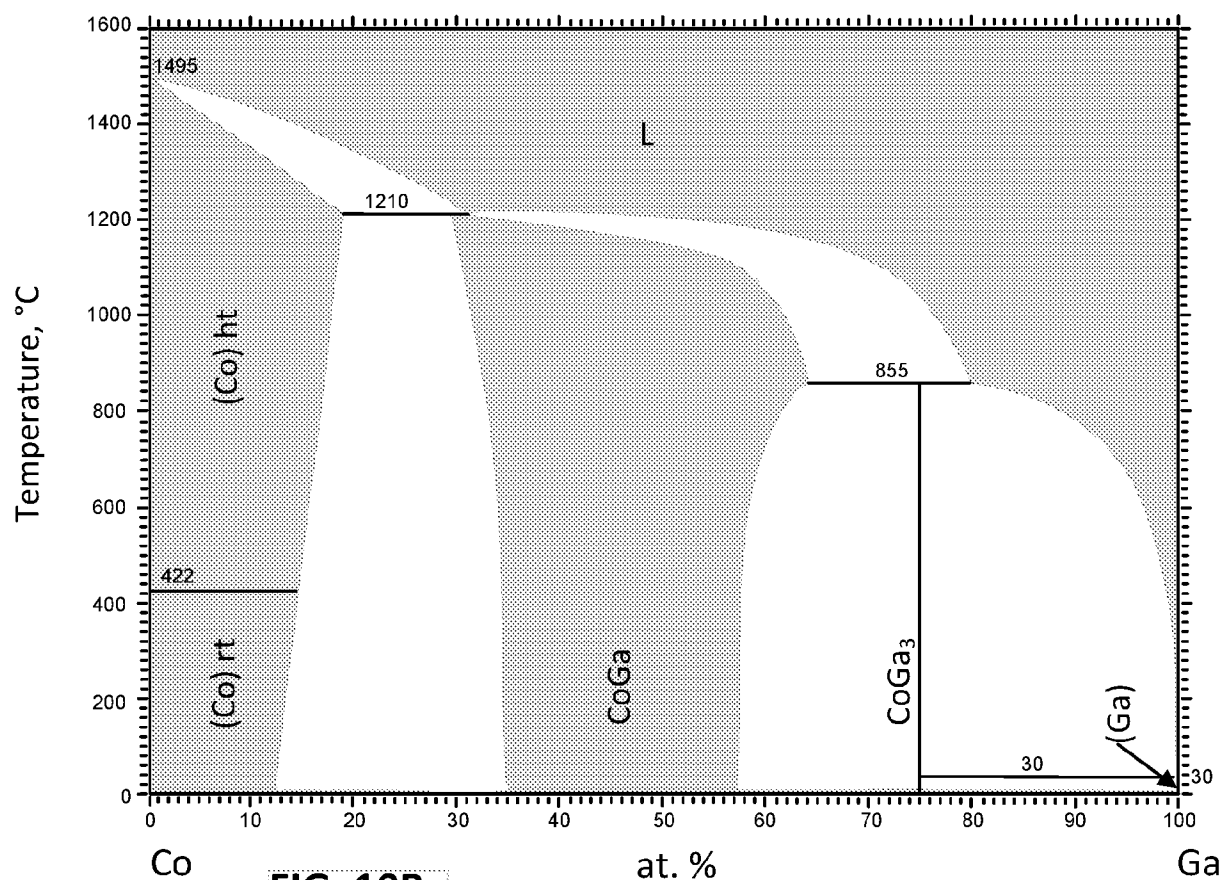


FIG. 10B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/027218**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/8238(2006.01)i, H01L 29/417(2006.01)i, H01L 29/66(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/8238; H01L 21/768; H01L 31/0392; H01L 21/67; H01L 29/78; H01L 29/786; H01L 29/417; H01L 21/00; H01L 29/66

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords:transistor, semiconducting oxide, resistance, oxygen-gettering material

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2014-0308812 A1 (REZA ARGHAVANI et al.) 16 October 2014 See paragraphs [0019], [0020] and figure 1.	1-24
A	US 2005-0017302 A1 (RANDY HOFFMAN) 27 January 2005 See paragraphs [0017], [0018] and figures 2, 3.	1-24
A	JP 2007-214481 A (TOSHIBA CORP.) 23 August 2007 See paragraphs [0020]-[0026] and figures 3, 4.	1-24
A	KR 10-0983544 B1 (KOREA ADVANCED INSTITUTE OF SCIENCE AND TECHNOLOGY) 27 September 2010 See paragraphs [0050]-[0056] and figures 3a-7d.	1-24
A	US 8647031 B2 (RANDY L. HOFFMAN et al.) 11 February 2014 See column 11, line 41 - column 12, line 3.	1-24



Further documents are listed in the continuation of Box C.



See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

30 January 2018 (30.01.2018)

Date of mailing of the international search report

30 January 2018 (30.01.2018)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/027218

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