(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
19 June 2008 (19.06.2008)

PCT

(10) International Publication Number
WO 2008/071905 A1

(51) International Patent Classification:
H01L 23/485 (2006.01)

(21) International Application Number:
PCT/GB2007/004500

(22) International Filing Date:
26 November 2007 (26.11.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
0624888.4 13 December 2006 (13.12.2006) GB

(71) Applicant *(for all designated States except US)*: **CAMBRIDGE SILICON RADIO LIMITED** [GB/GB]; Unit 400, Cambridge Science Park, Milton Road, Cambridge CB4 OWH (GB).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **STACEY, Simon, Johathan** [GB/GB]; 34 Alpe Street, Ipswich, Suffolk (GB).

(74) Agent: **PHILIP, Roy, Slingsby**; Page White & Farrer, Bedford House, John Street, London WC1N 2BF (GB).

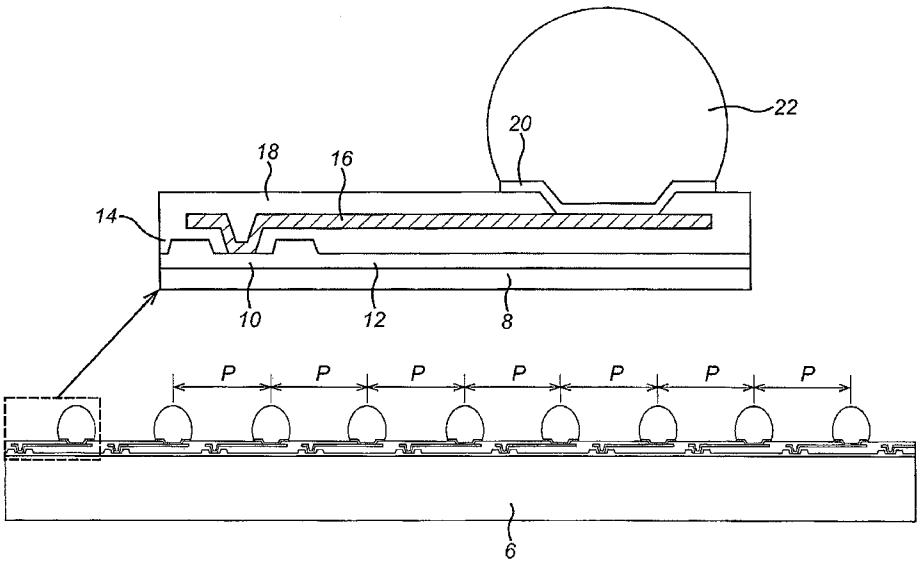
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *with amended claims*

Date of publication of the amended claims: 21 August 2008

(54) **Title:** CHIP MOUNTING



(57) **Abstract:** A device comprising a chip including a substrate defining one or more electronic devices and a printed circuit board electrically connected to the chip via one or more solder elements sandwiched between the chip and the printed circuit board, and the solder elements, said buffer layers having a Young's Modulus of 2.5GPa or less.

WO 2008/071905 A1

AMENDED CLAIMS
received by the International Bureau on 8th July 2008 (08.07.08)
original claims 1-22 remplaced by new claims 1-19.

1. A chip including a substrate defining one or more electronic devices and one or more solder elements located within the area of the chip and electrically connected to said one or more electronic devices, wherein the chip is provided with two buffer layers between the substrate and the solder elements and a patterned conductive layer sandwiched between the said buffer layers for electrically connecting said one or more solder elements to said one or more electronic devices, said buffer layers each having a Young's Modulus in the range of 1.6GPa to 2.4GPa.

2. A chip according to claim 1, wherein said buffer layers have a total thickness of more than 3 microns.

3. A chip according to claim 2, wherein said buffer layers have a total thickness in the range of 4 to 8 microns.

4. A chip according to claim 2, wherein said buffer layers have a total thickness of more than 10 microns.

5. A chip according to claim 4, wherein said buffer layers have a total thickness in the range of 13 to 20 microns.

6. A chip according to claim 4, wherein each of said two buffer layers has a thickness of more than 5 microns.

7. A chip according to claim 6, wherein each of said two buffer layers has a thickness in the range of about 6.5 microns to about 10 microns.

8. A chip according to claim 7, wherein each of said two buffer layers has a thickness of about 7.5 microns.

9. A chip according to any preceding claim, wherein said two buffer layers have the same composition.

10. A chip according to any preceding claim, wherein the two buffer layers each have a Young's Modulus of about 2 GPa.

11. A chip according to any preceding claim, wherein each buffer layer is located between each solder element and the substrate.

12. A chip according to any preceding claim, comprising an array of said solder elements spaced at a pitch of 0.5mm or less.

13. A chip according to any preceding claim, comprising an array of said solder elements spaced at a pitch of 0.4mm or less.

14. A chip according to any preceding claim, wherein the one or more solder elements are tin-based solder elements having a composition including about 4%wt. silver, and about 0.5%wt. copper.

15. A chip according to any preceding claim, wherein the solder elements are solder balls.

16. A chip according to any preceding claim, wherein the solder elements are solder bumps.

17. A chip according to any preceding claim, wherein the substrate is a semiconductor wafer.

18. A device comprising a chip as claimed in any preceding claim and a printed circuit board electrically connected to the chip via said one or more solder elements sandwiched between the chip and the printed circuit board.

19. A wireless communication device including a chip according to any of claims 1 to 17 or a device according to claim 18.