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(54) Title: WAFER LEVEL PACKAGING OF MEMS DEVICES

(57) Abstract: A MEMS device is disclosed. The MEMS device comprises a MEMS substrate and a CMOS substrate having a front surface, a back surface and one or more metallization layers. The front surface being bonded to the MEMS substrate. The MEMS device includes one or more conductive features on the back surface of the CMOS substrate and electrical connections between the one or more metallization layers and the one or more conductive features.

WAFER LEVEL PACKAGING OF MEMS DEVICES

CROSS-REFERENCE TO RELATED APPLICATION

[0001] Under 35 USC 119(e), this application claims priority to U.S. provisional application serial no. 61/452,545 filed on March 14, 2011.

FIELD OF THE INVENTION

[0002] The present invention relates generally to semiconductor devices, and more particularly to packaging of MEMS devices.

BACKGROUND OF THE INVENTION

[0003] Wafer-level packaging of semiconductor devices is a relatively new but widely used technology that allows semi-conductor and MEMS devices to be packaged on a wafer scale with solder balls attached directly to the die (typically through a stress-relief layer). This technology yields the smallest possible package size for any given device while at the same time reducing packaging cost by packaging an entire wafer of die in a batch process. The most common wafer-level packaging technologies (ex. Shellcase, uBGA, WAVE, and others) typically make direct contact to the CMOS wafer metallization, but cannot easily contact the top-layer of the MEMS since it is typically electrically isolated from the CMOS. In cases where the MEMS handle or cap wafer or a metal layer deposited onto the MEMS handle or cap wafer must be electrically contacted, the current wafer-level packaging technologies cannot be directly applied.

[0004] Accordingly, what is desired is a system and method which would overcome the above-identified issues. The method and system should be easy to implement, cost-effective, and adaptable to existing systems. The present invention addresses such a need.

SUMMARY OF THE INVENTION

[0005] A MEMS device is disclosed. The MEMS device comprises a MEMS substrate and a CMOS substrate having a front surface, a back surface and one or more metallization layers. The front surface being bonded to the MEMS substrate. The MEMS device includes one or more conductive features on the back surface of the CMOS substrate and electrical connections between the one or more metallization layers and the one or more conductive features.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Figure 1 is a diagram of a semiconductor device in accordance with an embodiment.

[0007] Figure 2A is a flow chart of a packaging process in accordance with the present invention.

[0008] Figure 2B is a diagram which illustrates building up a wafer level package utilizing the process of Figure 2A.

DETAILED DESCRIPTION

[0009] The present invention relates generally to semiconductor devices, and more particularly to the packaging of MEMS devices. The following description is

presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiments and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present invention is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features described herein.

[0010] A MEMS device often requires a MEMS handle electrical contact. This contact can either be used for RF shielding of the device or to make electrical contact to a MEMS handle wafer. A method and system in accordance with the present invention enables wafer-level packaging (WLP) also known as wafer-level chip scale packaging (WLCSP), of such MEMS devices using CMOS-side contact based on a Shellcase or Through Silicon Via (TSV) process, or any other wafer-level packaging process providing a CMOS-side electrical contact, while still providing a MEMS handle-side electrical connection.

[0011] The structure and process for wafer-level packaging of MEMS devices comprises:

[0012] 1. A MEMS device wafer comprising a CMOS substrate bonded to a MEMS substrate, the MEMS substrate comprising a handle wafer with cavities bonded to a patterned electrically conductive Device Layer with an insulating layer positioned between the two wafers.

[0013] 2. A top metallization layer electrically connected to the Device Layer comprising:

[0014] (a) A wedge-shaped opening penetrating completely through the Handle Wafer and insulating layers, and partially penetrating into the Device Wafer.

[0015] (b) A conducting layer deposited onto the MEMS substrate such that the conducting layer covers the sidewalls of the wedge-shaped opening including making physical contact to a portion of the Device Layer thereby electrically connecting the conductive layer to the portion of the Device layer. Optionally, the conducting layer may also make electrical contact to the Handle Wafer, thereby electrically connecting the Handle Wafer to the portion of the Device Wafer.

[0016] 3. One or more openings in the back-side of the CMOS substrate exposing one or more metal interconnection layer.

[0017] 4. An insulating layer coating the sidewalls of the one or more openings and the back-side of the CMOS substrate.

[0018] 5. A conductive layer coating the insulating layer on the back-side of the CMOS substrate and on sidewalls of the one or more openings and providing physical and electrical contact to the one or more metal interconnection layers.

[0019] 6. One or more solder-balls connected to the conductive layer.

[0020] In the preferred embodiment a MEMS bonded device wafer would comprise a standard CMOS wafer with an Aluminum or Copper top metallization layer eutecticly bonded to a MEMS wafer. To describe the features of the invention in more detail refer now to the following description in connection with the accompanying Figures. Figure 1 is a diagram of a semiconductor device 100 in accordance with an embodiment before processing. The semiconductor device

100 comprises a MEMS handle 102; a silicon oxide layer 103, a MEMS device layer 104, and a CMOS wafer 106.

[0021] The handle wafer 102 includes etched cavities and is coated by, for example, a thin silicon oxide layer and fusion bonded to a MEMS device layer 104. The MEMS device layer 104 is patterned to define the desired moveable or stationary structure.

[0022] Figure 2A is a flow chart of a packaging process in accordance with the present invention. Figure 2B is a diagram which illustrates building up a wafer level package utilizing the process of Figure 2A.

[0023] Referring now to Figures 2A and 2B together, initially both sides of the device (CMOS side 106 and MEMS handle 102), are ground down to the desired size, using step 202.

[0024] Thereafter, wedge shaped cuts are made in the non-functional region of the MEMS so as to cut completely through the handle wafer 102 and silicon oxide layer 103 and cut partially into the device layer 104, using step 204, leaving a wedge-shaped opening 108 in the device 100. In an alternate embodiment, the wedge-shaped opening can be created using a wet or dry etching of the handle wafer 102 and silicon oxide layer 103. The required wedge angle depends on the conformality of the metal deposition system used for the following metal deposition.

[0025] Next, a conductive metallization layer 110 is blanket deposited onto the MEMS side of the device 100, using step 206. The metallization (for example,

aluminum or copper) layer may be sputter deposited, evaporated, or deposited through plasma or thermally enhanced chemical vapor deposition (CVD).

[0026] The metallization layer 110 covers the top surface of the semiconductor device 100 as well as the side-walls of the wedge-shaped openings 108, thereby making a physical and electrical contact to the device layer 104. Due to the high doping of the device layer 104, an ohmic contact will be formed to the metallization layer 110. In some embodiments an additional anneal may be required to enhance diffusion of metallization into silicon to enhance electrical contact. In an alternate embodiment, the metallization layer 110 may comprise any electrically conductive metal or semi-conductor.

[0027] Next the device is packaged using a through-silicon-via (TSV) wafer level packaging process.

[0028] The TSV process begins with an opening 112 being etched in the back of the CMOS substrate 106 stopping on one of the CMOS metallization layers, using step 208. The CMOS substrate 106 metallization layer 107 may be any one of the existing CMOS metallization layers. The sidewalls of the opening 112 are then electrically passivated by depositing an insulating film 109(ex. silicon oxide, silicon nitride, polymer), using step 210. Typically the insulating film 109 will also deposit on the bottom surface of the opening 112, covering the previously exposed CMOS metallization layer 107.

[0029] The CMOS metallization layer 107 is then once again exposed by an etching or saw dicing process such that the insulating film 109 on the sidewalls of the opening is not removed. This etching or saw dicing process may expose the

surface, edges, or both of the CMOS metallization layer 107. A conductive interconnection layer, 114, (typically a metal layer composed of Aluminum or Copper) is deposited onto the back surface of the CMOS substrate 106 and into the passivated openings 112 so as to create electrical contact to the CMOS metallization layer 107.

[0030] The interconnection layer 114 is then patterned so as to create individual isolated contacts. A polymer stress-relief layer 116 would optionally be deposited on top of the interconnection layer 114 to reduce stress on the silicon die caused by board-level assembly, using step 212. The stress-relief layer 116 is patterned so as to create vias to the interconnection layer 114. Then a conductive redistribution layer 118 is deposited and patterned on top of the stress-relief layer 116, using step 214. Finally, solder balls 120 are defined on top of the redistribution layer 118 to facilitate soldering the packaged die to a printed circuit board, using step 216.

[0031] In a first alternate embodiment, the die may be packaged using Shellcase wedge-dicing type wafer level packaging process.

[0032] In a second alternate embodiment, the die may be packaged using any available packaging technology using wire bonding including but not limited to a Leadless Chip Carrier (LCC), a Quad Flat No Leads (QFN) or a Multichip module.

[0033] In a third alternate embodiment, the openings in the handle-wafer side of the MEMS may be etched rather than saw-diced. Furthermore, a conductive layer may be any metal or semi-conductor and may be deposited using

sputtering, Chemical Vapor Deposition (CVD), Plasma-Enhance Chemical Vapor Deposition (PECVD), Molecular Vapor Deposition (MVD), or any other thin film deposition method with sufficient conformality.

[0034] Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those variations would be within the spirit and scope of the present invention. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.

CLAIMS

What is claimed is:

1. A MEMS device comprising:

a MEMS substrate;

a CMOS substrate having a front surface, a back surface and one or more metallization layers; the front surface being bonded to the MEMS substrate;

one or more conductive features on the back surface of the CMOS substrate; and

electrical connections between the one or more metallization layers and the one or more conductive features.

2. The MEMS device of claim 1, wherein the conductive features are solder balls.

3. The MEMS device of claim 1, wherein the conductive features include a second conductive redistribution layer

4. The MEMS device of claim 3, wherein a stress relief layer is formed beneath the second conductive redistribution layer

5. The MEMS device of claim 3, wherein the conductive features are solder balls.

6. The MEMS device of claim 1, wherein the electrical connections comprise

one or more openings in the back-surface of the CMOS substrate exposing the one or more metallization layers;

a second insulating layer coating the sidewalls of the one or more openings in the back surface of the CMOS substrate; and

a conductive layer coating the insulating layer on the back surface of the CMOS substrate and on sidewalls of the one or more openings and providing physical and electrical contact to the one of more metallization layers.

7. The MEMS device of claim 1, wherein the MEMS substrate comprises

a handle wafer bonded to a patterned electrically conductive device layer with an insulating layer positioned between the two wafers

8. The MEMS device of claim 7 further comprising

an opening penetrating completely through the handle wafer and the insulating layer, and exposing a device layer; and

a second conductive layer deposited onto the MEMS substrate such that the second conductive layer at least partially covers the surface of the MEMS substrate and the sidewalls of the opening include making physical contact to the device layer, wherein the conductive layer is electrically connected to the device layer.

9. A MEMS device comprising:

a MEMS substrate, wherein the MEMS substrate includes a handle wafer bonded to a patterned electrically conductive device layer with an insulating layer positioned between the two wafers;

an opening penetrating completely through the handle wafer and the insulating layer, and exposing the device layer; and

a conductive layer deposited onto the MEMS substrate such that the conductive layer at least partially covers the surface of the MEMS substrate and the sidewalls of the opening including making physical contact to the device layer thereby electrically connecting the conductive layer to the device layer.

10. The MEMS device of claim 9, wherein the opening has sloped sidewalls.

11. The MEMS device of claim 10, wherein a CMOS substrate is bonded to the MEMS substrate.

12. The MEMS device of claim 11, wherein one or more openings in the back-side of the CMOS substrate exposing one or more metal interconnection layer.

13. The MEMS device wafer of claim 12, wherein a second insulating layer coats the sloped sidewalls of the one or more openings in the back-side of the CMOS substrate.

14. The MEMS device wafer of claim 13, wherein the conductive layer coats the insulating layer on the back-side of the CMOS substrate and on sidewalls of the one or more openings and provides physical and electrical contact to the one of more metal interconnection layers.

15. The MEMS device wafer of claim 9, wherein one or more solder-balls are connected to the conductive layer.

16. A MEMS device comprising:

a MEMS substrate, wherein the MEMS substrate includes a top layer connected to an electrically conductive bottom layer;

an opening penetrating completely through the top layer, and exposing the bottom layer; and

a second electrically conductive layer deposited onto the MEMS substrate such that the second electrically conductive layer at least partially covers the surface and the sidewalls of the opening including making physical contact to the bottom layer, wherein the second electrically conductive layer is electrically connected to the bottom layer.

17. The MEMS device of claim 16, wherein the opening has sloped sidewalls.

18. The MEMS device of claim 16, wherein a CMOS substrate is bonded to the MEMS substrate.

19. The MEMS device of claim 18, wherein one or more openings in the back-side of the CMOS substrate exposing one or more metal interconnection layer.

20. The MEMS device of claim 19, wherein a third electrically conductive layer coats the insulating layer on the back-side of the CMOS substrate and on sidewalls of the one or more openings and provides physical and electrical contact to the one of more metal interconnection layers.

21. The MEMS device wafer of claim 20, wherein one or more solder-balls are connected to the third conductive layer.

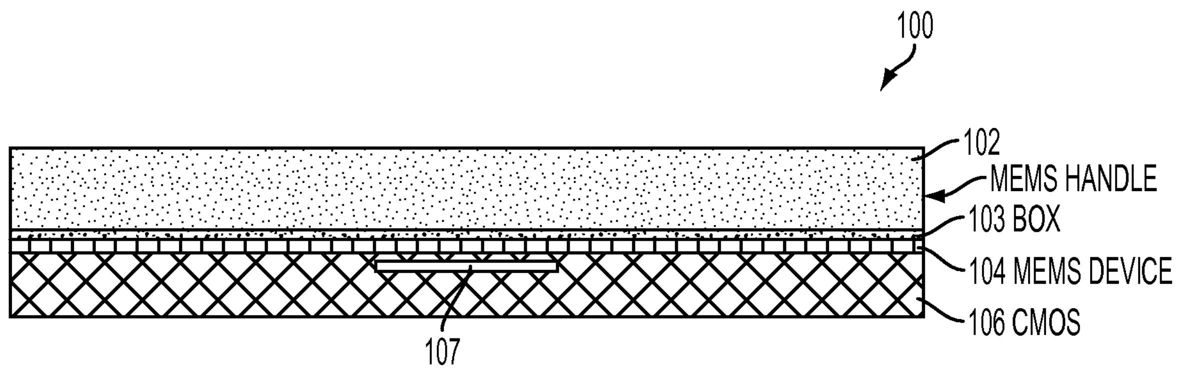

FIG. 1

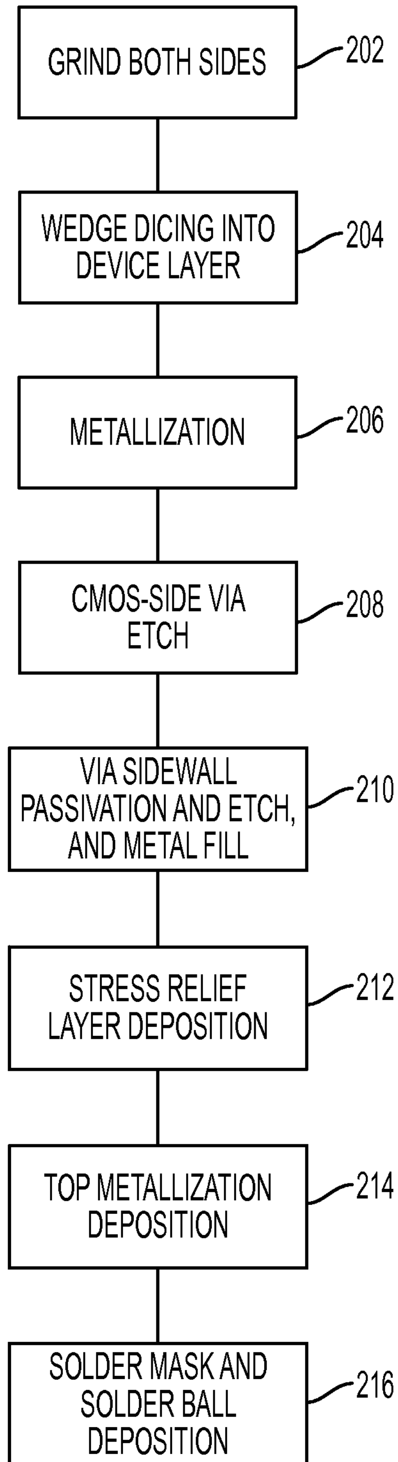

FIG. 2A

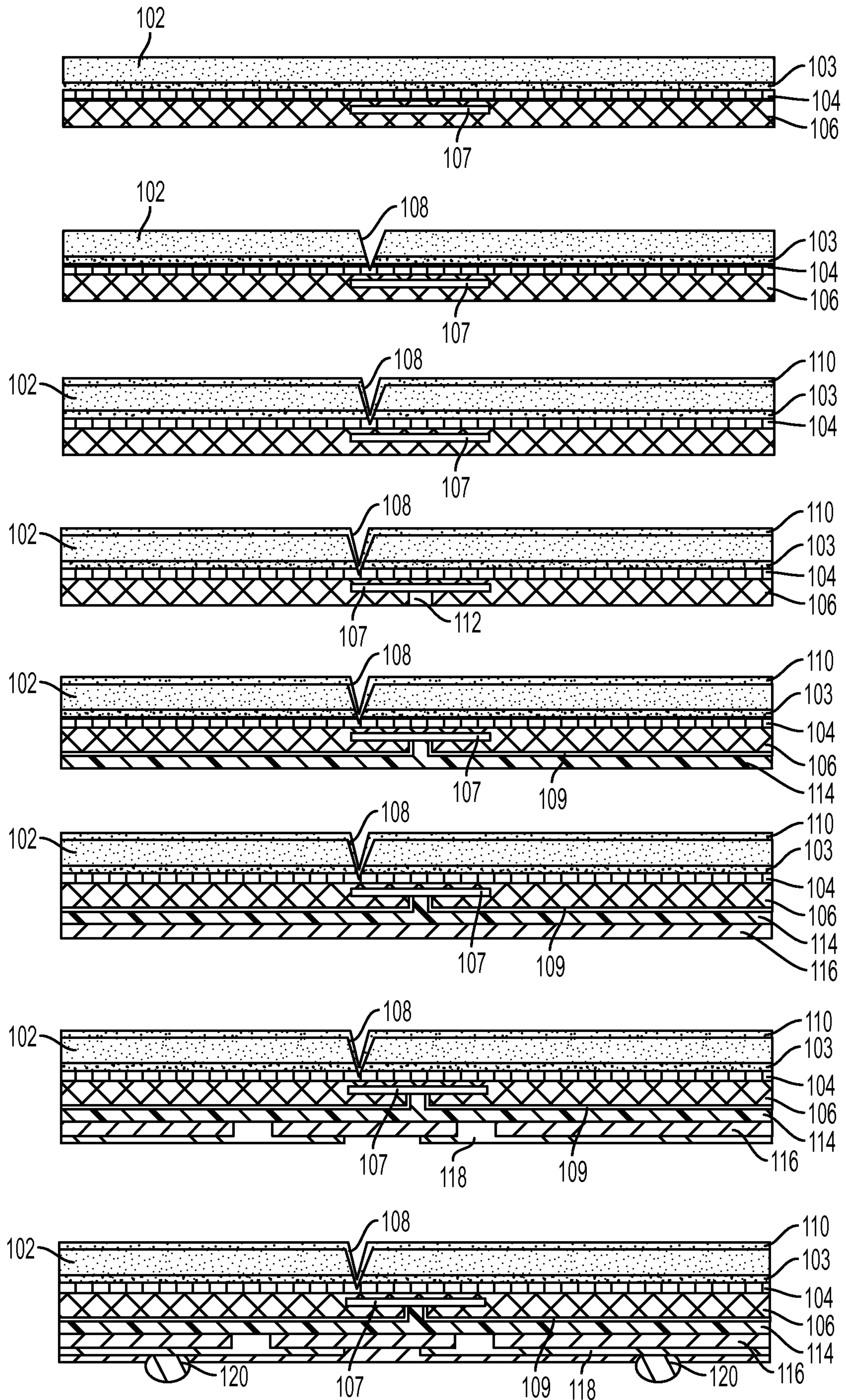

FIG. 2B