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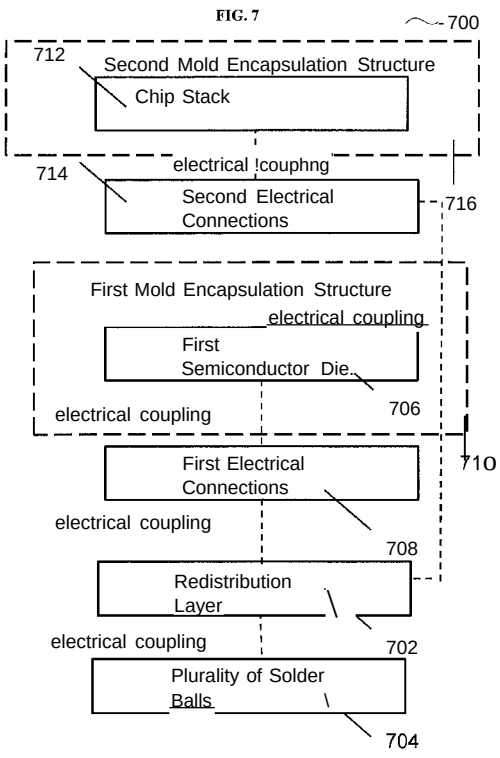
(54) **Title:** SEMICONDUCTOR PACKAGE AND METHOD OF FORMING THE SAME



(57) **Abstract:** Various embodiments may provide a semiconductor package. The semiconductor package may include a redistribution layer, a plurality of solder balls on a first side of the redistribution layer, a first semiconductor die over a second side of the redistribution layer opposite the first side, one or more first electrical connections electrically connecting the first semiconductor die to the redistribution layer, a first mold encapsulation structure covering the first semiconductor die, a chip stack including a plurality of second semiconductor dice over the first mold encapsulation structure, one or more second electrical connections electrically connecting each second semiconductor die of the plurality of second semiconductor dice to the redistribution layer, and a second mold encapsulation structure covering the chip stack. **A** width of the second mold encapsulation structure may be at least substantially equal to a width of the first encapsulation structure.

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SEMICONDUCTOR PACKAGE AND METHOD OF FORMING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of priority of Singapore application No. 10201601966Y filed on March 14, 2016, the contents of it being hereby incorporated by reference in its entirety for all purposes.

TECHNICAL FIELD

[0002] Various aspects of this disclosure relate to semiconductor packages and/or methods of forming semiconductor packages.

BACKGROUND

[0003] Fan-out wafer level packages are becoming more widely adopted in mobile applications due to low package profile and ability for multi-chips integration. The low package height of fan-out wafer level packages makes it ideal for package-on-package (PoP) stacking applications.

[0004] For mobile application, the desirable package height should be lower than 1 mm. However, conventional PoP stacks are very high due to the ball grid array (BGA) substrate and thick solder balls used to connect top and bottom package. Fan-out wafer level packages have been effective in reducing the package height, but considerable efforts are required to further reduce the stacked package height.

SUMMARY

[0005] Various embodiments may provide a semiconductor package. The semiconductor package may include a redistribution layer. The semiconductor package may also include a plurality of solder balls on a first side of the redistribution layer. The semiconductor package may further include a first semiconductor die over a second side of the redistribution layer opposite the first side. The semiconductor package may additionally include one or more first electrical connections electrically connecting the first semiconductor die to the redistribution layer. The semiconductor package also may include a first mold encapsulation structure covering the first semiconductor die. The semiconductor package may additionally include a chip stack including a plurality of second semiconductor dice over the first mold

encapsulation structure. The semiconductor package may further include one or more second electrical connections electrically connecting each second semiconductor die of the plurality of second semiconductor dice to the redistribution layer. The semiconductor package may also include a second mold encapsulation structure covering the chip stack. A width of the second mold encapsulation structure may be at least substantially equal to a width of the first encapsulation structure.

[0006] Various embodiments may provide a method of forming a semiconductor package. The method may include forming a redistribution layer. The method may also include forming a plurality of solder balls on a first side of the redistribution layer. The method may also include providing or forming a first semiconductor die over a second side of the redistribution layer opposite the first side. The method may further include forming one or more first electrical connections electrically connecting the first semiconductor die to the redistribution layer. The method may additionally include forming a first mold encapsulation structure covering the first semiconductor dice. The method may also include providing or forming a chip stack including a plurality of second semiconductor dice over the first mold encapsulation structure. The method may additionally include forming one or more second electrical connections electrically connecting each second semiconductor die of the plurality of second semiconductor dice to the redistribution layer. The method may further include forming a second mold encapsulation structure covering the chip stack. A width of the second mold encapsulation structure may be at least substantially equal to a width of the first encapsulation structure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The invention will be better understood with reference to the detailed description when considered in conjunction with the non-limiting examples and the accompanying drawings, in which:

FIG. 1 is a general schematic illustrating a semiconductor package according to various embodiments.

FIG. 2 is a schematic showing a cross-sectional side view of a semiconductor package according to various embodiments.

FIG. 3 is a schematic showing a cross-sectional side view of a semiconductor package according to various embodiments.

FIG. 4 is a schematic illustrating a method of forming a semiconductor package according to various embodiments.

FIG. 5A shows forming a sacrificial layer on a temporary carrier according to various embodiments.

FIG. 5B shows forming a redistribution layer (RDL) over or on the sacrificial layer according to various embodiments.

FIG. 5C shows forming a chip stack over the redistribution layer (RDL) according to various embodiments.

FIG. 5D shows forming of the mold encapsulation to cover the chip stacks according to various embodiments.

FIG. 5E shows the separation of the carrier from the reconstituted wafer according to various embodiments.

FIG. 5F shows the forming of the solder balls on the redistribution layer according to various embodiments.

FIG. 5G shows the dicing of the reconstituted wafer to form the semiconductor package according to various embodiments.

FIG. 6A shows forming a sacrificial layer on a temporary carrier according to various embodiments.

FIG. 6B shows forming a redistribution layer (RDL) over or on the sacrificial layer according to various embodiments.

FIG. 6C shows forming a chip stack over the redistribution layer (RDL) according to various embodiments.

FIG. 6D shows forming of the mold encapsulation to cover the chip stacks according to various embodiments.

FIG. 6E shows the separation of the carrier from the reconstituted wafer according to various embodiments.

FIG. 6F shows the forming of the solder balls on the redistribution layer according to various embodiments.

FIG. 6G shows the dicing of the reconstituted wafer to form the semiconductor package according to various embodiments.

FIG. 7 shows a general illustration of a semiconductor package according to various embodiments.

FIG. 8A is a schematic showing a cross-sectional side view of a semiconductor package according to various embodiments.

FIG. 8B is a schematic showing a cross-sectional side view of a semiconductor package according to various embodiments.

FIG. 9 is a schematic showing a cross-sectional side view of a semiconductor package according to various embodiments.

FIG. 10 is a schematic showing a cross-sectional side view of a semiconductor package according to various embodiments.

FIG. 11 is a schematic illustrating a method of forming a semiconductor package according to various embodiments.

FIG. 12A shows forming a sacrificial layer on a temporary carrier according to various embodiments.

FIG. 12B shows forming a redistribution layer (RDL) over or on the sacrificial layer according to various embodiments.

FIG. 12C shows forming of a masking layer on or over the redistribution layer (RDL) according to various embodiments.

FIG. 12D shows providing the first semiconductor dice and forming the one or more first electrical connections on the unmasked portion of the redistribution layer according to various embodiments.

FIG. 12E shows a molding process, i.e. deposition of a molding compound, according to various embodiments.

FIG. 12F shows a grinding process being used to remove a portion of mold layer, i.e. overmold, to expose the masking layer according to various embodiments.

FIG. 12G shows the removal of the masking layer according to various embodiments.

FIG. 12H shows providing or forming of chip stacks over the first mold encapsulation structures according to various embodiments.

FIG. 121 shows a second time molding process, i.e. another deposition of a molding compound, according to various embodiments.

FIG. 12J shows the removal of the carrier by debonding the sacrificial layer according to various embodiments.

FIG. 12K shows the forming of the solder balls on the redistribution layer according to various embodiments.

FIG. 12L shows the dicing or singulation of the molded wafer to form the semiconductor package according to various embodiments.

FIG. 13A shows forming a sacrificial layer on a temporary carrier according to various embodiments.

FIG. 13B shows forming a redistribution layer (RDL) over or on the sacrificial layer according to various embodiments.

FIG. 13C shows forming of a masking layer on or over the redistribution layer (RDL) according to various embodiments.

FIG. 13D shows providing the first semiconductor dice and forming the one or more first electrical connections on the unmasked portion of the redistribution layer according to various embodiments.

FIG. 13E shows a molding process, i.e. deposition of a molding compound, according to various embodiments.

FIG. 13F shows a grinding process being used to remove a portion of mold layer, i.e. overmold, to expose the masking layer according to various embodiments.

FIG. 13G shows the removal of the masking layer according to various embodiments.

FIG. 13H shows providing or forming of chip stacks over the first mold encapsulation structures according to various embodiments.

FIG. 131 shows a second time molding process, i.e. another deposition of a molding compound, according to various embodiments.

FIG. 13J shows the removal of the carrier by debonding the sacrificial layer according to various embodiments.

FIG. 13K shows the forming of the solder balls on the redistribution layer according to various embodiments.

FIG. 13L shows the dicing or singulation of the molded wafer to form the semiconductor package according to various embodiments.

FIG. 14A shows forming a sacrificial layer on a temporary carrier according to various embodiments.

FIG. 14B shows forming a redistribution layer (RDL) over or on the sacrificial layer according to various embodiments.

FIG. 14C shows forming of through mold interconnects (TMI) on the redistribution layer after forming the redistribution layer according to various embodiments.

FIG. 14D shows providing the first semiconductor dice and forming the one or more first electrical connections according to various embodiments.

FIG. 14E shows a molding process, i.e. deposition of a molding compound, to form first mold encapsulation structures according to various embodiments.

FIG. 14F shows a grinding process being used to remove a portion of the mold encapsulation structures, i.e. overmold, to expose the end portions of the through mold interconnects according to various embodiments.

FIG. 14G shows forming a further redistribution layer (RDL) over or on the first mold encapsulation structures according to various embodiments.

FIG. 14H shows providing or forming chip stacks on or over the further redistribution layer according to various embodiments.

FIG. 141 shows another molding process, i.e. deposition of a molding compound, to form second mold encapsulation structures on or over the further redistribution layer according to various embodiments.

FIG. 14J shows the removal of temporary carrier according to various embodiments.

FIG. 14K shows the forming of solder bumps and subsequent singulation of the molded wafer to form the semiconductor package according to various embodiments.

FIG. 15A shows forming a sacrificial layer on a temporary carrier according to various embodiments.

FIG. 15B shows forming a redistribution layer (RDL) over or on the sacrificial layer according to various embodiments.

FIG. 15C shows forming the first thermal vias and the through mold interconnects (TMI) according to various embodiments.

FIG. 15D shows providing the first semiconductor dice and forming the one or more first electrical connections according to various embodiments.

FIG. 15E shows a molding process, i.e. deposition of a molding compound, to form first mold encapsulation structures according to various embodiments.

FIG. 15F shows a mechanical backgrinding process being used to remove a portion of the first mold encapsulation structures, i.e. overmold, to expose the end portions of the through mold interconnects and the end portions of the first thermal vias according to various embodiments.

FIG. 15G shows forming of a thermal conductive layer and electrically conductive through vias on or above the first mold encapsulation structures.

FIG. 15H shows providing or forming chip stacks on or over the thermal conductive layer according to various embodiments.

FIG. 151 shows forming of the second thermal conductive vias according to various embodiments.

FIG. 15J shows another molding process, i.e. deposition of a molding compound, to form second mold encapsulation structures on or over the thermal conductive layer according to various embodiments.

FIG. 15K shows a mechanical backgrinding process being used to remove a portion of the second mold encapsulation structures, i.e. overmold, to expose the end portions of end portions of the second thermal vias according to various embodiments.

FIG. 15L shows the removal of temporary carrier according to various embodiments.

FIG. 15M shows the forming of solder bumps and thermal bumps, followed by subsequent singulation of the molded wafer to form the semiconductor package according to various embodiments.

DETAILED DESCRIPTION

[0008] The following detailed description refers to the accompanying drawings that show, by way of illustration, specific details and embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, and logical changes may be made without departing from the scope of the invention. The various embodiments are not necessarily mutually exclusive, as some embodiments can be combined with one or more other embodiments to form new embodiments.

[0009] Embodiments described in the context of one of the methods or packages are analogously valid for the other methods or packages. Similarly, embodiments described in the context of a method are analogously valid for a package, and vice versa.

[0010] Features that are described in the context of an embodiment may correspondingly be applicable to the same or similar features in the other embodiments. Features that are described in the context of an embodiment may correspondingly be applicable to the other embodiments, even if not explicitly described in these other embodiments. Furthermore,

additions and/or combinations and/or alternatives as described for a feature in the context of an embodiment may correspondingly be applicable to the same or similar feature in the other embodiments.

[001 1] The word "over" used with regards to a deposited material formed "over" a side or surface, may be used herein to mean that the deposited material may be formed "directly on", e.g. in direct contact with, the implied side or surface. The word "over" used with regards to a deposited material formed "over" a side or surface, may also be used herein to mean that the deposited material may be formed "indirectly on" the implied side or surface with one or more additional layers being arranged between the implied side or surface and the deposited material. In other words, a first layer "over" a second layer may refer to the first layer directly on the second layer, or that the first layer and the second layer are separated by one or more intervening layers.

[0012] The package as described herein may be operable in various orientations, and thus it should be understood that the terms "top", "bottom", etc., when used in the following description are used for convenience and to aid understanding of relative positions or directions, and not intended to limit the orientation of the package.

[0013] In the context of various embodiments, the articles "a", "an" and "the" as used with regard to a feature or element include a reference to one or more of the features or elements.

[0014] In the context of various embodiments, the term "about" or "approximately" as applied to a numeric value encompasses the exact value and a reasonable variance.

[0015] As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0016] For the sake of clarity and to avoid clutter, not all features in some of the figures have been labelled. Features which are similar to features that have already been labelled may not be labelled to improve clarity and to avoid clutter.

[0017] One area of improvement is to remove the top BGA substrate and/or thick solder balls. Various embodiments may provide a semiconductor package without the top BGA substrate and/or solder balls. Various embodiments may relate to a semiconductor package having a lower profile height compared to conventional semiconductor packages.

[0018] FIG. 1 is a general schematic illustrating a semiconductor package 100 according to various embodiments. The semiconductor package 100 may include a redistribution layer

102, a plurality of solder balls 104 electrically coupled to the redistribution layer 102, a chip stack 106 including a plurality of chips in vertical arrangement over the redistribution layer 102, electrical connections 108 coupling each chip to the redistribution layer 102. The semiconductor package 100 may further include a mold encapsulation 110 covering the chip stack 106.

[0019] In various embodiments, the electrical connections 108 may be or may include through silicon vias (TSVs). In various other embodiments, the electrical connections 108 may be or may include wirebonds.

[0020] In the present context, the chip stack 106 being covered by the mold encapsulation 110 may refer to at least one or some of the sides of the chip stack 106 are in contact with the mold encapsulation 110. In various embodiments, the chip stack 106 may be entirely be surrounded by the mold encapsulation 110 and the redistribution layer 102.

[0021] The mold encapsulation 110 may additionally cover the electrical connections 108.

[0022] FIG. 2 is a schematic showing a cross-sectional side view of a semiconductor package 200 according to various embodiments. The semiconductor package 200 may include a redistribution layer (RDL) 202, a plurality of solder balls 204 electrically coupled to the redistribution layer 202, a chip stack 206 including a plurality of chips (which may be referred to as TSV chips) in vertical arrangement over the redistribution layer 202, electrical connections 208, i.e. through silicon vias (TSVs), coupling each chip to the redistribution layer 202. Each chip may include a through silicon via extending from a first side of the chip to a second side of the chip opposite the first side. The TSV may be configured to connect the chip and/or any other chips above the chip in the package 200 with the RDL 202 and/or any other chips below the chip in the package 200. The plurality of solder balls 204 may be at a first side of the redistribution layer 202, and the chip stack 206 may be at a second side of the redistribution layer 202 opposite the first side. In other words, the chip stack 206 and the solder balls 204 may be on opposing sides on the redistribution layer 202. The TSVs 208 may be electrically coupled to the redistribution layer 202 via solder bumps 212 on the second side of the redistribution layer 202.

[0023] The semiconductor package 200 may further include a mold encapsulation 210 covering the chip stack 206. The mold encapsulation 210 may further cover the electrical connections 208.

[0024] As shown in FIG. 2, the RDL 202 may include a plurality of metallization 202a embedded in dielectric layers 202b. The metallization 202a may electrically connect the solder bumps 212 (and the TSV chips) at the second side of the RDL 202 to the solder balls 204 at the first side of the RDL 202. The metallization 202a in contact with the solder balls 204 may be referred to as under bump metallization (UBM).

[0025] FIG. 2 shows a stacked chip fan-out wafer level package 200 using TSV chips. The TSV chips may be stacked onto the thin film RDL 202 and the entire assembly may be encapsulated in a mold compound, e.g. epoxy compound, which forms the mold encapsulation 210. Solder balls 204 may be attached to the under bump metallization (UBM) on the RDL 202 for board level assembly.

[0026] FIG. 3 is a schematic showing a cross-sectional side view of a semiconductor package 300 according to various embodiments. The semiconductor package 300 may include a redistribution layer (RDL) 302, a plurality of solder balls 304 electrically coupled to the redistribution layer 302, a chip stack 306 including a plurality of chips in vertical arrangement over the redistribution layer 302, electrical connections 308, i.e. wirebonds, coupling each chip to the redistribution layer 302. A first end of a wirebond 308 may be connected to a chip while a second end of the wirebond 308 may be connected to the RDL 302. Neighbouring chips in the chip stack 306 may be joined by a die attach adhesive film (DAF) 312. FIG. 3 shows a first chip attached to the RDL 302 using a first die attach adhesive film 312, a second chip attached to the first chip using a second die attach adhesive film 312, and a third chip attached to the second chip using a third die attach adhesive film 312. The plurality of solder balls 304 may be at a first side of the redistribution layer 302, and the chip stack 306 may be at a second side of the redistribution layer 302 opposite the first side. In other words, the chip stack 306 and the solder balls 304 may be on opposing sides on the redistribution layer 302.

[0027] The semiconductor package 300 may further include a mold encapsulation 310 covering the chip stack 306. The mold encapsulation 310 may also cover the electrical connections 308.

[0028] Similar to FIG. 2, FIG. 3 shows that the RDL 302 may include a plurality of metallization 302a embedded in dielectric layers 302b. The metallization 302a may electrically connect (the second ends of) the wirebonds 308 at the second side of the RDL

302 to the solder balls 304 at the first side of the RDL 302. The metallization 302a in contact with the solder balls 304 may be referred to as under bump metallization (UBM).

[0029] FIG. 3 shows a stacked chip fan-out wafer level package using wire-bonded chips. The chips may be stacked onto the RDL layer 302 with die attach adhesive film (DAF) 312 and I/Os of the chips are connected with wire-bonds 308 to the RDL 302. The entire assembly may be encapsulated in mold compound, e.g. epoxy compound, which forms the mold encapsulation 310. Solder balls 304 may be attached to the UBM for board level assembly.

[0030] FIG. 4 is a schematic 400 illustrating a method of forming a semiconductor package according to various embodiments. The method may include, in 402, forming a redistribution layer. The method may also include, in 404, forming a plurality of solder balls 404 electrically coupled to (a first side of) the redistribution layer. The method may also include, in 406, providing or forming a chip stack including a plurality of chips in vertical arrangement over (a second side of) the redistribution layer. The method may additionally include, in 408, forming or providing electrical connections coupling each chip to the redistribution layer. The method may further include, in 410, forming a mold encapsulation covering the chip stack.

[0031] For avoidance of doubt, the method steps shown in FIG. 4 may not necessarily be in sequence. For instance, the plurality of solder balls may be formed after forming the mold encapsulation.

[0032] FIGS. 5A-G show a method of forming a semiconductor package as shown in FIG. 2 according to various embodiments.

[0033] FIG. 5A shows forming a sacrificial layer 516 on a temporary carrier 514 according to various embodiments. The method may include providing the temporary carrier 514. The sacrificial layer 516 may be deposited over the surface of the temporary carrier 514.

[0034] FIG. 5B shows forming a redistribution layer (RDL) 502 over or on the sacrificial layer 516 according to various embodiments. UBMs may be formed over the sacrificial layer 516 using a semi-additive process. The remaining RDL 502, including metallization 502a and the dielectric 502b, may be processed over or on top of the UBMs. Smaller UBMs may be fabricated on the RDL 502. The UBMs may be on a first side of the RDL 502 and the smaller UBMs may be on a second side of the RDL 502 opposite the first side.

[0035] FIG. 5C shows forming a chip stack 508 over the redistribution layer (RDL) 502 according to various embodiments. TSV chips may be stacked and assembled over the RDL 502 to form the chip stacks 506. Solder bumps 512 may be formed on the smaller UBMs to connect TSVs 508 of the TSV chips with the redistribution layer 502.

[0036] FIG. 5D shows forming of the mold encapsulation 510 to cover the chip stacks 506 according to various embodiments. A wafer level molding process may be used to encapsulate the assembled chips in mold epoxy compound.

[0037] FIG. 5E shows the separation of the carrier 514 from the reconstituted wafer according to various embodiments. The reconstituted wafer may include the redistribution layer 502, the solder bumps 512, the chip stacks 506 including the through silicon vias 508, and the mold encapsulation 510. The reconstituted wafer may be separated from the carrier 514 by de-bonding of the sacrificial layer 516.

[0038] FIG. 5F shows the forming of the solder balls on the redistribution layer 502 according to various embodiments. Solder balls 504 may be attached to front side UBMs of the RDL 502.

[0039] FIG. 5G shows the dicing of the reconstituted wafer to form the semiconductor package according to various embodiments.

[0040] FIGS. 6A-G show a method of forming a semiconductor package as shown in FIG. 3 according to various embodiments. The processing steps may be similar to that shown in FIGS. 5A-G, except that chips are attached onto RDL 602 with die attach adhesive 612.

[0041] FIG. 6A shows forming a sacrificial layer 616 on a temporary carrier 614 according to various embodiments. The method may include providing the temporary carrier 614. The sacrificial layer 616 may be deposited over the surface of the temporary carrier 614.

[0042] FIG. 6B shows forming a redistribution layer (RDL) 602 over or on the sacrificial layer 616 according to various embodiments. UBMs may be formed over the sacrificial layer 616 using a semi-additive process. The remaining RDL 602, including metallization 602a and the dielectric 602b, may be processed over or on top of the UBMs. Wire-bond pads may be fabricated on the RDL 602. The wire-bond pads and the UBMs may be on opposing sides of the RDL 602.

[0043] FIG. 6C shows forming a chip stack 608 over the redistribution layer (RDL) 602 according to various embodiments. The integrated circuit (IC) chips may be stacked and

assembled over the RDL 602 to form the chip stacks 608. Wire-bonds may be used to connect each chip to wire-bond pads on the RDL 602.

[0044] FIG. 6D shows forming of the mold encapsulation 610 to cover the chip stacks 606 according to various embodiments. A wafer level molding process may be used to encapsulate the assembled chips in mold epoxy compound.

[0045] FIG. 6E shows the separation of the carrier 614 from the reconstituted wafer according to various embodiments. The reconstituted wafer may include the redistribution layer 602, the wirebonds 608, the chip stacks 606, and the mold encapsulation 610. The reconstituted wafer may be separated from the carrier 614 by de-bonding of the sacrificial layer 616.

[0046] FIG. 6F shows the forming of the solder balls on the redistribution layer 602 according to various embodiments. Solder balls 604 may be attached to front side UBM.

[0047] FIG. 6G shows the dicing of the reconstituted wafer to form the semiconductor package according to various embodiments.

[0048] FIG. 7 shows a general illustration of a semiconductor package 700 according to various embodiments. The semiconductor package 700 may include a redistribution layer 702. The semiconductor package 700 may also include a plurality of solder balls 704 on a first side of the redistribution layer 702. The semiconductor package 700 may further include a first semiconductor die 706 over a second side of the redistribution layer 702 opposite the first side. The semiconductor package 700 may additionally include one or more first electrical connections 708 electrically connecting the first semiconductor die 706 to the redistribution layer 702. The semiconductor package also may include a first mold encapsulation structure 710 covering the first semiconductor die 706.

[0049] The semiconductor package 700 may additionally include a chip stack 712 including a plurality of second semiconductor dice over the first mold encapsulation structure 710. In other words, the second semiconductor dice may be arranged vertically with respect to each other. The semiconductor package 700 may further include one or more second electrical connections 714 electrically connecting each second semiconductor die of the plurality of second semiconductor dice to the redistribution layer 702. The semiconductor package 700 may also include a second mold encapsulation structure 716 covering the chip stack 712. A width of the second mold encapsulation structure 716 may be at least substantially equal to a width of the first encapsulation structure 710.

[0050] In other words, the semiconductor package 700 may include a first encapsulation structure 710 and a second encapsulation structure 716 over a redistribution layer 702. A plurality of solder balls 704 may be on an opposite side of the redistribution layer 702. The first encapsulation structure 710 may be between the redistribution layer 702 and the second encapsulation structure 716, and may be of equal or smaller width compared to the second encapsulation structure 716. The first encapsulation structure 710 may cover the first semiconductor die 706. The second encapsulation structure 716 may cover the chip stack 712.

[0051] In various embodiments, the plurality of second semiconductor dice may be in vertical arrangement, i.e. form a vertical stacked arrangement. In various other embodiments, the plurality of second semiconductor dice may be in lateral arrangement. In other words, the plurality of second semiconductor dice may be arranged in a side by side planar arrangement over the first mold encapsulation structure 710.

[0052] The first mold encapsulation structure 710 may further cover the one or more first electrical connections 708. The second mold encapsulation structure may further cover the one or more second electrical connections 714.

[0053] In various embodiments, the redistribution layer 702 may include a plurality of dielectric layers and a plurality of interconnection elements (alternatively referred to as interconnects or metallization) electrically connecting the first side of the redistribution layer to the second side of the redistribution layer. The plurality of interconnection elements may be embedded or at least partially be covered by the plurality of dielectric layers. An interconnection element may be separated from another interconnection element by one or more dielectric layers.

[0054] The width of the second mold encapsulation structure 716 may be greater than the width of the first encapsulation structure 710. The width of the first mold encapsulation structure 710 may be the dimension that is substantially parallel to the redistribution layer 702. Similarly, the width of the second mold encapsulation structure 716 may be the dimension that is substantially parallel to the redistribution layer 702.

[0055] In various embodiments, the chip stack 712 may include semiconductor dice of equal sizes or widths. The plurality of second semiconductor dice may be of substantially same size or width.

[0056] In various embodiments, the chip stack 712 may include semiconductor dice of unequal sizes or widths. One second semiconductor die of the plurality of second semiconductor dice may have a size or width different from another second semiconductor die of the plurality of second semiconductor dice.

[0057] In various embodiments, the first electrical connections 708 may be solder bumps. In various other embodiments, the first electrical connections 708 may be wirebonds.

[0058] In various embodiments, the second electrical connections 714 may be wirebonds. In various other embodiments, the second electrical connections 714 may be solder bumps and/or through silicon vias. The one or more second electrical connections 714 may refer to or include a plurality of second electrical connections 714.

[0059] In various embodiments, a portion of the first mold encapsulation structure 710 may be between the first semiconductor die 706 and the chip stack 712.

[0060] The semiconductor package 700 may include a further redistribution layer between the first mold encapsulation structure 710 and the second mold encapsulation structure 716. The one or more second electrical connections 714 or the semiconductor package 700 may include one or more through mold interconnects extending through the first mold encapsulation structure 710 and electrically connecting a first side of the further redistribution layer to the second side of the redistribution layer 702. The semiconductor package 700 may further include a plurality of wirebonds electrically connecting the chip stack 712, i.e. the plurality of second semiconductor dice, to a second side of the further redistribution layer.

[0061] The semiconductor package 700 may further include a thermal conductive layer between the first mold encapsulation structure 710 and the second mold encapsulation structure 716. The semiconductor package 700 may also include one or more first thermal vias extending from the first side of the redistribution layer 702 through the redistribution layer 702 and the first mold encapsulation 710 to the thermal conductive layer. The semiconductor package 700 may additionally include one or more second thermal vias extending from the thermal conductive layer through the second mold encapsulation structure 716. The one or more second electrical connections 714 or the semiconductor die 700 may include one or more through mold interconnects extending through the first mold encapsulation layer 710; one or more electrically conductive through vias extending from the one or more through mold vias through the thermal conductive layer; and a plurality of

wirebonds connecting the chip stack 712, i.e. the plurality of second semiconductor dice, to the one or more electrically conductive through vias.

[0062] FIG. 8A is a schematic showing a cross-sectional side view of a semiconductor package 800a according to various embodiments. The semiconductor package 800a may include a redistribution layer 802, which may include a plurality of interconnection elements 802a and a plurality of dielectric layers 802b. The semiconductor package 800 may also include a plurality of solder balls 804 on a first side of the redistribution layer 802. The semiconductor package 800a may further include a first semiconductor die 806, e.g. a smaller sized flip chip such as a logic integrated circuit (IC) chip, on or over a second side of the redistribution layer 802 opposite the first side. The first semiconductor die 806 may be electrically connected to the redistribution layer 802, i.e. to one or more interconnection elements 802b (e.g. under-bump metallization) via solder bumps 808. The die 806 may be assembled to the redistribution layer 802 by reflowing solder bumps 808 onto the under-bump metallization. The solder bumps 808 may be referred to as first electrical connections.

[0063] The semiconductor package also may include a first mold encapsulation structure 810 (e.g. including mold epoxy) covering the first semiconductor die 806 and the one or more first electrical connections 808. The first mold encapsulation structure 810 may only be over or on a portion of the redistribution layer 802, with a further portion of the redistribution layer 802 not covered by the first mold encapsulation structure 810. In other words, some of the bond or wirebonding pads on the redistribution layer 802 may not be covered by the first mold encapsulation structure 810.

[0064] The semiconductor package 800a may additionally include a chip stack 812 including a plurality of second semiconductor dice in vertical arrangement over or on the first mold encapsulation structure 810. The first mold encapsulation structure 810 may provide mechanical support for the plurality of second semiconductor dice, which may be larger sized chips such as wide input/output (I/O) memory integrated circuit (IC) chips with wirebonding pads. The plurality of second semiconductor dice may be stacked using die attach adhesive films 818. For instance, a second semiconductor die may be attached to the first mold encapsulation structure 810 using a die attach adhesive film 818, while a further second semiconductor die may be attached to the semiconductor die using a further die attach adhesive film 818.

[0065] The semiconductor package 800a may further include one or more second electrical connections 814, i.e. wirebonds, electrically connecting each second semiconductor die, e.g. the I/O of each die, of the plurality of second semiconductor dice to the redistribution layer 802. The semiconductor package 800a may also include a second mold encapsulation structure 816 covering the chip stack 812 and the one or more second electrical connections 814 to form the semiconductor package 800a, which may be referred to as a single embedded package. A width of the second mold encapsulation structure 816 may be substantially equal to or greater than a width of the first encapsulation structure 808.

[0066] FIG. 8B is a schematic showing a cross-sectional side view of a semiconductor package 800b according to various embodiments. The semiconductor package 800b may be similar to the semiconductor package 800a. However, instead of using solder bumps 808 to connect the first semiconductor die 806 to the redistribution layer 802, the semiconductor package 800b may include one or more wire bonds 820 to electrically connect the first semiconductor die 806 to the redistribution layer 802. In other words, the one or more first electrical connections 820 may be one or more wire bonds 820. The semiconductor package 800b may further include a die attach adhesive film 822 to attach the first semiconductor die 806 to the redistribution layer 802. The semiconductor package 800b may allow different sized integrated circuit (IC) chips to be connected via wirebonding, without the need of through mold interconnects (TMI).

[0067] FIG. 9 is a schematic showing a cross-sectional side view of a semiconductor package 900 according to various embodiments. The semiconductor package 900 may include a redistribution layer 902 (alternatively referred to as a bottom RDL). The redistribution layer 902 may include a plurality of dielectric layers 902b and a plurality of interconnection elements 902a electrically connecting a first side of the redistribution layer 902 to a second side of the redistribution layer 902.

[0068] The semiconductor package 900 may also include a plurality of solder balls 904 on the first side of the redistribution layer 902. The semiconductor package 900 may further include a first semiconductor die 906 (alternatively referred to as bottom IC chip) over the second side of the redistribution layer 902 opposite the first side. The semiconductor package 900 may additionally include one or more first electrical connections 908 electrically connecting the first semiconductor die 906 to the redistribution layer 902. In various embodiments, the one or more first electrical connections 908 may be solder bumps as

illustrated in FIG. 9. The bottom flip chip 906 may be assembled to the bottom RDL 902 by reflowing the solder bumps 908 to the UBMs of the redistribution layer 902. However, it may also be envisioned that the one or more electrical connections 908 may be wirebonds similar to that wirebonds 820 shown in FIG. 8B. The semiconductor package 900 also may include a first mold encapsulation structure 910 covering the first semiconductor die 906. The first semiconductor die 906 may be encapsulated in mold epoxy. The first mold encapsulation structure 910 may further cover the one or more first electrical connections 908.

[0069] The semiconductor package 900 may additionally include a chip stack 912 including a plurality of second semiconductor dice in vertical arrangement over the first mold encapsulation structure 910. The semiconductor package 900 may also include a second mold encapsulation structure 916 covering the chip stack 912.

[0070] The semiconductor package 900 may also include a further redistribution layer 920 (alternatively referred to as top RDL) between the first mold encapsulation structure and the second mold encapsulation structure 916. The further redistribution layer 920 may include a plurality of dielectric layers 920b and a plurality of interconnection elements 920a electrically connecting a first side of the further redistribution layer 920 to a second side of the further redistribution layer 920.The second mold encapsulation structure 916 may be on or over the further redistribution layer 920 to form a single embedded package. The chip stack 912 may be on or over the further redistribution layer 920.

[0071] The semiconductor package 900 may further include one or more through mold interconnects 922 (TMIs) extending through the first mold encapsulation structure and electrically connecting the first side of the further redistribution layer 920 to the second side of the redistribution layer 902. The second mold encapsulation structure 916 may be on or over the entire second side of the further redistribution layer 920. The first mold encapsulation structure 910 may be on or over the entire second side of the redistribution layer 902.

[0072] The semiconductor package 900 may also include a plurality of wirebonds 914 electrically connecting the plurality of second semiconductor dice to the second side of the further redistribution layer 920. In various embodiments, the one or more second electrical connections electrically connecting each second semiconductor die of the plurality of second semiconductor dice to the redistribution layer 902 may include one or more wirebonds 914 and the one or more through mold interconnects 922. The one or more second electrical

connections may further include the plurality of interconnection elements 920a in the further redistribution layer 920. The plurality of interconnection elements 920 may connect the wirebonds 914 with the through mold interconnects 922.

[0073] A width of the second mold encapsulation structure 916 may be substantially equal to a width of the first encapsulation structure 910.

[0074] In various embodiments, the one or more through mold interconnects 922 may be conductive pillars, such as metal pillars. The metal pillars may be copper pillars. In various other embodiments, the one or more through mold interconnects 922 may be vertical wire-bonds.

[0075] FIG. 10 is a schematic showing a cross-sectional side view of a semiconductor package 1000 according to various embodiments. The semiconductor package 1000 may include a redistribution layer 1002. The redistribution layer 1002 may include a plurality of dielectric layers 1002b and a plurality of interconnection elements 1002a electrically connecting a first side of the redistribution layer 1002 to a second side of the redistribution layer 1002.

[0076] The semiconductor package 1000 may also include a plurality of solder balls 1004 on the first side of the redistribution layer 1002. The semiconductor package 1000 may further include a first semiconductor die 1006 (alternatively referred to as IC chip) over the second side of the redistribution layer 1002 opposite the first side. The semiconductor package 1000 may additionally include one or more first electrical connections 1008 electrically connecting the first semiconductor die 1006 to the redistribution layer 1002. In various embodiments, the one or more first electrical connections 1008 may be solder bumps as illustrated in FIG. 10. The bottom flip chip 1006 may be assembled to the bottom RDL 1002 by reflowing the solder bumps 1008 to the UBMs of the redistribution layer 1002. However, it may also be envisioned that the one or more electrical connections 1008 may be wirebonds similar to that wirebonds 820 shown in FIG. 8B. The semiconductor package 1000 also may include a first mold encapsulation structure 1010 covering the first semiconductor die 1006. The first semiconductor die 1006 may be encapsulated in mold epoxy. The first mold encapsulation structure 1010 may further cover the one or more first electrical connections 1008.

[0077] The semiconductor package 1000 may additionally include a chip stack 1012 including a plurality of second semiconductor dice in vertical arrangement over the first mold

encapsulation structure 1010. The semiconductor package 1000 may also include a second mold encapsulation structure 1016 covering the chip stack 1012. The second semiconductor dice may be attached using die attach adhesive films 1018 (DAFs). Neighbouring second semiconductor dice may be adhered using a die attach adhesive film 1018. The chip stack 1012 may be attached to the thermal conductive layer 1020 using a die attach adhesive film 1018.

[0078] The semiconductor package 1000 may also include a thermal conductive layer 1020 between the first mold encapsulation structure 1010 and the second mold encapsulation structure 1016. The thermal conductive layer 1020 may be configured to form a thermal distribution pathway to draw accumulated heat away from the first semiconductor die 1006 and the chip stack 1012 (including the plurality of second semiconductor dice).

[0079] The semiconductor package 1000 may include one or more first thermal vias 1024a extending from the first side of the redistribution layer 1002 through the redistribution layer 1002 and the first mold encapsulation 1010 to the thermal conductive layer 1020. Thermal bumps 1026 may be formed on the first side of the redistribution layer 1002 and in thermal contact with the one or more first thermal vias 1024a. In other words, the one or more first thermal vias 1024a may be configured to transmit heat between the thermal conductive layer 1020 and the thermal bumps 1026. The thermal bumps 1026 may be solder bumps but may be configured to conduct heat instead of current. The one or more first thermal vias 1024a may extend through the thickness of the redistribution layer 1002 and the first mold encapsulation 1010.

[0080] The semiconductor package 1000 may also include one or more second thermal vias 1024b extending from the thermal conductive layer 1020 through the second mold encapsulation structure 1016. The one or more second thermal vias 1024b may extend through the thickness of the second mold encapsulation structure 1016 so that the thermal conductive layer 1020 is connected to the top surface of the second mold encapsulation 1016.

[0081] The thermal conductive layer 1020 may be connected by first thermal vias 1024a to the thermal bumps 1026, and may be connected to the top surface of the package 900 by second thermal vias 1026b. The positioning of the thermal conductive layer 1020 between the chip stack 1012 and the first semiconductor die 1006, as well as the connection with thermal vias 1024a, 1024b may provide an effective pathway where heat can be directed away from the IC chips 1006, 1012. The bottom thermal vias 1024a may be connected to the printed

circuit board (PCB) by thermal bumps 1026 and heat may be directed from the chips 1006, 1012 to the PCB. The top thermal vias 1024b may be connected to a heat sink or a heat spreader that is attached to top of the package 1000 to improve heat dissipation. This package structure may be suitable for IC chips with high power requirement where thermal cooling measure is essential. The thermal conductive layer 1020 may, for instance, include aluminum nitride (A1N).

[0082] The semiconductor package 1000 or the one or more second electrical connections may further include one or more through mold interconnects 1022 (TMIs) extending through the first mold encapsulation structure 1010, one or more electrically conductive through vias 1028 extending from the one or more through mold vias 1022 through the thermal conductive layer 1020, and a plurality of wirebonds 1014 connecting the plurality of second semiconductor dice to the one or more electrically conductive through vias 1028. The one or more electrically conductive through vias 1028 may extend from the first side of the thermal conductive layer 1020 to the second side of the thermal conductive layer 1020, and may be configured to provide an electrical pathway through the thermal conductive layer 1020. The second semiconductor dies in chip stack 1012 may be electrically connected to the redistribution layer 1002 via the plurality of wirebonds 1014, the one or more through mold vias 1022, and the one or more electrically conductive through vias 1028.

[0083] The second mold encapsulation structure 1016 may be on or over the entire second side of the thermal conductive layer 1020. The first mold encapsulation structure 910 may be on or over the entire second side of the redistribution layer 1002.

[0084] A width of the second mold encapsulation structure 1016 may be substantially equal to a width of the first encapsulation structure 1010.

[0085] FIG. 11 is a schematic 1100 illustrating a method of forming a semiconductor package according to various embodiments. The method may include, in 1102, forming a redistribution layer. The method may also include, in 1104, forming a plurality of solder balls on a first side of the redistribution layer. The method may also include, in 1106, providing or forming a first semiconductor die over a second side of the redistribution layer opposite the first side. The method may further include, in 1108, forming one or more first electrical connections electrically connecting the first semiconductor die to the redistribution layer. The method may additionally include, in 1110, forming a first mold encapsulation structure covering the first semiconductor dice. The method may also include, in 1112, providing or

forming a chip stack including a plurality of second semiconductor dice over the first mold encapsulation structure. The method may additionally include, in 1114, forming one or more second electrical connections electrically connecting each second semiconductor die of the plurality of second semiconductor dice to the redistribution layer. The method may further include, in 1116, forming a second mold encapsulation structure covering the chip stack. A width of the second mold encapsulation structure may be at least substantially equal to a width of the first encapsulation structure.

[0086] In other words, the method may relate to forming a semiconductor package as described herein. The method may include forming the redistribution layer, providing a first semiconductor die, forming first electrical connections to connect the first semiconductor die to the redistribution layer, forming the first mold encapsulation structure, providing a chip stack including a plurality of second semiconductor dice over the first encapsulating structure, forming second electrical connections to connect the second semiconductor dice to the redistribution layer, and forming the second encapsulation structure.

[0087] For avoidance of doubt, the method steps shown in FIG. 11 may not necessarily be in sequence. For instance, the plurality of solder balls may be formed after forming the second mold encapsulation structure.

[0088] Forming the redistribution layer may include providing a temporary carrier. The method may include forming a sacrificial release layer over temporary carrier. The method may also include forming a first layer on the sacrificial release layer. The first layer may include a first dielectric and one or more first conductive lines. The method may additionally include forming a second layer on the first layer, the second layer include a second dielectric and one or more second conductive lines. The one or more first conductive lines may be in electrical connection with the one or more second conductive lines. The method may further include forming additional layers including additional dielectric and additional conductive lines. The first layer, the second layer, and any further layers may form the redistribution layer.

[0089] The method may also include forming a masking layer on the redistribution layer so that a first portion of the redistribution layer is covered by the masking layer and a second portion of the redistribution layer is exposed.

[0090] The method may further include providing the first semiconductor die and forming the one or more first electrical connections on the second portion of the redistribution layer,

i.e. the exposed or unmasked portion of the redistribution layer. The semiconductor die may be provided and the one or more electrical connections may be formed within a cavity defined by the masking layer.

[0091] The method may also include depositing a molding compound over the first semiconductor die. The molding compound may be deposited into the cavity. The molding compound may also be deposited over the one or more electrical connections. The method may further include removing the masking layer to form the first mold encapsulation structure covering the first semiconductor die.

[0092] The method may further include removing the temporary carrier. The method may also include removing the sacrificial release layer. The temporary carrier and/or the sacrificial release layer may be removed after forming the second mold encapsulation structure.

[0093] In various embodiments, the method may include providing further first semiconductor dice over the second side of the redistribution layer opposite the first side. The method may also include providing further chip stacks over the first mold encapsulation structure so that each further chip stack is over a respective further first semiconductor die. The method may additionally include forming the second mold encapsulation structure by covering the plurality of chips stacks comprising the chip stack and the further chip stacks to form a wafer-level intermediate structure. The method may further include singulating or dicing the wafer-level intermediate structure to form the semiconductor package.

[0094] In various embodiments, the method may further include forming one or more through mold interconnects on the second side of the redistribution layer after forming the redistribution layer and before providing the semiconductor die over the second side of the redistribution layer. The method may additionally include forming a further redistribution layer on the first mold encapsulation structure after forming the first mold encapsulation structure so that the one or more through mold interconnects extend through the first mold encapsulation structure from the second side of the redistribution layer to a first side of the further redistribution layer. The method may also include providing the chip stack on a second side of the further redistribution layer. The method may additionally include electrically connecting the plurality of second semiconductor dice to the first side of the further redistribution layer via a plurality of wirebonds.

[0095] In various embodiments, the method may include forming one or more first thermal vias. The method may further include forming a thermal conductive layer on the first

mold encapsulation layer after forming the first mold encapsulation structure. The method may also include forming one or more second thermal vias. The method may additionally include forming the second mold encapsulation layer so that the thermal conductive layer is between the first mold encapsulation structure and the second mold encapsulation structure. The one or more first thermal vias may extend from the first side of the redistribution layer through the redistribution layer and the first mold encapsulation structure to the thermal conductive layer. The one or more second thermal vias may extend from the thermal conductive layer through the second mold encapsulation structure.

[0096] The method may further include forming one or more through mold interconnects on the second side of the redistribution layer so that the one or more mold interconnects extend from the second side of the redistribution layer through the first mold encapsulation layer to the thermal conductive layer. The method may additionally include forming one or more electrically conductive through vias on the thermal conductive layer so that the one or more electrically conductive through vias are in electrical connection with the one or more through mold interconnects. The method may also include forming a plurality of wire bonds from the plurality of second semiconductor dice to the one or more electrically conductive through vias. The one or more second electrical connections may include the one or more through mold interconnects extending through the first mold encapsulation layer, the one or more electrically conductive through vias extending from the one or more through mold vias through the thermal conductive layer; and the plurality of wirebonds connecting the plurality of second semiconductor dice to the one or more electrically conductive through vias.

[0097] In various embodiments, the plurality of second semiconductor dice may be in vertical arrangement, i.e. form a vertical stacked arrangement. In various other embodiments, the plurality of second semiconductor dice may be in lateral arrangement. In other words, the plurality of second semiconductor dice may be arranged in a side by side planar arrangement over the first mold encapsulation structure.

[0098] Various embodiments may relate to chip level stacking at wafer level. Various embodiments may relate to chip level stacking at wafer level with a substrate in between.

[0099] FIGS. 12A-L show a method of forming a semiconductor package as shown in FIG. 8A according to various embodiments.

[00100] FIG. 12A shows forming a sacrificial layer 1226 on a temporary carrier 1224 according to various embodiments. The method may include providing the temporary carrier

1224. The sacrificial layer 1226 may be deposited over the surface of the temporary carrier 1224.

[00101] FIG. 12B shows forming a redistribution layer (RDL) 1202 over or on the sacrificial layer 1226 according to various embodiments. UBM may be formed over the sacrificial layer 1226 using a semi-additive process. The remaining RDL 1202, including metallization 1202a and the dielectric 1202b, may be processed over or on top of the UBMs. Smaller UBMs as well as wirebonding pads may be fabricated on the RDL 1202.

[00102] FIG. 12C shows forming of a masking layer 1228 on or over the redistribution layer (RDL) 1202 according to various embodiments. The masking layer 1228 may include a sacrificial material with a specified or predetermined thickness. The masking layer 1228 may be formed on or over the redistribution layer 1202 so that a first portion of the redistribution layer 1202 is covered by the masking layer 1228 and a second portion of the redistribution layer 1202 is exposed. The first portion may be referred to as the masked portion, while the second portion may be referred to as the unmasked or exposed portion. The masking layer 1228 may cover the portion of the redistribution layer 1202 with wirebonding pads.

[00103] FIG. 12D shows providing the first semiconductor dice 1206 and forming the one or more first electrical connections 1208 on the unmasked portion of the redistribution layer according to various embodiments. The semiconductor dice 1206 may be provided and the one or more electrical connections 1208, i.e. solder bumps, may be formed within cavities defined by the masking layer 1228. The solder bumps 1208 may be formed on the smaller UBMs in the RDL layer 1202.The first semiconductor dice 1206 may be assembled on or over the RDL layer 1202 by refiowing the solder bumps 1208. The first semiconductor dice may be flip chips.

[00104] FIG. 12E shows a molding process, i.e. deposition of a molding compound, according to various embodiments. The molding compound, e.g. mold epoxy may be deposited onto the cavities defined by the masking layer 1228. The mold layer 1210 formed may cover the first semiconductor dice 1206. The mold layer 1210 may further surround or cover the solder bumps 1208. The mold layer 1210 formed may initially extend or protrude out of the masking layer 1228.

[00105] FIG. 12F shows a grinding process being used to remove a portion of mold layer 1210, i.e. overmold, to expose the masking layer 1228 according to various embodiments.

[00106] FIG. 12G shows the removal of the masking layer 1228 according to various embodiments. The removal of the masking layer 1228 may form a plurality of first mold encapsulation structures 1210 with cavities between neighboring first mold encapsulation structures 1210. The removal of the masking layer 1228 may also expose or reveal the wirebonding pads. The absence of molding compound in the exposed areas may also help to reduce wafer warpage, thus facilitating the forming or assembly of a chip stack subsequently. In various alternate embodiments, the first mold encapsulation structures 1210 with cavities between neighboring first mold encapsulation structures 1210 may be formed from the molding layer by laser or dry etching after molding.

[00107] FIG. 12H shows providing or forming of chip stacks 1212 over the first mold encapsulation structures according to various embodiments. Each chip stack may include a plurality of second semiconductor dice arranged vertically with respect to one another. In other words, each stack 1212 includes a plurality of second semiconductor dice in vertical arrangement. Each chip stack 1212 may be held by die attach adhesive films (DAF) 1218. Neighbouring second semiconductor dice may be held together by die attach adhesive films 1218. The chip stacks 1212 may be attached to the first mold encapsulation structures 1210 using die attach adhesive films 1218.

[00108] One or more second electrical connections 1214, i.e. wirebonds, may be formed to electrically connect each second semiconductor die of the plurality of second semiconductor dice to the redistribution layer 1202. The wirebonds 1214 may connect the input/output pads (I/O pads) present on the second semiconductor die to the exposed wirebonding pads present on the RDL 1202.

[00109] FIG. 121 shows a second time molding process, i.e. another deposition of a molding compound, according to various embodiments. The molding compound may cover the chip stacks 1212. The molding compound may further cover the wirebonds 1214. The molding compound may form the second mold encapsulation structure 1216.

[001 10] FIG. 12J shows the removal of the carrier 1224 by debonding the sacrificial layer 1226 according to various embodiments. The carrier 1224 may be separated from the molded wafer including the redistribution layer 1202, the first semiconductor die 1206, the solder bumps 1208, the first mold encapsulation structures 1210, the chip stacks 1212 with the die attach adhesive films 1218, the wirebonds 1214, and the second mold encapsulation structures 1216.

[001 11] FIG. 12K shows the forming of the solder balls 1204 on the redistribution layer 1202 according to various embodiments. Solder balls 1204 may be attached to front side UBM.

[001 12] FIG. 12L shows the dicing or singulation of the molded wafer to form the semiconductor package according to various embodiments.

[001 13] FIGS. 13A-L show a method of forming a semiconductor package as shown in FIG. 8B according to various embodiments. The method may be similar to the method shown in FIGS. 12A-L but with the first semiconductor die being a wirebond chip instead of a flip chip.

[001 14] FIG. 13A shows forming a sacrificial layer 1326 on a temporary carrier 1324 according to various embodiments. The method may include providing the temporary carrier 1324. The sacrificial layer 1326 may be deposited over the surface of the temporary carrier 1324.

[001 15] FIG. 13B shows forming a redistribution layer (RDL) 1302 over or on the sacrificial layer 1326 according to various embodiments. UBM may be formed over the sacrificial layer 1326 using a semi-additive process. The remaining RDL 1302, including metallization 1302a and the dielectric 1302b, may be processed over or on top of the UBMs. Wirebonding pads may be fabricated on the RDL 1302.

[001 16] FIG. 13C shows forming of a masking layer 1328 on or over the redistribution layer (RDL) 1302 according to various embodiments. The masking layer 1328 may include a sacrificial material with a specified or predetermined thickness. The masking layer 1328 may be formed on or over the redistribution layer 1302 so that a first portion of the redistribution layer 1302 is covered by the masking layer 1328 and a second portion of the redistribution layer 1302 is exposed. The first portion may be referred to as the masked portion, while the second portion may be referred to as the unmasked or exposed portion.

[001 17] FIG. 13D shows providing the first semiconductor dice 1306 and forming the one or more first electrical connections 1320 on the unmasked portion of the redistribution layer according to various embodiments. The semiconductor dice 1306 may be provided within cavities defined by the masking layer 1328. The one or more first electrical connections 1320 may be formed or made via wirebonds. The wirebonds 1320 may connect the input/output (I/O) pads on the first semiconductor dice 1306 to some of the wirebonding pads on the RDL layer 1302, i.e. the wirebonding pads on the exposed portion of the RDL 1302. The first

semiconductor dice 1306 may be attached to the RDL 1302 via die attach adhesive films (DAF) 1322. The first semiconductor dice 1306 may be wirebond chips.

[00118] FIG. 13E shows a molding process, i.e. deposition of a molding compound, according to various embodiments. The molding compound, e.g. mold epoxy may be deposited onto the cavities defined by the masking layer 1328. The mold layer 1310 formed may cover the first semiconductor dice 1306. The mold layer 1310 may further cover the wirebonds 1320. The mold layer 1310 formed may initially extend or protrude out of the masking layer 1328.

[001 19] FIG. 13F shows a grinding process being used to remove a portion of mold layer 1310, i.e. overmold, to expose the masking layer 1328 according to various embodiments.

[00120] FIG. 13G shows the removal of the masking layer 1328 according to various embodiments. The removal of the masking layer 1328 may form a plurality of first mold encapsulation structures 1310 with cavities between neighboring first mold encapsulation structures 1310. The removal of the masking layer 1328 may also expose or reveal the remaining wirebonding pads. The absence of molding compound in the exposed areas may also help to reduce wafer warpage, thus facilitating the forming or assembly of a chip stack subsequently. In various alternate embodiments, the first mold encapsulation structures 1310 with cavities between neighboring first mold encapsulation structures 1310 may be formed from the molding layer by laser or dry etching after molding.

[00121] FIG. 13H shows providing or forming of chip stacks 1312 over the first mold encapsulation structures according to various embodiments. Each chip stack may include a plurality of second semiconductor dice arranged vertically with respect to one another. In other words, each stack 1312 includes a plurality of second semiconductor dice in vertical arrangement. Each chip stack 1312 may be held by die attach adhesive films (DAF) 1318. Neighbouring second semiconductor dice may be held together by die attach adhesive films 1318. The chip stacks 1312 may be attached to the first mold encapsulation structures 1310 using die attach adhesive films 1318.

[00122] One or more second electrical connections 1314, i.e. wirebonds, may be formed to electrically connect each second semiconductor die of the plurality of second semiconductor dice to the redistribution layer 1302. The wirebonds 1314 may connect the input/output pads (I/O pads) present on the second semiconductor die to the exposed wirebonding pads present on the RDL 1302.

[00123] FIG. 131 shows a second time molding process, i.e. another deposition of a molding compound, according to various embodiments. The molding compound may cover the chip stacks 1312. The molding compound may further cover the wirebonds 1314. The molding compound may form the second mold encapsulation structure 1316.

[00124] FIG. 13J shows the removal of the carrier 1324 by debonding the sacrificial layer 1326 according to various embodiments. The carrier 1324 may be separated from the molded wafer including the redistribution layer 1302, the first semiconductor die 1306, the die attach adhesive films 1322, the wirebonds 1320 ,the first mold encapsulation structures 1210, the chip stacks 1312 with the die attach adhesive films 1318, the wirebonds 1314, and the second mold encapsulation structures 1316.

[00125] FIG. 13K shows the forming of the solder balls 1304 on the redistribution layer 1302 according to various embodiments. Solder balls 1304 may be attached to front side UBM.

[00126] FIG. 13L shows the dicing or singulation of the molded wafer to form the semiconductor package according to various embodiments.

[00127] FIGS. 14A-K show a method of forming a semiconductor package as shown in FIG. 9 according to various embodiments.

[00128] FIG. 14A shows forming a sacrificial layer 1426 on a temporary carrier 1424 according to various embodiments. The method may include providing the temporary carrier 1424. The sacrificial layer 1426 may be deposited over the surface of the temporary carrier 1424.

[00129] FIG. 14B shows forming a redistribution layer (RDL) 1402 over or on the sacrificial layer 1426 according to various embodiments. UBM may be formed over the sacrificial layer 1426 using a semi-additive process. The remaining RDL 1402, including metallization 1402a and the dielectric 1402b, may be processed over or on top of the UBMs. Smaller UBMs may be fabricated on the RDL 1402. The redistribution layer 1402 may be referred to as the bottom RDL.

[00130] FIG. 14C shows forming of through mold interconnects (TMIs) 1422 on the redistribution layer after forming the redistribution layer 1402 according to various embodiments. The TMIs 1422 may be formed so that the TMIs 1422 are in electrical connection with some of the smaller UBMs in the RDL 1402.

[00131] FIG. 14D shows providing the first semiconductor dice 1406 and forming the one or more first electrical connections 1408 according to various embodiments. The semiconductor dice 1406 may be provided and the one or more electrical connections 1408, i.e. solder bumps, may be formed. The solder bumps 1408 may be formed on some or remaining of the smaller UBMs in the RDL 1402.The first semiconductor dice 1406 may be assembled on or over the RDL layer 1402 by reflowing the solder bumps 1408. The first semiconductor dice 1406 may be flip chips.

[00132] FIG. 14E shows a molding process, i.e. deposition of a molding compound, to form first mold encapsulation structures 1410 according to various embodiments. The first mold encapsulation structures 1410 formed may cover the first semiconductor dice 1406. The first mold encapsulation structures 1410 may further surround or cover the solder bumps 1408. The first mold encapsulation structures 1410 formed may initially cover the end portions of the through mold interconnects 1422 and the top surfaces of the first semiconductor dice 1406.

[00133] FIG. 14F shows a grinding process being used to remove a portion of the mold encapsulation structures 1410, i.e. overmold, to expose the end portions of the through mold interconnects 1422 according to various embodiments.

[00134] FIG. 14G shows forming a further redistribution layer (RDL) 1420 over or on the first mold encapsulation structures 1410 according to various embodiments. The further redistribution layer 1420 may include metallization 1420a and the dielectric 1420b. The metallization 1420 may be in electrical connection with the through mold interconnects 1422, which are at a first side of the further redistribution layer 1420. The further redistribution layer 1420 may include wirebonding pads or UBMs on a second side opposite the first side. The further redistribution layer 1420 may be referred to as top RDL.

[00135] FIG. 14H shows providing or forming chip stacks 1412 on or over the further redistribution layer 1420 according to various embodiments. Each chip stack may include a plurality of second semiconductor dice arranged vertically with respect to one another. In other words, each stack 1412 may include a plurality of second semiconductor dice in vertical arrangement. Each chip stack 1412 may be held by die attach adhesive films (DAF) 1418. Neighbouring second semiconductor dice may be held together by die attach adhesive films 1418. The chip stacks 1412 may be attached to the further redistribution layer 1420 using die attach adhesive films 1418. Wirebonds 1414 may be used to connect the I/O pads on each

second semiconductor die to UBMs or wirebonding pads on the further redistribution layer 1420.

[00136] FIG. 141 shows another molding process, i.e. deposition of a molding compound, to form second mold encapsulation structures 1416 on or over the further redistribution layer 1420 according to various embodiments. The second mold encapsulation structures 1416 may cover the chip stacks 1412 to form a single package. The second mold encapsulation structures 1416 may also cover the wirebonds 1414.

[00137] FIG. 14J shows the removal of temporary carrier 1424 according to various embodiments. The molded wafer may be separated from the temporary carrier 1424 by debonding the sacrificial layer 1426. The molded wafer may include the redistribution layer 1402, the first semiconductor dice 1406 with solder bumps 1408, through mold interconnects 1422, first mold encapsulation structures 1410, the further redistribution layer 1420, chip stacks 1412 with DAFs 1418 and wire bonds 1414, and the second mold encapsulation structures 1416.

[00138] FIG. 14K shows the forming of solder bumps 1404 and subsequent singulation of the molded wafer to form the semiconductor package according to various embodiments. The solder bumps 1404 may be formed on the UBMs on the redistribution layer 1402.

[00139] FIGS. 15A-M show a method of forming a semiconductor package as shown in FIG. 10 according to various embodiments.

[00140] FIG. 15A shows forming a sacrificial layer 1532 on a temporary carrier 1530 according to various embodiments. The method may include providing the temporary carrier 1530. The sacrificial layer 1532 may be deposited over the surface of the temporary carrier 1530.

[00141] FIG. 15B shows forming a redistribution layer (RDL) 1502 over or on the sacrificial layer 1532 according to various embodiments. UBM may be formed over the sacrificial layer 1532 using a semi-additive process. The remaining RDL 1502, including metallization 1502a and the dielectric 1502b, may be processed over or on top of the UBMs. Smaller UBMs may be fabricated on the sacrificial layer 1532. First thermal vias 1524a may also be formed on the redistribution layer 1502 and extending through the RDL 1502. The first thermal vias 1524a may extend through the thickness of the redistribution layer 1502

[00142] FIG. 15C shows forming the first thermal vias 1524a and the through mold interconnects (TMI) 1522 according to various embodiments. The first thermal vias 1524a

extending through the redistribution layer 1502 may be extended so that the vias 1524a protrude from the surface of the redistribution layer 1502. A portion of each via 1524a may be above the redistribution layer 1502. Through mold interconnects 1522 may be formed on some of the smaller UBMs on the redistribution layer 1502.

[00143] FIG. 15D shows providing the first semiconductor dice 1506 and forming the one or more first electrical connections 1508 according to various embodiments. The semiconductor dice 1506 may be provided and the one or more electrical connections 1508, i.e. solder bumps, may be formed. The solder bumps 1508 may be formed on some or remaining of the smaller UBMs in the RDL layer 1502.The first semiconductor dice 1506 may be assembled on or over the RDL layer 1502 by reflowing the solder bumps 1508. The first semiconductor dice 1506 may be flip chips.

[00144] FIG. 15E shows a molding process, i.e. deposition of a molding compound, to form first mold encapsulation structures 1510 according to various embodiments. The first mold encapsulation structures 1510 formed may cover the first semiconductor dice 1506. The first mold encapsulation structures 1510 may further surround or cover the solder bumps 1508. The first mold encapsulation structures 1510 formed may initially cover the end portions of the through mold interconnects 1522, the end portions of the first thermal vias 1524a, and the top surfaces of the first semiconductor dice 1506.

[00145] FIG. 15F shows a mechanical backgrinding process being used to remove a portion of the first mold encapsulation structures 1510, i.e. overmold, to expose the end portions of the through mold interconnects 1522 and the end portions of the first thermal vias 1524a according to various embodiments.

[00146] FIG. 15G shows forming of a thermal conductive layer 1520 and electrically conductive through vias 1528 on or above the first mold encapsulation structures 1510. The thermal conductive layer 1520 may be formed so that the thermal conductive layer 1520 is in thermal contact with the first thermal vias 1524a. The electrically conductive through vias 1528 may be formed so that the electrically conductive through vias 1528 are in electrical connection with the through mold interconnects 1522. The electrically conductive through vias 1528 may extend through the thickness of the thermal conductive layer 1520.

[00147] FIG. 15H shows providing or forming chip stacks 1512 on or over the thermal conductive layer 1520 according to various embodiments. Each chip stack 1512 may include a plurality of second semiconductor dice arranged vertically with respect to one another. In

other words, each stack 1512 may include a plurality of second semiconductor dice in vertical arrangement. Each chip stack 1512 may be held by die attach adhesive films (DAF) 1518. Neighbouring second semiconductor dice may be held together by die attach adhesive films 1518. The chip stacks 1512 may be attached to the thermal conductive layer 1520 using die attach adhesive films 1518. The second semiconductor dice may be wirebond chips. Wirebonds 1514 may be used to connect the I/O pads on each second semiconductor die to the electrically conductive through vias 1528 extending though the thermal conductive layer 1520.

[00148] FIG. 151 shows forming of the second thermal conductive vias 1524b according to various embodiments. The second thermal conductive vias 1524b may be formed on the thermal conductive layer 1520 and may be in thermal contact with the thermal conductive layer 1520.

[00149] FIG. 15J shows another molding process, i.e. deposition of a molding compound, to form second mold encapsulation structures 1516 on or over the thermal conductive layer 1520 according to various embodiments. The second mold encapsulation structures 1516 may cover the chip stacks 1512 to form a single package. The second mold encapsulation structures 1516 may also cover the wirebonds 1514 and may also initially cover the end portions of the second thermal vias 1524b.

[00150] FIG. 15K shows a mechanical backgrinding process being used to remove a portion of the second mold encapsulation structures 1516, i.e. overmold, to expose the end portions of end portions of the second thermal vias 1524b according to various embodiments.

[00151] FIG. 15L shows the removal of temporary carrier 1530 according to various embodiments. The molded wafer may be separated from the temporary carrier 1530 by debonding the sacrificial layer 1532. The molded wafer may include the redistribution layer 1502, the first semiconductor dice 1506 with solder bumps 1508, through mold interconnects 1522, first mold encapsulation structures 1510, first thermal vias 1524a, the thermal conductive layer 1520, chip stacks 1512 with DAFs 1518 and wire bonds 1514, the second mold encapsulation structures 1516, and the second thermal vias 1524b.

[00152] FIG. 15M shows the forming of solder bumps 1504 and thermal bumps 1526, followed by subsequent singulation of the molded wafer to form the semiconductor package according to various embodiments. The solder bumps 1504 may be formed on the UBMs on the redistribution layer 1502. The solder bumps 1504 may be formed so that the solder bumps

1504 are in electrical connection with the metallization 1504a, 1520a, the TMIs 1522, the first semiconductor dice 1506 and/or the second semiconductor dice. The thermal bumps may be formed so that the thermal bumps 1526 are in thermal contact with the thermal vias 1524a, 1524b and the thermal conductive layer 1520.

[00153] The semiconductor packages described herein may include a plurality of chips and may be referred to as multi-chip packages. The multi-chip packages may be traced by X-ray inspection and scanning electron microscopy (SEM) to identify various features. Various embodiments may relate to advanced packaging, fan-out wafer level packaging, and/or package on package (PoP). In various embodiments, the semiconductor package may be a three dimensional (3D) stacked chip fan-out wafer level package.

[00154] In various embodiments, the fabrication process may involve fabricating RDL on a temporary carrier. Chips with TSVs may be stacked onto the RDL and electrical connections may be formed using solder joints. Alternatively, chips may be stacked using die attach adhesive films and may be connected to the RDL with wirebonds. A mold process may be used to encapsulate the RDK and stacked chips. The temporary carrier may be removed and the molded wafer may be diced into packages. The method may form a fan-out wafer level package with 3D stacked chips.

[00155] Various embodiments may have a low height profile as there is no substrate. Various embodiments may not have through mold interconnects.

[00156] In various embodiments, the chips may be connected using different interconnection methods.

[00157] The different interconnection methods may include stacking TSV chips and forming electrical connections to RDLs using micro-bump joints and/or stacking wirebond chips using die attach adhesive films and wirebonding the I/Os of the chips to the RDL layer. Additionally or alternatively, smaller sized chips, e.g. logic chips may be attached onto the RDL using flip chip method or wirebonding and encapsulated first to form a larger pedestal in which the larger sized chips, e.g. memory chips may be stacked onto. The I/Os of the larger chips may be connected to the RDL using wirebonding. A second molding may be carried out to encapsulate the entire stack.

[00158] Various embodiments may involve direct stacking of chips onto RDL and forming interconnects (e.g. solder bumps, wirebonding) to RDL. Various embodiments may relate to encapsulation of stacked chips to form a single embedded package. Wafer level molding may

be used to form the single package. In various embodiments, no package on package stacking may be required. In various embodiments, no additional RDL processing may be required after encapsulation.

[00159] Conventional 3D fan-out wafer level packages may require additional RDL processing on package backside to facilitate chip stacking. Further conventional packages may include a substrate which contributes to the package height. Also, in conventional packages, there are solder ball interconnects between the top package and the bottom package which further increases the package height. In addition, conventional package may require drilling and filling of through mold vias (TMVs).

[00160] In contrast, various embodiments may not require the ball grid array (BGA) substrate, which in turn lead to a lower package height. In various embodiments, the package height may be lower than 1 mm. Various embodiments may not need TMV processing. Various embodiments may not require additional RDL processing on package backside to facilitate chip stacking, which lower costs. Various embodiments may have shorter interconnection length as the substrate and PoP solder balls are not required.

[00161] In additional various embodiments may be compatible with semiconductor packaging processes, which lead to lower costs.

[00162] While the invention has been particularly shown and described with reference to specific embodiments, it should be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. The scope of the invention is thus indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced.

CLAIMS

1. A semiconductor package comprising:

a redistribution layer;

a plurality of solder balls on a first side of the redistribution layer;

a first semiconductor die over a second side of the redistribution layer opposite the first side;

one or more first electrical connections electrically connecting the first semiconductor die to the redistribution layer;

a first mold encapsulation structure covering the first semiconductor die;

a chip stack comprising a plurality of second semiconductor dice over the first mold encapsulation structure;

one or more second electrical connections electrically connecting each second semiconductor die of the plurality of second semiconductor dice to the redistribution layer; and

a second mold encapsulation structure covering the chip stack;

wherein a width of the second mold encapsulation structure is at least substantially equal to a width of the first encapsulation structure.

2. The semiconductor package of claim 1,

wherein the redistribution layer comprises a plurality of dielectric layers and a plurality of interconnection elements electrically connecting the first side of the redistribution layer to the second side of the redistribution layer.

3. The semiconductor package of claim 1,

wherein the width of the second mold encapsulation structure is greater than the width of the first encapsulation structure.

4. The semiconductor package of claim 1,

wherein one second semiconductor die of the plurality of second semiconductor dice has a size different from another second semiconductor die of the plurality of second semiconductor dice.

5. The semiconductor package of claim 1,

wherein the first electrical connections are solder bumps.

6. The semiconductor package of claim 1,

wherein the first electrical connections are wirebonds.

7. The semiconductor package of claim 1,

wherein the one or more second electrical connections are wirebonds.

8. The semiconductor package of claim 1,

wherein a portion of the first mold encapsulation structure is between the first semiconductor die and the chip stack.

9. The semiconductor package of claim *1*, further comprising:

a further redistribution layer between the first mold encapsulation structure and the second mold encapsulation structure;

wherein the one or more second electrical connections comprise:

one or more through mold interconnects extending through the first mold encapsulation structure and electrically connecting a first side of the further redistribution layer to the second side of the redistribution layer; and

a plurality of wirebonds electrically connecting the plurality of second semiconductor dice to a second side of the further redistribution layer.

10. The semiconductor package of claim 1, further comprising:

a thermal conductive layer between the first mold encapsulation structure and the second mold encapsulation structure;

one or more first thermal vias extending from the first side of the redistribution layer through the redistribution layer and the first mold encapsulation to the thermal conductive layer; and

one or more second thermal vias extending from the thermal conductive layer through the second mold encapsulation structure;

wherein the one or more second electrical connections comprise:

one or more through mold interconnects extending through the first mold encapsulation layer;

one or more electrically conductive through vias extending from the one or more through mold vias through the thermal conductive layer; and

a plurality of wirebonds connecting the plurality of second semiconductor dice to the one or more electrically conductive through vias.

11. A method of forming a semiconductor package, the method comprising:

forming a redistribution layer;

forming a plurality of solder balls on a first side of the redistribution layer;

providing a first semiconductor die over a second side of the redistribution layer opposite the first side;

forming one or more first electrical connections electrically connecting the first semiconductor die to the redistribution layer;

forming a first mold encapsulation structure covering the first semiconductor die;

providing a chip stack comprising a plurality of second semiconductor dice over the first mold encapsulation structure;

forming one or more second electrical connections electrically connecting each second semiconductor die of the plurality of second semiconductor dice to the redistribution layer; and

forming a second mold encapsulation structure covering the chip stack;

wherein a width of the second mold encapsulation structure is at least substantially equal to a width of the first encapsulation structure.

12. The method of claim 11,

wherein forming the redistribution layer comprises:

providing a temporary carrier;

forming a sacrificial release layer over temporary carrier;

forming a first layer on the sacrificial release layer, the first layer comprising a first dielectric and one or more first conductive lines; and

forming a second layer on the first layer, the second layer comprising a second dielectric and one or more second conductive lines;

wherein the one or more first conductive lines are in electrical connection with the one or more second conductive lines.

13. The method of claim 11, further comprising:

forming a masking layer on the redistribution layer so that a first portion of the redistribution layer is covered by the masking layer and a second portion of the redistribution layer is exposed.

14. The method of claim 13, further comprising:

providing the first semiconductor die and forming the one or more first electrical connections on the second portion of the redistribution layer; and

depositing a molding compound over the first semiconductor die.

15. The method of claim 14, further comprising:

removing the masking layer to form the first mold encapsulation structure covering the first semiconductor die.

16. The method of claim 11,

wherein the plurality of solder balls are formed after forming the second mold encapsulation structure.

17. The method of claim 11, further comprising:

providing further first semiconductor dice over the second side of the redistribution layer opposite the first side;

providing further chip stacks over the first mold encapsulation structure so that each further chip stack is over a respective further first semiconductor die;

forming the second mold encapsulation structure by covering the plurality of chips stacks comprising the chip stack and the further chip stacks to form a wafer-level intermediate structure; and

singulating the wafer-level intermediate structure to form the semiconductor package.

18. The method of claim 11, further comprising:

forming one or more through mold interconnects on the second side of the redistribution layer after forming the redistribution layer and before providing the semiconductor die over the second side of the redistribution layer; and

forming a further redistribution layer on the first mold encapsulation structure after forming the first mold encapsulation structure so that the one or more through mold interconnects extend through the first mold encapsulation structure from the second side of the redistribution layer to a first side of the further redistribution layer;

providing the chip stack on a second side of the further redistribution layer; and

electrically connecting the plurality of second semiconductor dice to the first side of the further redistribution layer via a plurality of wirebonds.

19. The method of claim 11, further comprising:

forming one or more first thermal vias;

forming a thermal conductive layer on the first mold encapsulation layer after forming the first mold encapsulation structure;

forming one or more second thermal vias; and

forming the second mold encapsulation layer so that the thermal conductive layer is between the first mold encapsulation structure and the second mold encapsulation structure;

wherein the one or more first thermal vias extend from the first side of the redistribution layer through the redistribution layer and the first mold encapsulation structure to the thermal conductive layer; and

wherein the one or more second thermal vias extend from the thermal conductive layer through the second mold encapsulation structure.

20. The method of claim 19, further comprising:

forming one or more through mold interconnects on the second side of the redistribution layer so that the one or more through mold interconnects extend from the second side of the redistribution layer through the first mold encapsulation layer to the thermal conductive layer;

forming one or more electrically conductive through vias on the thermal conductive layer so that the one or more electrically conductive through vias are in electrical connection with the one or more through mold interconnects; and

forming a plurality of wire bonds from the plurality of second semiconductor dice to the one or more electrically conductive through vias;

wherein the one or more second electrical connections comprise:

the one or more through mold interconnects extending through the first mold encapsulation layer;

the one or more electrically conductive through vias extending from the one or more through mold vias through the thermal conductive layer; and

the plurality of wirebonds connecting the plurality of second semiconductor dice to the one or more electrically conductive through vias.

FIG. 1

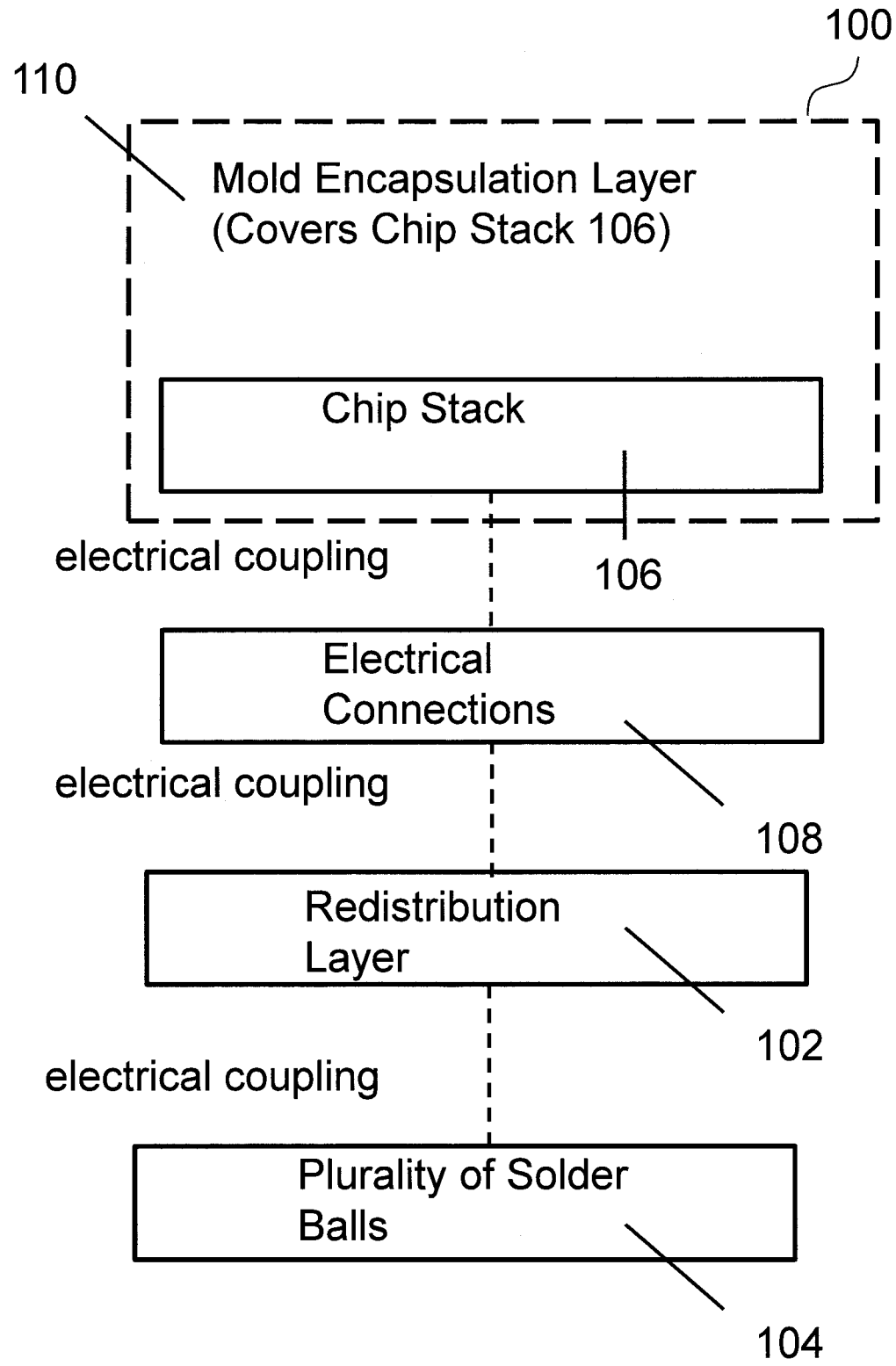

100
110
Mold Encapsulation Layer
(Covers Chip Stack 106)
Chip Stack
electrical coupling
106
Electrical
Connections
electrical coupling
108
Redistribution
Layer
102
electrical coupling
Plurality of Solder
Balls
104

FIG. 2

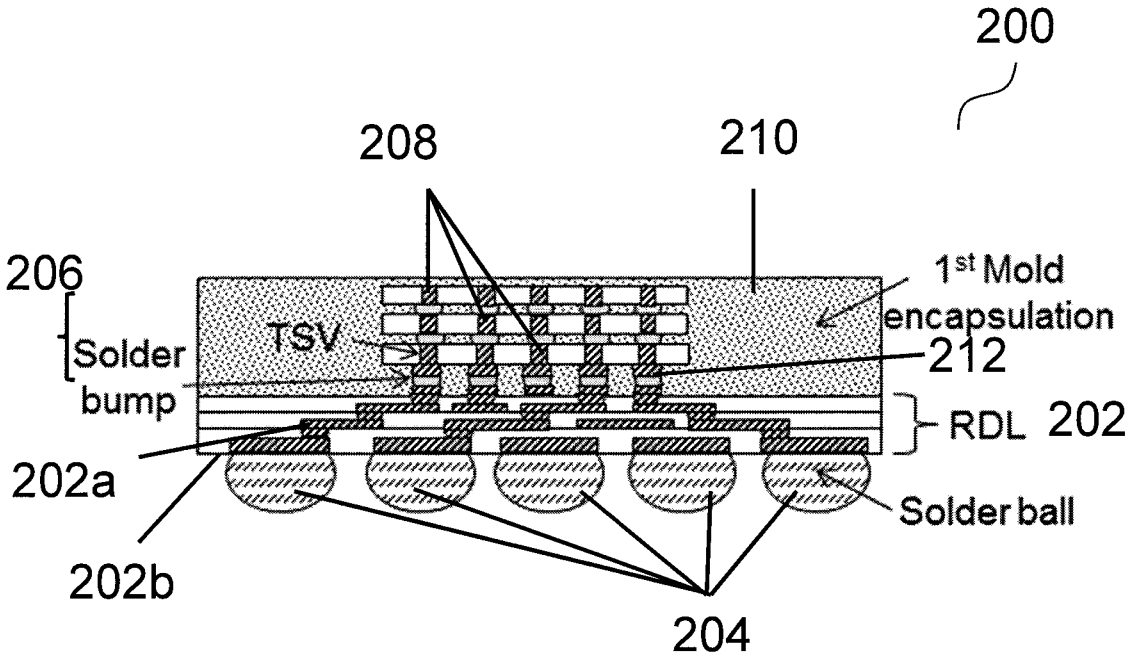

200
208
210
206
1st Mold encapsulation
TSV
Solder bump
212
RDL 202
202a
Solder ball
202b
204

FIG. 3

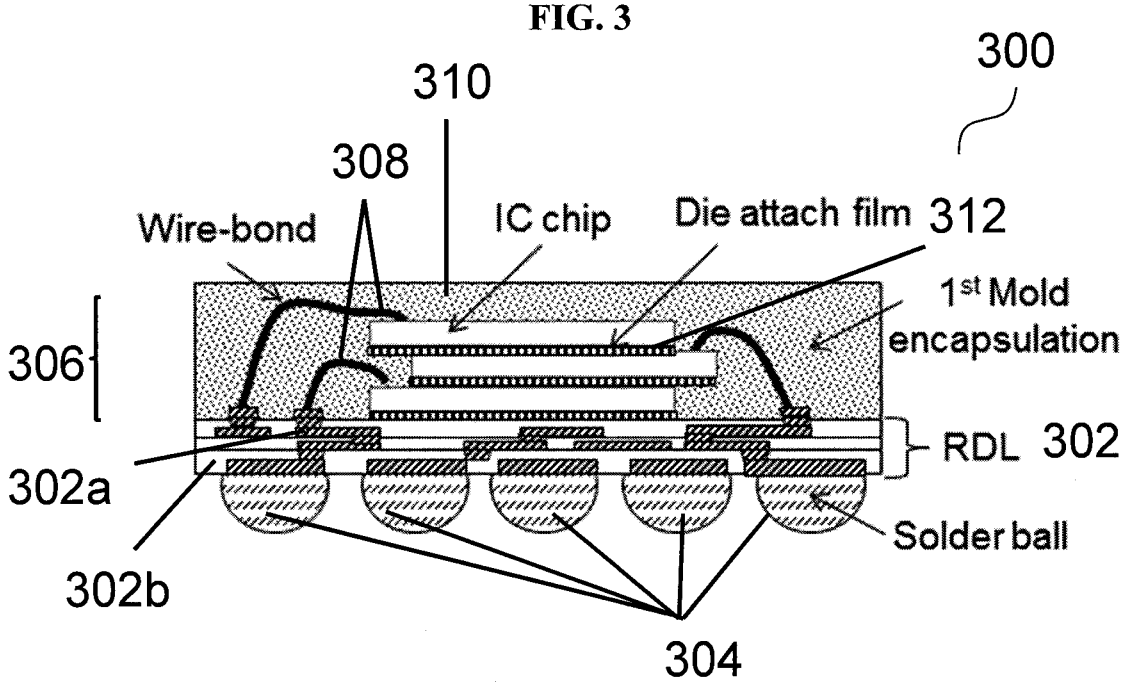

300
310
308
Wire-bond
IC chip
Die attach film 312
1st Mold encapsulation
306
RDL 302
302a
Solder ball
302b
304

FIG. 4

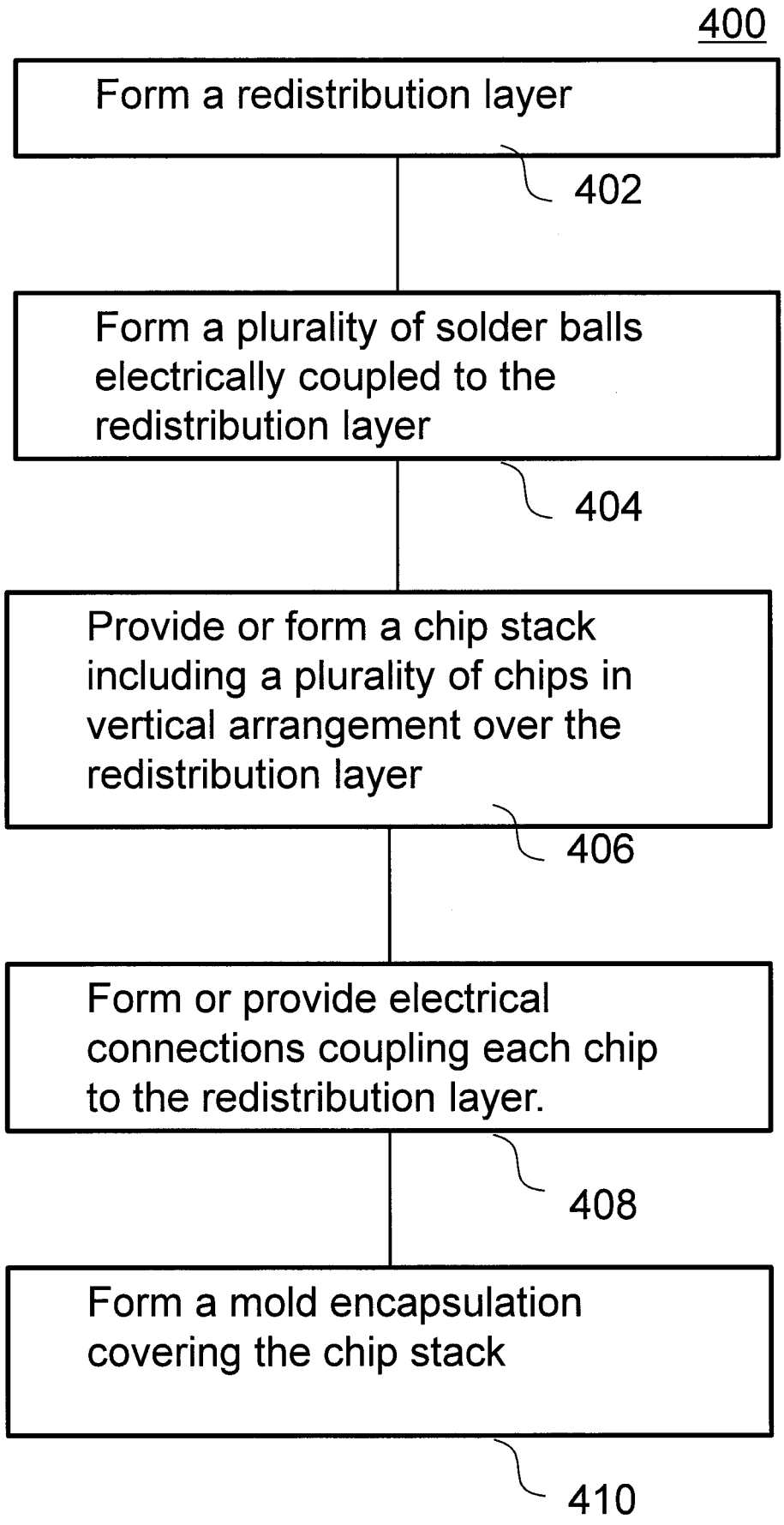
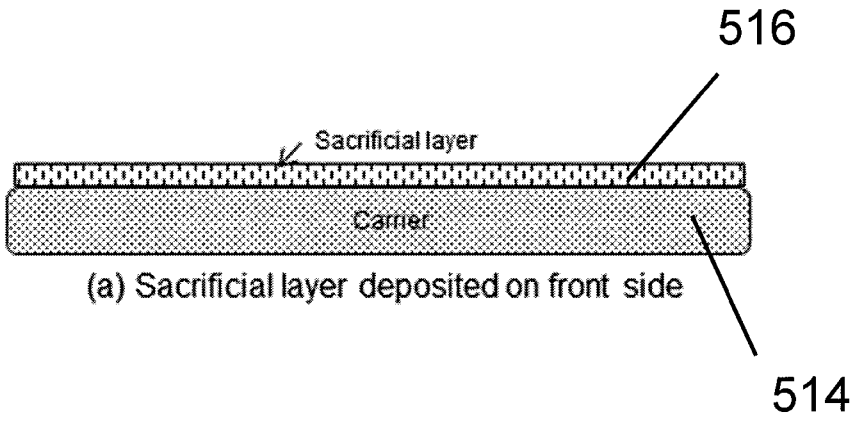
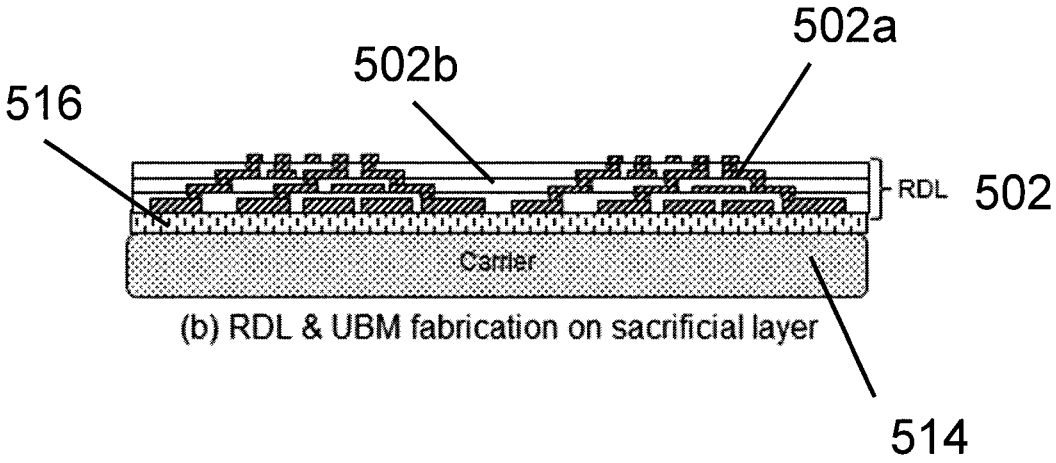

400
Form a redistribution layer
402
Form a plurality of solder balls electrically coupled to the redistribution layer
404
Provide or form a chip stack including a plurality of chips in vertical arrangement over the redistribution layer
406
Form or provide electrical connections coupling each chip to the redistribution layer.
408
Form a mold encapsulation covering the chip stack
410

FIG. 5A



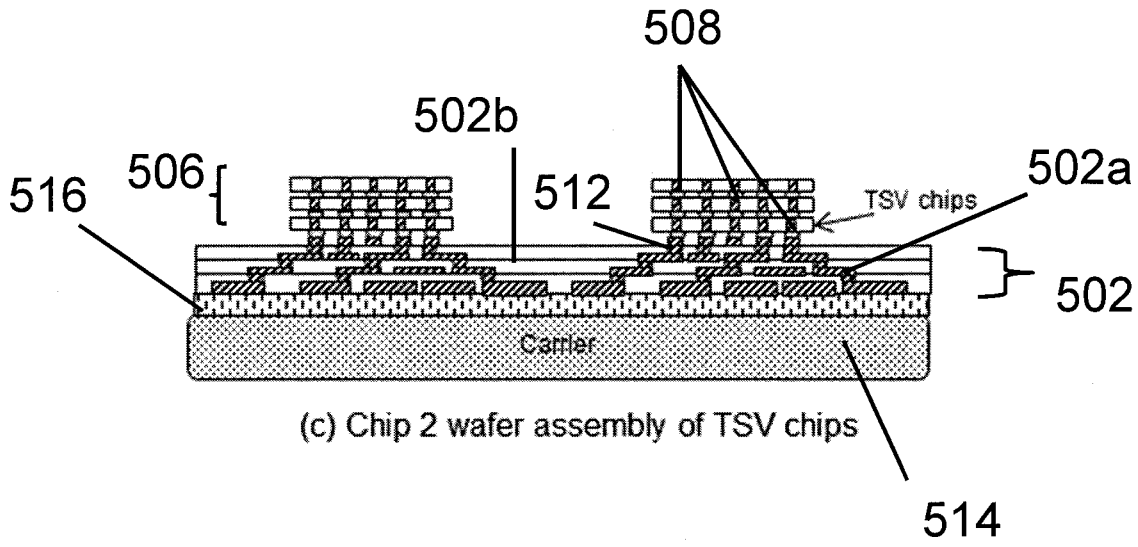
(a) Sacrificial layer deposited on front side

FIG. 5B



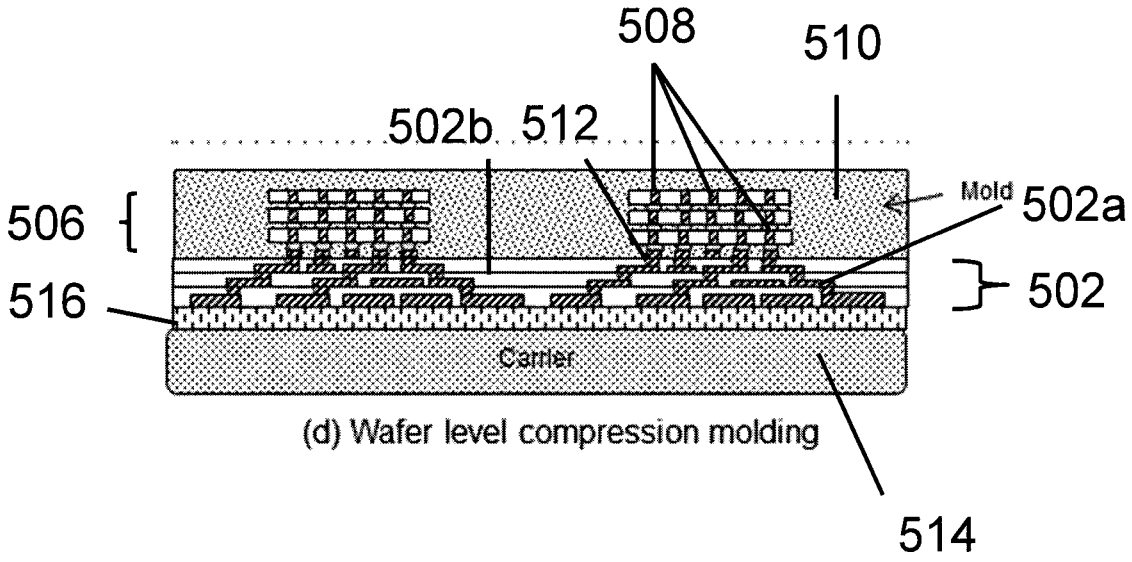
(b) RDL & UBM fabrication on sacrificial layer

FIG. 5C



(c) Chip 2 wafer assembly of TSV chips

FIG. 5D



(d) Wafer level compression molding

FIG. 5E

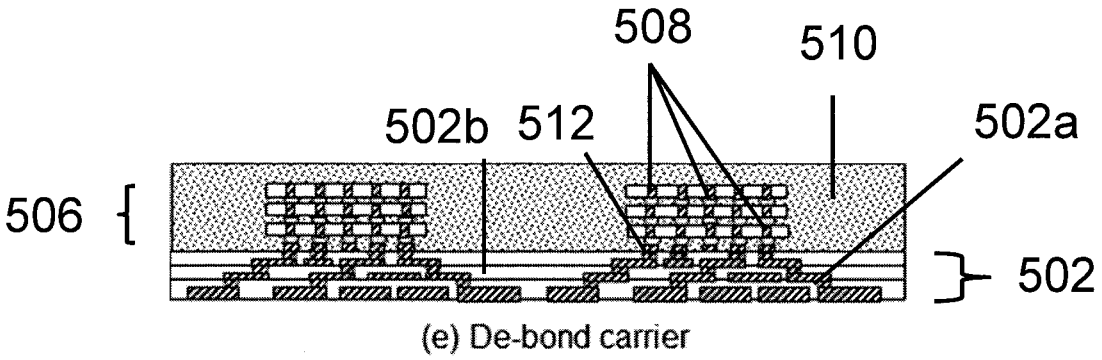

508
510
502b
512
502a
506
502
(e) De-bond carrier

FIG. 5F

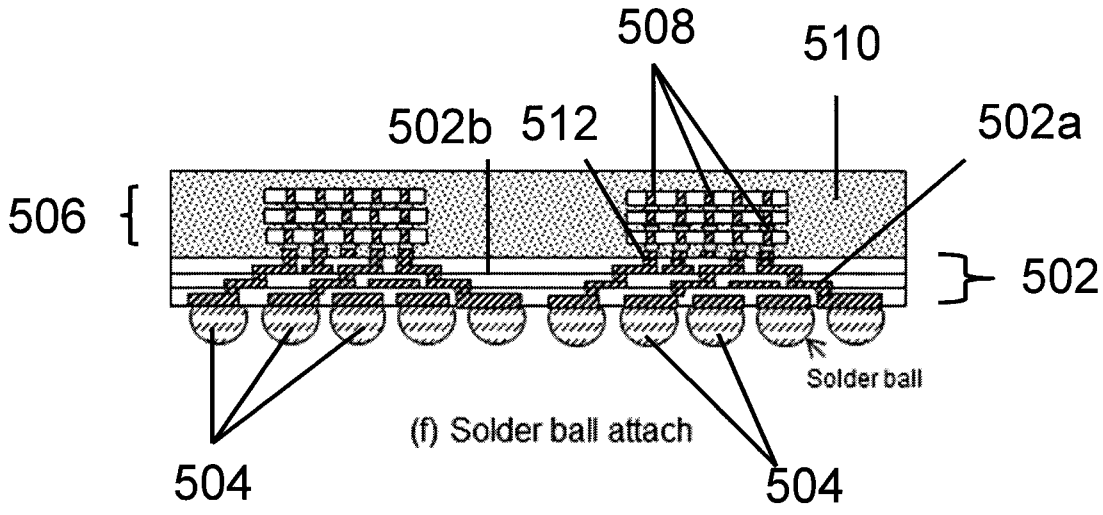

508
510
502b
512
502a
506
502
Solder ball
(f) Solder ball attach
504
504

FIG. 5G

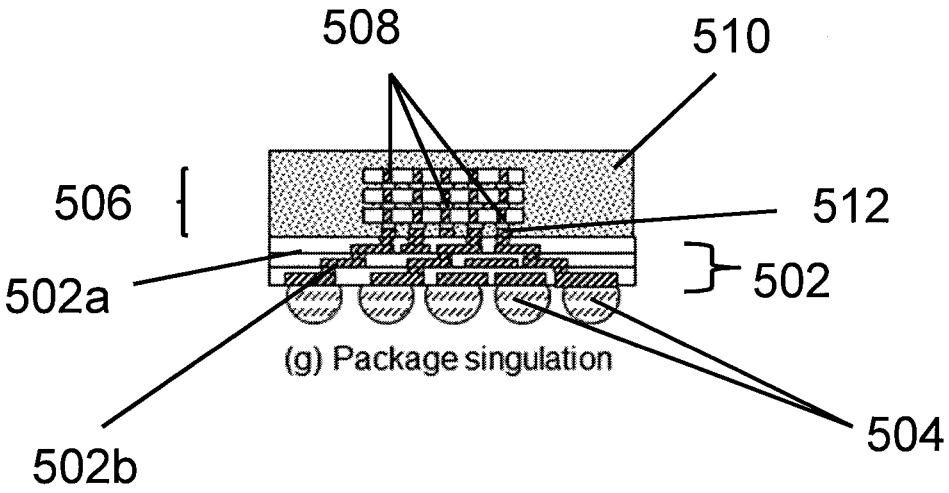


FIG. 6A

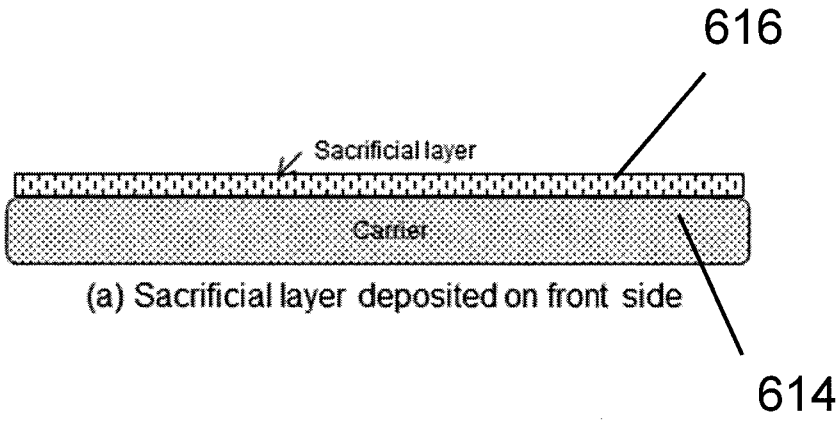

616
Sacrificial layer
Carrier
(a) Sacrificial layer deposited on front side
614

FIG. 6B

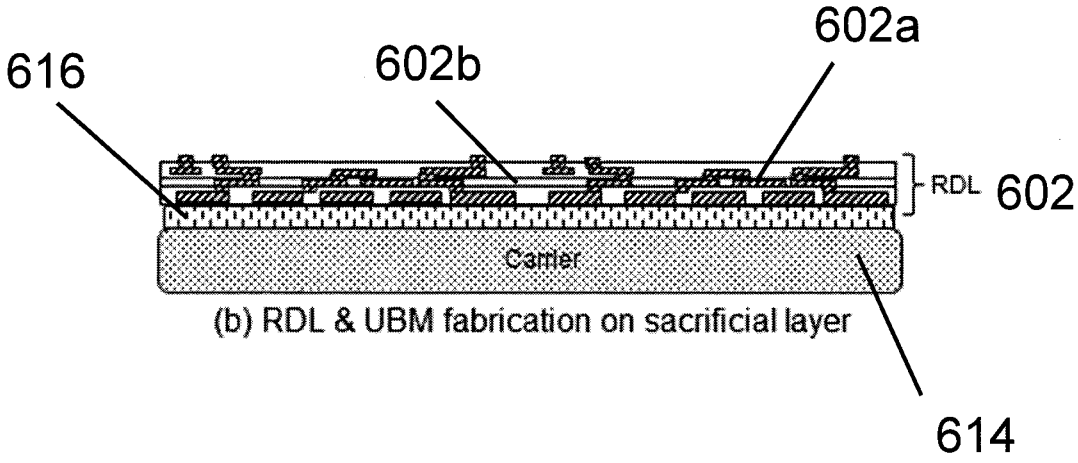
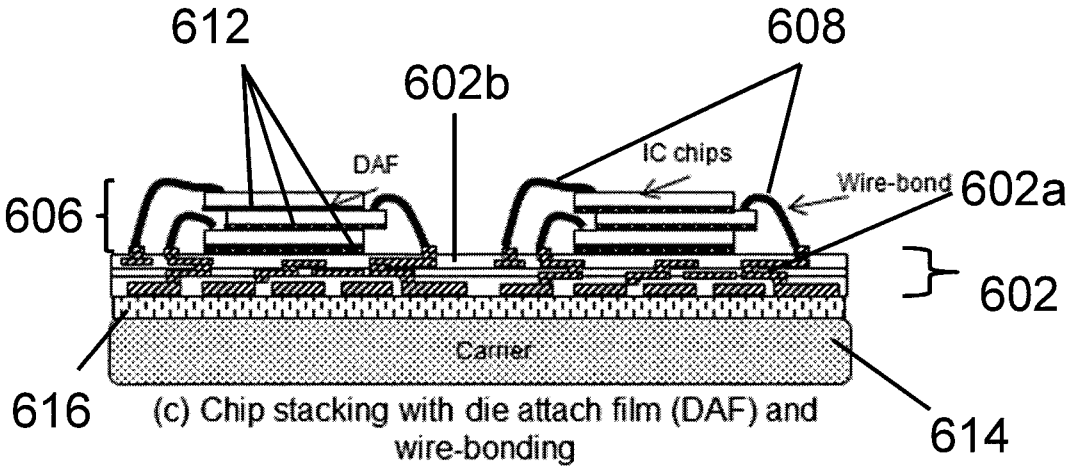
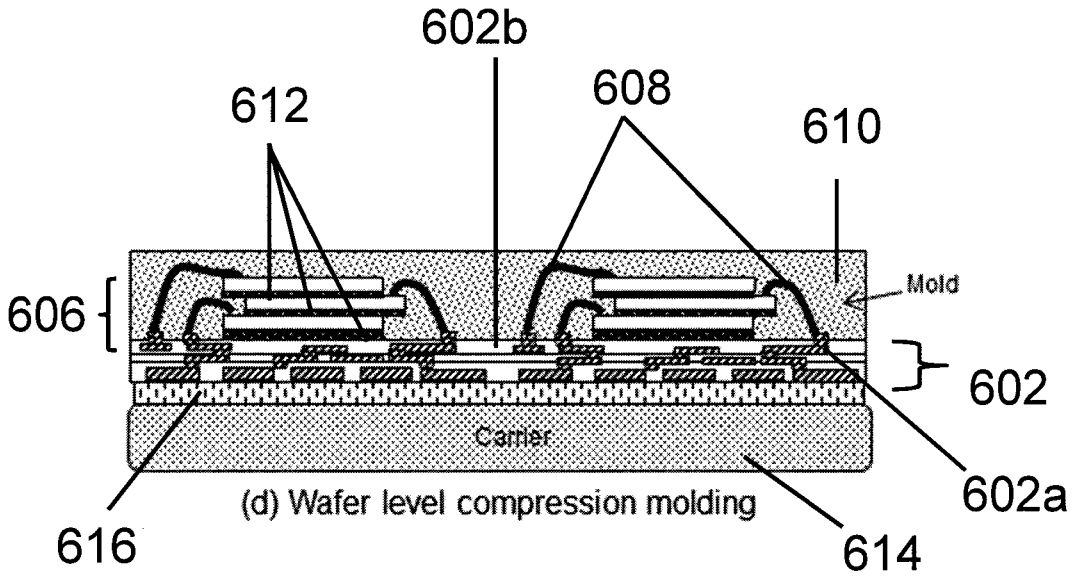

602a
616
602b
RDL
602
Carrier
(b) RDL & UBM fabrication on sacrificial layer
614

FIG. 6C



(c) Chip stacking with die attach film (DAF) and wire-bonding

FIG. 6D



(d) Wafer level compression molding

FIG. 6E

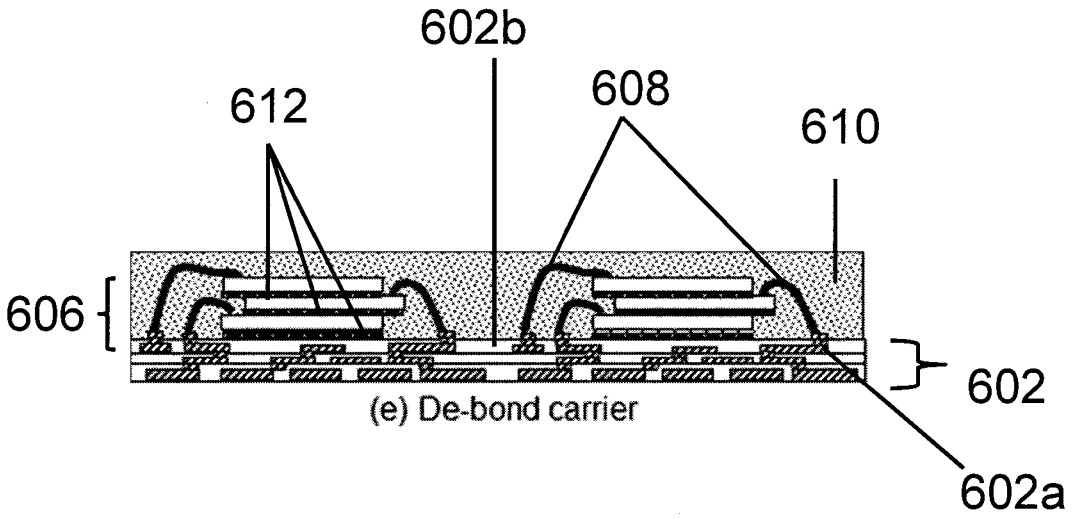

602b
612
608
610
606
602
602a
(e) De-bond carrier

FIG. 6F

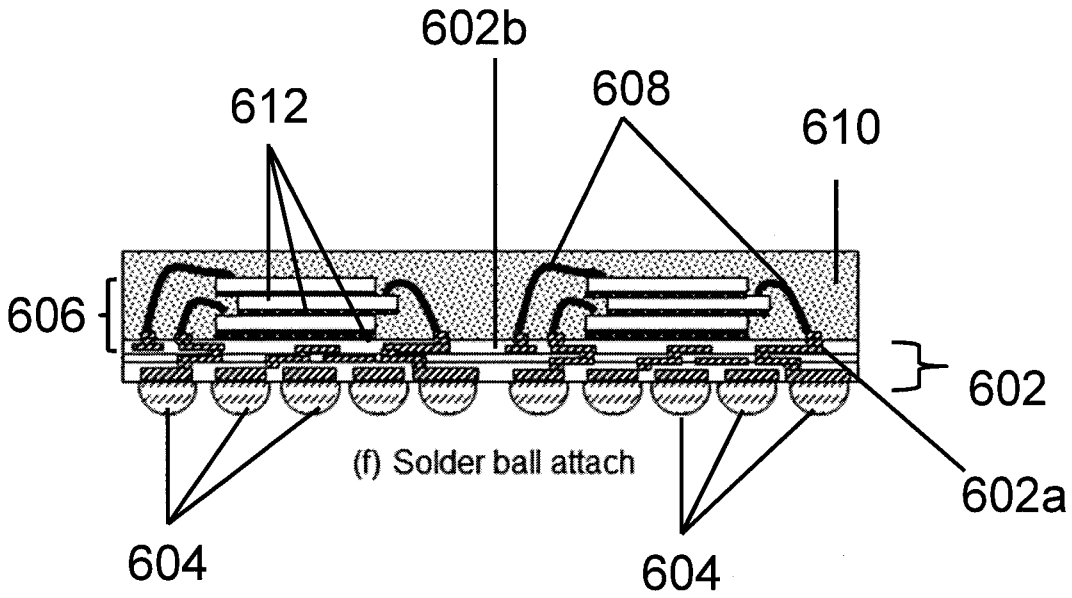

602b
612
608
610
606
602
(f) Solder ball attach
602a
604
604

FIG. 6G

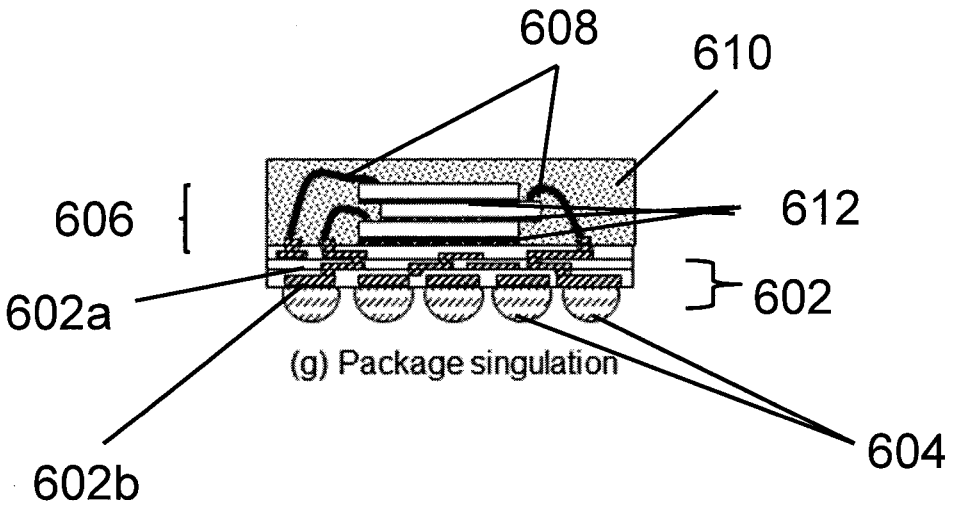


FIG. 7

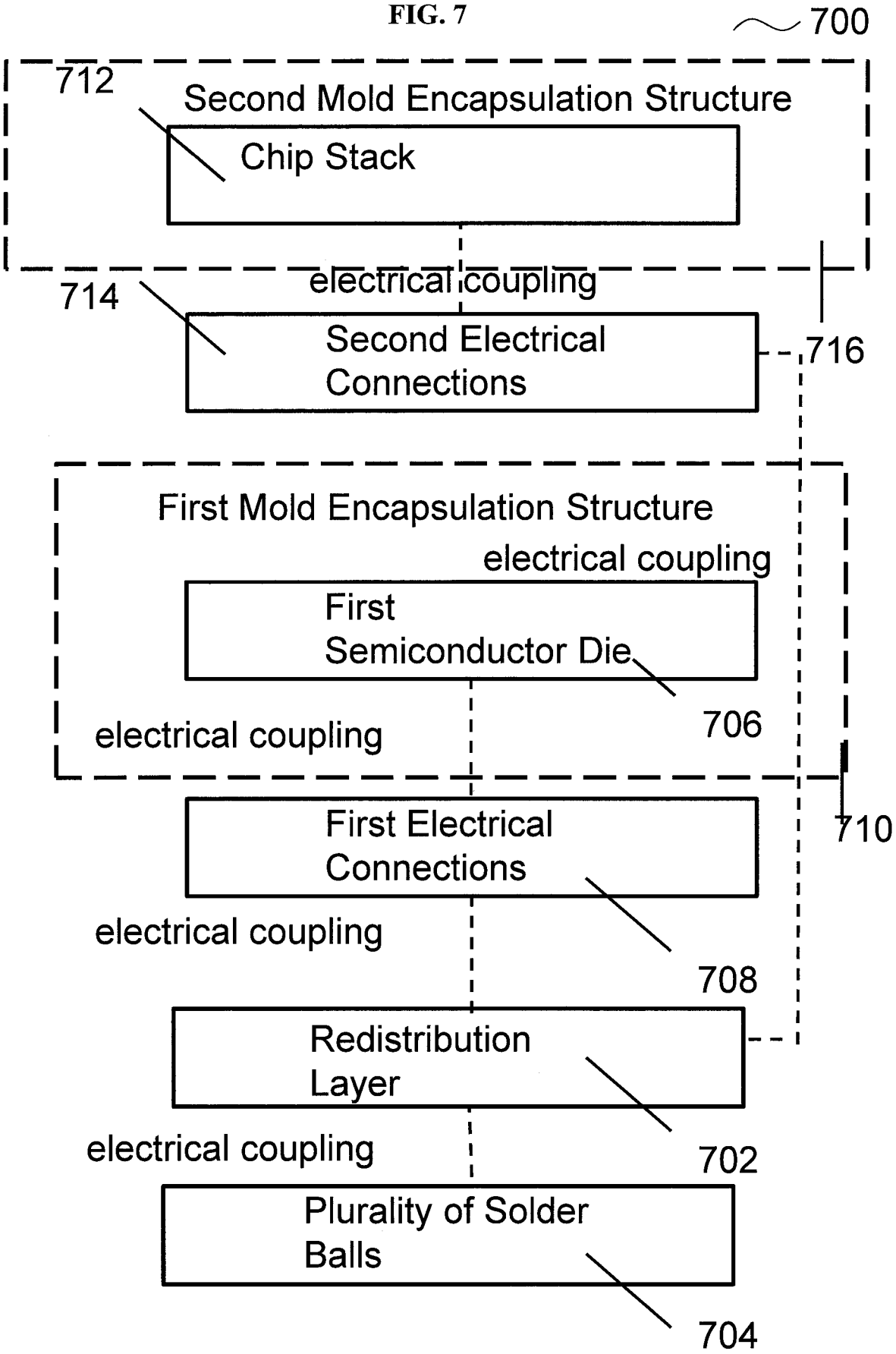

700
712
Second Mold Encapsulation Structure
Chip Stack
electrical coupling
714
Second Electrical Connections
716
First Mold Encapsulation Structure
electrical coupling
First Semiconductor Die
706
electrical coupling
710
First Electrical Connections
electrical coupling
708
Redistribution Layer
electrical coupling
702
Plurality of Solder Balls
704

FIG. 8A

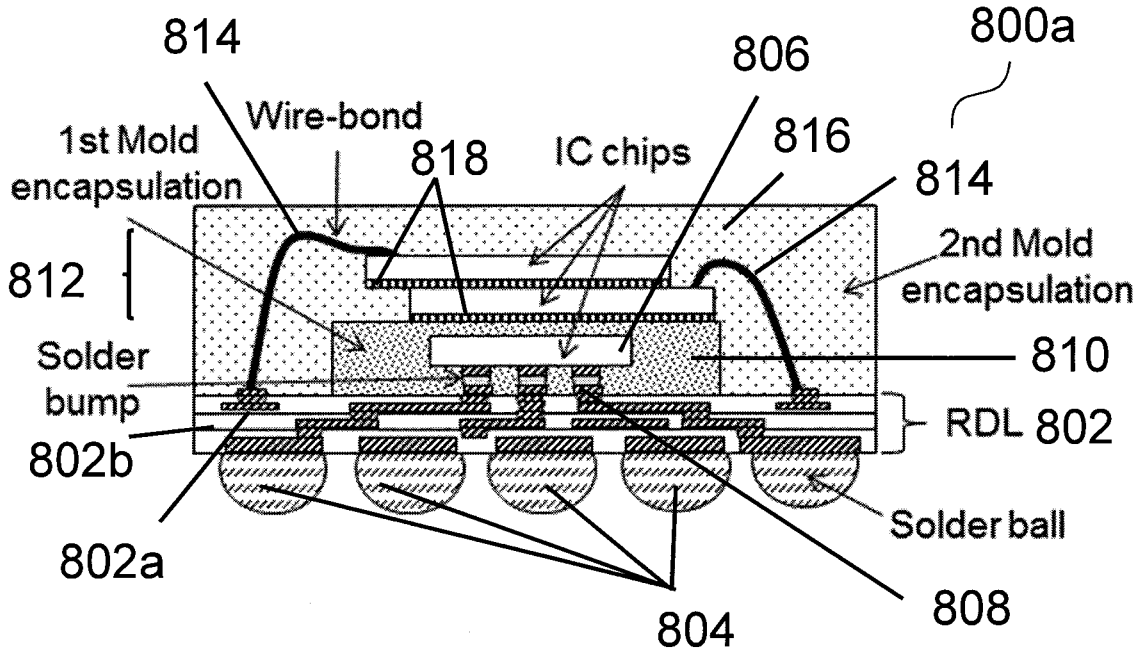
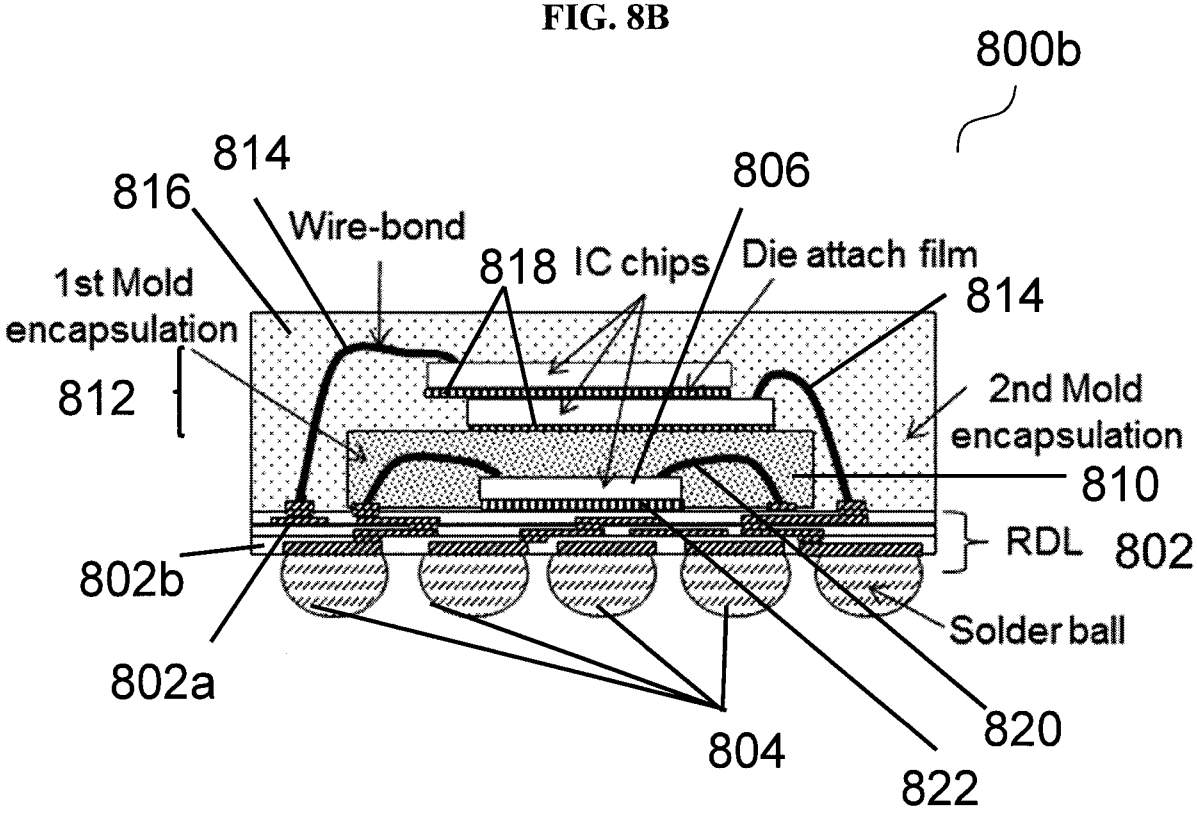

814
Wire-bond
1st Mold encapsulation
818
IC chips
806
816
800a
814
2nd Mold encapsulation
812
Solder bump
810
RDL 802
802b
Solder ball
802a
808
804

FIG. 8B


800b
814
816
Wire-bond
818
IC chips
806
Die attach film
1st Mold encapsulation
814
812
2nd Mold encapsulation
810
RDL 802
802b
Solder ball
802a
820
804
822

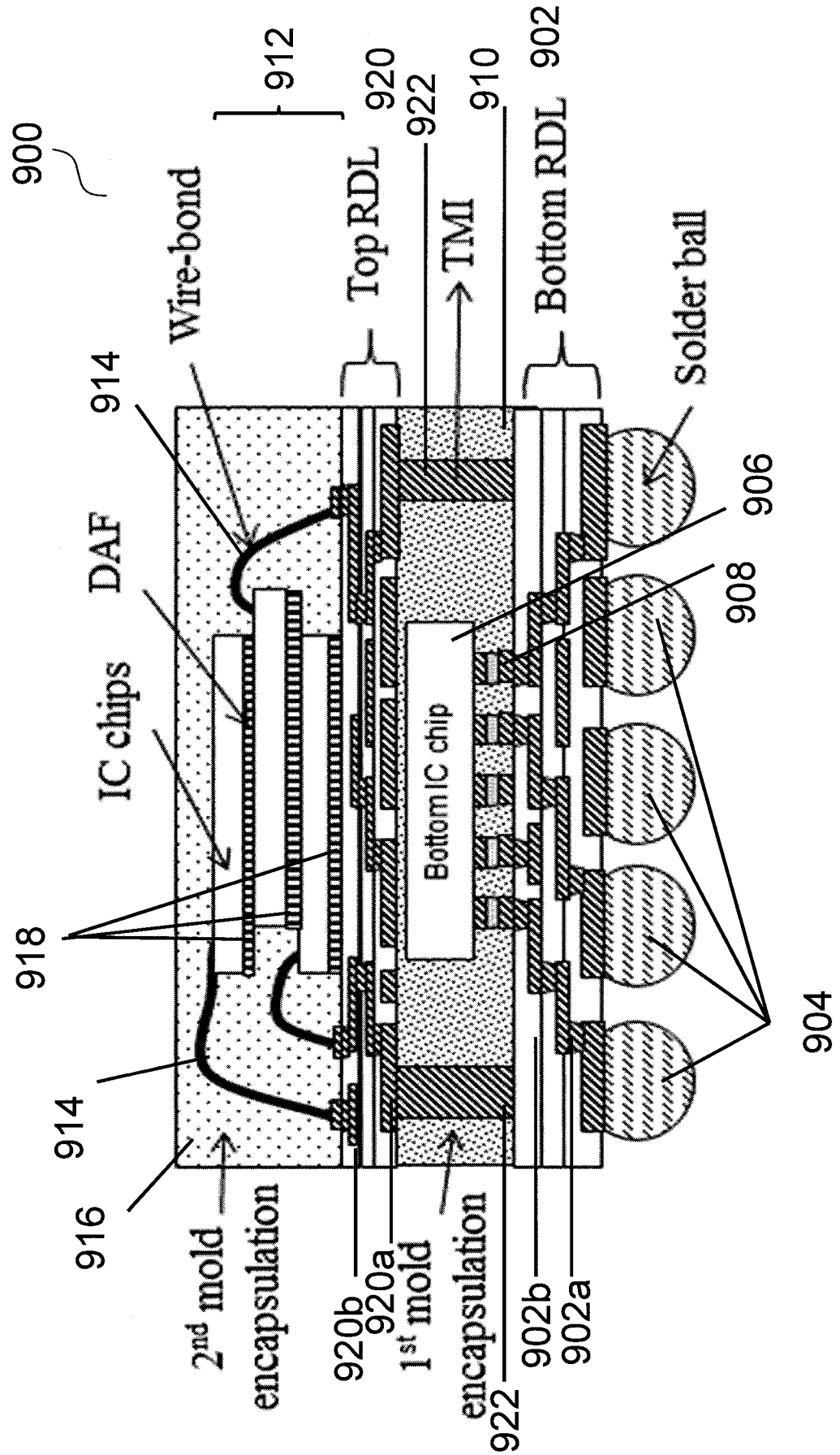

900
912
920
922
910
902
Wire-bond
Top RDL
TMI
Bottom RDL
Solder ball
914
DAF
IC chips
906
908
Bottom IC chip
918
914
916
904
2nd mold encapsulation
920b
920a
1st mold encapsulation
922
902b
902a

FIG. 9

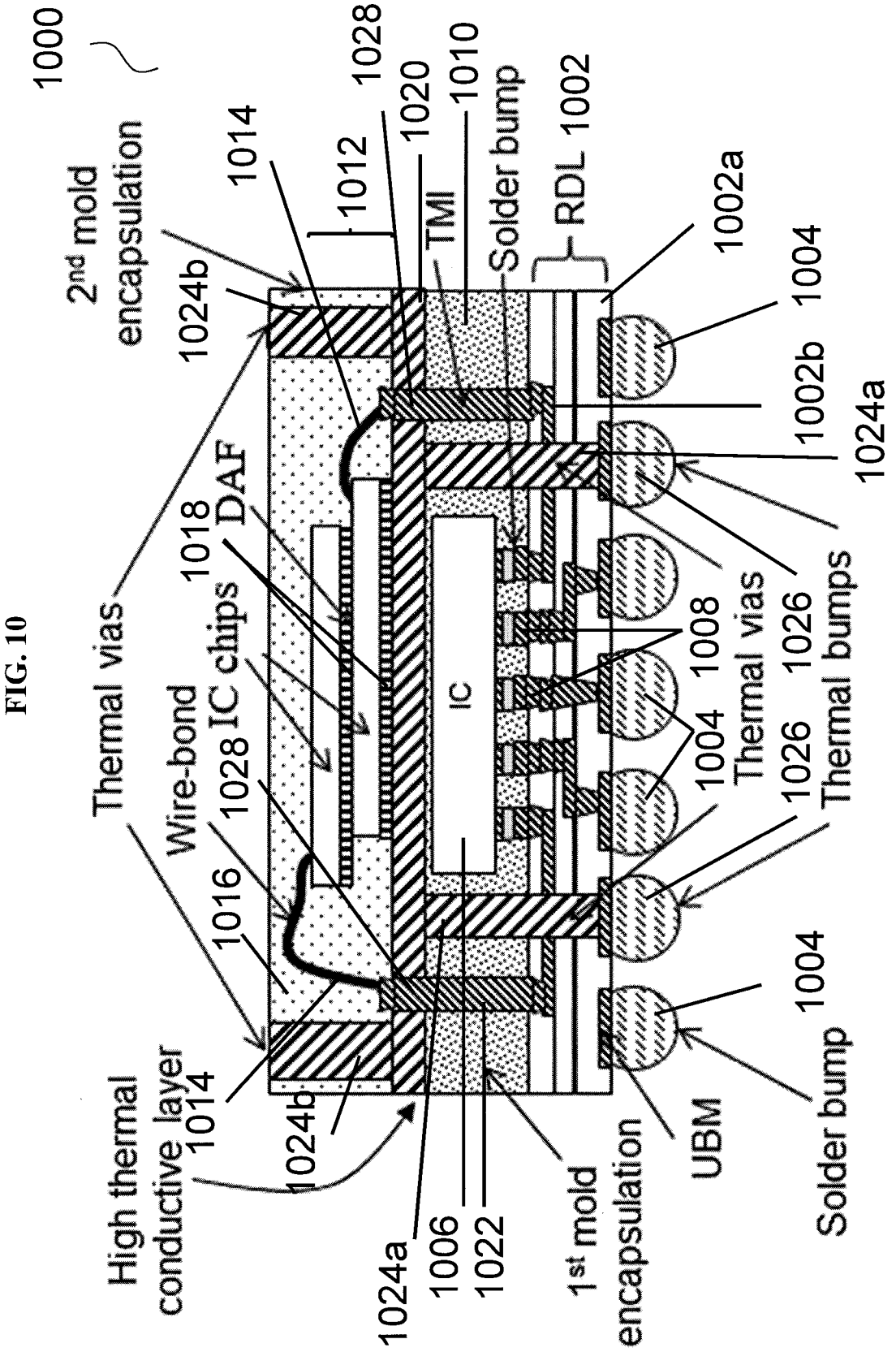

1000
2nd mold encapsulation
1024b
1014
1012
1028
1020
TMI
1010
Solder bump
RDL 1002
1002a
1004
1002b
1024a
Thermal vias
1018
DAF
Wire-bond
1028
IC chips
1016
IC
1008
1004
Thermal vias
1026
1026
Thermal bumps
High thermal conductive layer
1014
1024b
1024a
1006
1022
1st mold encapsulation
UBM
1004
Solder bump

FIG. 10

FIG. 11

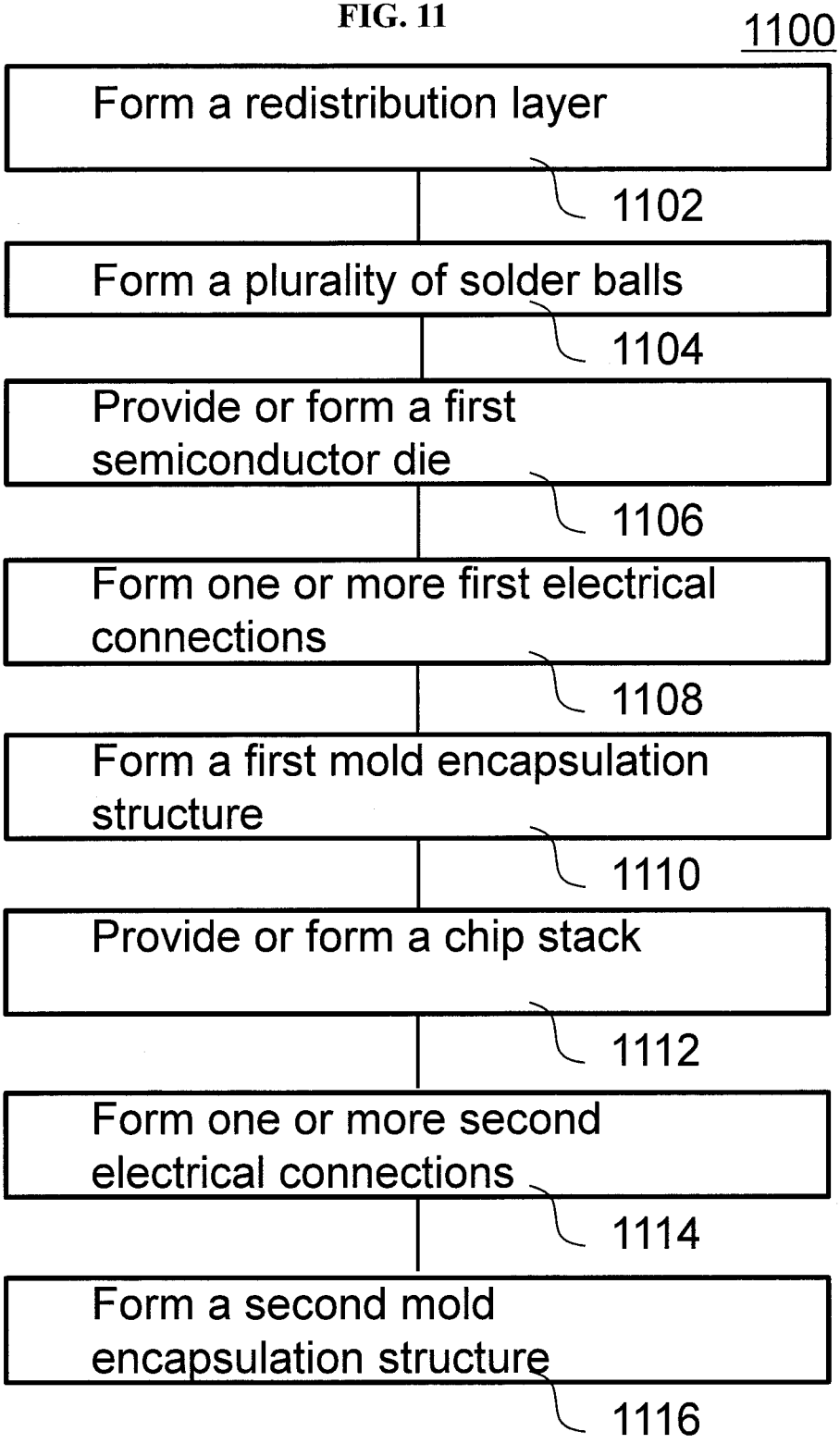

1100
Form a redistribution layer
1102
Form a plurality of solder balls
1104
Provide or form a first semiconductor die
1106
Form one or more first electrical connections
1108
Form a first mold encapsulation structure
1110
Provide or form a chip stack
1112
Form one or more second electrical connections
1114
Form a second mold encapsulation structure
1116

FIG. 12A

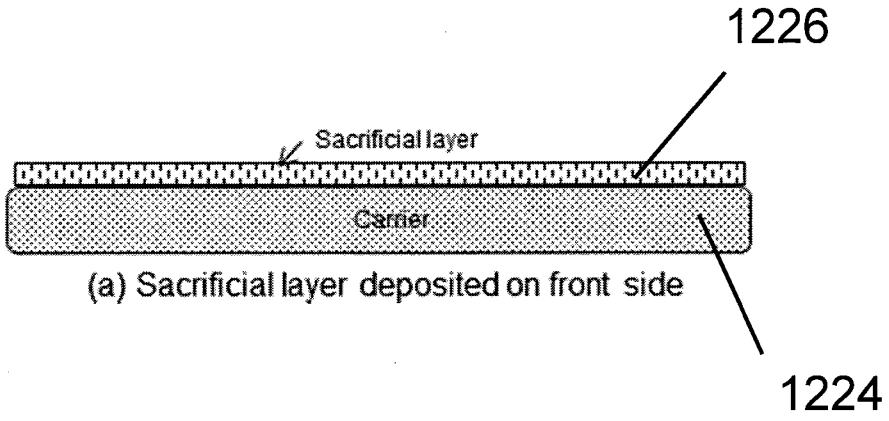


FIG. 12B

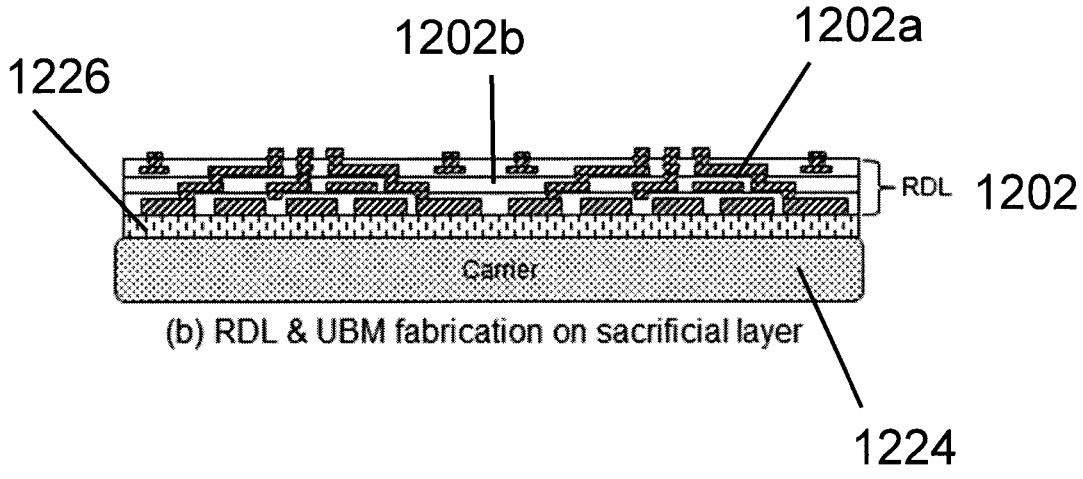


FIG. 12C

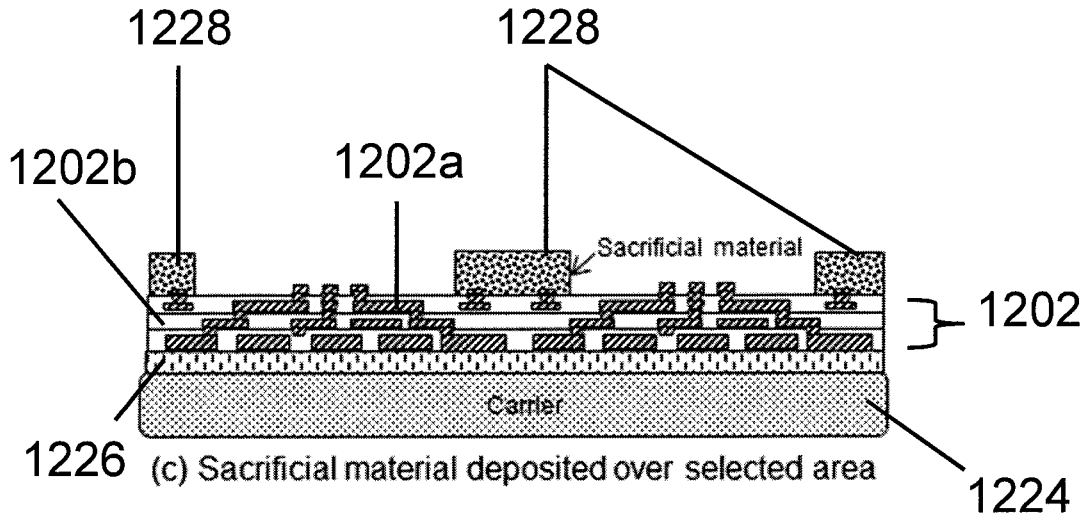


FIG. 12D

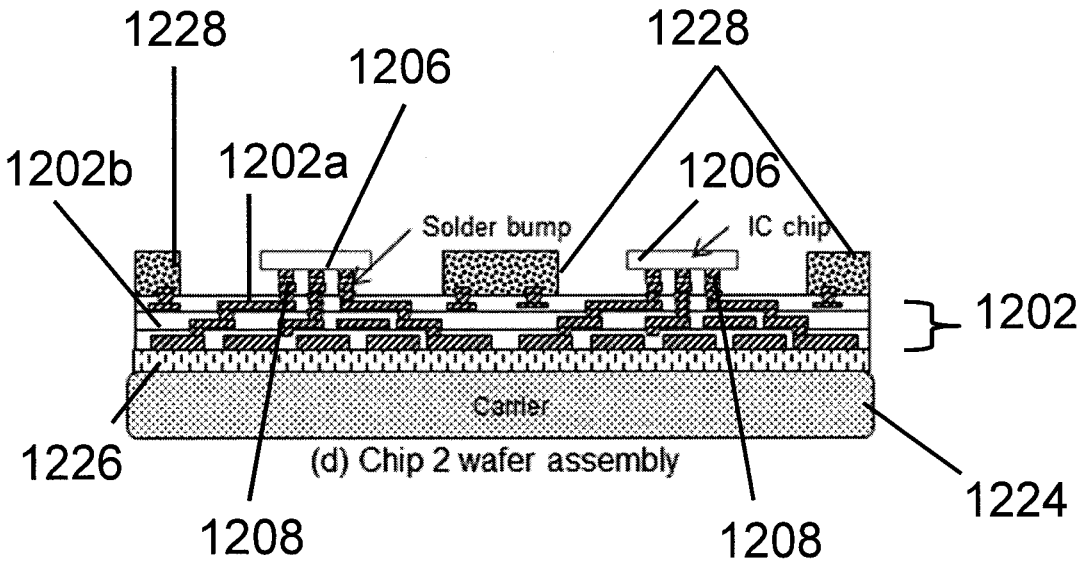


FIG. 12E

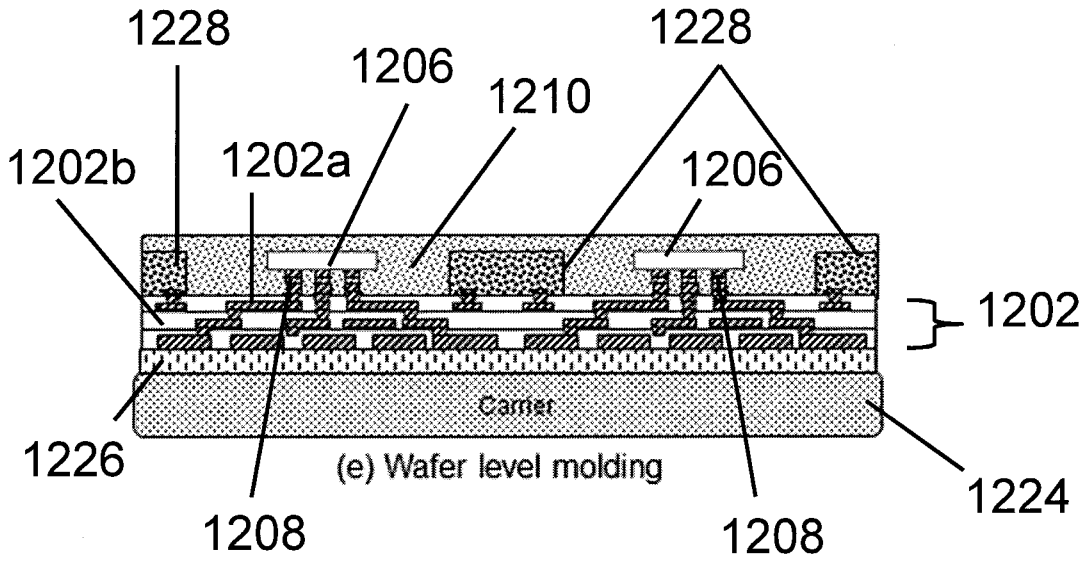


FIG. 12F

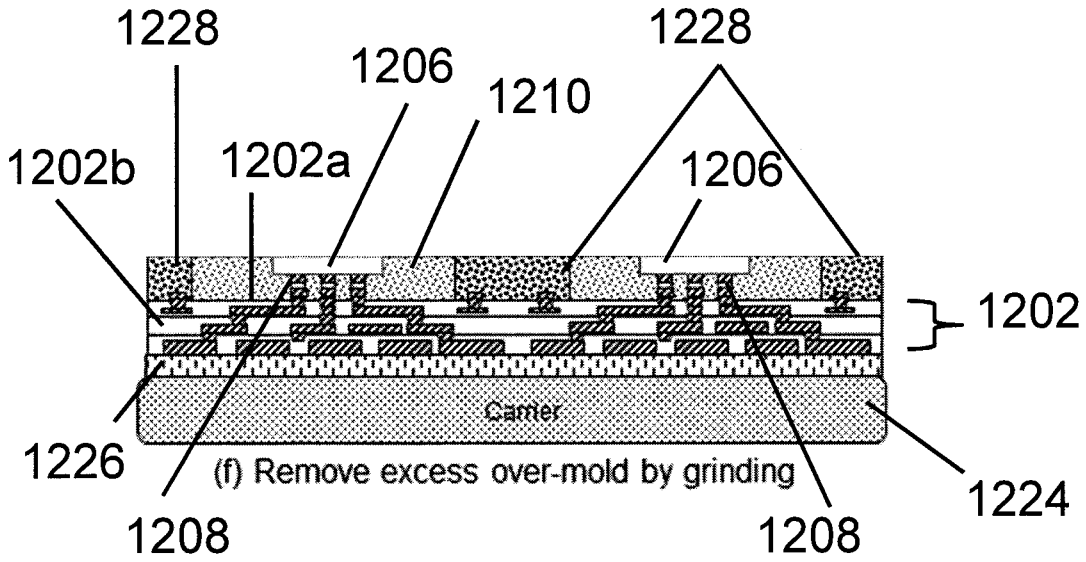


FIG. 12G

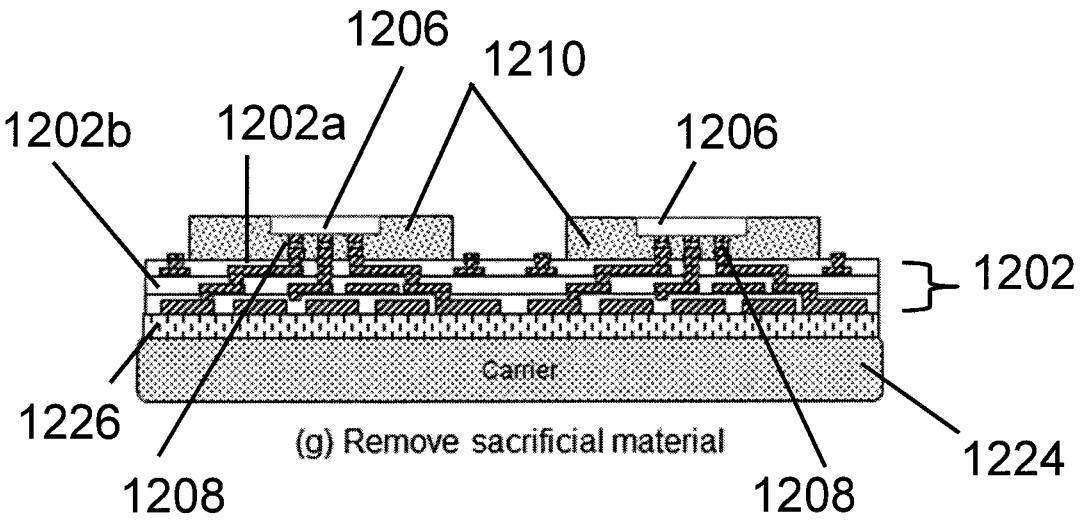


FIG. 12H

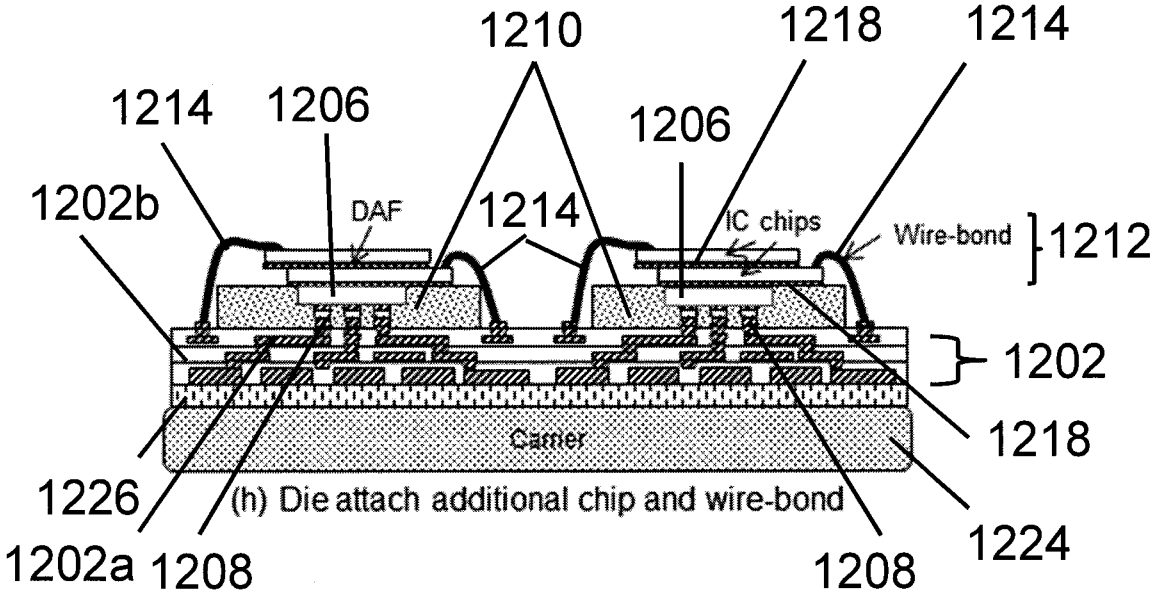


FIG. 12I

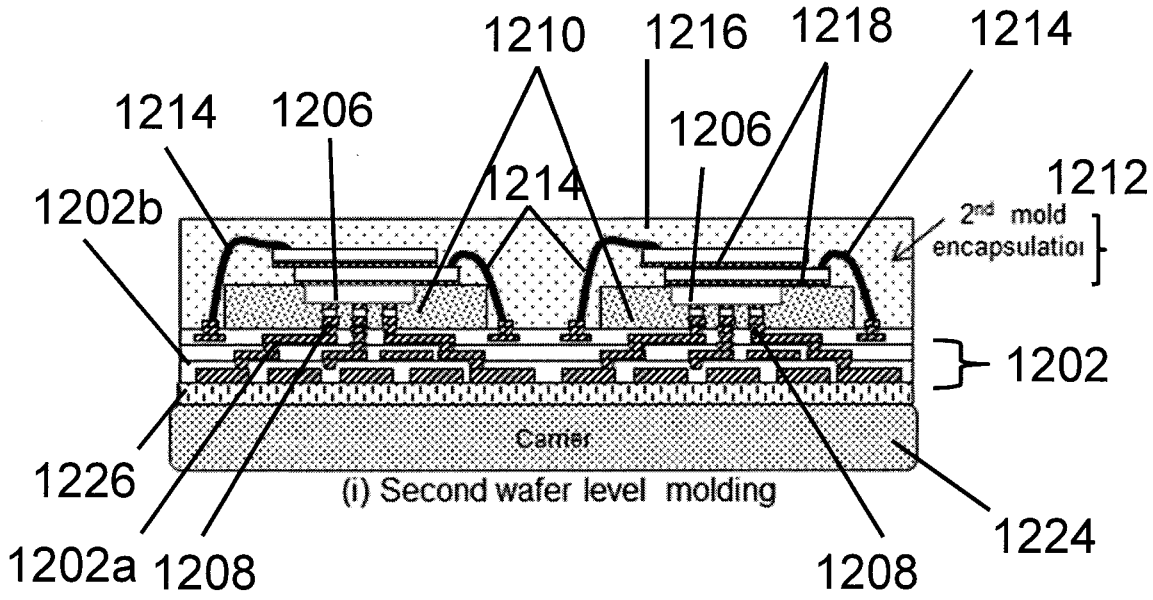


FIG. 12J

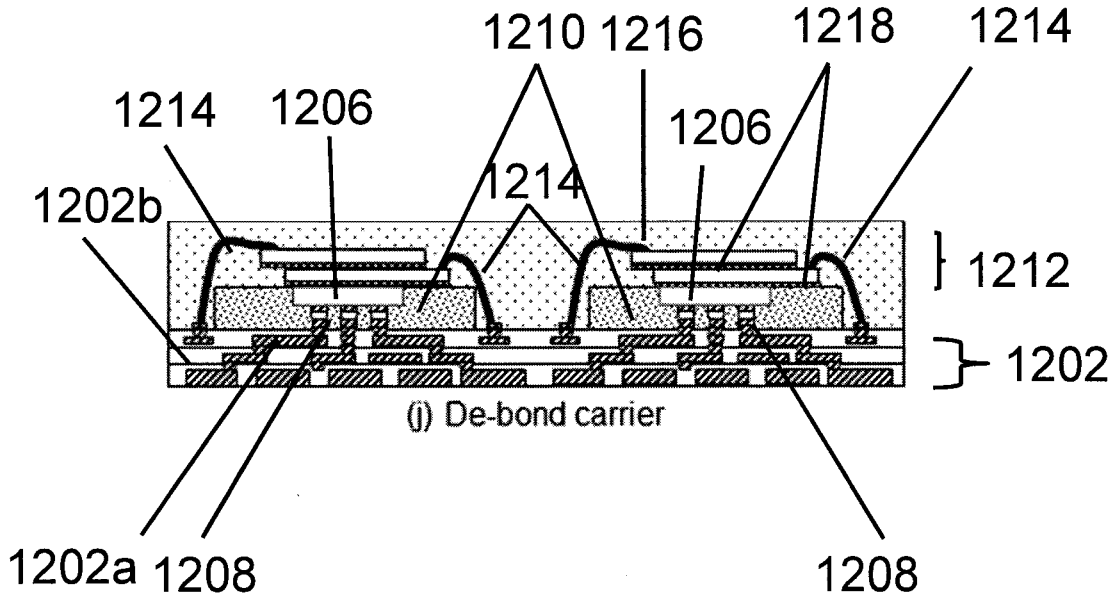


FIG. 12K

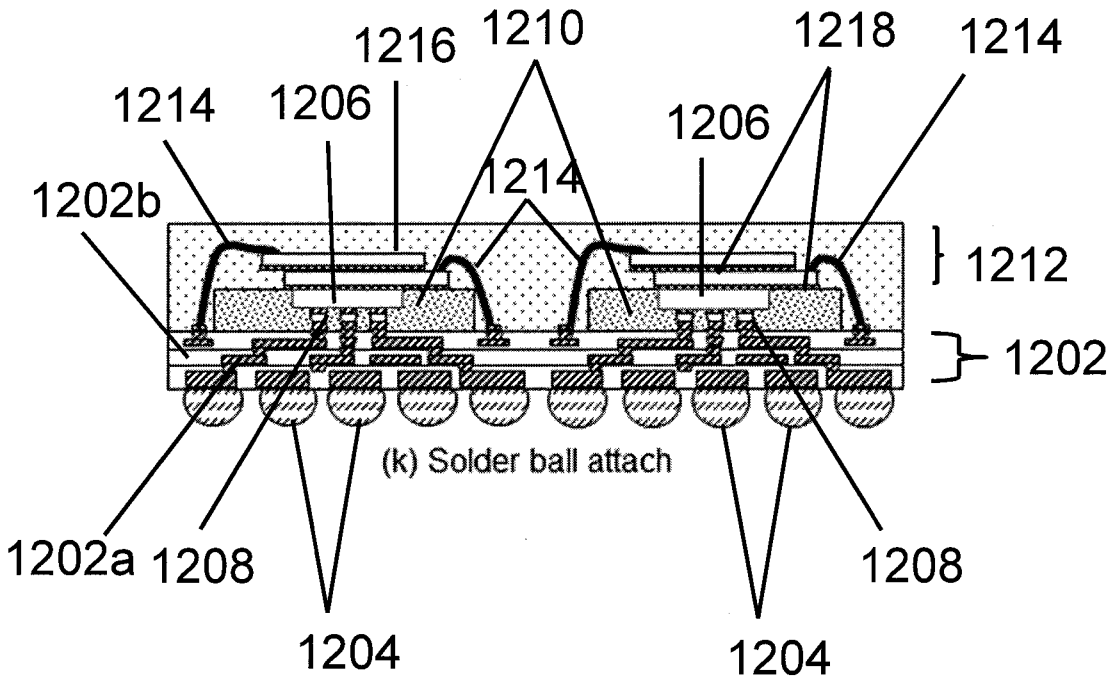


FIG. 12L

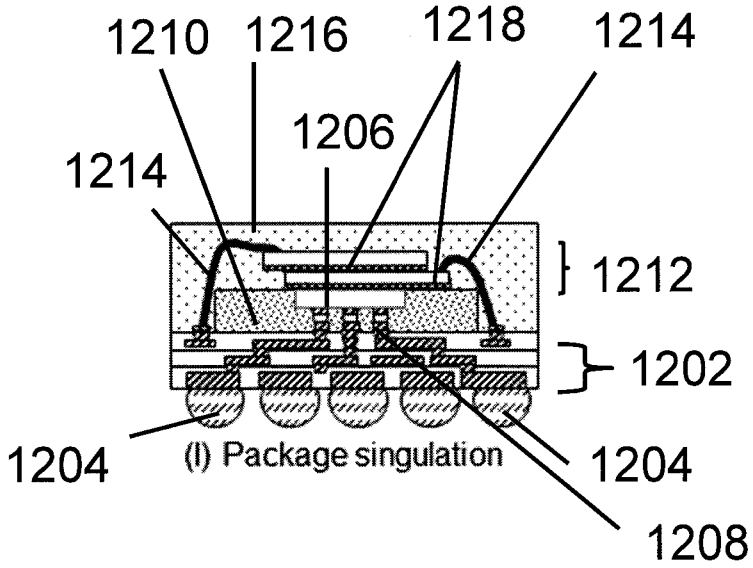


FIG. 13A

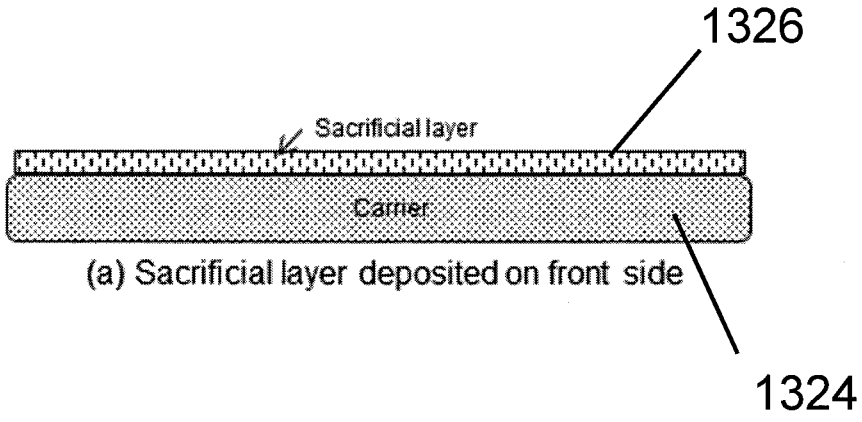


FIG. 13B

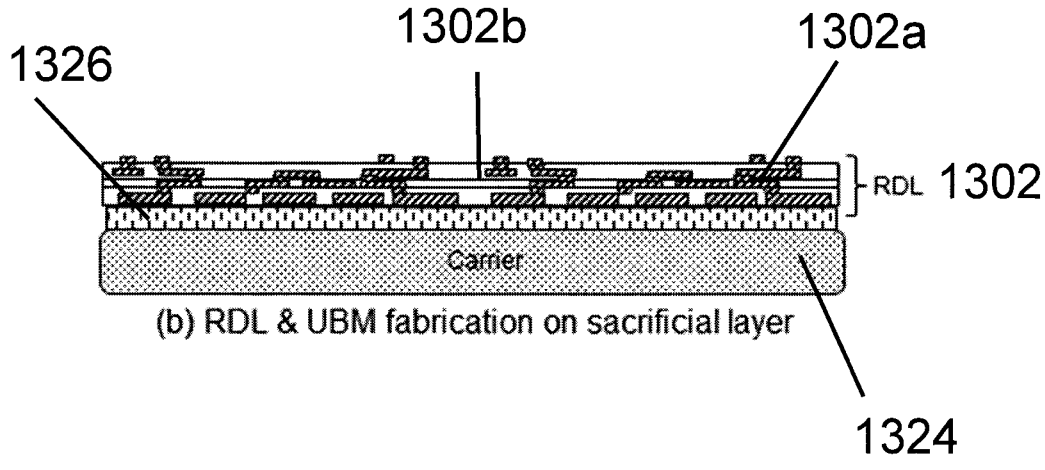
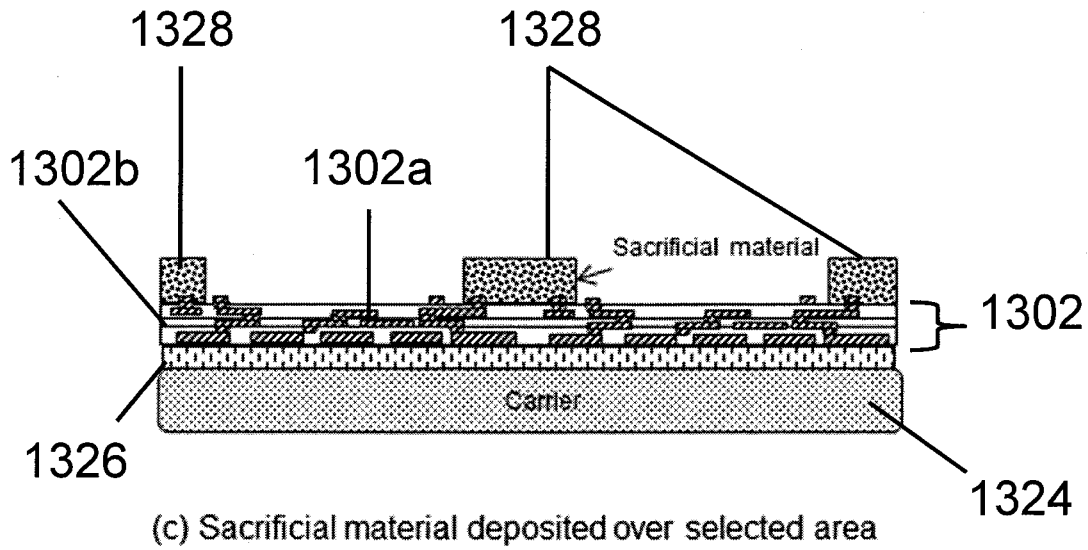
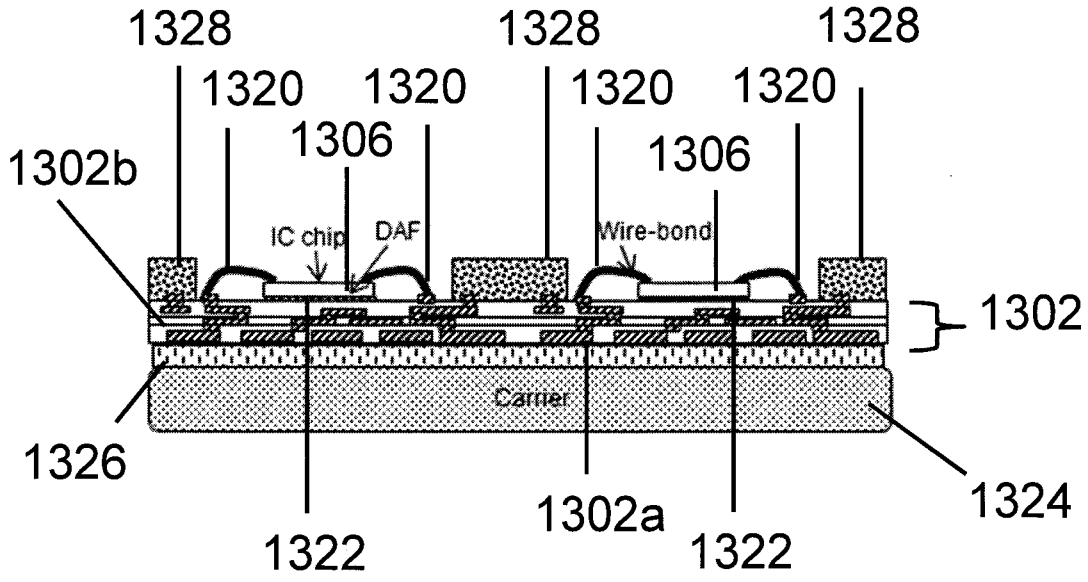


FIG. 13C



(c) Sacrificial material deposited over selected area

FIG. 13D



(d) Die attach first chip and wire-bond

FIG. 13E

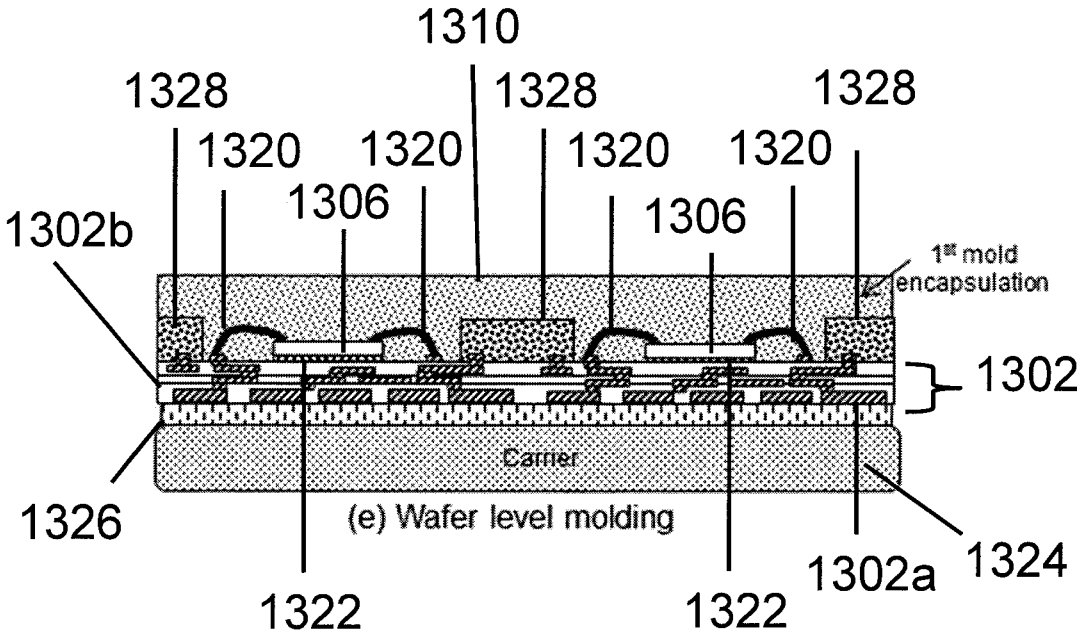


FIG. 13F

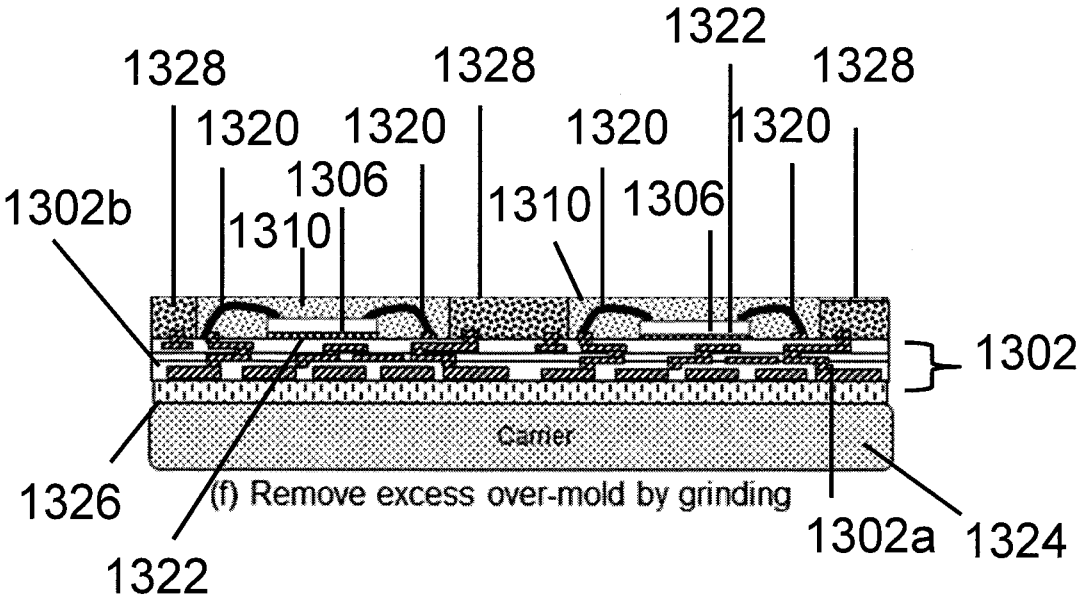


FIG. 13G

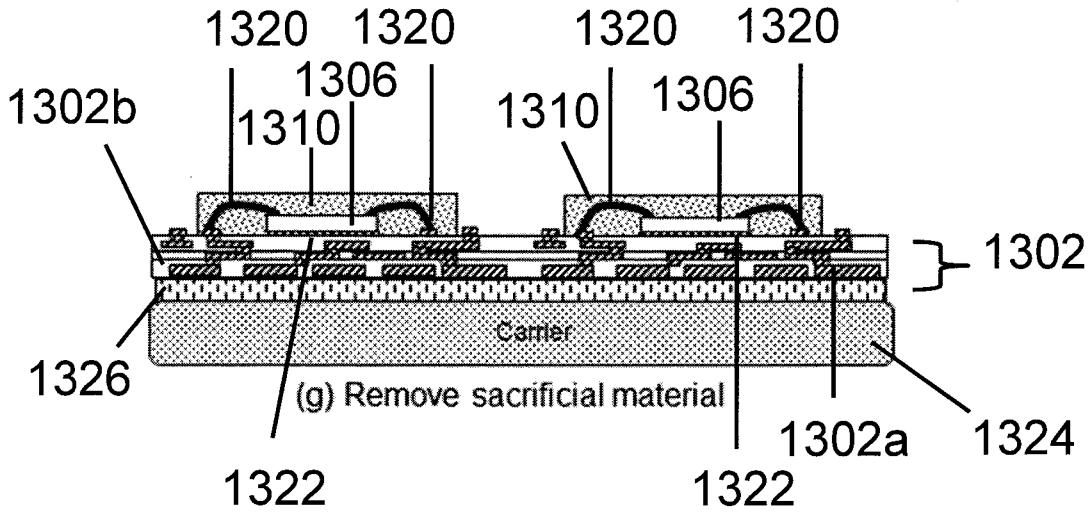
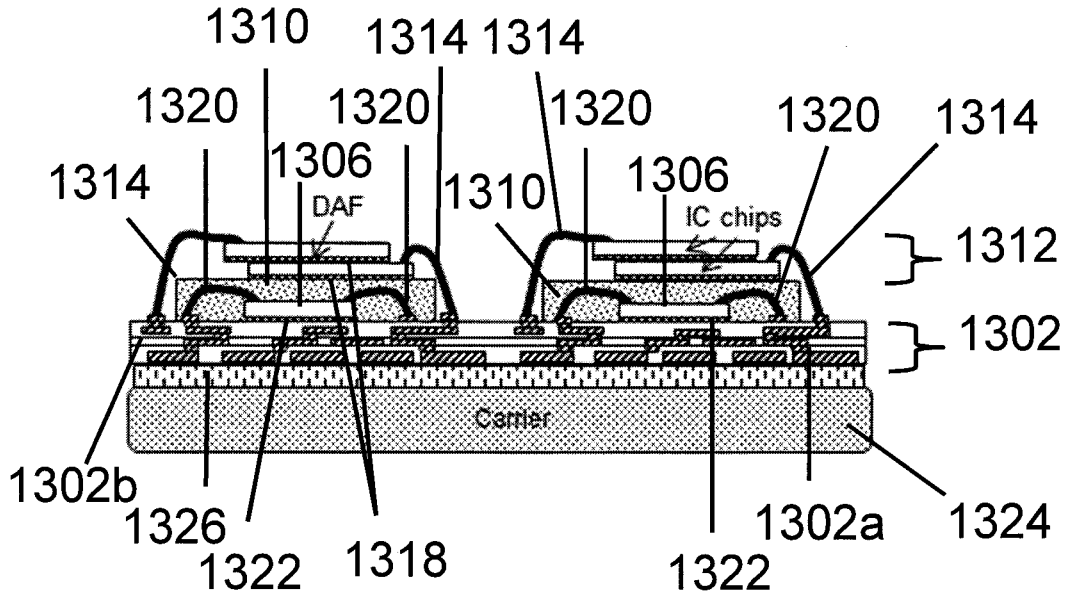
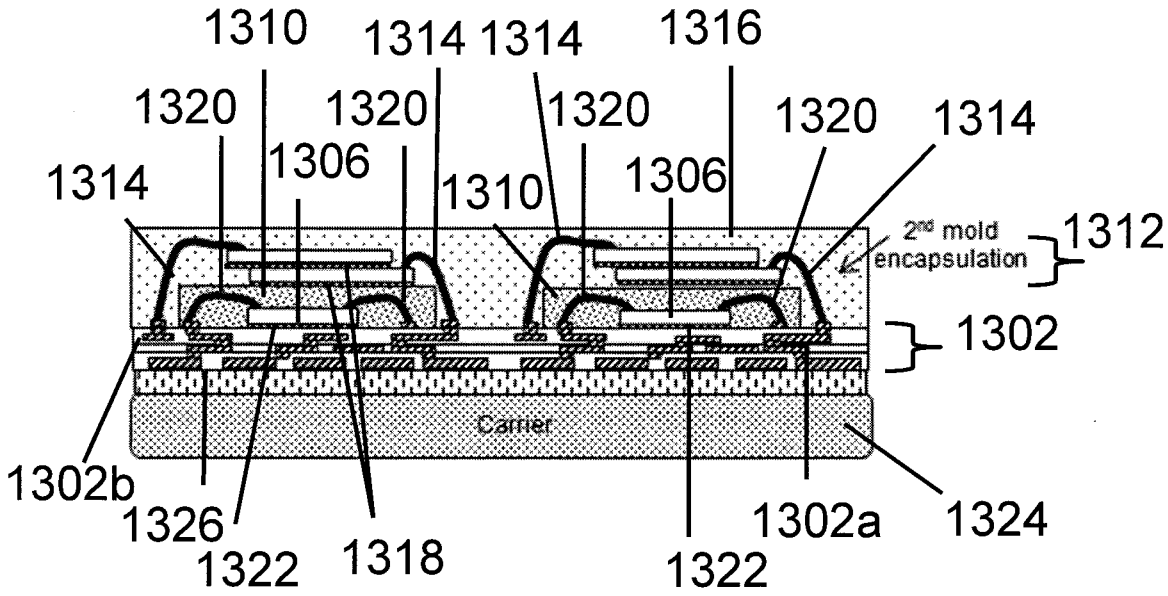


FIG. 13H



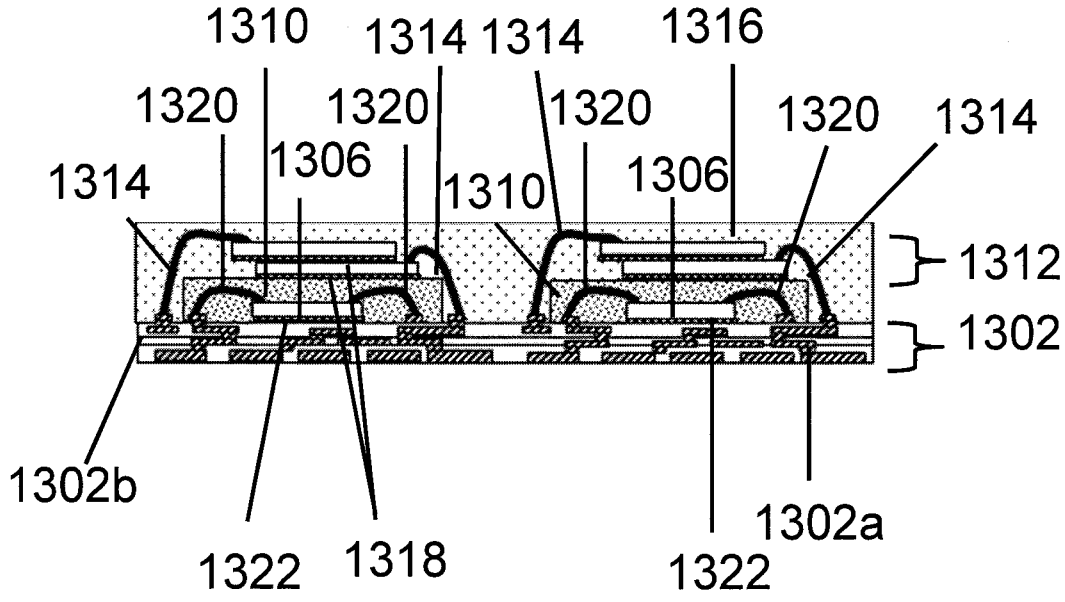
(h) Die attach additional top chips and wire-bond

FIG. 13I



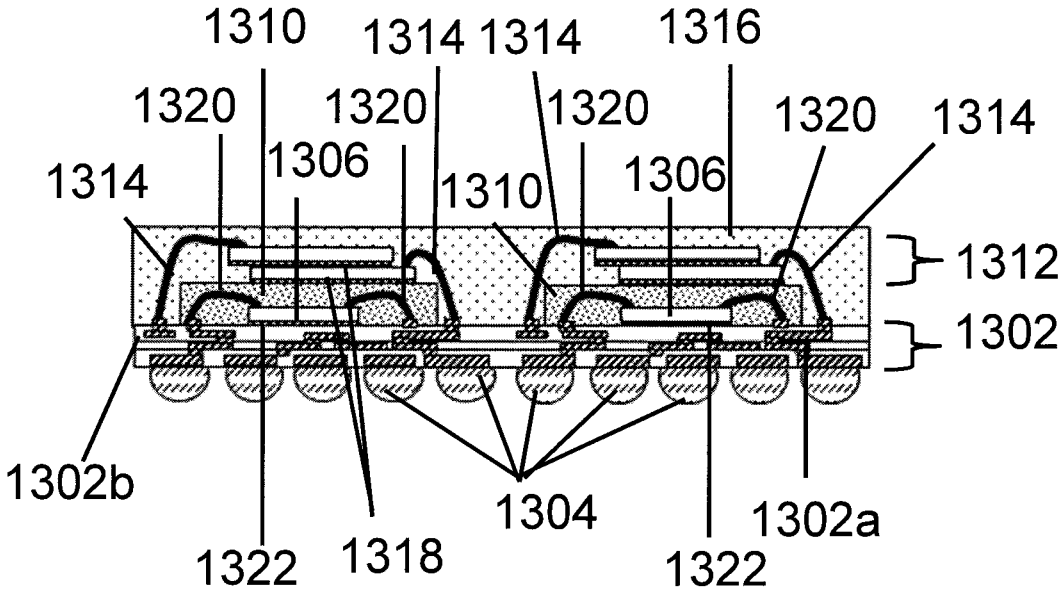
(i) Second wafer level molding

FIG. 13J



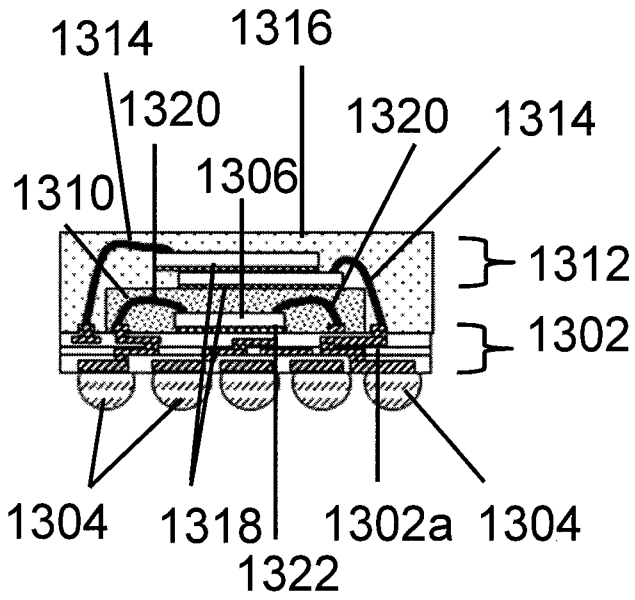
(j) De-bond carrier

FIG. 13K



(k) Solder ball attach

FIG. 13L



(l) Package singulation

FIG. 14A

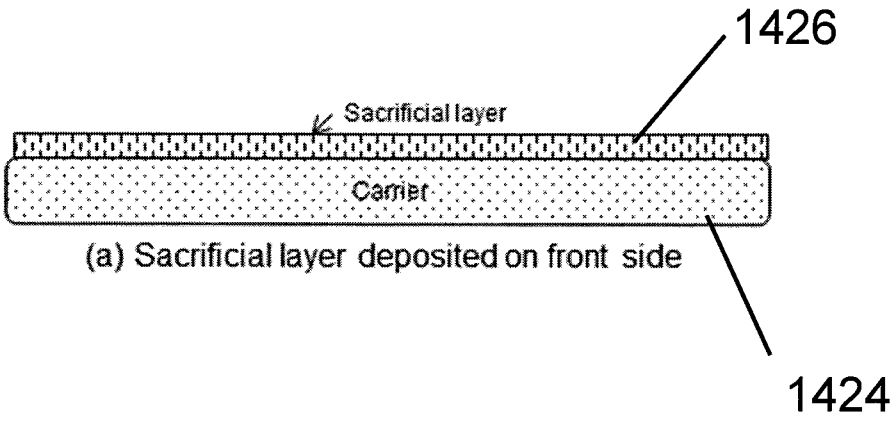


FIG. 14B

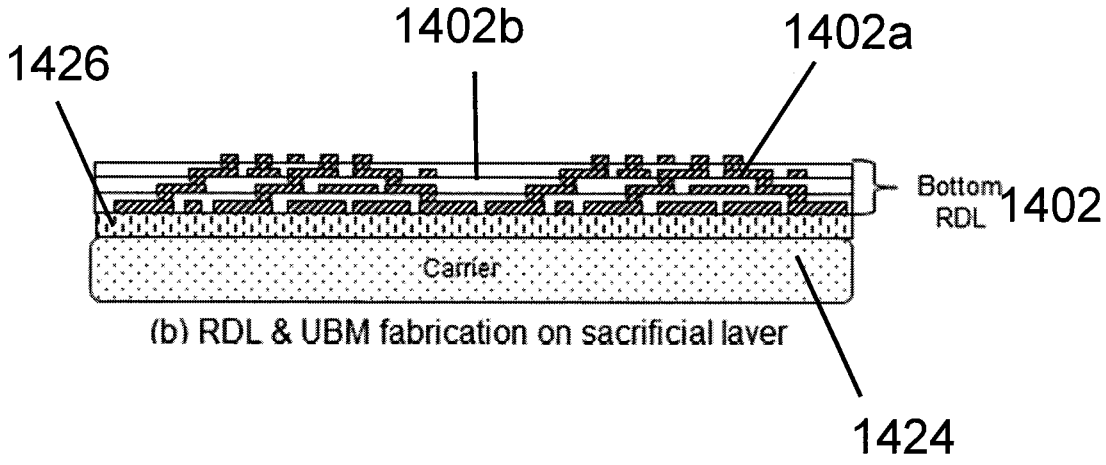
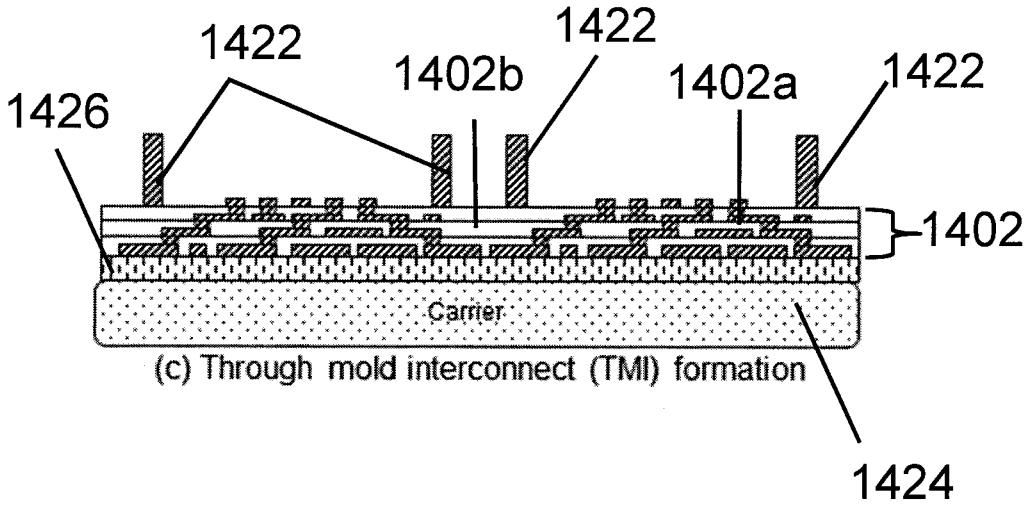
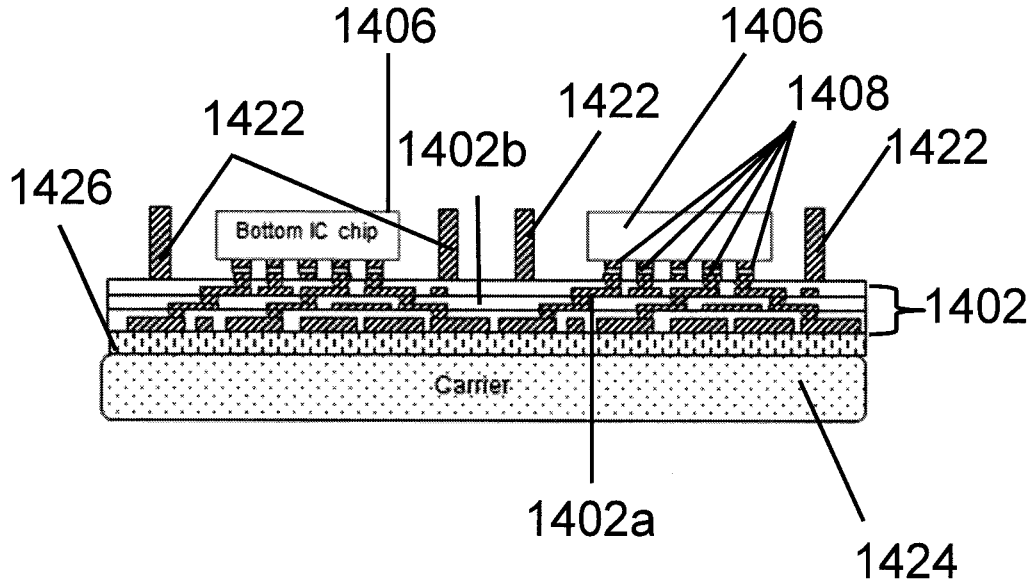


FIG. 14C



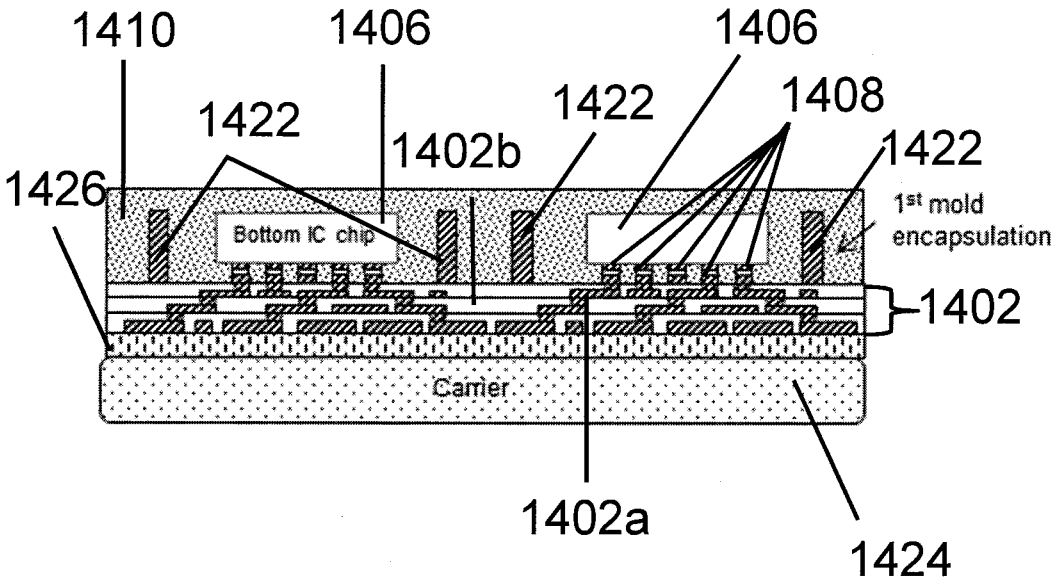
(c) Through mold interconnect (TMI) formation

FIG. 14D



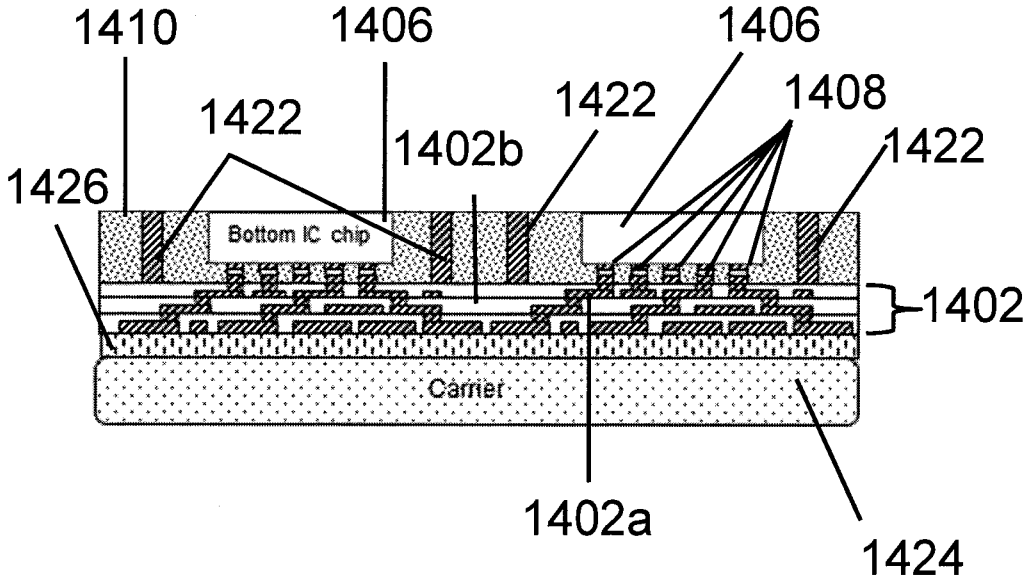
(d) Chip 2 wafer assembly

FIG. 14E



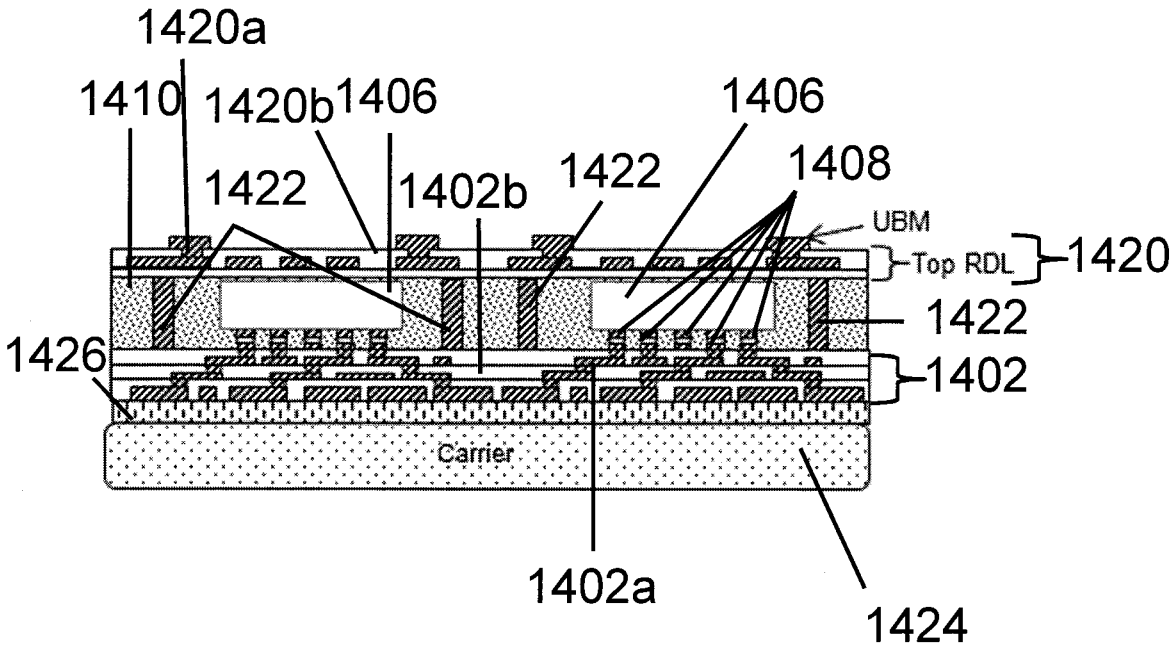
(e) Wafer level compression molding

FIG. 14F



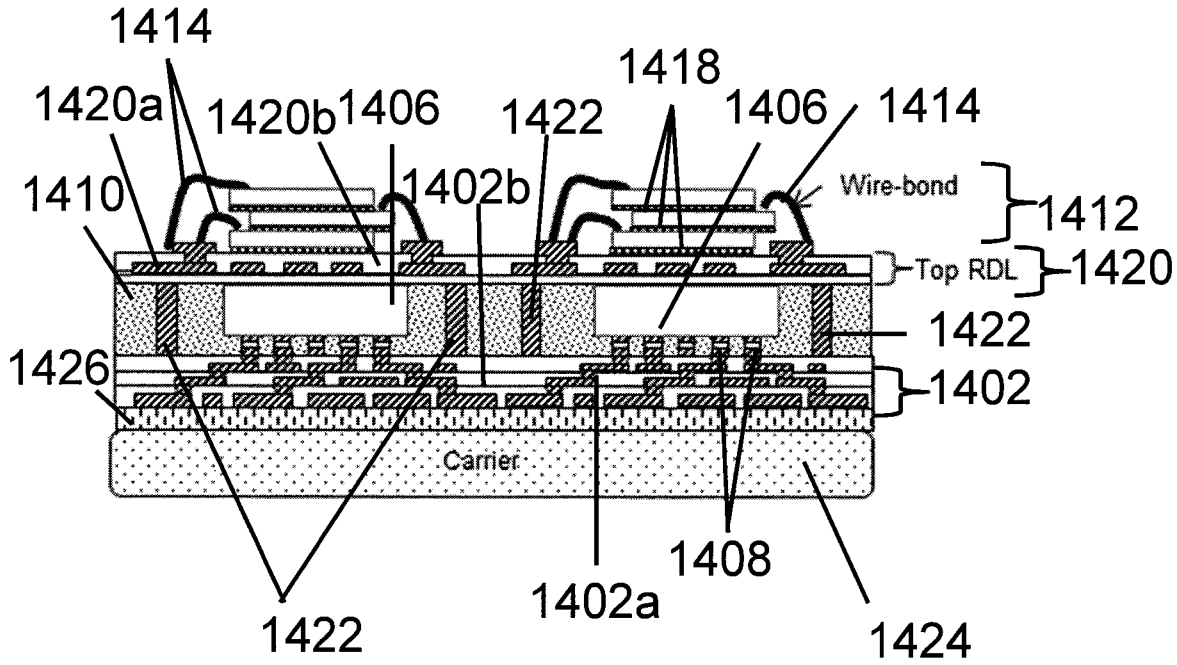
(f) Backgrind to expose TMI

FIG. 14G



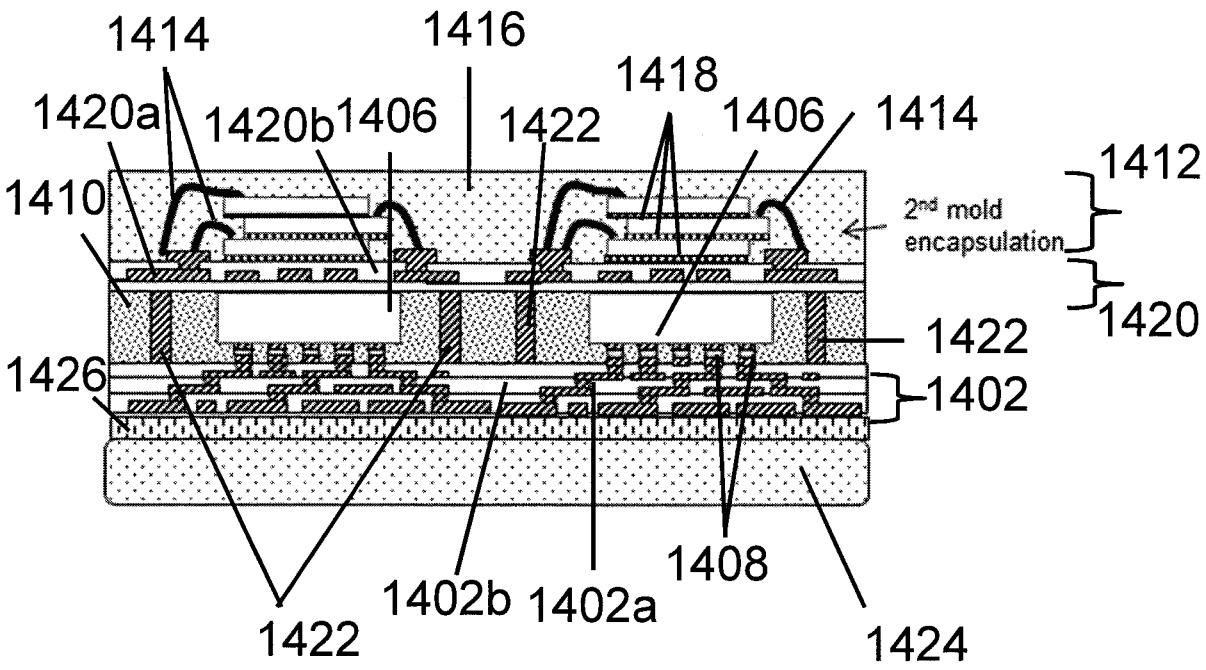
(g) Top RDL & UBM layer

FIG. 14H



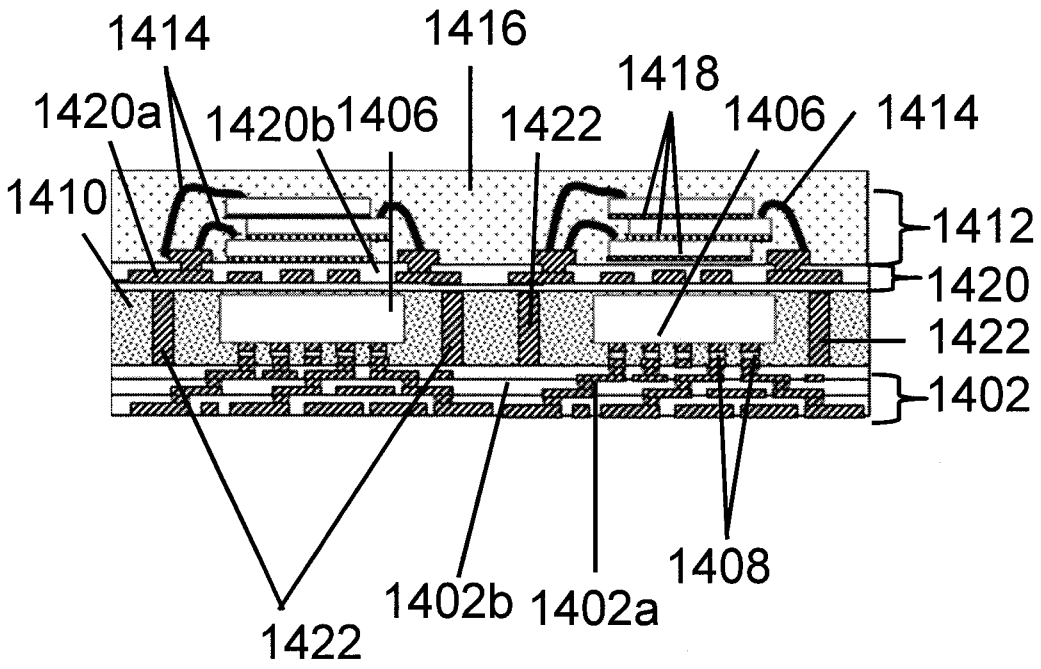
(h) Top chips stacking with DAF & wire-bonding

FIG. 14I



(i) 2nd wafer level molding of top chips

FIG. 14J



(j) De-bond carrier

FIG. 14K

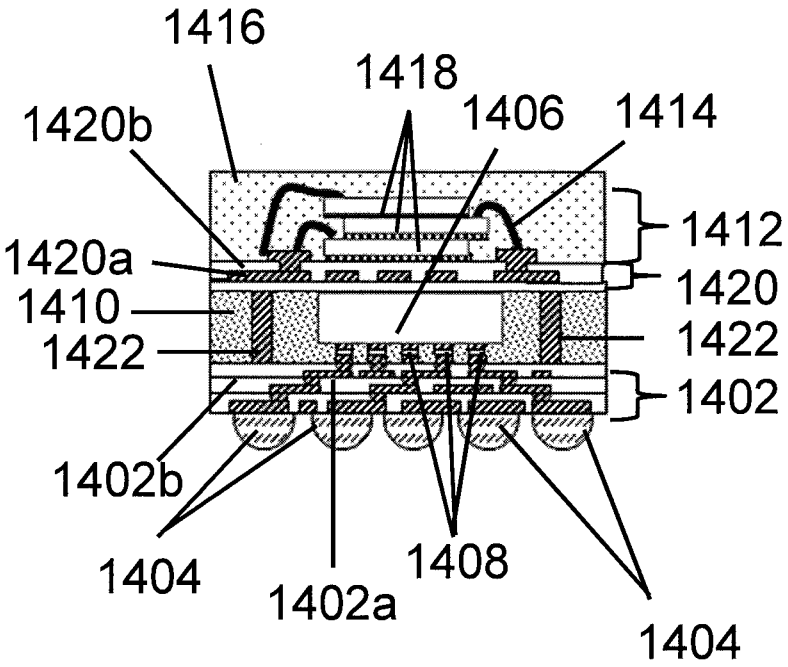

1416
1418
1406
1414
1420b
1412
1420a
1420
1410
1422
1422
1402
1402b
1404
1408
1402a
1404

FIG. 15A

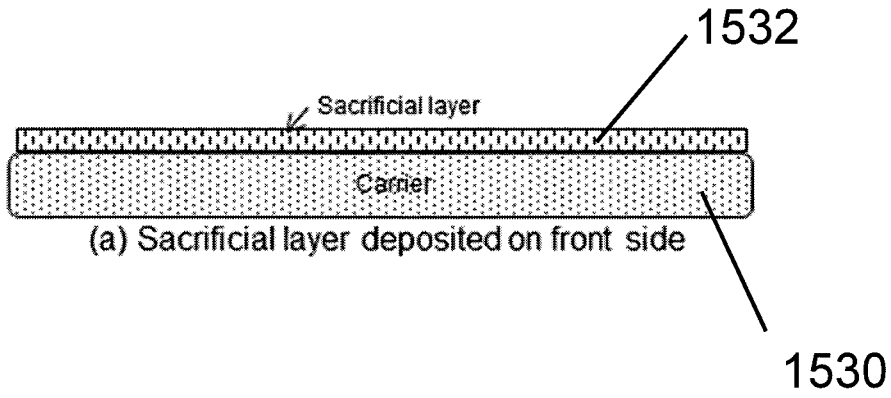


FIG. 15B

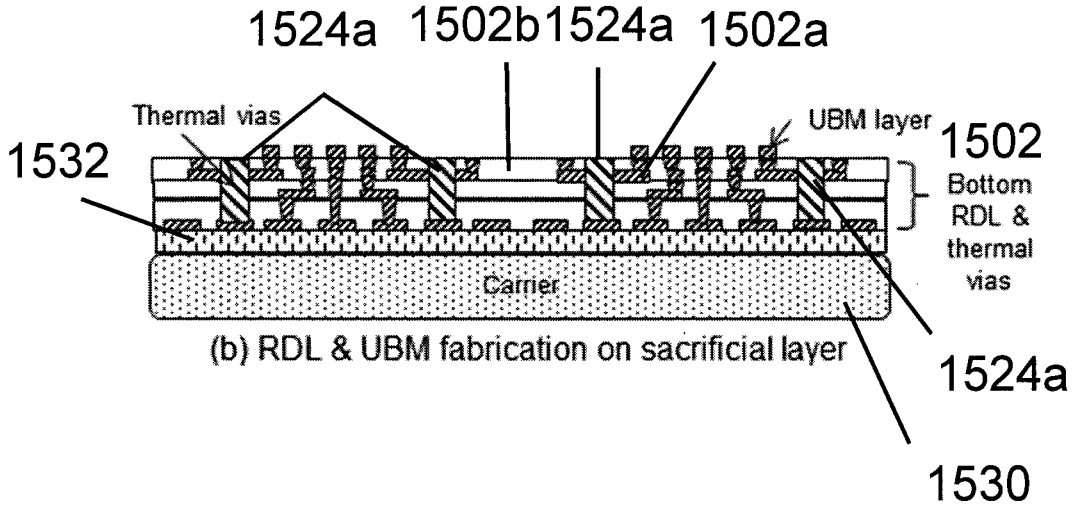
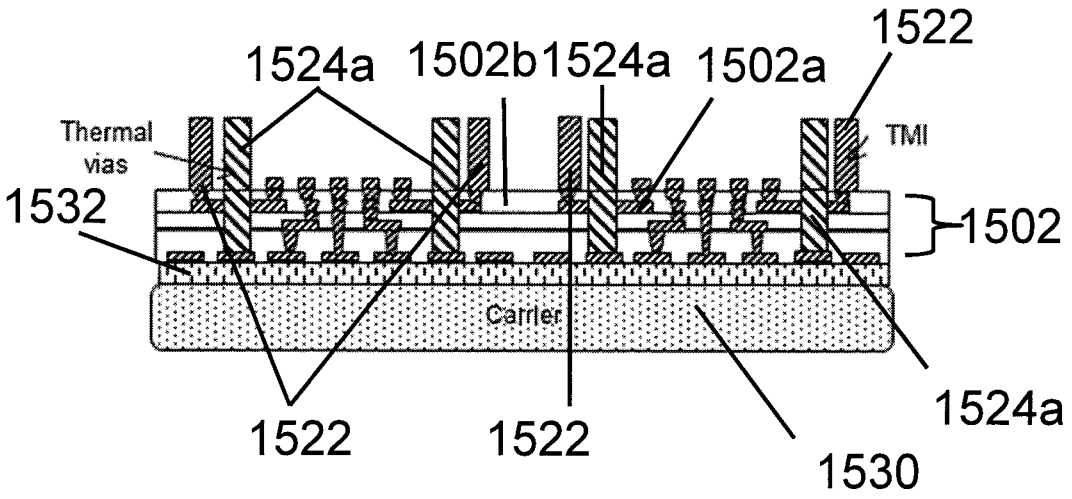
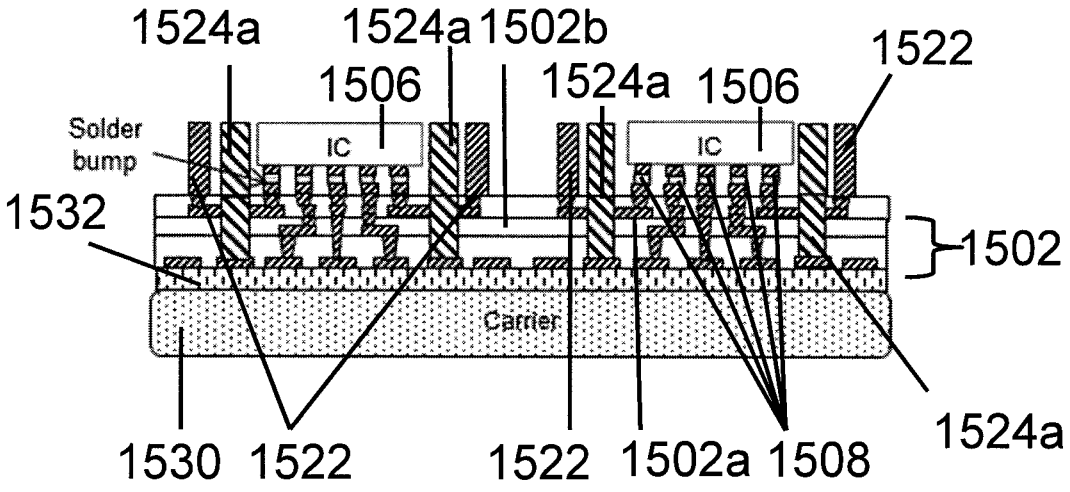


FIG. 15C



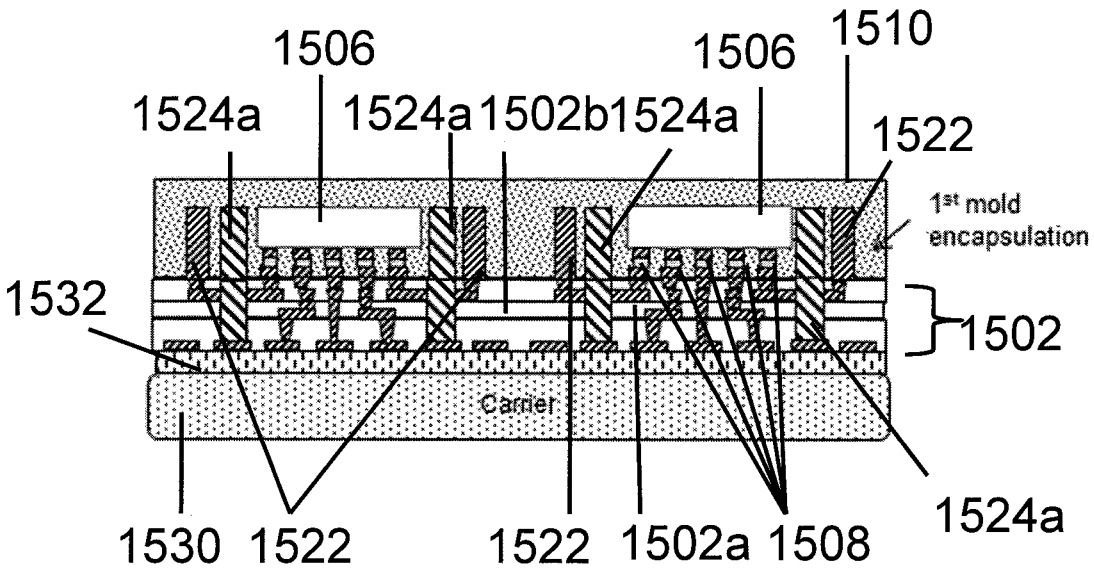
(c) Through mold interconnect (TMI) & thermal vias formation

FIG. 15D



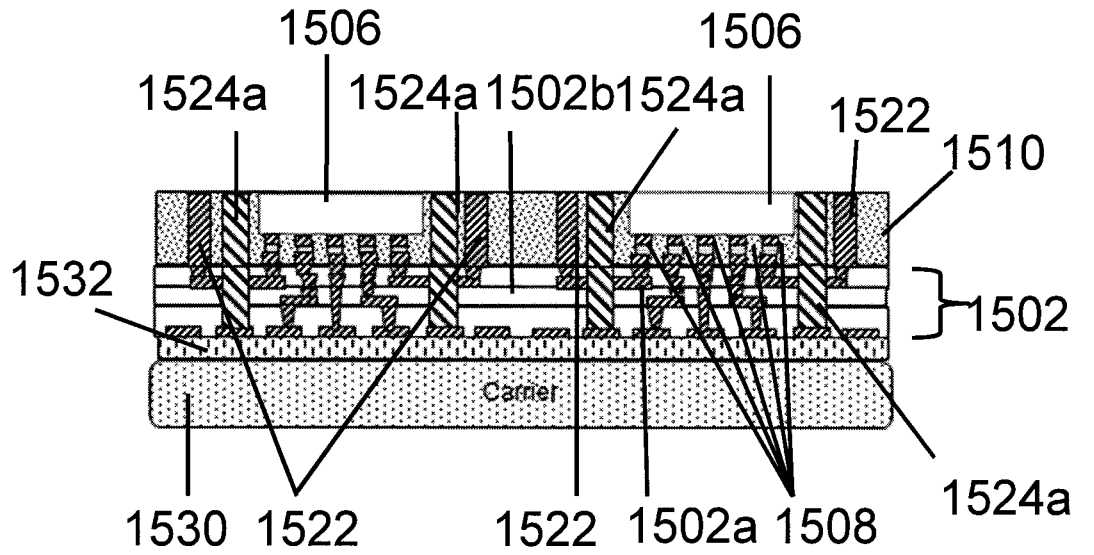
(d) IC chips reflowed assembled to wafer

FIG. 15E



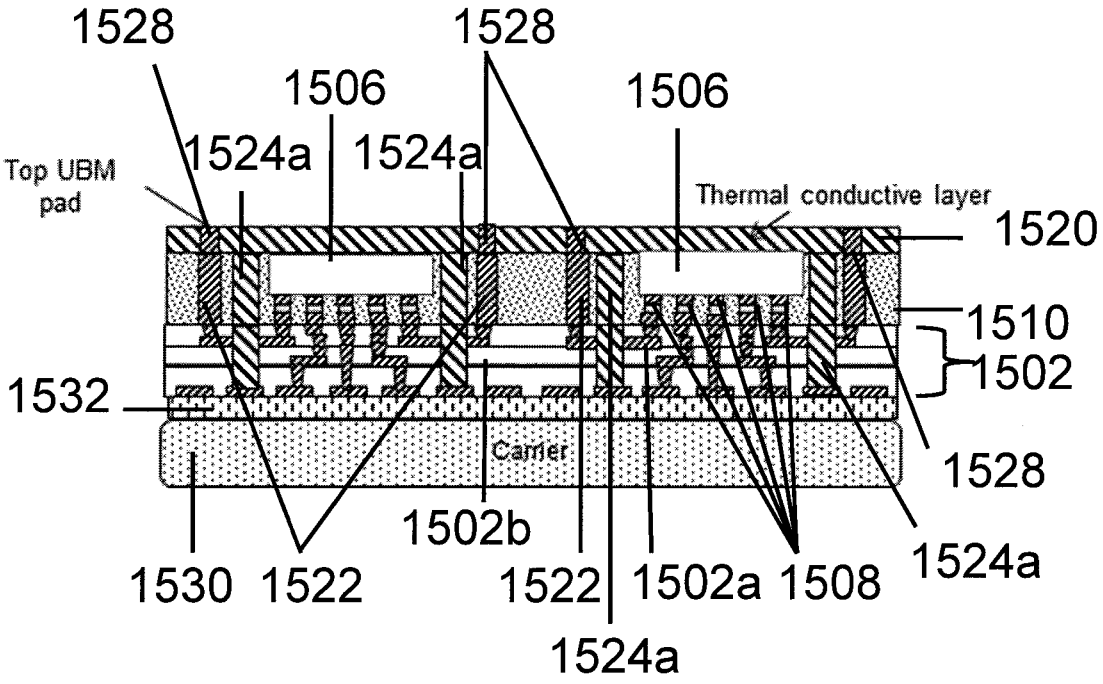
(e) Wafer level molding

FIG. 15F



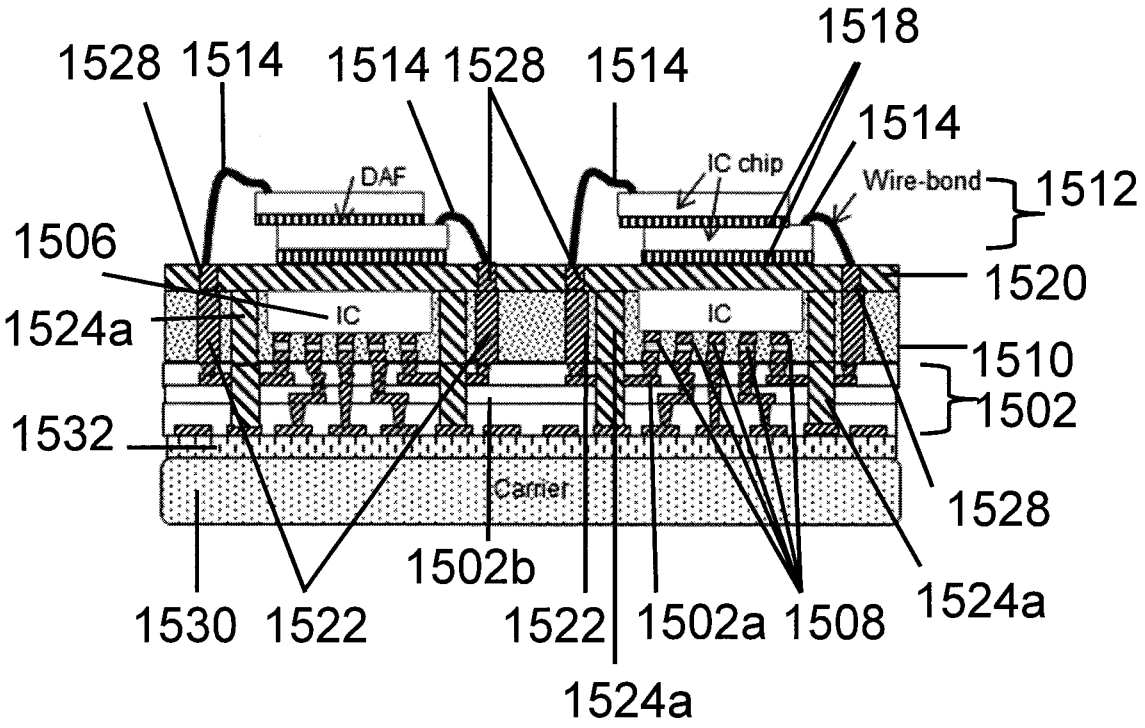
(f) Backgrind to expose TMI & thermal via

FIG. 15G



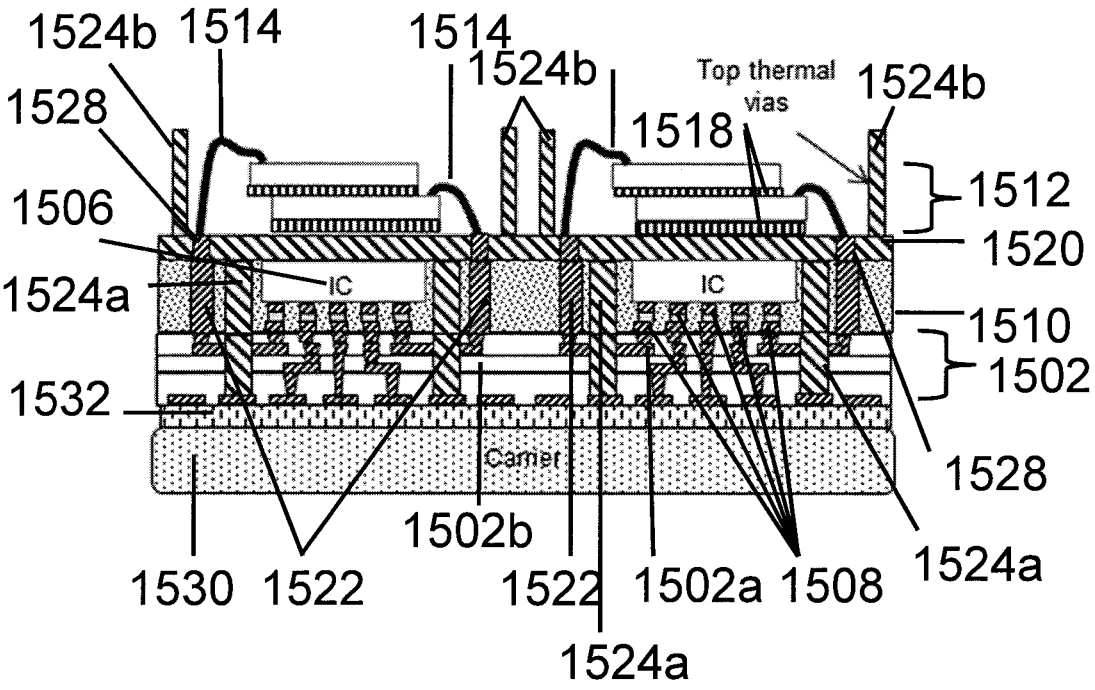
(g) Thermal conductive layer and Top UBM pad

FIG. 15H



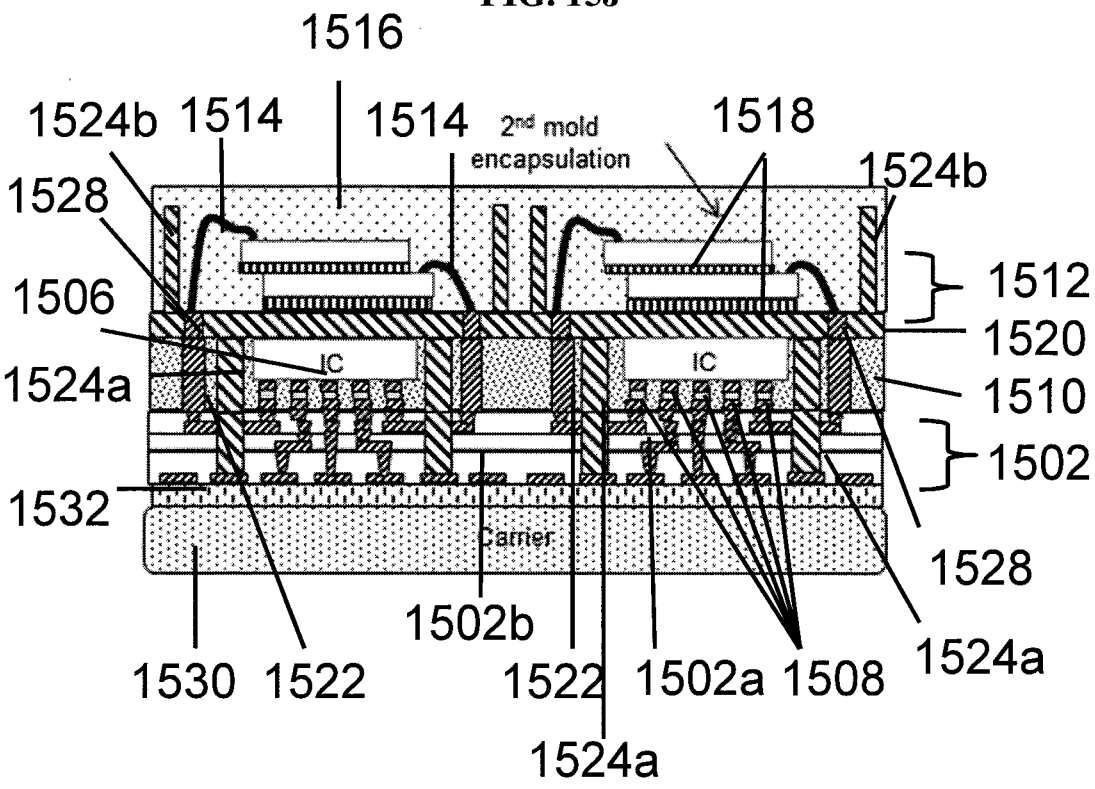
(h) Chip stacking & wire-bond

FIG. 15I



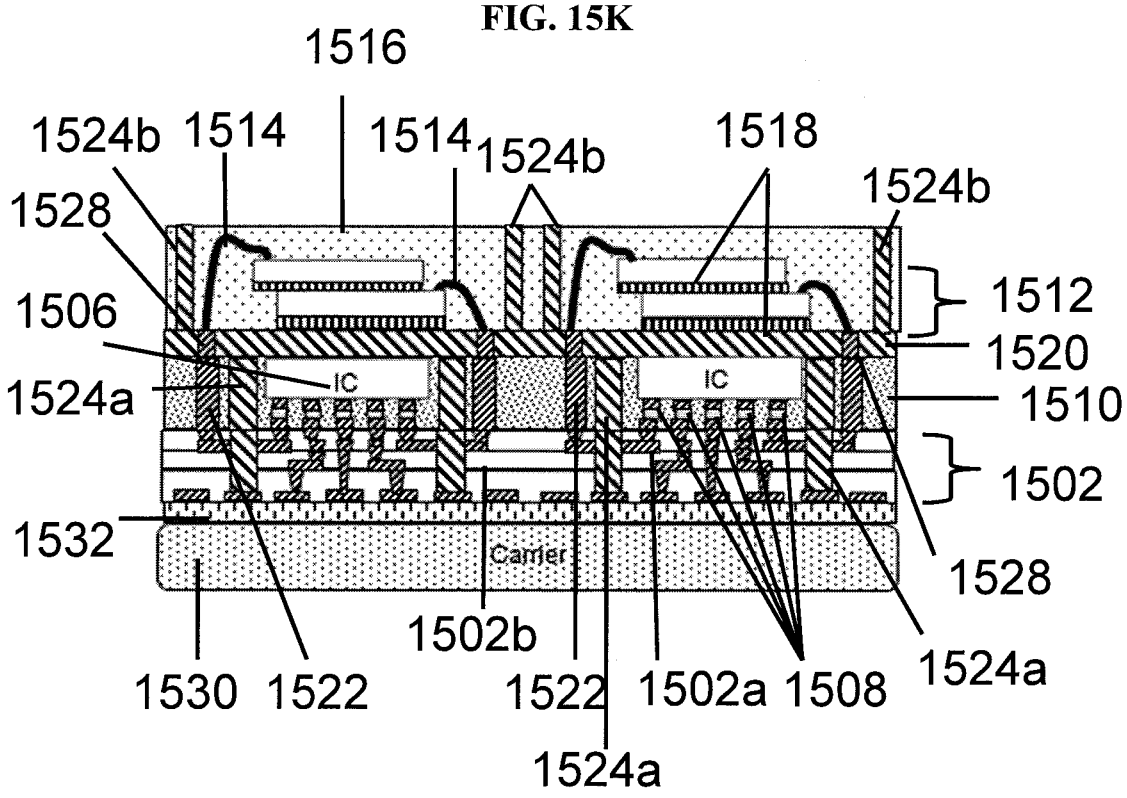
(i) Top thermal vias formation

FIG. 15J



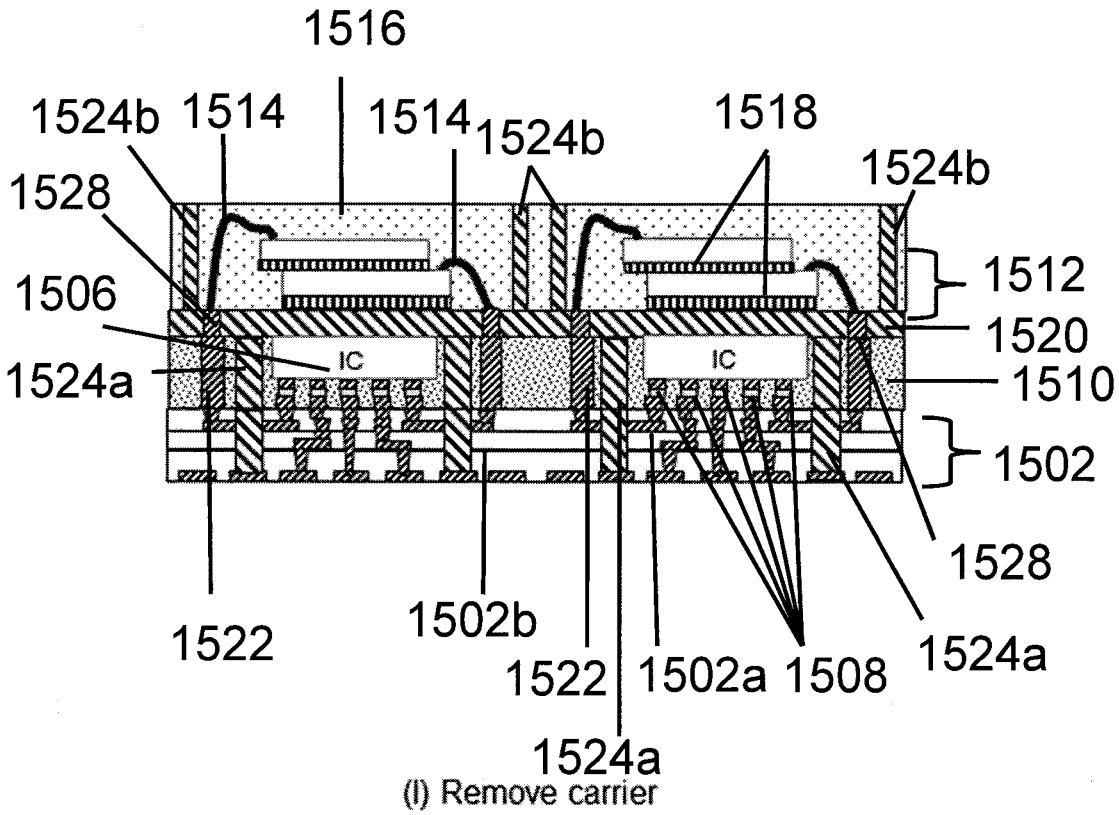
(j) 2nd wafer level molding of top chips

FIG. 15K



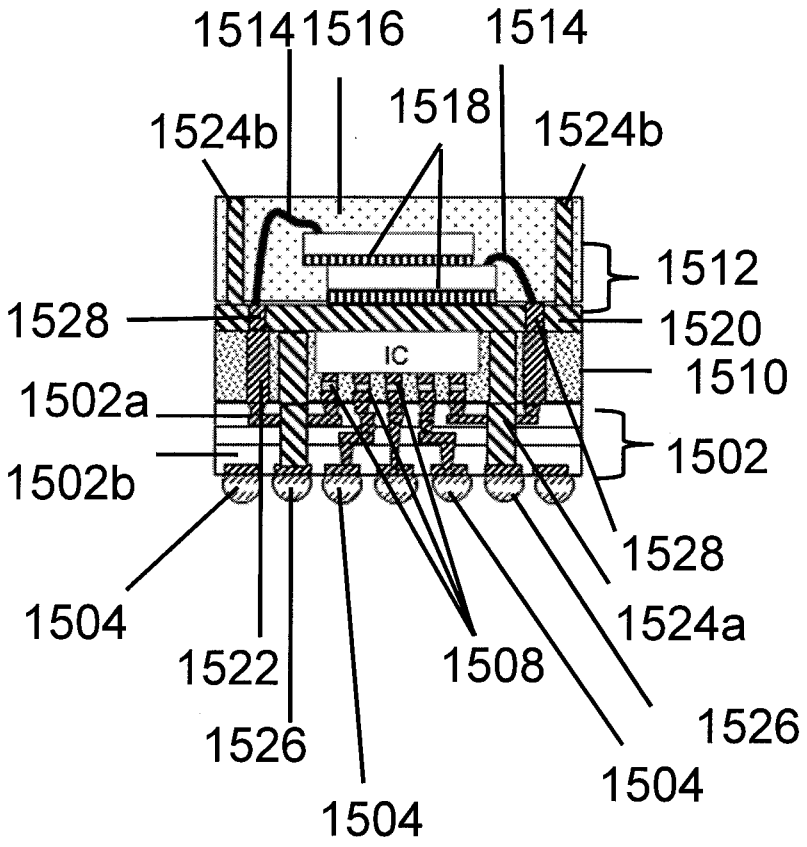
(k) Backgrind to expose thermal vias

FIG. 15L



(l) Remove carrier

FIG. 15M



(m) Solder ball attach and singulated to package

INTERNATIONAL SEARCH REPORT

International application No.

PCT/SG2017/050118

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/31 (2006.01) ***H01L 21/56 (2006.01)*** *H01L 23/488 (2006.01)*

According to International Patent Classification (IPC)

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

FAMPAT: redistribution layer, RDL, wire bonding, double encapsulation, mold, fan out, wafer level packaging and related terms

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2015/0206865 A1 (YU C.-H. ET AL.) 23 July 2015 Para. [0025]-[0041]; Fig. 11-25	1-3, 6-13, 17-20
X	US 2008/0073771 A1 (SEO H.-S. ET AL.) 27 March 2008 Para. [0032]-[0034]; Fig. 4	1-4, 6-11, 17-20
X	US 2006/0267175 A1 (LEE Y. G.) 30 November 2006 Para. [0035]; Fig. 3	1, 3-4, 6-11, 17-20
X	US 2013/0062761 A1 (LIN C.-W. ET AL.) 14 March 2013 Para. [0030]-[0046]; Fig. 1, 10-20	1-20
A	US 2013/0075926 A1 (BAE J. H. ET AL.) 28 March 2013 Whole document	

☒ Further documents are listed in the continuation of Box C. **S** See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
22/05/2017 *(day/month/year)*	30/05/2017 *(day/month/year)*

Name and mailing address of the ISA/SG	Authorized officer
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2017/050118

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2004/0227240 A1 (BOLKEN T. O. ET AL.) 18 November 2004 Whole document	
A	US 2008/0211079 A1 (ONODERA M.) 4 September 2008 Whole document	

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/SG201 7/0501 18

Note: This Annex lists known patent family members relating to the patent documents cited in this International Search Report. This Authority is in no way liable for these particulars which are merely given for the purpose of information.

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