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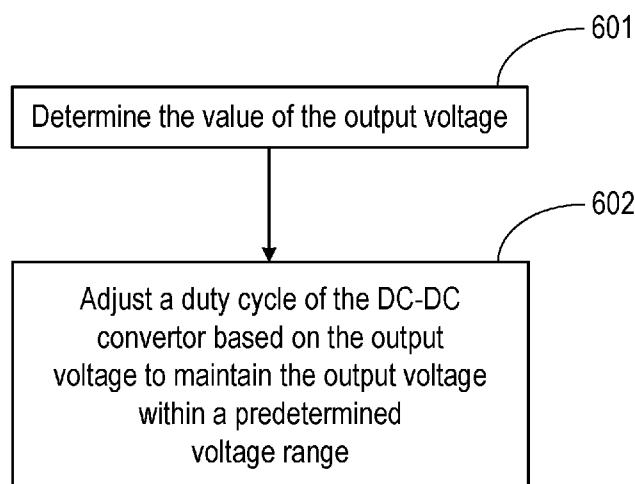


FIG. 6

(57) Abstract: A DC-DC converter and a corresponding method for maintaining an output voltage of the DC-DC converter, wherein the DC-DC converter is configured to operate in a discontinuous conduction mode, within a predetermined voltage range. The method comprises adjusting a duty cycle of the DC-DC converter based on the output voltage to maintain the output voltage within a predetermined voltage range; wherein the duty cycle of the DC-DC converter is adjusted by switching between a first switching frequency to a second switching frequency, and the first switching frequency and the second switching frequency are selected such that the first switching frequency and the second switching frequency fall outside of at least one predefined disallowed frequency band.

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A DC-DC CONVERTER

Technical Field

- 5 Embodiments disclosed herein relate to methods and apparatus for adapting DC-DC converter switching frequencies to maintain operation outside of predefined disallowed frequency bands.

Background

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Portable devices are becoming more common in every aspect of our lives. For example, many consumers listen to their music from portable audio players. These portable devices become easier and more enjoyable to use when they are provided in small packages, offering the same capabilities while still having long lasting battery charge. To support these longer lasting devices, the operating voltage of many of the components inside is often reduced to reduce the power consumption. However, this reduction in operating voltage may affect the sound output of the portable device as the volume level of an audio signal is proportional to the output voltage. A boost converter may therefore be used to increase the operating voltage for select components within a portable device that would benefit from higher operating voltages, for example, audio amplifiers which may require high voltages to provide high volumes.

Figure 1 illustrates a conventional audio amplifier comprising a boost converter. The audio amplifier comprises a battery supply 102 which is configured to provide a voltage V_p to a boost converter 104. The boost converter 104 increases the voltage V_p to a boost voltage V_{bst} . In this example, a speaker amplifier 108 is configured to receive the boost voltage V_{bst} and output an analog audio signal sig from a digital to analog converter (DAC). The speaker amplifier increases the low power signal sig with the power received from the boost converter to generate a signal to drive a speaker 110. The boost voltage V_{bst} is higher than the supply voltage V_p which allows the speaker amplifier 108 to provide louder audio signals through the speaker 110 than would be possible using only the supply voltage V_p .

Portable devices are becoming increasingly complex systems where the ability of a given integrated circuit to co-exist with a neighbouring integrated circuit (IC) on a printed circuit board or in a physically adjacent area may become increasingly important to the system

or device designer. Interference between the operation of any two ICs may occur not necessarily due to a direct connection between the two, but due to electromagnetic interference produced by one in a frequency or frequency range where operation of the other is susceptible to interference. A boost converter may for instance create a large switching voltage as a part the V_{bst} generation process. This switching voltage can often cause electromagnetic interference with other nearby ICs or other sub-systems on the portable device. The boost converter may also create noise in the battery supply (V_p) each time it switches. This switching can cause noise to be injected onto a power supply which may be shared by other ICs in a portable device. Some ICs are more susceptible than others to noise on the power supply and performance can suffer as a result. As the portable devices become increasingly complex, so do the requirements to avoid multiple frequency bands of operation.

Summary

According to embodiments described herein there is provided a method for maintaining an output voltage of a DC-DC converter, configured to operate in a discontinuous conduction mode, within a predetermined voltage range. The method comprises adjusting a duty cycle of the DC-DC converter based on the output voltage to maintain the output voltage within a predetermined voltage range; wherein the duty cycle of the DC-DC converter is adjusted by switching between a first switching frequency to a second switching frequency, and the first switching frequency and the second switching frequency are selected such that the first switching frequency and the second switching frequency fall outside of at least one predefined disallowed frequency band.

According to some embodiments there is provided a DC-DC converter configured to in a discontinuous conduction mode and to maintain an output voltage within a predetermined voltage range. The DC-DC converter comprises a controller, wherein the controller comprises an input configured to receive an indication of the output voltage; and an adjustment block configured to adjust a duty cycle of the DC-DC converter based on the output voltage to maintain the output voltage within a predetermined voltage range; wherein the duty cycle of the DC-DC converter is adjusted by switching between a first switching frequency to a second switching frequency, and the first switching frequency and the second switching frequency are selected such that the first switching frequency and the second switching frequency fall outside of at least one predefined disallowed frequency band.

Brief Description of the Drawings

5 For a better understanding of the present invention, and to show how it may be put into effect, reference will now be made, by way of example only, to the accompanying drawings, in which:-

Figure 1 is an example of a conventional audio amplifier comprising a boost converter in
10 accordance with the prior art;

Figure 2 is an example block diagram of a DC-DC converter in accordance with the present disclosure

15 Figure 3a is an example timing diagram illustrating the operation of a boost converter in a continuous conduction mode, CCM, in accordance with embodiments of the present disclosure;

Figure 3b is an example timing diagram illustrating the operation of a boost converter in
20 a continuous conduction mode, CCM, in accordance with embodiments of the present disclosure;

Figure 4 is an example timing diagram illustrating the operation of a boost converter in discontinuous conduction mode, DCM, in accordance with embodiments of the present
25 disclosure;

Figure 5 is an example timing diagram illustrating the operation of the DC-DC converter in DCM, in accordance with embodiments of the present disclosure;

30 Figure 6 is an example flow chart diagram illustrating a method for maintaining an output voltage of a DC-DC converter in a predetermined voltage range, while operating in a discontinuous conduction mode, in accordance with embodiments of the present disclosure;

Figure 7 is an example timing diagram illustrating the operation of a DC-DC converter when switching from a first switching frequency to a second switching frequency, in accordance with embodiments of the present disclosure;

- 5 Figure 8 is an example flow chart illustrating a method of reducing the duty cycle of a DC-DC converter to maintain the boost voltage within a predetermined voltage range, in accordance with embodiments of the present disclosure;

- 10 Figure 9 is an example flow chart illustrating a method of increasing the duty cycle of a DC-DC converter to maintain the boost voltage within a predetermined voltage range, in accordance with embodiments of the present disclosure;

- 15 Figure 10 is an example flow chart illustrating a method of reducing the duty cycle of a DC-DC converter to maintain the boost voltage within a predetermined voltage range, in accordance with embodiments of the present disclosure;

- 20 Figure 11 is an example flow chart illustrating a method of increasing the duty cycle of a DC-DC converter to maintain the boost voltage within a predetermined voltage range, in accordance with embodiments of the present disclosure;

Figure 12 is an example timing diagram illustrating the operation of a DC-DC converter in accordance with embodiments of the present disclosure;

- 25 Figure 13 is an example timing diagram illustrating the NFET 206 conducting and non-conducting states as the duty cycle is decreased in accordance with embodiments of the present disclosure;

- 30 Figure 14 is an example timing diagram illustrating the energy as a function of frequency for different frequencies using the same duty cycle in accordance with embodiments of the present disclosure;

- Figure 15 is an example graph illustrating the switching frequencies available to the boost converter when unconstrained by any predefined disallowed frequency band containing disallowed frequencies in accordance with embodiments of the present disclosure;

Figure 16 is a graph illustrating an example where two predefined disallowed frequency bands have been set containing disallowed frequencies in accordance with the present disclosure;

- 5 Figure 17 is a graph illustrating an example comprising a single predefined disallowed frequency band in accordance with the present disclosure;

Figure 18 is graph illustrating an example comprising three predefined disallowed frequency bands in accordance with the present disclosure;

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Figure 19 is graph illustrating an example comprising four predefined disallowed frequency bands in accordance with the present disclosure;

- 15 Figure 20 is an example block diagram of a DC-DC converter 1800 in accordance with the present disclosure.

Description

- The description below sets forth example embodiments according to this disclosure.
- 20 Further example embodiments and implementations will be apparent to those having ordinary skill in the art. Further, those having ordinary skill in the art will recognize that various equivalent techniques may be applied in lieu of, or in conjunction with, the embodiments discussed below, and all such equivalents should be deemed as being encompassed by the present disclosure.

25

- Figure 2** illustrates an example DC-DC converter 200 in accordance with some embodiments of the present disclosure. The DC-DC converter 200 comprises a battery supply 202 which provides a supply voltage V_P to the DC-DC converter 200. The DC-DC converter 200 comprises an inductor 204 connected to the battery supply 202. The DC-
- 30 DC converter 200 further comprises two switches 206 and 208 and a capacitor 210. The switches 206 and 208 are in this example implemented as an n-channel field effect transistor (NFET) 206 and a p-channel field effect transistor (PFET) 208.

- In this example implementation, the inductor 204 is coupled to the drain of the PFET 208 and the drain of the NFET 206. The drain of the PFET 208 and the drain of the NFET 206 are also coupled together.
- 35

The capacitor 210 is coupled between the source of the PFET 208 and ground. The source of the NFET 206 is coupled to ground. Both the gate of the PFET 208 and the gate of the NFET 206 are coupled to a level shifting and driving block 214 which controls
5 whether the PFET and NFET are in conducting or non-conducting states. An amplifier or other signal processing circuitry may be connected to receive the boost voltage from the source of the PFET 208.

For example, during a first time period, the NFET 206 may be switched on to a
10 conducting state which couples the inductor 204 to ground, while the PFET 208 is switched off to a non-conducting state. This switching configuration causes the supply voltage V_P to fall across the inductor 204 and therefore cause current to flow through the inductor 204 thereby storing energy in the inductor.

15 During a second time period, the NFET 206 may be switched off into a non-conducting state while the PFET 208 may be switched on to a conducting state. This switching configuration causes the inductor to couple to ground through the capacitor 210. Thus, the energy stored in the inductor 204 during the first time period is transferred to the capacitor 210 during the second time period. As energy is stored in the capacitor 210,
20 the voltage across the capacitor increases and allows the boost voltage V_{bst} to increase beyond the supply voltage V_P .

A controller 222 may control the duration of the first and second time periods in order to regulate the transfer of power from the inductor to the capacitor and thus regulate the
25 level of the boost voltage V_{bst} .

It will be appreciated that such a boost converter may operate in two distinct modes: continuous conduction mode, CCM and discontinuous conduction mode, DCM.

30 **Figure 3a** illustrates the operation of a boost converter in a continuous conduction mode, CCM. In this state, the boost converter operates with two switching states S_1 and S_2 per switching cycle. As previously described during state S_1 , NFET 206 is in a conducting state and PFET 208 is in a non-conducting state. During this period, the current is drawn across the inductor storing energy in the conductor. In switching state S_2 , as described
35 previously, the PFET 208 is in a conducting state and the NFET 206 is in a non-

conducting state. During this period, the energy stored in the inductor is transferred to the capacitor and the current through the inductor drops.

5 The controller may control the length of the duty cycle in order to maintain the output voltage within a predetermined range. In other words, if V_{bst} goes too high, the time spent in state S_1 may be reduced and if V_{bst} drops below a minimum voltage V_{min} , then the time spent in state S_1 may be increased.

10 In some examples, the switching state is switched from state S_1 to state S_2 when the current across the inductor reaches a maximum value. The switching state may be switched from state S_2 to state S_1 at the beginning of each clock cycle as illustrated by the begin switching frequency cycle pulses in Figure 3a.

15 However, when the load current decreases, in other words a higher resistance is coupled to receive the boost voltage V_{bst} , the inductor current also decreases. In this case, if the boost converter is left to operate in continuous conduction mode, then the inductor current may become negative in each switching period, as illustrated in **Figure 3b**. This negative current may waste power by passing unnecessary current across the inductor.

20 The boost converter may therefore be operated in discontinuous conduction mode (DCM). In DCM, there may be, for example, three different switching states. States S_1 and S_2 are the same as illustrated for CCM in Figures 3a and 3b, but in third state S_3 , both the NFET 206 and the PFET 208 are off.

25 As the PFET 208 is switched off, this switch deactivation stops any current flowing back through the inductor in a negative direction, thereby pinning or maintaining the inductor current at 0A as illustrated in **Figure 4**. This mode thereby avoids the power wasted by the negative current through the inductor illustrated in Figure 3b.

30 **Figure 5** illustrates an example of the operation of the DC-DC converter in DCM.

In this example, the DC-DC converter is configured to maintain the boost voltage V_{BST} within the predetermined voltage range between a maximum voltage V_{Max} and a minimum voltage V_{Min} . Therefore, when the voltage goes above the maximum voltage
35 V_{MAX} , the DC-DC converter may decrease the duty cycle of the DC-DC converter. In other words, the controller 222 illustrated in Figure 2 may decrease the amount of time

spent in switching state S_1 . This time decrease will reduce the energy stored in the inductor during the switching period, and therefore reduce the energy transferred to the capacitor, thereby reducing the boost voltage V_{BST} .

- 5 Equivalently, when the voltage drops below the minimum voltage V_{MIN} , the DC-DC converter may increase the duty cycle of the DC-DC converter. In other words, the controller 222 illustrated in Figure 2 may increase the amount of time spent in switching state S_1 . This time increase will increase the energy stored in the inductor during the switching period, and therefore increase the energy transferred to the capacitor, thereby
10 increasing the boost voltage V_{BST} .

According to some embodiments, it may also be desirable, for low enough loads, to reduce the switching frequency in order to further reduce the power consumption of the boost converter. By reducing the switching frequency, the time spent in the state S_3 can
15 be increased, thereby saving more power by not wasting current across the inductor.

Furthermore, a lower switching frequency reduces the power consumption across the capacitor.

- 20 **Figure 6** illustrates a method for maintaining an output voltage of a DC-DC converter in a predetermined voltage range, while operating in a discontinuous conduction mode, for example as illustrated in Figure 4.

In step 601, the DC-DC convertor determines the value of the output voltage of the DC-
25 DC convertor.

In step 602, the DC-DC converter adjusts a duty cycle of the DC-DC converter based on the output voltage to maintain the output voltage within a predetermined voltage range. For example, the duty cycle of the DC-DC converter may be adjusted by switching
30 between a first switching frequency and a second switching frequency. The first switching frequency and the second switching frequency may be selected such that the first switching frequency and the second switching frequency fall outside of at least one predefined disallowed frequency band.

- 35 For example, in some embodiments at least one predefined disallowed frequency band may be in place which comprises frequencies which should not be used by the DC-DC

converter. For example, one or more frequencies in the at least one predefined disallowed frequency band may be used for integrated circuits with some other application within a device comprising the DC-DC converter. In some embodiments, the electromagnetic interference (EMI) with switching frequencies within the predefined
5 disallowed frequency bands is unpredictable, and therefore it may be desirable to avoid using the frequencies within the predefined disallowed frequency bands. Therefore, the embodiments disclosed herein allow the boost converter's switching frequency and duty cycle to be manipulated in order to avoid electromagnetic interference or power supply noise injection which can be problematic for other sub-systems or ICs within the portable
10 device.

When changing switching frequencies to decrease or increase the duty cycle of the DC-DC converter, the frequencies may also be selected such that the time period of the switching frequencies are multiples of the time period of the clock frequency used by the
15 DC-DC converter. In this way, the switching periods of the lower frequencies will comprise an integer number of clock periods.

For example, consider a DC-DC converter utilizing a clock frequency of X kHz. This high frequency may be used as the highest switching frequency available to the DC-DC
20 converter. The second switching frequency may then be $X/2$ kHz. A third switching frequency of $X/3$ kHz may also be available, and so on.

The time period of the first switching frequency, which is equal to the clock frequency, will be $1/X$ seconds. The time period of the second frequency will be $2/X$ seconds, and
25 the time period of the third switching frequency will be $3/X$ seconds, and so on.

These switching frequencies may therefore comprise an integer number of clock cycles.

Therefore, when switching from the first switching frequency to the second switching
30 frequency, the DC-DC converter effectively skips a switching period as illustrated in **Figure 7**.

Figure 7 illustrates the operation of a DC-DC converter when switching from a first switching frequency equal to the clock frequency, to a second switching frequency.

In the first and second illustrated clock periods, the DC-DC converter is operating with the first switching frequency. However, mid-way through the second clock cycle, the DC-DC converter decides to lower the switching frequency, potentially due to the boost voltage V_{BST} being above the maximum voltage threshold V_{MAX} as illustrated in Figure 5.

5

The DC-DC converter may then switch to the second switching frequency for the 3rd to the 6th clock cycles. It can be seen that the second switching frequency effectively skips the 4th clock cycle and the 6th clock cycle by staying the third switching state S_3 and pinning the inductor current to zero.

10

Figure 8 illustrates a method of reducing the duty cycle of a DC-DC converter to maintain the boost voltage within a predetermined voltage range according to some embodiments.

In particular, the embodiment shown in figure 8 performs the steps of responsive to the output voltage being above the predetermined voltage range when using the first switching frequency, first decreasing the duty cycle by decreasing the on time of the DC-DC converter until a minimum duty cycle for the first switching frequency is reached, and responsive to the output voltage remaining above the predetermined voltage range when using the first switching frequency, switching to the second switching frequency.

20

In step 801 the DC-DC converter determines whether the boost voltage V_{BST} is above the maximum voltage threshold V_{MAX} . If the boost voltage V_{BST} is below the threshold V_{MAX} the method returns to the start.

If in step 801 the DC-DC converter determines that the boost voltage V_{BST} is above the maximum threshold V_{MAX} , the method passes to step 802 in which the DC-DC converter determines whether an on time T_{S1} that the DC-DC converter in the state S_1 , is greater than a minimum value, T_{S1MIN} . An on time of the DC-DC converter may be considered a period of time during which the current across the inductor of the DC-DC converter is being increased. In the example illustrated in Figure 4, this on time may be understood as the period that the DC-DC convertor remains in the state S_1 , i.e. the time for which the NFET is in a conducting state.

The minimum on time T_{S1MIN} may be a minimum duty cycle for the frequency at which the DC-DC converter is operating.

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If in step 802 the DC-DC converter determines that the on time T_{S1} of the DC-DC converter is greater than T_{S1MIN} , then the method passes to step 803 in which the DC-DC converter reduces the on time of the DC-DC converter. The method will then return to the start. In some embodiments, the on time of the DC-DC converter may be reduced by a predetermined increment.

If in step 802 the DC-DC converter determines that the on time T_{S1} of the DC-DC converter is not greater than the minimum on time T_{S1MIN} , the method then passes to step 804 in which the DC-DC converter determines whether the switching frequency F_S is greater than a minimum switching frequency F_{SMIN} .

If in step 804 the DC-DC converter determines that the switching frequency F_S is greater than the minimum switching frequency F_{SMIN} , the method passes to step 805 in which the DC-DC converter reduces the switching frequency. In some embodiments, the switching frequency may be decreased by increasing the time period of the switching frequency by one clock period. The method may then pass back to the start. In other words, by decreasing the switching frequency the DC-DC converter switches from the first switching frequency to the second switching frequency.

If in step 804 the DC-DC converter determines that the switching frequency F_S is not greater than the minimum switching frequency, the method may end in step 806.

It will be appreciated that the steps 801 to 805 may be performed iteratively until either the voltage has dropped below the maximum threshold V_{MAX} or both the minimum on time T_{S1MIN} and the minimum switching frequency F_{SMIN} have been reached.

In some embodiments the switching frequency may be decreased from a starting frequency F_{START} by increasing N by one in the following equation:

$$F_N = (F_{START})/(N+1)$$

Figure 9 illustrates a method of increasing the duty cycle of a DC-DC converter to maintain the boost voltage within a predetermined voltage range according to some embodiments.

The embodiment illustrated in figure 9 performs the steps of, responsive to the output voltage being below the predetermined voltage range when using the second switching frequency, first increasing the duty cycle by increasing an on time of the DC-DC converter until a maximum duty cycle for the second switching frequency is reached, and
5 responsive to the output voltage remaining below the predetermined voltage range when using the second switching frequency, switching to the first switching frequency.

In step 901, the DC-DC converter determines whether the boost voltage V_{BST} is below the minimum voltage threshold V_{MIN} . If the boost voltage V_{BST} is above the minimum
10 threshold V_{MIN} the method returns to the start.

If in step 901, the DC-DC converter determines that the boost voltage V_{BST} is below the minimum threshold V_{MIN} , the method passes to step 902 in which the DC-DC converter determines whether an on time of the DC-DC converter, T_{S1} , is less than a maximum
15 value, T_{S1MAX} . An on time of the DC-DC converter may be defined as a period of time during which the current across the inductor of the DC-DC converter is being increased. In the example illustrated in Figure 4, this on time may be understood as the period during which the DC-DC converter is in state S_1 , i.e. the time for which the NFET is in a conducting state.

20 The maximum on time T_{S1MAX} may be a maximum duty cycle for the frequency at which the DC-DC converter is operating.

If in step 902 the DC-DC converter determines that the on time T_{S1} of the DC-DC
25 converter is less than T_{S1MAX} , then the method passes to step 903 in which the DC-DC converter increases the on time T_{S1} of the DC-DC converter. The method will then return to the start. In some embodiments, the on time T_{S1} of the DC-DC converter may be increased by a predetermined increment.

30 If in step 902 the DC-DC converter determines that the on time T_{S1} of the DC-DC converter is not less than the maximum on time T_{S1MAX} , the method then passes to step 904 in which the DC-DC converter determines whether the switching frequency F_S is less than a maximum switching frequency F_{SMAX} .

35 If in step 904 the DC-DC converter determines that the switching frequency F_S is less than the maximum switching frequency F_{SMAX} , the method passes to step 805 in which

the DC-DC converter increases the switching frequency. In some embodiments, the switching frequency may be increased by decreasing the time period of the switching frequency by one clock period. The method may then pass back to the start. In other words, by increasing the switching frequency, the DC-DC converter switches from the
 5 second switching frequency to the first switching frequency.

If in step 904 the DC-DC converter determines that the switching frequency F_s is not less than the maximum switching frequency $F_{S\text{MAX}}$, the method may end in step 806.

10 It will be appreciated that the steps 901 to 905 may be performed iteratively until either the voltage has risen above the minimum threshold V_{MIN} or both the maximum on time $T_{S1\text{MAX}}$ and the maximum switching frequency $F_{S\text{MAX}}$ have been reached.

In some embodiments the switching frequency may be increased from a starting
 15 frequency F_{START} by decreasing N by one in the following equation:

$$F_N = (F_{\text{START}})/(N+1)$$

20 **Figure 10** illustrates a method of reducing the duty cycle of a DC-DC converter to maintain the boost voltage within a predetermined voltage range according to some embodiments.

In particular, the embodiment shown in Figure 10 performs the steps of responsive to
 25 the output voltage being above the predetermined voltage range when using the first switching frequency, first switching to the second switching frequency; and responsive to the output voltage remaining above the predetermined voltage range when using the second switching frequency, decreasing the duty cycle by decreasing the on time of the DC-DC converter until a minimum duty cycle for the second switching frequency is
 30 reached.

In step 1001 the DC-DC converter determines whether the boost voltage V_{BST} is above the maximum voltage threshold V_{MAX} . If the boost voltage V_{BST} is below the threshold V_{MAX} , the method returns to the start.

35

If in step 1001 the DC-DC converter determines that the boost voltage V_{BST} is above the maximum threshold V_{MAX} , the method passes to step 1002 in which the DC-DC converter determines whether the switching frequency F_s is greater than a minimum switching frequency F_{SMIN} .

5

If in step 1002 the DC-DC converter determines that the switching frequency F_s is greater than the minimum switching frequency F_{SMIN} , the method passes to step 1003 in which the DC-DC converter reduces the switching frequency. In some embodiments, the switching frequency may be decreased by increasing the time period of the switching frequency by one clock period. In other words, by reducing the switching frequency the DC-DC converter switches from using the first switching frequency to using a second switching frequency. The method may then pass back to the start.

If in step 1002 the DC-DC converter determines that the switching frequency F_s is not greater than the minimum switching frequency, the method pass to step 1004 in which the DC-DC converter the DC-DC converter determines whether an on time T_{S1} during which the DC-DC converter is in state S_1 , is greater than a minimum value, T_{S1MIN} . An on time T_{S1} of the DC-DC converter may be considered a period of time during which the current across the inductor of the DC-DC converter is being increased. In the example illustrated in Figure 4, this on time T_{S1} may be understood as the period during which the DC-DC converter is in state S_1 , i.e. the time for which the NFET is in a conducting state.

The minimum on time T_{S1MIN} may be a minimum duty cycle for the frequency at which the DC-DC converter is operating.

25

If in step 1004 the DC-DC converter determines that the on time T_{S1} of the DC-DC converter is greater than T_{S1MIN} , then the method passes to step 1005 in which the DC-DC converter reduces the on time of the DC-DC converter. The method will then return to the start. In some embodiments, the on time of the DC-DC converter may be reduced by a predetermined increment.

30

If in step 1004 the DC-DC converter determines that the on time T_{S1} of the DC-DC converter is not greater the T_{S1MIN} , the method may end in step 1006.

It will be appreciated that the steps 1001 to 1005 may be performed iteratively until either the voltage has dropped below the maximum threshold V_{MAX} or both the minimum on time T_{S1MIN} and the minimum switching frequency F_{SMIN} have been reached.

- 5 In some embodiments the switching frequency may be decreased from a starting frequency F_{START} by increasing N by one in the following equation:

$$F_N = (F_{START})/(N+1).$$

- 10 **Figure 11** illustrates a method of increasing the duty cycle of a DC-DC converter to maintain the boost voltage within a predetermined voltage range according to some embodiments.

- In particular, the embodiment shown in Figure 11 performs the steps of responsive to the output voltage being above the predetermined voltage range when using the first switching frequency, first switching to the second switching frequency; and responsive to the output voltage remaining above the predetermined voltage range when using the second switching frequency, decreasing the duty cycle by decreasing the on time of the DC-DC converter until a minimum duty cycle for the second switching frequency is reached.

- In step 1101 the DC-DC converter determines whether the boost voltage V_{BST} is below the minimum voltage threshold V_{MIN} . If the boost voltage V_{BST} is above the minimum threshold V_{MIN} , the method returns to the start.

- 25 If in step 1101 the DC-DC converter determines that the boost voltage V_{BST} is below the minimum threshold V_{MIN} , the method passes to step 1102 in which the DC-DC converter determines whether the switching frequency F_S is less than a maximum switching frequency F_{SMAX} .

- 30 If in step 1102 the DC-DC converter determines that the switching frequency F_S is less than the maximum switching frequency F_{SMAX} , the method passes to step 1103 in which the DC-DC converter increases the switching frequency. In some embodiments, the switching frequency may be increased by decreasing the time period of the switching frequency by one clock period. In other words, by increasing the switching frequency the

DC-DC converter switches from using the first switching frequency to the second switching frequency. The method may then pass back to the start.

If in step 1102 the DC-DC converter determines that the switching frequency F_s is not less than the maximum switching frequency F_{sMAX} , the method passes to step 1104 in which the DC-DC converter determines whether an on time T_{S1} during which the DC-DC converter is in state S_1 , is less than a maximum value, T_{S1MAX} . An on time T_{S1} of the DC-DC converter may be defined as a period of time during which the current across the inductor of the DC-DC converter is being increased. In the example illustrated in Figure 4, this may be understood as the period during which the DC-DC converter is in state S_1 , i.e. the time for which the NFET is in a conducting state.

The maximum on time T_{S1MAX} may be a maximum duty cycle for the frequency at which the DC-DC converter is operating.

If in step 1104 the DC-DC converter determines that the on time T_{S1} of the DC-DC converter is less than T_{S1MAX} , then the method passes to step 1105 in which the DC-DC converter increases the on time T_{S1} of the DC-DC converter. The method will then return to the start. In some embodiments, the on time T_{S1} of the DC-DC converter may be increased by a predetermined increment.

If in step 1104 the DC-DC converter determines that the on time T_{S1} of the DC-DC converter is not less than the maximum on time T_{S1MAX} , the method may end in step 1106.

It will be appreciated that the steps 1101 to 1105 may be performed iteratively until either the voltage has risen above the minimum threshold V_{MIN} or both the maximum on time T_{S1MAX} and the maximum switching frequency F_{sMAX} have been reached.

In some embodiments the switching frequency may be increased from a starting frequency F_{START} by decreasing N by one in the following equation:

$$F_N = (F_{START})/(N+1).$$

Figure 12 illustrates an example of the operation of a DC-DC converter according to some embodiments.

The DC-DC converter monitors the output voltage V_{BST} , for example, as illustrated in
5 Figure 2, the controller 222 may receive an indication of the output voltage V_{BST} via an analog-to-digital converter 220. The controller 222 may then adjust the duty cycle of the DC-DC converter accordingly.

For example, as illustrated in Figure 12, if at a time t_1 the boost voltage V_{BST} goes above
10 a maximum threshold voltage V_{MAX} , the controller 222 be configured to determine whether to decrease the duty cycle.

In some embodiments, the DC-DC converter is configured to decrease the duty cycle responsive to the boost voltage V_{BST} remaining above the maximum voltage V_{MAX} for a
15 predetermined time. For example, the controller 222 may comprise a filter counter configured to count clock cycles from when the voltage first passes above the maximum threshold V_{MAX} at a time t_1 , until the amplitude passes back below the maximum threshold at a time t_2 . In this example, at the time t_2 the filter counter has not yet counted a predetermined number X of clock cycles. The DC-DC converter may therefore not
20 decrease the duty cycle. This manner of control avoids unnecessary decreasing of the duty cycle due to transient peaks in the boost voltage V_{BST} .

However, at time t_3 the boost voltage V_{BST} passes back above the maximum threshold V_{MAX} , this time for long enough for the filter counter to count X clock cycles twice. In this
25 example, a wait counter is also implemented where the filter counter waits a predetermined time between counting each set of X clock cycles. The controller therefore decreases the duty cycle twice after each time the filter counter counts X clock cycles. The boost voltage passes below the maximum threshold at time t_4 before the filter counter can count X clock cycles for a third time, and therefore the duty cycle is not
30 decreased a third time.

It will be appreciated that the duty cycle may be decreased as described with respect to Figure 8 or 10 by decreasing the on time of the DC-DC converter and/or the switching frequency.

It will be appreciated that the DC-DC converter may be equivalently configured to increase the duty cycle responsive to the boost voltage remaining below the minimum voltage V_{MIN} for a predetermined time. For example, the controller 222 may comprise a filter counter configured to count clock cycles from when the voltage first passes below the minimum threshold V_{MIN} to when the voltage passes back above the threshold V_{MIN} . Again, if the filter counter does not reach a predetermined number of clock cycles Y (where Y may or may not be equal to X) in this time, the controller may be configured not to increase the duty cycle. This manner of control avoids unnecessary increasing of the duty cycle due to transient troughs in the boost voltage V_{BST} .

Again, it will be appreciated that the duty cycle may be increased as described with respect to Figure 9 or 11 by increasing the on time of the DC-DC converter and/or the switching frequency.

Figure 13 illustrates the NFET 206 conducting and non-conducting states as the duty cycle is decreased. In this example, the duty cycle is decreased according to the method described in Figure 8, but it will be appreciated that the duty cycle may be increased or decreased according to any of the methods described above.

At first, in this example, the duty cycle is $3x/T_1$. The duty cycle is then decreased to $2x/T_1$ by decreasing the on time of the DC-DC converter from $3x$ to $2x$. The duty cycle is then decreased to x/T_1 by decreasing the on time of the DC-DC converter from $2x$ to x .

As x is the minimum on time for the DC-DC converter, the duty cycle is then decreased to $x/(2T_1)$ by decreasing the switching frequency from $1/T_1$ to $1/(2T_1)$. Again, the duty cycle may be further decreased from $x/(2T_1)$ to $x/(3T_1)$ by decreasing the switching frequency from $1/(2T_1)$ to $1/(3T_1)$.

Figure 14 illustrates the energy as a function of frequency for different frequencies using the same duty cycle.

Another possible reason to alter the switching frequency of the DC-DC converter may be to change the concentration of the energy within the frequency band as illustrated in Figure 14.

In Figure 14a, the NFET on and off times are illustrated. The duty cycle is x/T_1 and the switching frequency is $1/T_1$. The graph 1300 illustrates how the energy is therefore concentrated around the frequency $1/T_1$.

- 5 In Figure 14b, the duty cycle is $2x/2T_1$ which is equivalent to x/T_1 , in other words, the same as in Figure 13a. However, the switching frequency is $1/(2T_1)$. The graph 1401 therefore illustrates how the energy is now concentrated around the lower frequency of $1/(2T_1)$.
- 10 As the energy in the frequency band may be altered by changing the switching frequency, as illustrated in Figure 14. If, for example, a concentration of energy is desired that is concentrated around a frequency $1/T_1$ but in this example $1/T_1$ is not an allowed switching frequency, in other words the frequency $1/T_1$ falls within the predefined disallowed frequency band, then two or more allowable switching frequencies which do
- 15 not fall within the predefined disallowed frequency band, falling either side of the desired switching frequency, may be utilized to create the same energy distribution around the switching frequency $1/T_1$.

Figure 15 illustrates the switching frequencies available to the boost converter when unconstrained by any predefined disallowed frequency band containing disallowed frequencies. As illustrated, the boost converter has a minimum and maximum possible switching frequency. In this example, f_{MIN0} is the minimum switching frequency of the boost converter when allowed to operate without any predefined disallowed frequency bands containing disallowed frequencies. In this example, f_{MAX0} is the maximum

20 switching frequency of the boost converter when allowed to operate without any predefined disallowed frequency bands containing disallowed frequencies.

Figure 16 illustrates an example where two predefined disallowed frequency bands have been set containing disallowed frequencies. In this example, a first predefined disallowed frequency band between f_{MIN0} and a frequency f_{MIN1} is introduced and a second predefined disallowed frequency band between f_{MAX1} and f_{MAX0} is introduced. The values f_{MIN1} and f_{MAX1} are then set as maximum and minimum switching frequencies for the boost converter in order to ensure that the boost converter does not use switching frequencies in either of the predefined disallowed frequency bands. In this example, the predefined

30 disallowed frequency bands sit at either end of the allowed switching frequencies.

35

Figure 17 illustrates an example comprising a single predefined disallowed frequency band has been set containing disallowed frequencies. In this example, the predefined disallowed frequency band falls between the frequencies f_{MAX1} and f_{MIN1} . The frequencies between f_{MAX1} and f_{MIN1} may therefore be considered as disallowed. Two frequency bands are provided that the boost converter may use between f_{MIN0} and f_{MAX1} and f_{MIN2} and f_{MAX0} . In this example therefore, the boost converter may select a frequency between f_{MIN0} and f_{MAX1} and f_{MIN2} and f_{MAX0} . In circumstances where the desired energy concentration is between f_{MAX1} and f_{MIN2} , the boost converter may select a frequency between f_{MIN0} and f_{MAX1} and a different frequency between f_{MIN2} and f_{MAX0} and may then alternate between the two switching frequencies in such a way that the energy may be concentrated between the frequencies f_{MAX1} and f_{MIN2} .

In some embodiments therefore, the DC-DC converter may be configured to alternate between a first switching frequency and a second switching frequency wherein the first switching frequency is higher than the predefined disallowed frequency band and the second switching frequency is lower than the predefined disallowed frequency band.

Figure 18 illustrates an example comprising three predefined disallowed frequency bands. In this example, a first predefined disallowed frequency band falls between f_{MIN0} and a frequency f_{MIN1} and a second frequency bend falls between f_{MAX2} and f_{MAX0} . These disallowed frequency bands are equivalent to those illustrated in Figure 16 in that they are at the ends of the possible frequencies that the boost converter is capable of using. However, in this example, the predefined disallowed frequency band between f_{MAX1} and f_{MIN2} is also disallowed. In this example, therefore only the frequencies between f_{MIN1} and f_{MAX1} and the frequencies between f_{MIN2} and f_{MAX2} may be used by the boost converter. Similarly to as described with regards to Figure 17, the boost converter may alternate between a switching frequency between f_{MIN1} and f_{MAX1} and a switching frequency between f_{MIN2} and f_{MAX2} in order to concentrate the energy between the frequencies f_{MAX1} and f_{MIN2} .

Figure 19 illustrates an example comprises four predefined disallowed frequency bands. In this example, the frequencies between f_{MIN0} and f_{MIN1} , between f_{MAX1} and f_{MIN2} , between f_{MAX2} and f_{MIN3} and between f_{MAX3} and f_{MIN4} are disallowed.

As previously, the boost convertor may alternate between frequencies outside of these predefined disallowed frequency bands containing disallowed frequencies to concentrate

the energy within the predefined disallowed frequency bands without actually using the frequencies within those predefined disallowed frequency bands.

Figure 20 illustrates a DC-DC converter 2000 according to some embodiments. The DC-
5 DC converter 2000 comprises a controller 2001. The controller 2001 comprises an input
2002 configured to receive an indication of the output voltage.

The controller 2001 further comprises an adjustment block 2003 configured to adjust a
duty cycle of the DC-DC converter based on the output voltage to maintain the output
10 voltage within a predetermined voltage range. The duty cycle of the DC-DC converter is
adjusted by switching between a first switching frequency to a second switching
frequency. The first switching frequency and the second switching frequency are
selected such that the first switching frequency and the second switching frequency fall
outside of at least one predefined disallowed frequency band. As described previously,
15 the at least one predefined disallowed frequency band may comprise disallowed
frequencies.

There is therefore provided methods and apparatus for maintaining an output voltage of
a DC-DC converter, configured to operate in a discontinuous conduction mode, within a
20 predetermined voltage range.

It should be noted that the above-mentioned embodiments illustrate rather than limit the
invention, and that those skilled in the art will be able to design many alternative
embodiments without departing from the scope of the appended claims. The word
25 “comprising” does not exclude the presence of elements or steps other than those listed
in the claim, “a” or “an” does not exclude a plurality, and a single feature or other unit
may fulfill the functions of several units recited in the claims. Any reference numerals or
labels in the claims shall not be construed so as to limit their scope. Terms such as
amplify or gain include possible applying a scaling factor or less than unity to a signal.

CLAIMS

1. A method for maintaining an output voltage of a DC-DC converter, configured to operate in a discontinuous conduction mode, within a predetermined voltage range, the
5 method comprising:
adjusting a duty cycle of the DC-DC converter based on an output voltage to maintain the output voltage within a predetermined voltage range; wherein
the duty cycle of the DC-DC converter is adjusted by switching between a first switching frequency to a second switching frequency, and
10 the first switching frequency and the second switching frequency are selected such that the first switching frequency and the second switching frequency fall outside of at least one predefined disallowed frequency band.
2. The method of claim 1 wherein the second switching frequency is equal to $1/N$ of
15 the first switching frequency.
3. The method of claim 1 wherein the DC-DC converter is configured for use in a device and the at least one predefined disallowed frequency band comprises frequencies reserved for use with other components in the device.
20
4. The method of claim 1 further comprising:
adjusting the duty cycle of the DC-DC converter by decreasing an on time of the DC-DC converter.
- 25 5. The method of claim 4 further comprising: responsive to the output voltage being above the predetermined voltage range when using the first switching frequency, first decreasing the duty cycle by decreasing the on time of the DC-DC converter until a minimum duty cycle for the first switching frequency is reached, and
responsive to the output voltage remaining above the predetermined voltage range
30 when using the first switching frequency, switching to the second switching frequency.
6. The method of claim 5 further comprising:
responsive to the output voltage remaining above the predetermined voltage range when using the second switching frequency, switching to a third switching frequency
35 wherein the third frequency is $1/N+1$ times the second frequency.

7. The method of claim 4 further comprising:
responsive to the output voltage being below the predetermined voltage range
when using the second switching frequency, first increasing the duty cycle by increasing
an on time of the DC-DC converter until a maximum duty cycle for the second switching
5 frequency is reached, and
responsive to the output voltage remaining below the predetermined voltage range
when using the second switching frequency, switching to the first switching frequency.
8. The method of claim 7 further comprising:
10 responsive to the output voltage remaining below the predetermined voltage range
when using the first switching frequency, switching to a third switching frequency wherein
the third frequency is greater than the first frequency.
9. The method of claim 4 further comprising: responsive to the output voltage being
15 above the predetermined voltage range when using the first switching frequency, first
switching to the second switching frequency; and
responsive to the output voltage remaining above the predetermined voltage range
when using the second switching frequency, decreasing the duty cycle by decreasing
the on time of the DC-DC converter until a minimum duty cycle for the second switching
20 frequency is reached.
10. The method of claim 9 further comprising:
responsive to the output voltage remaining above the predetermined voltage range
when using the second switching frequency, switching to a third switching frequency
25 wherein the third frequency is $1/N+1$ times the second frequency.
11. The method of claim 4 further comprising:
responsive to the output voltage being below the predetermined voltage range
when using the second switching frequency, switching to the first switching frequency
30 and
responsive to the output voltage remaining below the predetermined voltage range
when using the first switching frequency, increasing the duty cycle by increasing an on
time of the DC-DC converter until a maximum duty cycle for the first switching frequency
is reached.
35
12. The method of claim 11 further comprising:

responsive to the output voltage remaining below the predetermined voltage range when using the first switching frequency, switching to a third switching frequency wherein the third frequency is greater than the first frequency.

5 13. The method of claim 1 further comprising:

alternating between the first switching frequency and the second switching frequency, wherein the first switching frequency is higher than the predefined disallowed frequency band and the second switching frequency is lower than the predefined disallowed frequency band.

10

14. The method of claim 1 wherein the at least one predefined disallowed frequency band comprises two or more separate predefined disallowed frequency bands.

15. A DC-DC converter configured to in a discontinuous conduction mode and to
15 maintain an output voltage within a predetermined voltage range, the DC-DC converter comprising a controller, wherein the controller comprises:

an input configured to receive an indication of the output voltage; and

an adjustment block configured to adjust a duty cycle of the DC-DC converter based on the output voltage to maintain the output voltage within a predetermined
20 voltage range; wherein

the duty cycle of the DC-DC converter is adjusted by switching between a first switching frequency to a second switching frequency, and

the first switching frequency and the second switching frequency are selected such that the first switching frequency and the second switching frequency fall outside of
25 at least one predefined disallowed frequency band.

16. The DC-DC converter of claim 15 wherein the second switching frequency is equal to $1/N$ of the first switching frequency.

30 17. The DC-DC converter of claim 15 wherein the DC-DC converter is configured for use in a device and the at least one predefined disallowed frequency band comprises frequencies reserved for use with other components in the device.

18. The DC-DC converter of claim 15 wherein the adjustment block is further
35 configured to adjust the duty cycle of the DC-DC converter by decreasing an on time of the DC-DC converter.

19. The DC-DC converter of claim 18 wherein the adjustment block is further configured to: responsive to the output voltage being above the predetermined voltage range when using the first switching frequency, first decrease the duty cycle by decreasing the on time of the DC-DC converter until a minimum duty cycle for the first switching frequency is reached, and
responsive to the output voltage remaining above the predetermined voltage range when using the first switching frequency, switch to the second switching frequency.
20. The DC-DC converter of claim 19 wherein the adjustment block is further configured to: responsive to the output voltage remaining above the predetermined voltage range when using the second switching frequency, switch to a third switching frequency wherein the third frequency is $1/N+1$ times the second frequency.
21. The DC-DC converter of claim 18 wherein the adjustment block is further configured to: responsive to the output voltage being below the predetermined voltage range when using the second switching frequency, first increase the duty cycle by increasing an on time of the DC-DC converter until a maximum duty cycle for the second switching frequency is reached, and
responsive to the output voltage remaining below the predetermined voltage range when using the second switching frequency, switch to the first switching frequency.
22. The DC-DC converter of claim 21 wherein the adjustment block is further configured to: responsive to the output voltage remaining below the predetermined voltage range when using the first switching frequency, switch to a third switching frequency wherein the third frequency is greater than the first frequency.
23. The DC-DC converter of claim 18 wherein the adjustment block is further configured to: responsive to the output voltage being above the predetermined voltage range when using the first switching frequency, first switch to the second switching frequency; and
responsive to the output voltage remaining above the predetermined voltage range when using the second switching frequency, decrease the duty cycle by decreasing the on time of the DC-DC converter until a minimum duty cycle for the second switching frequency is reached.

24. The DC-DC converter of claim 23 wherein the adjustment block is further configured to: responsive to the output voltage remaining above the predetermined voltage range when using the second switching frequency, switch to a third switching frequency wherein the third frequency is $1/N+1$ times the second frequency.

5

25. The DC-DC converter of claim 18 wherein the adjustment block is further configured to: responsive to the output voltage being below the predetermined voltage range when using the second switching frequency, switch to the first switching frequency and

10 responsive to the output voltage remaining below the predetermined voltage range when using the first switching frequency, increase the duty cycle by increasing an on time of the DC-DC converter until a maximum duty cycle for the first switching frequency is reached.

15 26. The DC-DC converter of claim 25 wherein the adjustment block is further configured to:

responsive to the output voltage remaining below the predetermined voltage range when using the first switching frequency, switch to a third switching frequency wherein the third frequency is greater than the first frequency.

20

27. The DC-DC converter of claim 15 wherein the adjustment block is configured to alternate between the first switching frequency and the second switching frequency, wherein the first switching frequency is higher than the predefined disallowed frequency band and the second switching frequency is lower than the predefined disallowed frequency band.

25

28. The DC-DC converter of claim 15 wherein the at least one predefined disallowed frequency band comprises two or more separate predefined disallowed frequency bands.

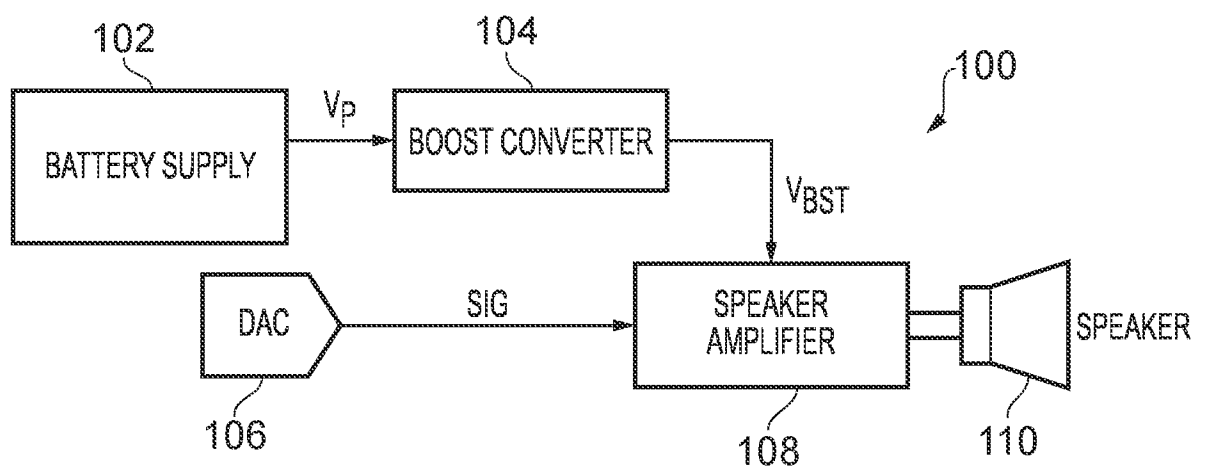


FIG. 1 (Prior Art)

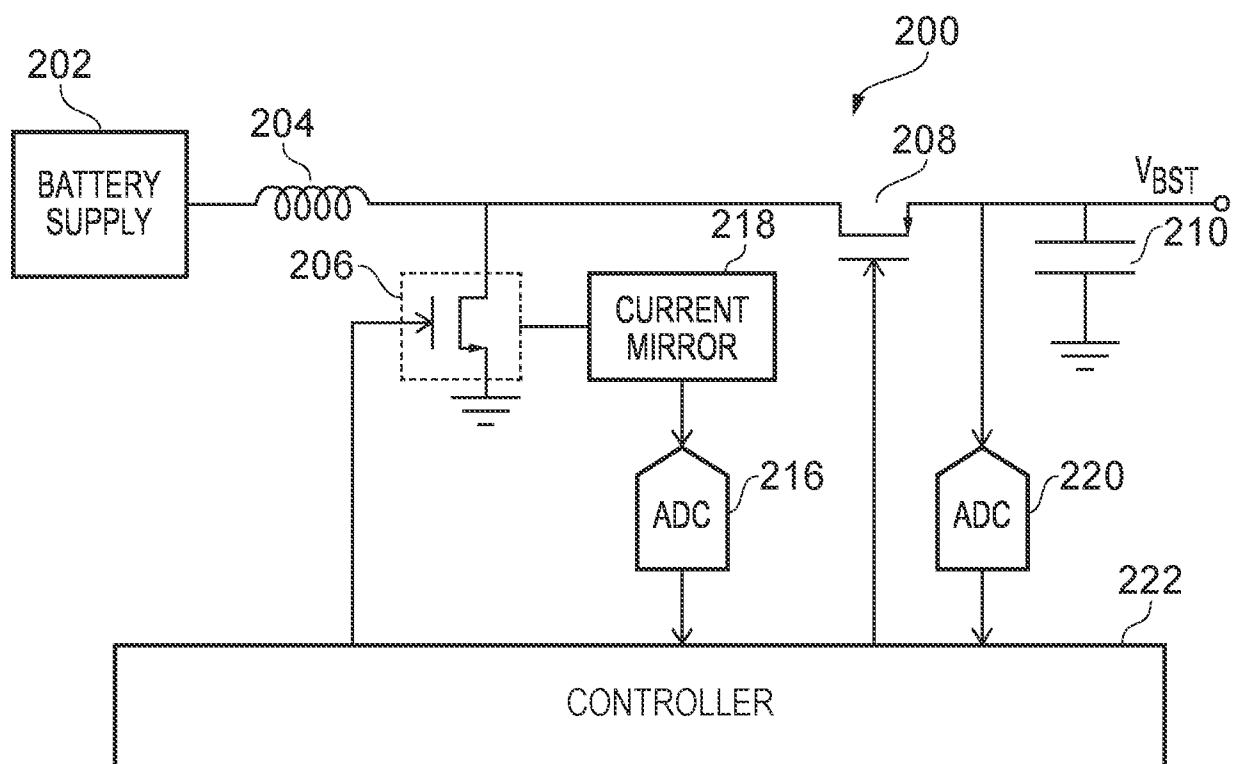


FIG. 2

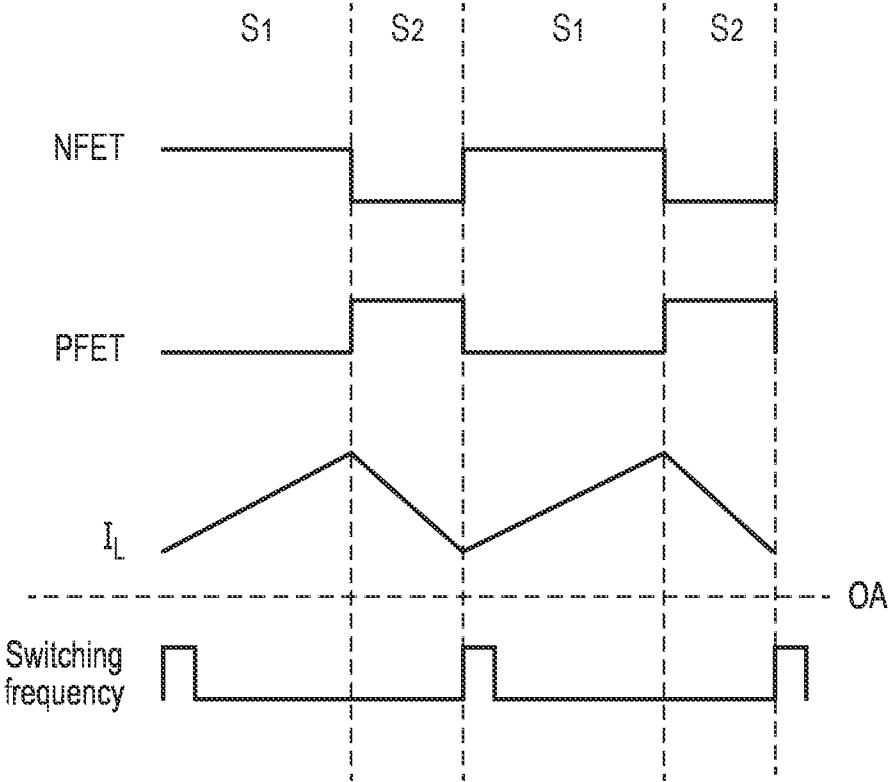


FIG. 3a

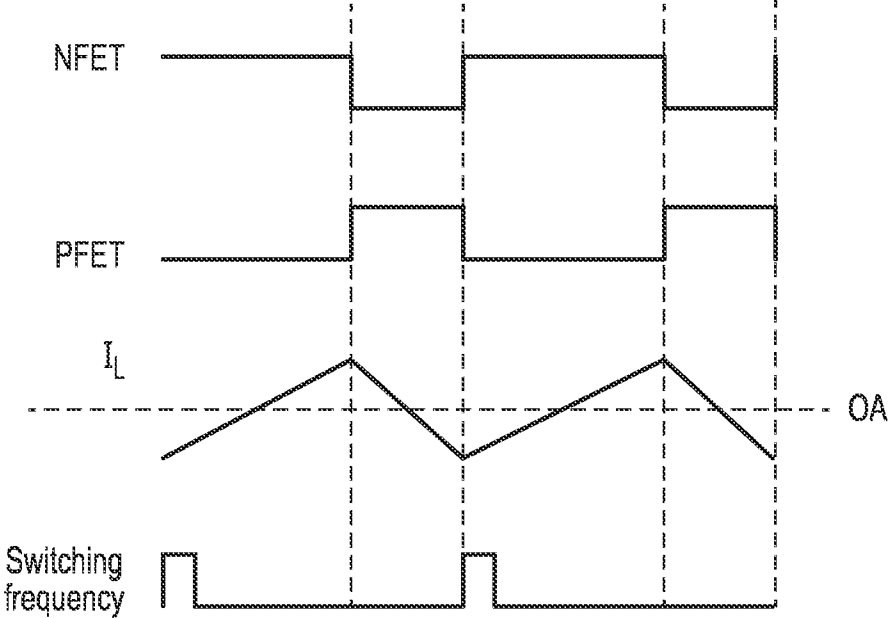


FIG. 3b

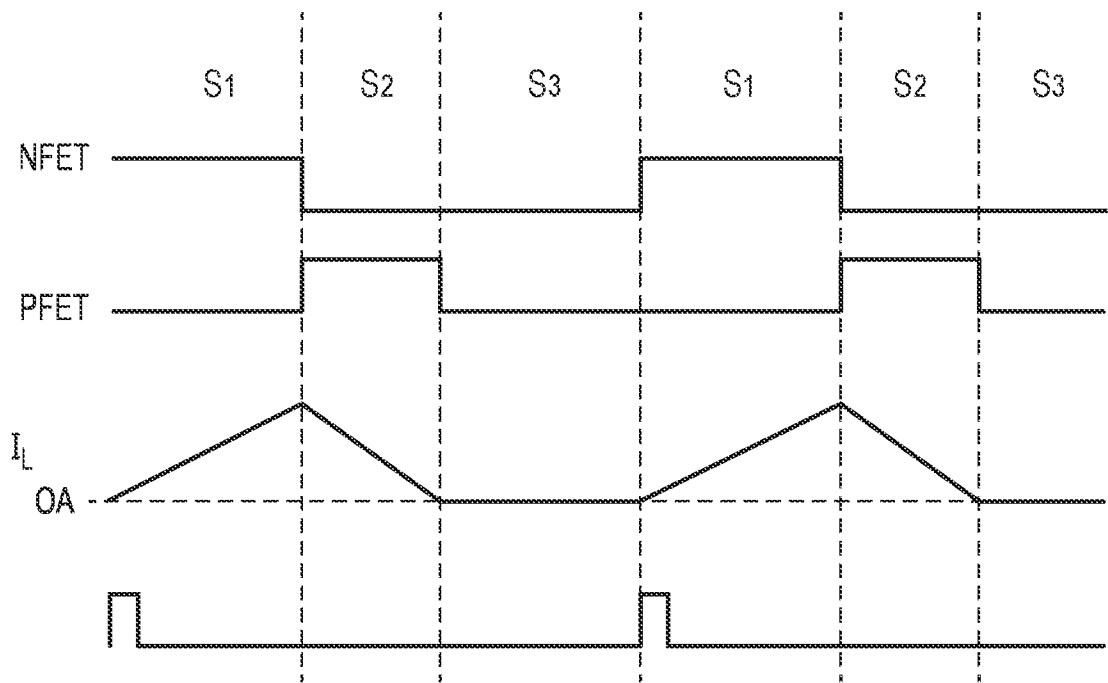


FIG. 4

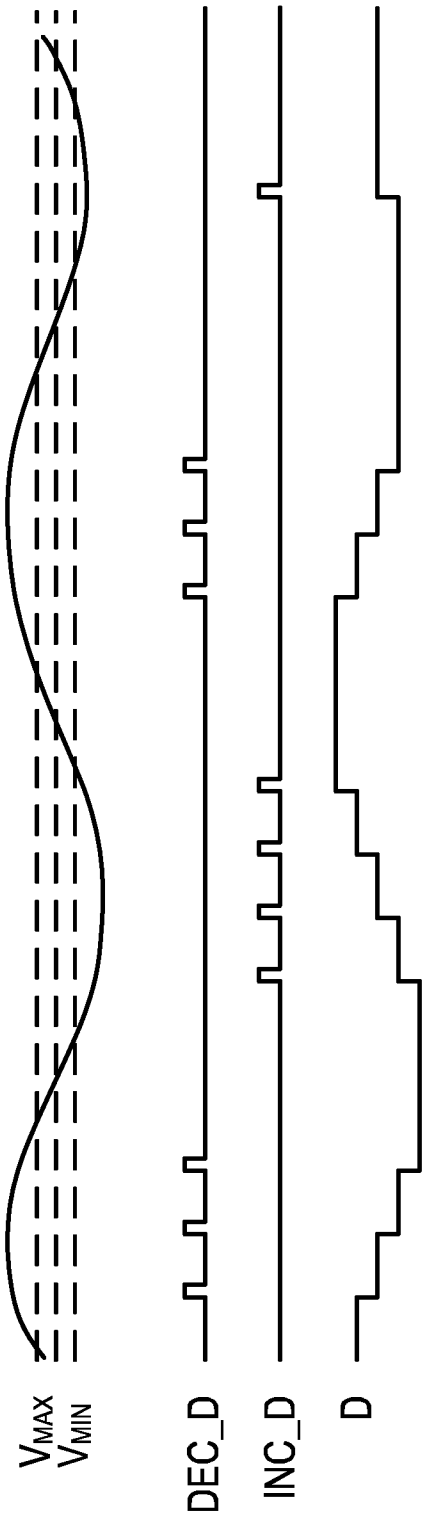


FIG. 5

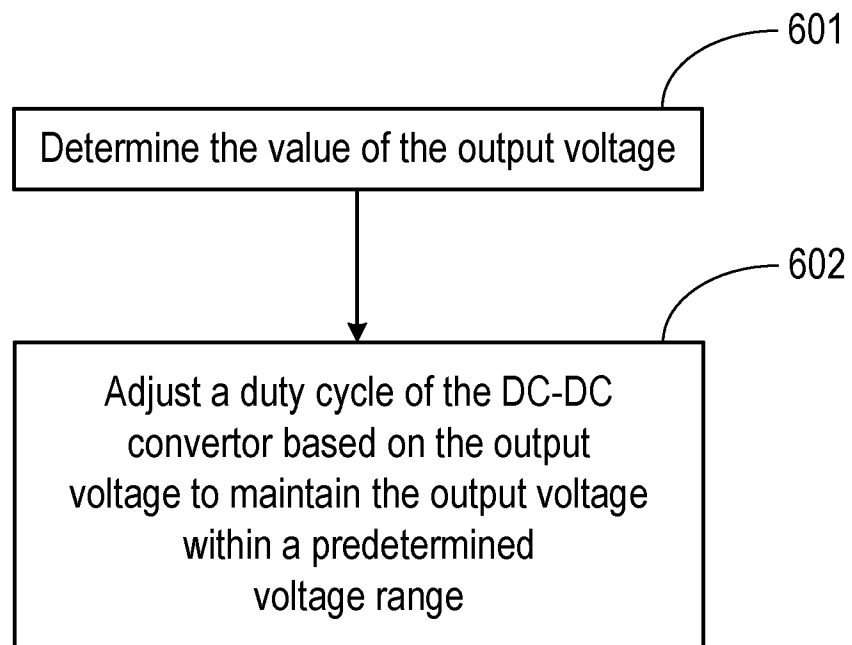


FIG. 6

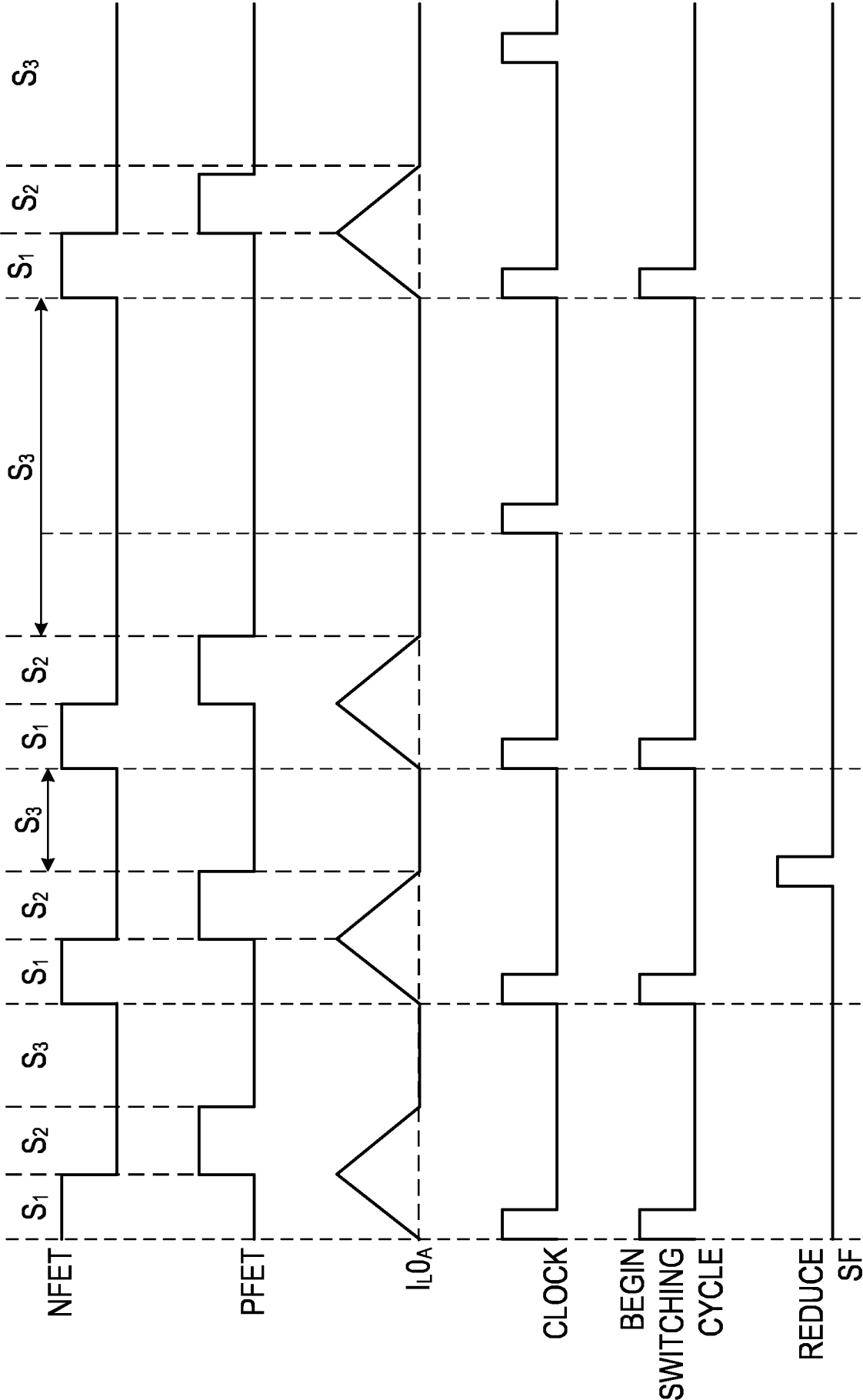


FIG. 7

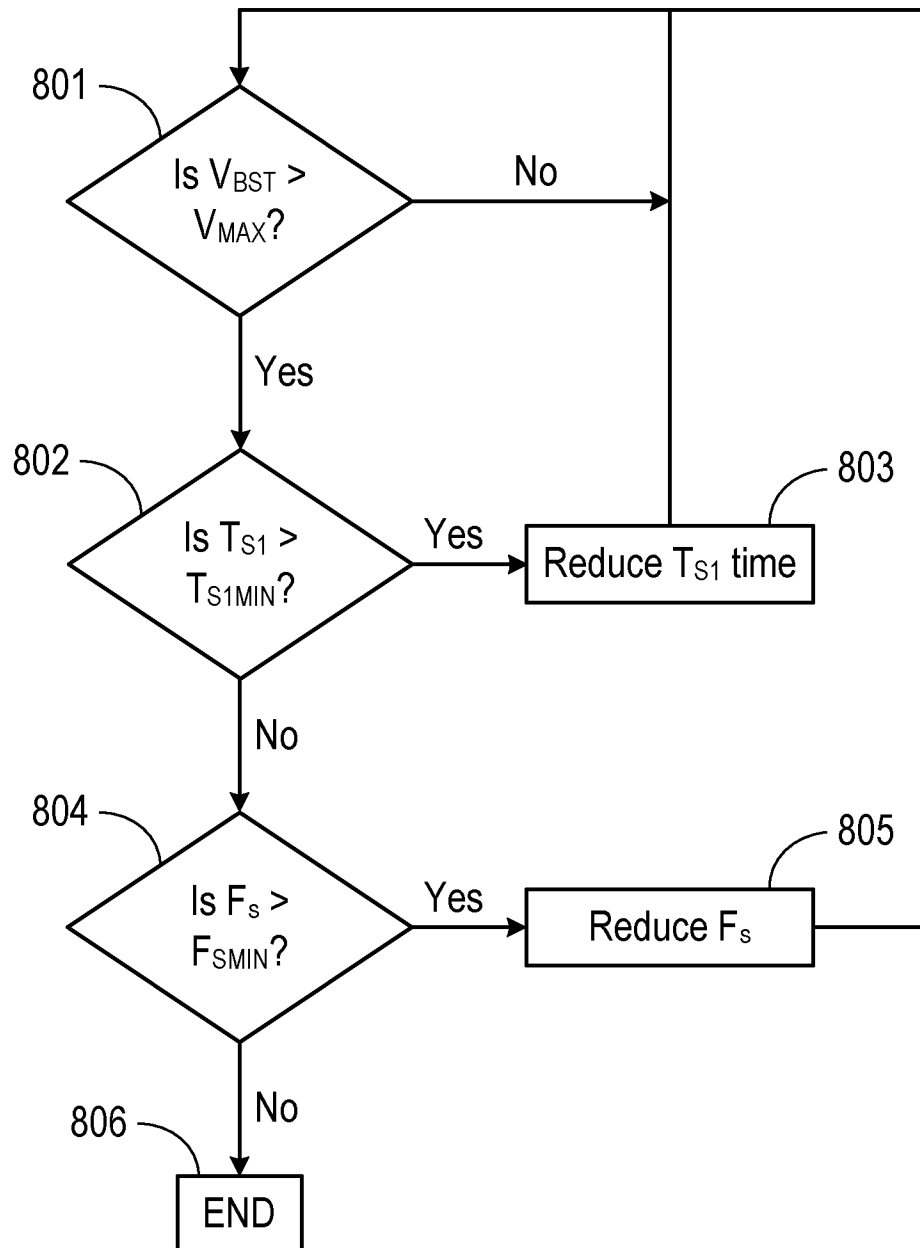


FIG. 8

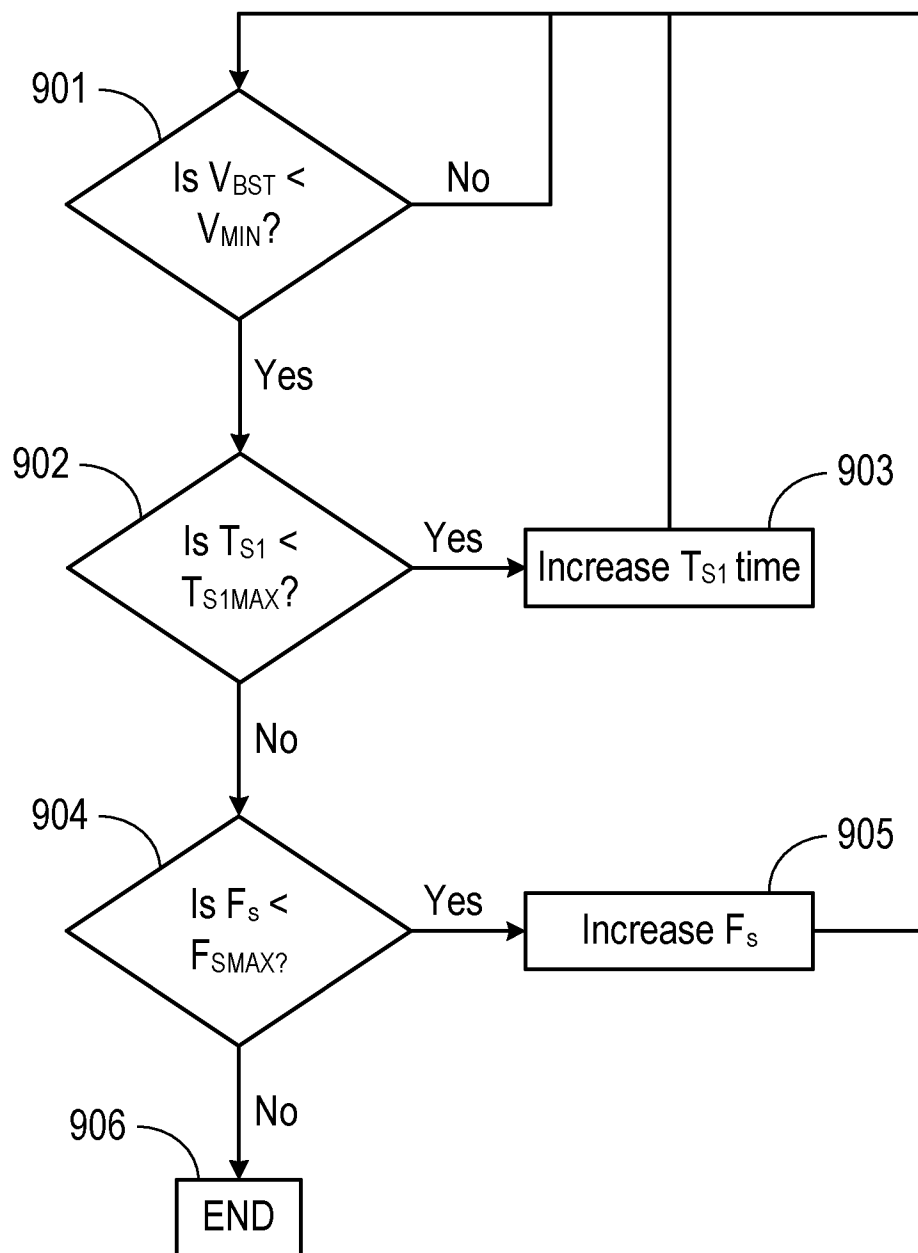


FIG. 9

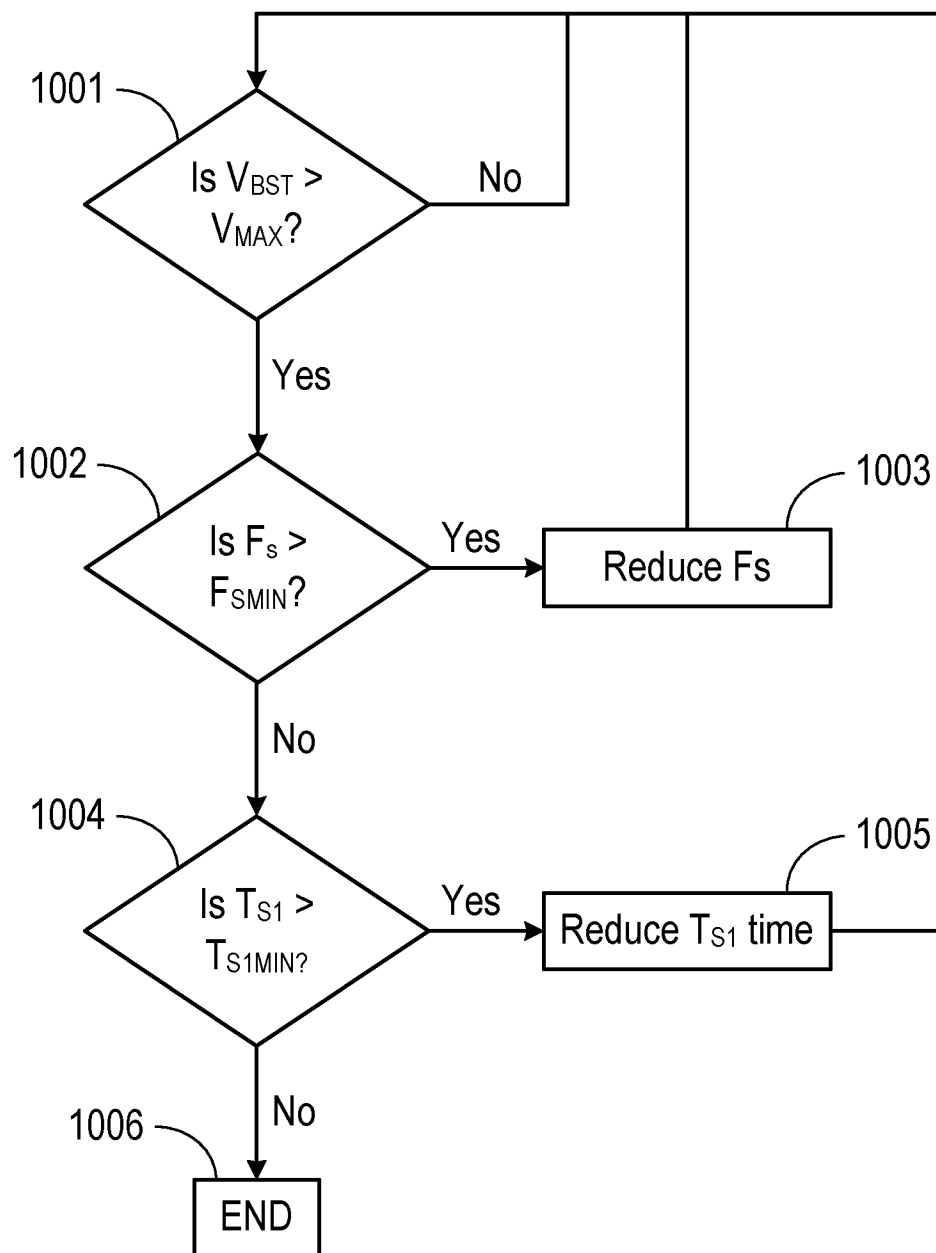


FIG. 10

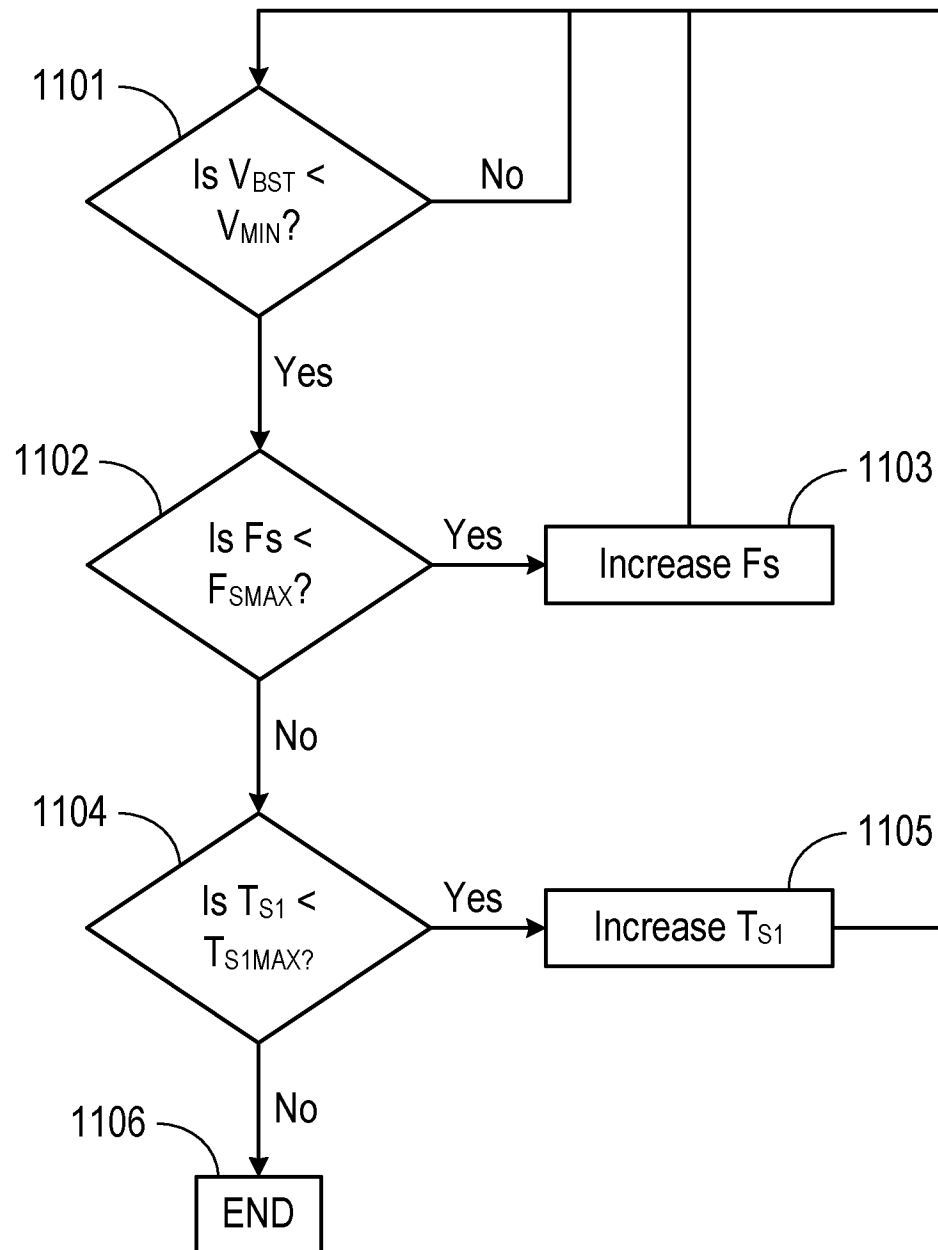


FIG. 11

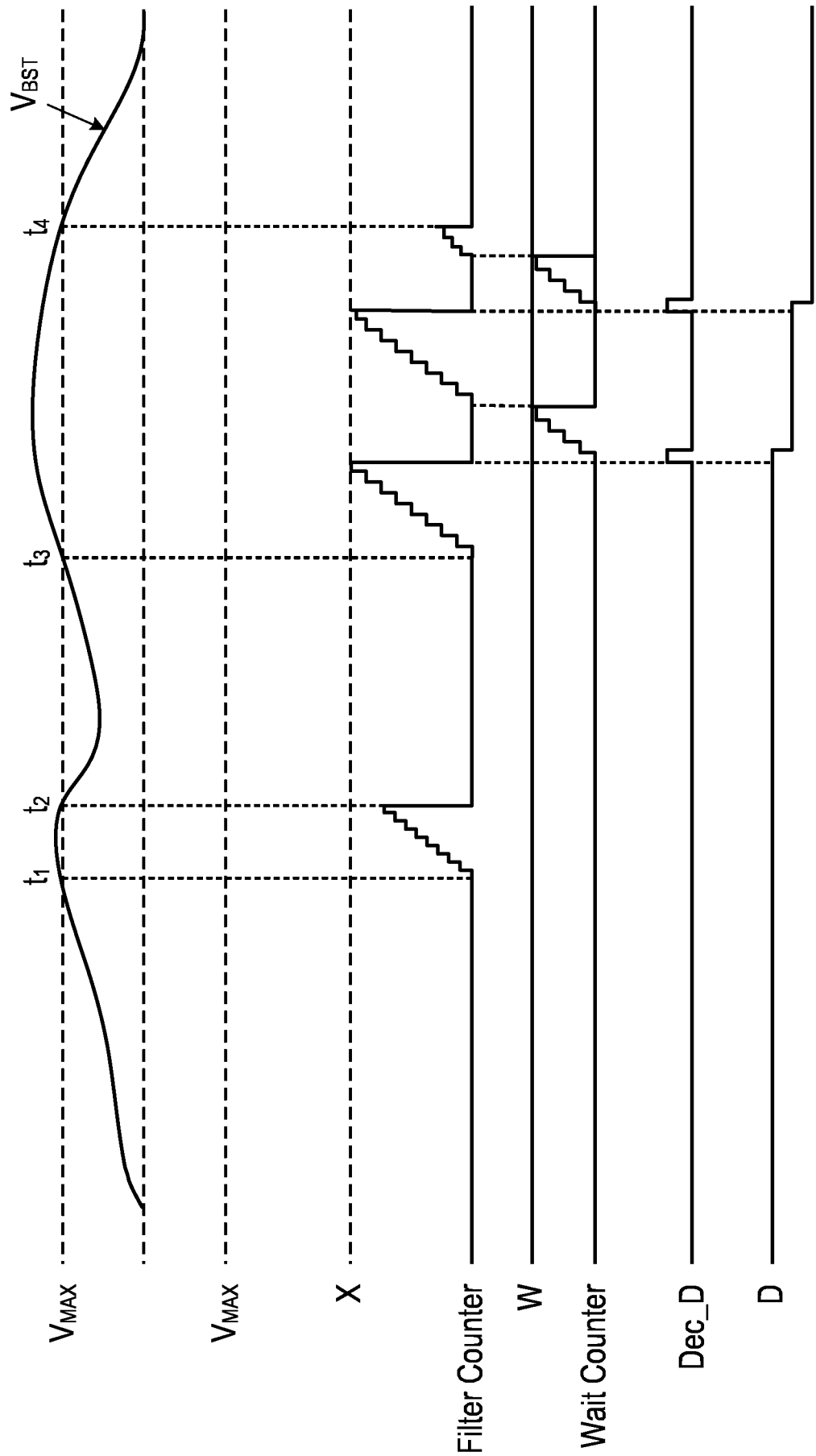


FIG. 12

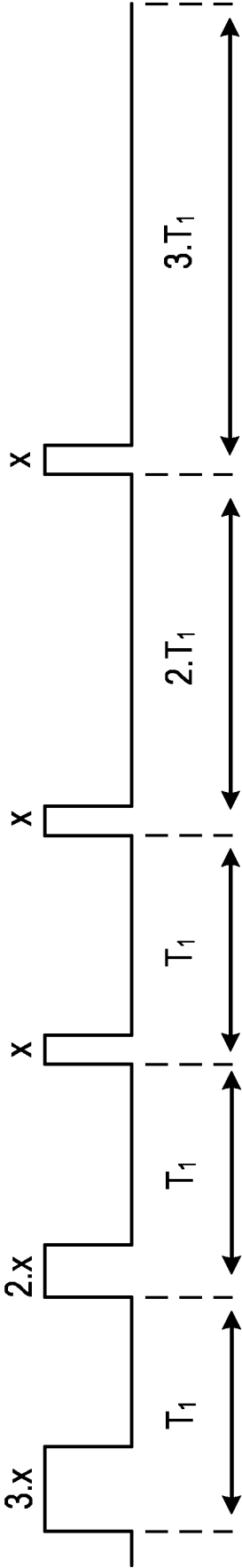


FIG. 13

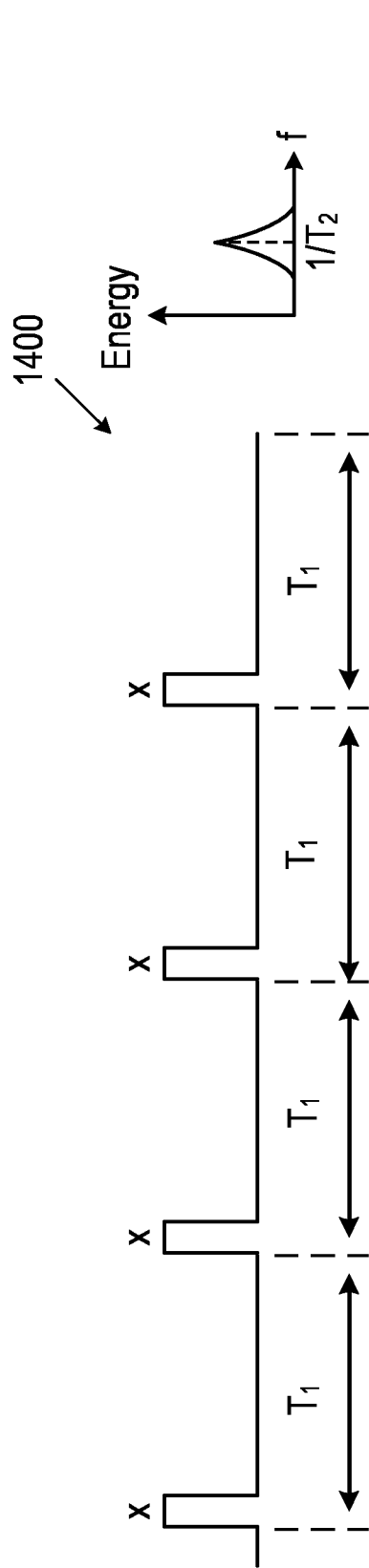


FIG. 14A

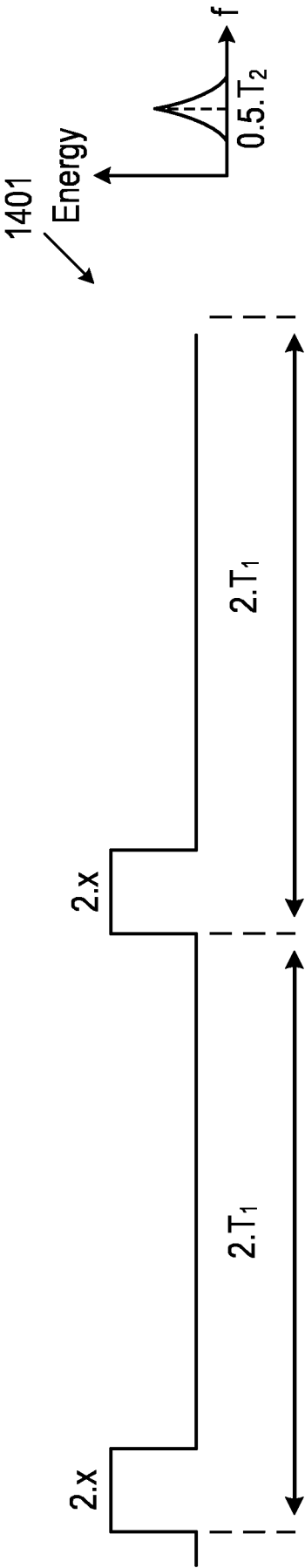


FIG. 14B

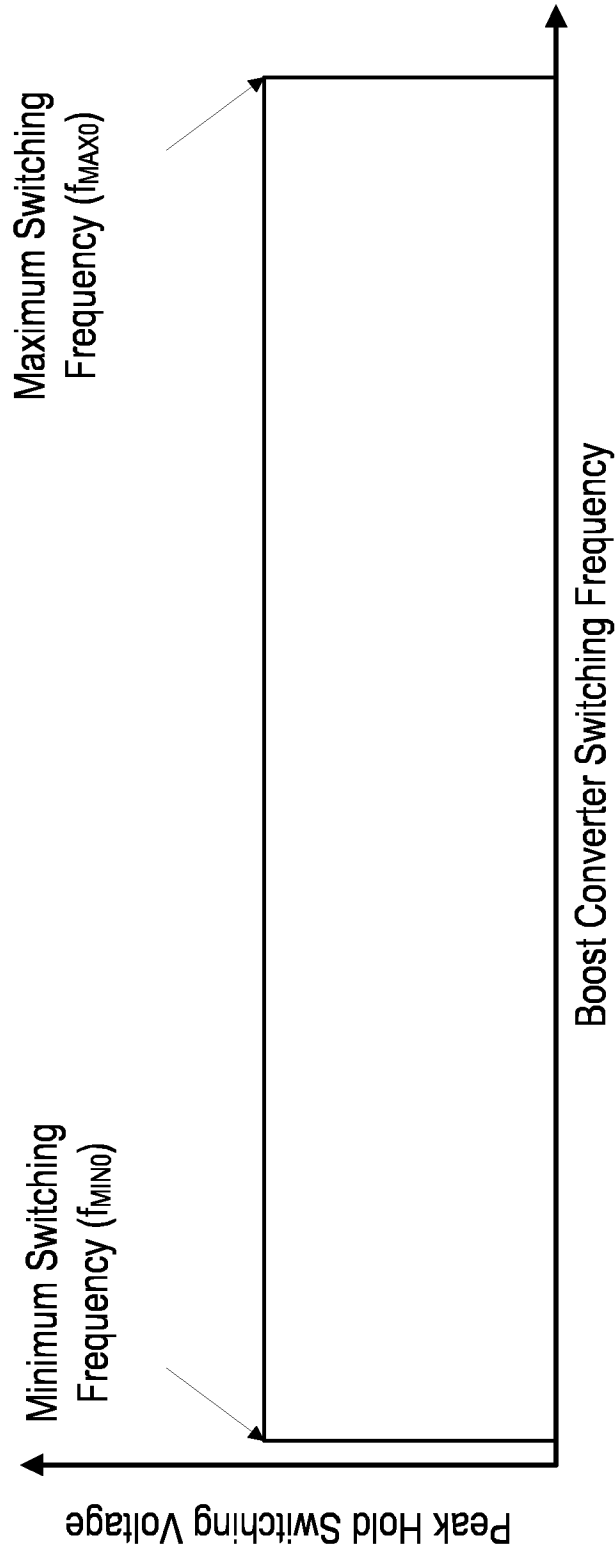


FIG. 15

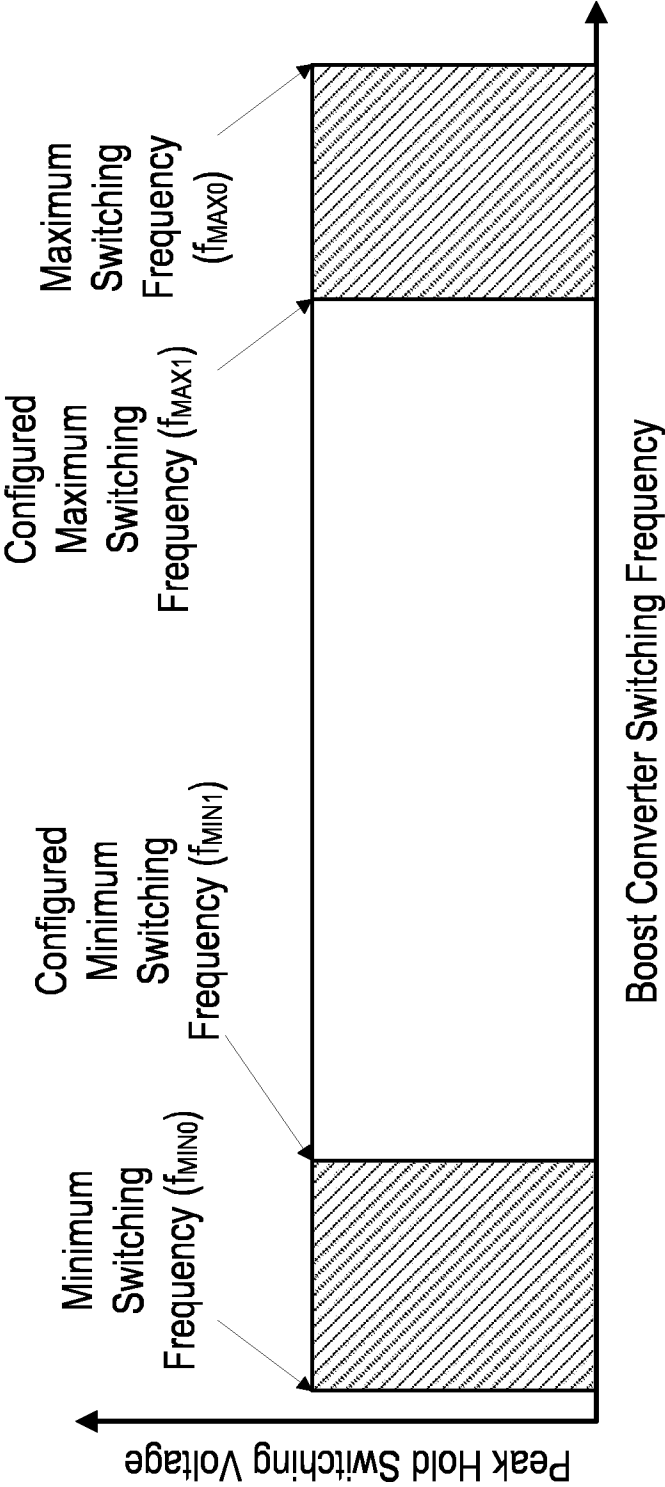


FIG. 16

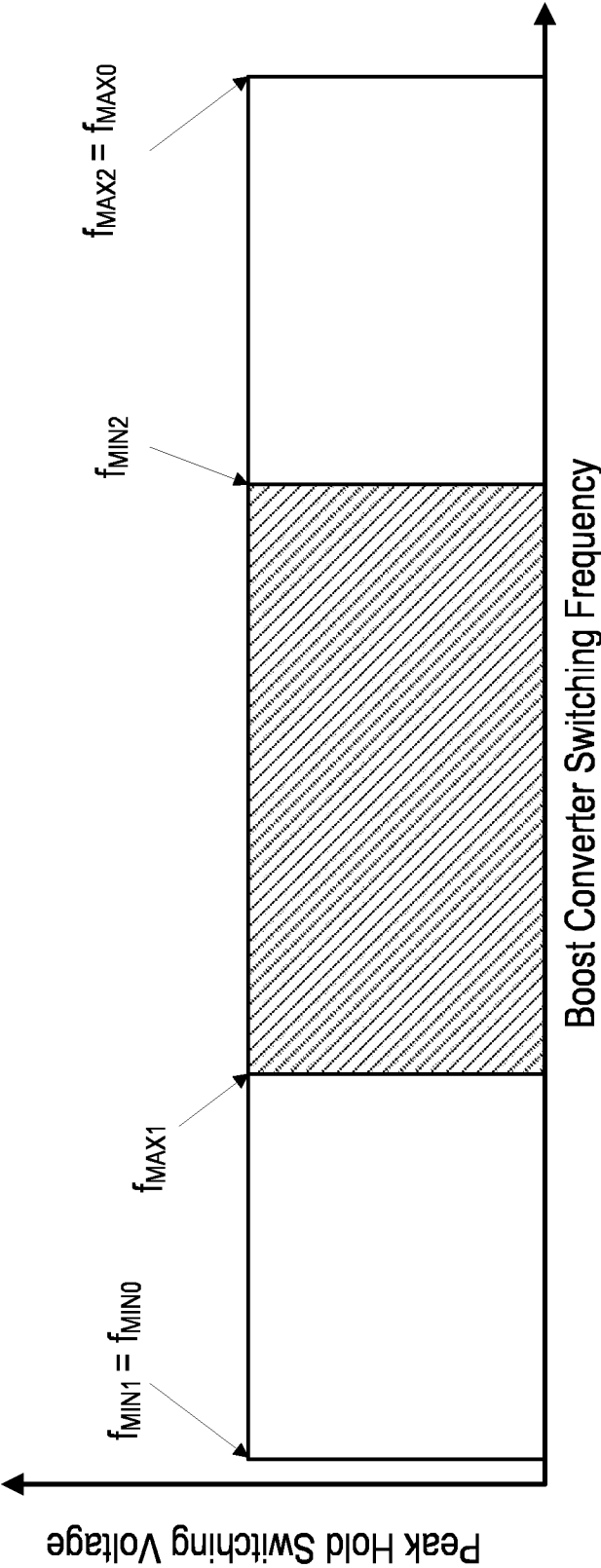


FIG. 17

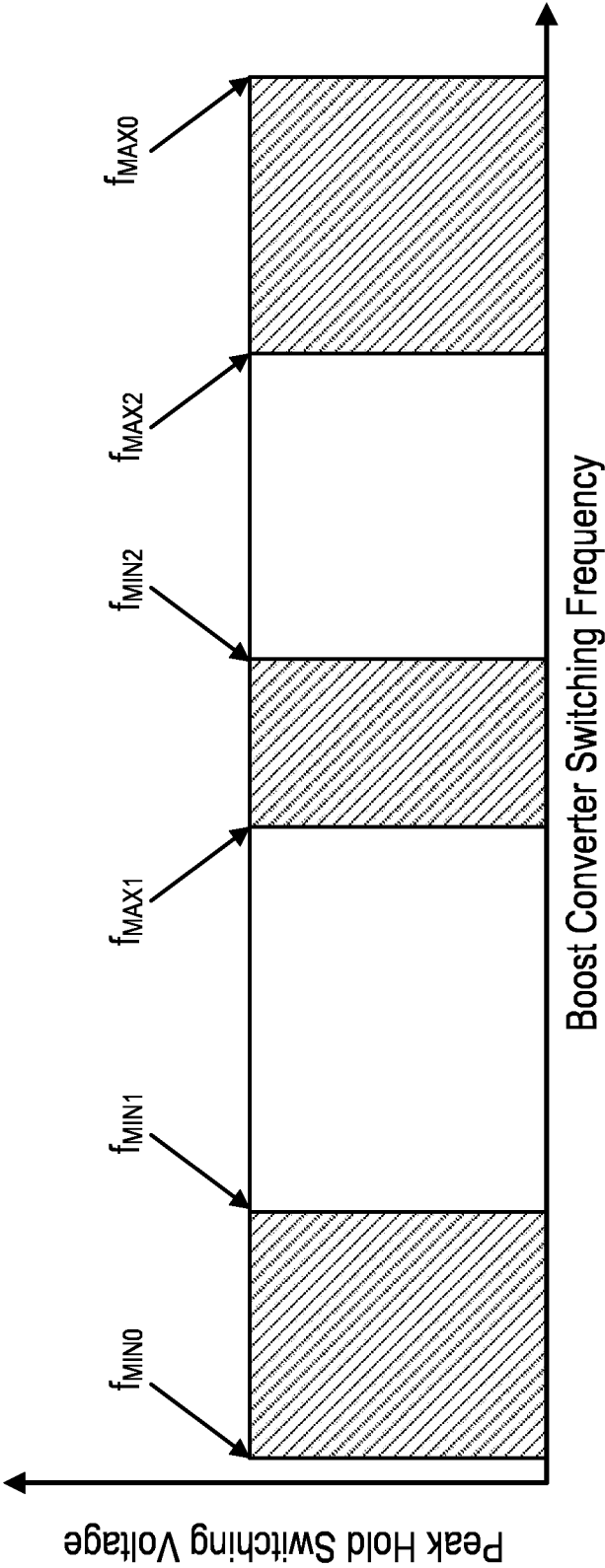


FIG. 18

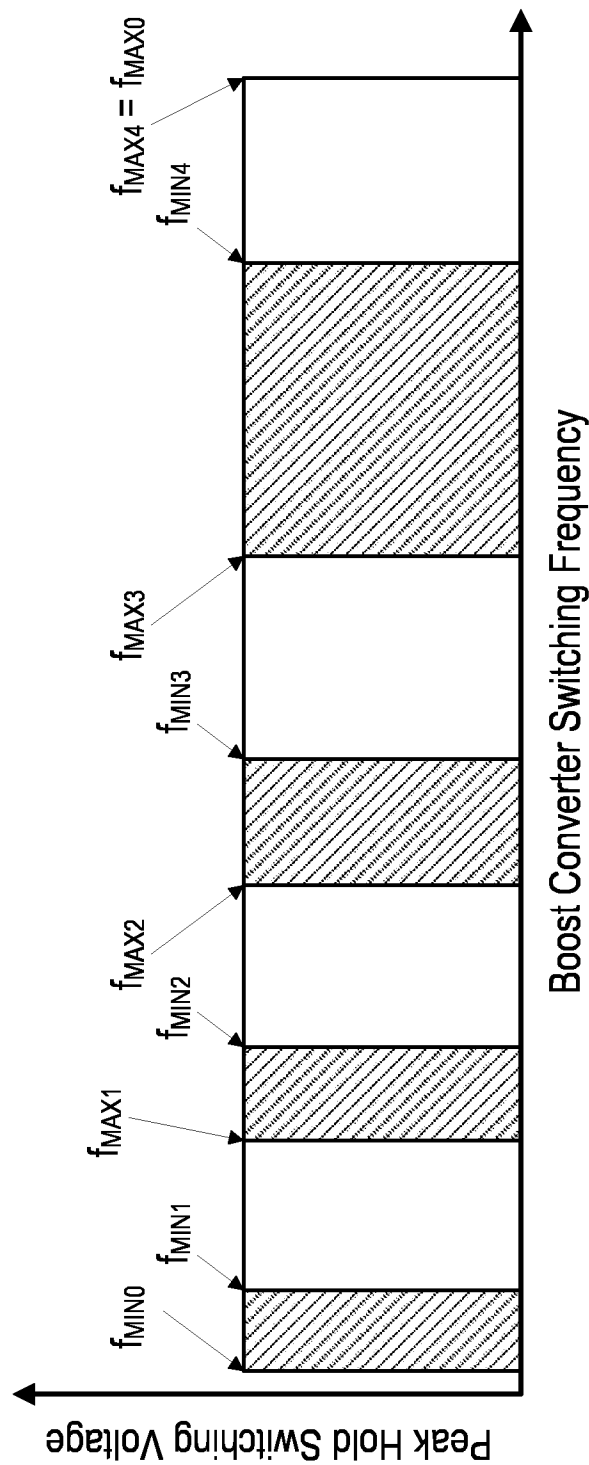


FIG. 19

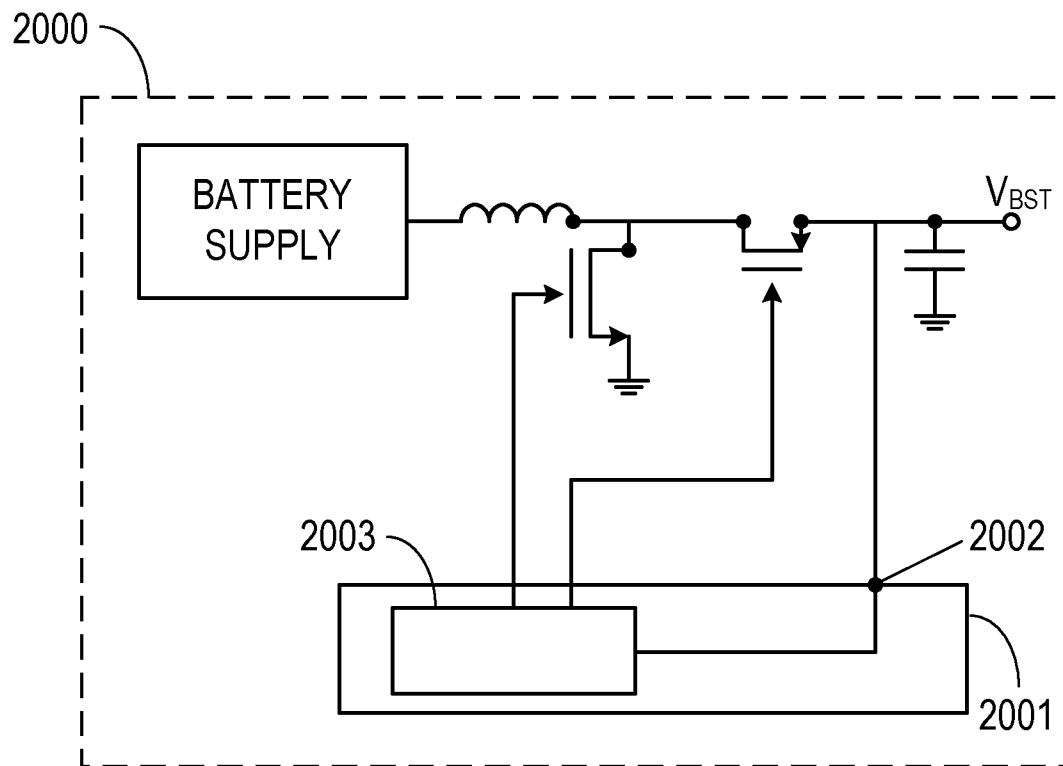


FIG. 20

INTERNATIONAL SEARCH REPORT

International application No

PCT/GB2018/051383

A. CLASSIFICATION OF SUBJECT MATTER
 INV. H02M1/44 H02M3/156
 ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
 H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 6 127 816 A (HIRST B MARK [US]) 3 October 2000 (2000-10-03) column 5, line 3 - line 50; figures 2-4 -----	1-28
Y	US 2014/354257 A1 (PAUL RAJARSHI [US] ET AL) 4 December 2014 (2014-12-04) paragraph [0021]; figures 2,5,6 -----	1-28
A	US 2014/035654 A1 (JIANG LIJIE [CN] ET AL) 6 February 2014 (2014-02-06) abstract; figure 1 -----	1-28
A	US 2015/229211 A1 (WALSH GREGORY [GB] ET AL) 13 August 2015 (2015-08-13) abstract; figures 1,2 -----	1-28



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

22 August 2018

Date of mailing of the international search report

10/09/2018

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Authorized officer

Marannino, M

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/GB2018/051383

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