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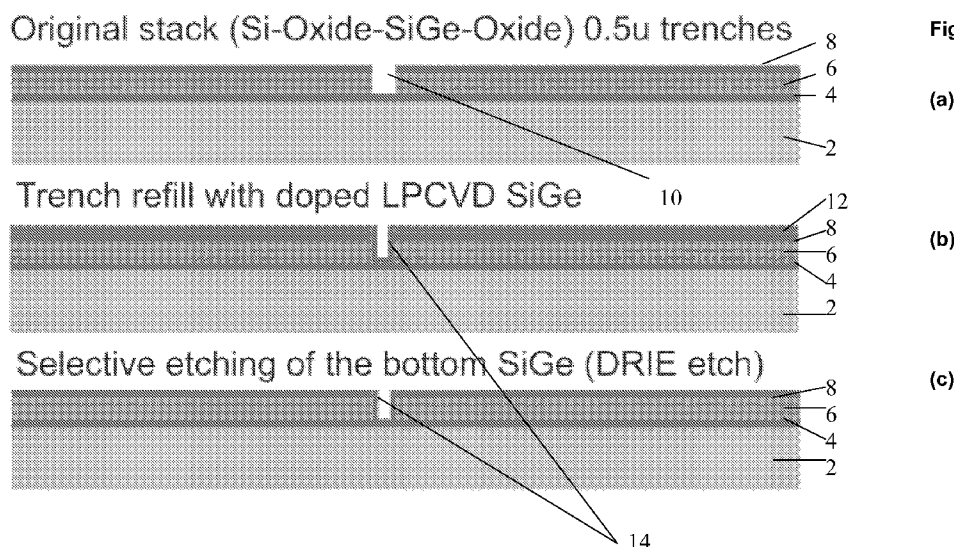


Figure 1

(57) Abstract: A method for forming narrow gaps, for example gaps narrower than 400nm, e.g. less than 200nm or 100 nm, between elements of a MEMS structure is described, as well as a method for forming micromachined or MEMS structures comprising narrow gaps. The method may for example be used for forming high frequency micromechanical resonators comprising narrow transduction gaps.

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METHOD FOR FORMING MEMS STRUCTURES COMPRISING NARROW GAPS

The present invention relates to MEMS technology especially to methods of forming MEMS structures with narrow gaps, e.g. gaps that are less than lithographic dimensions as well as to device having the MEMS structures with narrow gaps.

Background

MEMS resonators are a potential candidate to replace off-chip frequency selective mechanical components such as for example reference crystal devices, local oscillators, or building blocks in frequency selective filters, which may be used in wireless communications systems.

In capacitive MEMS resonators, actuation of a resonating structure is based on electrostatic forces and sensing is based on capacitive detection. Strong electromechanical coupling between the capacitive resonating structure and the electrodes for driving or sensing the small vibrations of such a resonating structure may be obtained by providing a large transduction area and a small transduction gap between the resonating structure and the electrodes, giving rise to a large capacitive area and a low motional resistance. The gap width has the most significant contribution in the motional resistance. For a capacitive resonator, the motional resistance is proportional to g^4 , wherein g is the resonator-electrode transduction gap width. In order to minimize device insertion losses, it would be desirable to create a sub-100 nm transduction gap between the electrodes and the resonating structure.

Providing a narrow transduction gap requires process technologies that can yield 10-100 nanometer capacitive gaps between the resonating structure and the corresponding drive and sense electrodes. A number of methods for forming very narrow gaps have been described, for example methods based on e-beam lithography, methods based on using a thin sacrificial spacer that is etched free at the end of the process to create a narrow gap, methods based on DRIE etching (Deep Reactive Ion Etching) of ultra narrow trenches, etc. These methods generally comprise stringent lithography requirements, a complex process flow and/or complex etching techniques.

In "High Aspect-Ratio Combined Poly and Single-Crystal Silicon (HARPSS) MEMS technology", J. of Microelectromechanical Systems, Vol. 9, No. 3, 2000, F. Ayazi et al. describe a process for forming a MEMS capacitive resonator with narrow gaps. The process is based on etching deep trenches with straight sidewalls in a silicon substrate, forming a sacrificial oxide layer in the trenches and refilling the trenches with polysilicon for creating electrodes. After a deep dry-release step to release thick microstructures from the substrate, the sacrificial oxide layer is removed, thereby forming narrow gaps. The width of the gaps is defined by the thickness of the sacrificial oxide layer and thus can be scaled down to the tens of nanometer range. This process uses different process steps for forming the resonating structure and the electrodes and it is performed at high temperatures (up to 920°C).

In US 2005/0250236 a damascene process is described for defining narrow gaps between a resonating structure and the drive and sense electrodes. The process is based on forming thin blades in a sacrificial material, for example boron-doped poly-Ge. Narrow blades are obtained by first defining 0.5µm minimum width lines by means of lithography, followed by photoresist ashing to reduce the minimum line width to e.g. 50 nm. After transferring the photoresist pattern to the Ge layer and removing the photoresist layer, a poly SiGe structural layer is deposited for forming a resonating structure and the electrodes. The blade is then selectively removed so that a narrow gap remains between the resonating structure and the electrodes. This process allows forming the resonating structure and the drive and sense electrodes in one SiGe deposition step. Furthermore, the process may be performed at temperatures not exceeding 450°C, allowing for post-CMOS processing of resonators. However, the process is rather complex. It requires for example minimization of sidewall taper in the etched Ge structures, there may be adhesion problems for the narrow Ge-blades, and the tall and narrow blades might collapse during further processing.

Summary of the Invention

The present invention relates to a method for forming narrow gaps, for example gaps narrower than 400nm, e.g. less than 200nm or 100 nm, between elements of a MEMS structure, and to a method for forming micromachined or MEMS structures comprising narrow gaps. The method may for example be used for

forming high frequency micromechanical resonators comprising narrow transduction gaps.

An advantage of the present invention is that it provides a simple method for forming narrow gaps, especially a simple method for forming MEMS structures comprising narrow gaps for example gaps narrower than 100 nm, e.g. between elements of a MEMS structure, such as for example narrow transduction gaps between a resonating structure and the corresponding electrodes in a MEMS capacitive resonator. It is an advantage of embodiments of the present invention that there is no need for complex process steps, complex etching techniques or lithography steps with stringent requirements. Embodiments of the present invention simplify considerably the process flow as compared to some prior art methods, because the requirements for lithography and for the DRIE etching aspect ratio are more relaxed, leading to a more economical technology. Embodiments of the method for forming MEMS structures comprising a narrow gap between elements, e.g. between a resonating structure and the corresponding electrodes of a MEMS resonator, allow forming these elements in a single deposition step, leading to a simpler and cheaper process than some prior art solutions. Furthermore, the method may be performed at temperatures below 450°C, thus allowing for post-CMOS processing and integration of e.g. MEMS capacitive resonator structures. It is a further aspect of the present invention to provide a capping method or zero-level packaging method for MEMS structures comprising narrow gaps, the capping method being integrated with the method for forming narrow gaps.

A method for manufacturing a micromachined or MEMS structure comprising at least one narrow gap, e.g. a narrow gap between a first structural element and a second structural element, is provided, the method comprising: depositing a first layer of a structural material on a substrate; forming at least one trench in the first layer of structural material, the at least one trench e.g. being arranged for defining the first structural element and the second structural element; and depositing a second layer, e.g. a second layer of the structural material, for partially refilling and narrowing the at least one trench, thereby forming the at least one narrow gap. A structural material or an element comprising a structural material is one that is left, at least in part, in the final MEMS device, i.e. it is not a sacrificial layer although it can be patterned or partly

removed. The method may comprise forming a dielectric layer on the substrate before depositing the first layer of structural material. Depositing the second layer of structural material may preferentially be done by means of a conformal deposition technique, such as for example LPCVD (Low Pressure Chemical Vapor Deposition).

In a preferred embodiment, the at least one trench may have sidewalls that form a substantially right angle with an average surface plane of the substrate. The at least one trench may extend through the first layer of structural material. The structural material may for example be silicon germanium.

The at least one gap may for example be narrower than 400nm, e.g. less than 200 nm, e.g. narrower than 100 nm.

Depositing the second layer of structural material may comprise depositing a layer of doped silicon germanium, such as for example Boron doped silicon germanium. The method may further comprise removing the second layer of structural material from the bottom of the trench, for example for avoiding short-circuits in the final structure.

The deposition of the second layer can also be done by selectively forming more of the second layer on the at least one trench sidewalls rather than on the bottom of the trench. Such a selective deposition of the second layer can be carried out with a flow of hydrogen. The flow of hydrogen can be between 200 and 1200 sccm, optionally 400 and 1000 sccm.

Alternatively, depositing the second layer of structural material may comprise depositing a layer of undoped silicon germanium. It is an advantage of depositing a layer of undoped silicon germanium that the incubation time for nucleation on a dielectric surface may be sufficiently large for preventing deposition of the second layer of structural material at the bottom of the at least one trench, in case a dielectric material is present at the bottom of the at least one trench. The need for removing the second layer of structural material from the bottom of the trench may thus be avoided. The initially undoped SiGe layer may be doped afterwards, for example for improving the electrical performance of a MEMS device to be formed.

Depositing the second layer of structural material may comprise performing a plurality of alternating deposition steps and etching steps, wherein the deposition steps comprise for example LPCVD deposition of a thin layer of

doped silicon germanium, e.g. Boron doped silicon germanium, and wherein the etching steps comprise for example an RF plasma treatment, e.g. an H₂ RF plasma treatment. It is an advantage of performing a plurality of alternating deposition steps and etching steps that the incubation time for nucleation of the second layer of doped structural material, e.g. doped silicon germanium, on a dielectric surface may be increased and may be sufficiently large for preventing deposition of the second layer of doped structural material at the bottom of the at least one trench, in case a dielectric material is present at the bottom of the at least one trench. The need for removing the second layer of structural material from the bottom of the trench may thus be avoided for doped structural material layers, e.g. doped silicon germanium layers. Alternatively, the need for doping the second layer of structural material after selective deposition may be avoided.

Any method of the present invention may for example be used for forming a resonator structure, wherein the at least one narrow gap is a transduction gap between a resonating element and a corresponding electrode.

Any method of the present invention may be performed at temperatures not exceeding 450°C. The substrate may comprise an integrated circuit, for example a CMOS circuit.

Furthermore a method is provided for forming a sealed cap or zero-level package over a micromachined or MEMS structure comprising narrow gaps, the method for forming a sealed cap being integrated with the method for forming the MEMS structure. Forming a sealed cap over the MEMS structure may comprise, after forming the at least one trench and before depositing the second layer of structural material, depositing a sacrificial layer; depositing a cap layer over the sacrificial layer; and forming a plurality of openings in the cap layer, the width of the plurality of openings being smaller than the width of the at least one trench. The cap layer may comprise the structural material, e.g. silicon germanium. After forming the plurality of openings in the cap layer, the underlying MEMS structure may be released, at the same time removing the sacrificial layer. Then a second layer of undoped structural material may be deposited or a second layer of doped structural material may be deposited by alternating deposition steps and etching steps, thereby refilling and narrowing the at least one trench and closing the plurality of openings in the cap layer. It is an advantage of the method for forming a sealed cap that refilling and narrowing the at least one trench and

closing the plurality of openings in the cap layer may be performed in a single process step. The remaining gap width may thus be defined by the difference between the initial trench width and the width of the openings in the cap layer, and can thus be accurately controlled by this self-limiting process.

5 The invention, both as to organization and method of operation, together with features and advantages thereof, may best be understood by reference to the following detailed description when read with the accompanying drawings.

Brief Description of the Drawings

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Figure 1 illustrates a process flow for forming narrow gaps, wherein trenches are partially refilled with doped SiGe.

Figure 2 is a SEM photograph showing a silicon substrate with a silicon oxide / structural SiGe layer / silicon oxide stack, wherein trenches are formed through

15 the top oxide layer and the SiGe layer.

Figure 3 illustrates a process flow for forming narrow gaps, wherein trenches are partially refilled with undoped SiGe.

Figure 4 shows experimental results of the selective deposition of doped SiGe layers, for different SiGe deposition times and with a 120 s H₂ plasma treatment
20 in between the SiGe deposition steps.

Figure 5 shows experimental results of the selective deposition of doped SiGe layers, for five 200 s SiGe deposition steps and for different H₂ plasma treatment times in between the deposition steps.

Figure 6 is a SEM photograph showing a structure after trench refilling with
25 doped LPCVD SiGe.

Figure 7 is a SEM photograph showing the top part of a structure after trench refilling with doped LPCVD SiGe.

Figure 8 is a SEM photograph showing the bottom part of a structure after trench refilling with doped LPCVD SiGe.

30 Figure 9 is a SEM photograph showing a structure after trench refilling with doped LPCVD SiGe and after a single DRIE passivation/etch cycle, wherein the duration of the passivation step is 5s.

Figure 10 is a SEM photograph showing the top part of a structure after trench refilling with doped LPCVD SiGe and after a single DRIE passivation/etch cycle,

wherein the duration of the passivation step is 5s.

Figure 11 is a SEM photograph showing the bottom part of a structure after trench refilling with doped LPCVD SiGe and after a single DRIE passivation/etch cycle, wherein the duration of the passivation step is 5s.

- 5 Figure 12 is a SEM photograph showing a structure after trench refilling with doped LPCVD SiGe and after a single DRIE passivation/etch cycle, wherein the duration of the passivation step is 6s.

- Figure 13 is a SEM photograph showing the top part of a structure after trench refilling with doped LPCVD SiGe and after a single DRIE passivation/etch cycle,
10 wherein the duration of the passivation step is 6s.

Figure 14 is a SEM photograph showing the bottom part of a structure after trench refilling with doped LPCVD SiGe and after a single DRIE passivation/etch cycle, wherein the duration of the passivation step is 6s.

- Figure 15 illustrates a process flow for forming and capping a MEMS resonator,
15 wherein sealing of openings in the cap layer and refilling of the trenches for forming narrow gaps between the underlying resonating structure and the resonator electrodes are performed in a single process step.

Figure 16 illustrates the deposition selectivity modulated by H₂ flow in accordance with an embodiment of the present invention.

- 20 Figure 17 illustrates optimisation of the deposition selectivity by modulating H₂ flow in accordance with an embodiment of the present invention. For each line the higher one (bigger thickness) of a pair is always the deposition on the SiGe substrate.

25 Detailed Description of the illustrative embodiments

- In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the invention and how it may be practiced in particular embodiments. However it will be understood that the present invention may be practiced without these specific details. In other
30 instances, well-known methods, procedures and techniques have not been described in detail, so as not to obscure the present invention. While the present invention will be described with respect to particular embodiments and with reference to certain drawings, the reference is not limited hereto. The drawings included and described herein are schematic and are not limiting the scope of

the invention. It is also noted that in the drawings, the size of some elements may be exaggerated and, therefore, not drawn to scale for illustrative purposes.

Furthermore, the terms first, second and the like in the description are used for distinguishing between similar elements and not necessarily for
5 describing a sequence, either temporally, spatially, in ranking or in any other manner. It is to be understood that the terms so used are interchangeable under appropriate circumstances and that the embodiments of the invention described herein are capable of operation in other sequences than described or illustrated herein.

10 Moreover, the terms top, bottom, over, under and the like in the description are used for descriptive purposes and not necessarily for describing relative positions. It is to be understood that the terms so used are interchangeable under appropriate circumstances and that the embodiments of the invention described herein are capable of operation in other orientations than
15 described or illustrated herein.

It is to be noticed that the term "comprising" should not be interpreted as being restricted to the means listed thereafter; it does not exclude other elements or steps. It is thus to be interpreted as specifying the presence of the stated features, integers, steps or components as referred to, but does not preclude the
20 presence or addition of one or more other features, integers, steps or components, or groups thereof. Thus, the scope of the expression "a device comprising means A and B" should not be limited to devices consisting only of components A and B.

The invention will now be described by a detailed description of several
25 embodiments. It is clear that other embodiments of the invention can be configured according to the knowledge of persons skilled in the art without departing from the true spirit or technical teaching of the invention.

The term "substrate" may include any underlying material or materials that may be used, or upon which a device in accordance as described herein may be
30 formed. The substrate may for example include a semiconductor substrate such as e.g. doped silicon, a gallium arsenide (GaAs), a gallium arsenide phosphide (GaAsP), an indium phosphide (InP), a germanium (Ge), or a silicon germanium (SiGe) substrate. The substrate may include for example an insulating layer such as a SiO₂ or a Si₃N₄ layer in addition to a semiconductor substrate portion. The

substrate may comprise electrical circuitry, e.g. at least one transistor, e.g. CMOS transistor. The term "substrate" is thus used to define generally the elements for layers that underlie a layer or portions of interest. Also, the substrate may be any other base on which a layer is formed, for example a glass or metal layer.

In the following, the detailed description relates to a method for forming MEMS capacitive resonators comprising narrow gaps between a resonating structure and the corresponding electrodes. However, the present invention is not limited thereto, and more generally relates to a method for forming micromachined or MEMS structures comprising narrow gaps and to a method for forming narrow gaps between elements, e.g. structural elements, of a structure, e.g. MEMS structure. The description below is given for SiGe-based MEMS structures. However, other materials may be used for forming the MEMS structures.

The method for forming MEMS structures comprising narrow gaps, e.g. narrow gaps between a resonating structure and the corresponding electrodes, is based on first forming a structure comprising relatively wide trenches (e.g. trenches with a width in the range between 250 nm and 2 μ m) followed by partially refilling the trenches, thereby narrowing the trenches and defining narrow gaps (e.g. less than 400nm, e.g. less than 200 nm wide gaps, e.g. less than 100 nm wide gaps).

A process for forming a micromachined structure comprising narrow gaps is illustrated in Figure 1. In the embodiment shown, a silicon wafer is used as a substrate 2, the wafer being covered by a first silicon oxide layer 4. However, other substrates may be used, depending on the application, and other dielectric materials may be used for forming a layer 4 on the substrate 2. The dielectric layer 4 may be applied on the substrate by means of any suitable technique known by a person skilled in the art. Its thickness may for example be in the range between 100 nm and several micrometers. On the first dielectric layer 4 a structural layer 6, e.g. a SiGe layer, is deposited using a technique known by a person skilled in the art, such as for example a PECVD (Plasma Enhanced Chemical Vapor Deposition), PACVD (Plasma Assisted Chemical Vapor Deposition) or LPCVD (Low Pressure Chemical Deposition) technique. The appropriate thickness of the SiGe layer 6 depends on the specific application.

For example, for application in a resonator structure, the thickness of the SiGe layer 6 may e.g. be in the range between a few μm and several tens of μm . After SiGe deposition, a hard mask layer 8 is deposited on top of the structural SiGe layer. The hard mask layer 8 may e.g. be a second silicon oxide layer or any
5 other suitable layer known by a person skilled in the art such as for example a silicon nitride layer. This layer 8 acts as a sacrificial hard mask layer for selective etching, e.g. DRIE etching, of a SiGe layer in a subsequent process step, as described below. The thickness and the properties of the hard mask layer 8 may be selected as a function of the duration of the SiGe etching step (a.o. related to
10 the thickness of the SiGe layer 4) and as a function of the final release step. Alternatively a resist layer may be used as a mask for the structural layer etch.

In a next step, relatively wide trenches 10, for example trenches with a width in the range between 250 nm and 2 μm , e.g. depending on the lithographic tools available and/or used, are etched through the hard mask layer 8, e.g. the
15 second silicon oxide layer 8, and through the structural layer 6, e.g. structural SiGe layer (see Fig. 1a). Etching of these trenches may be done for example by means of DRIE or other anisotropic techniques such as for example ion milling. Figure 2 is a SEM photograph of a structure at this stage of the process, wherein the first silicon oxide layer has a thickness of 1 μm , the thickness of the structural
20 SiGe layer is 4 μm and the thickness of the second silicon oxide layer is 1.1 μm . The width of the trenches in Figure 2 is 1.5 μm . A small indicator at the bottom (37.6 nm), indicates the amount of overetch in the oxide at the trench bottom, which in an ideal case would be zero.

Narrow gaps 14 may then be obtained by partially refilling the trenches 10
25 with a layer 12, e.g. a SiGe layer, by means of a conformal deposition technique, such as for example an LPCVD technique. The deposition may for example be performed at a temperature of 450°C or at a temperature lower than 450°C. The thickness of the layer 12 for partially refilling the trench may be determined based on the initial trench width and on the gap width to be obtained. Materials
30 other than SiGe may be used for refilling the trenches. For resonator applications a layer with substantially the same mechanical properties as the structural layer may be preferred for refilling the trenches.

As illustrated in Figure 1b, partial trench refilling may be done with a doped SiGe layer 12, e.g. a B-doped SiGe layer. The SiGe layer 12 may grow

both on the trench sidewalls and on the silicon oxide surfaces (i.e. at the bottom of the trench and on the hard mask layer) although selective disposition only on the sidewalls is preferred. The bottom SiGe layer (i.e. the SiGe layer deposited at the bottom of the trench during trench refilling) then is removed to avoid short-circuits in the final structures (Fig. 1c). Anisotropic etching techniques suitable for etching straight trenches may be used for removing the bottom SiGe layer, such as for example pure physical processes (e.g. ion milling) or chemically assisted processes (e.g. DRIE etching). In a preferred embodiment the bottom SiGe layer may be removed with a Bosch-type DRIE (Deep Reactive Ion Etching) technique. This is a chemically assisted anisotropic etching technique that alternates repeatedly between a passivation step and an etch step. During a passivation step, a passivation layer or protective layer is grown, protecting the entire structure from chemical attack. The protective layer may be thicker on vertical walls than on horizontal planes, due to the nature of the electrical fields in the DRIE etcher. During the etch step, a gas or gas mixture is used that etches the layer used for partially refilling the trenches, e.g. SiGe layer. Part of this layer may be removed from the horizontal surfaces, e.g. from the trench bottom, while the passivation layer still remains on the vertical surfaces, e.g. the trench sidewalls, and protects these surfaces. The passivation/etch steps are repeated many times, resulting in a large number of very small etch steps taking place mainly at the bottom of the trenches. The passivation steps and the etching steps may be alternated in such a way as to get a profile that has substantially straight sidewalls (i.e. a profile wherein the sidewalls form a substantially straight angle with an average surface plane of the wafer).

In an alternative process flow, illustrated in Figure 3, the trenches may be partially refilled with undoped SiGe (Fig. 3b). It is an advantage of using undoped SiGe that it deposits selectively on conductive layers but not on oxides, because of a substantial incubation time on oxides, as e.g. described in "Effects of SiH_4 , GeH_4 and B_2H_6 on the Nucleation and Deposition of Polycrystalline $\text{Si}_{1-x}\text{Ge}_x$ Films", J. Electrochem. Soc., Vol. 141, No. 9, September 1994. By varying the Ge concentration in the undoped SiGe layer, the incubation time on the oxide may be influenced. Using this approach, there may be only SiGe deposition on the sidewalls of the trench and not at the bottom, thus avoiding the need for removing a bottom SiGe layer as in the process flow of Figure 1. The initially

undoped SiGe layer may be doped afterwards, for example for optimizing the electrical performance of the MEMS device. This doping may for example be done by means of a sinter step, giving rise to diffusion of dopants out of the first layer of structural material.

5 In another alternative process flow, the trenches may be partially refilled with doped SiGe with good deposition selectivity, i.e. with an incubation time that is substantially larger on dielectric layers than on conductive layers. The process for selective deposition of a doped SiGe layer comprises performing a plurality of alternating deposition steps and etching steps, wherein the deposition steps may
10 comprise for example LPCVD deposition of a thin layer of doped silicon germanium, e.g. Boron doped silicon germanium, and wherein the etching steps may comprise for example an RF plasma treatment, e.g. an H₂ RF plasma treatment. On dielectric layers, e.g. oxide layers, there is a need for a seed layer enabling the growth of an LPVCD SiGe layer. The RF plasma treatment steps
15 between the deposition steps may alter the seed layer formed on a dielectric layer, e.g. the oxide layer at the bottom of the trenches, in such a way that it prolongs the incubation time for nucleation on a dielectric layer and hence increases the selectivity of deposition on a conductive layer versus a dielectric layer. This deposition selectivity may be sufficiently large for preventing
20 deposition of doped SiGe at the bottom of the trenches, in case a dielectric material is present at the bottom of the trenches. By repeating the deposition-etch sequence the thickness of the doped SiGe layer can be increased to the desired thickness, whereas there is no or little deposition on the dielectric layer. Using this approach, there may be doped SiGe deposition only on the sidewalls
25 of the trench and not at the bottom, thus avoiding the need for removing a bottom doped silicon germanium layer or avoiding the need for doping a SiGe layer after selective deposition of undoped SiGe. If needed a short blanket etch can be performed to remove any seed deposition on the dielectric layer at the bottom of the trench.

30 This method of selective deposition by performing alternating deposition and etching steps can be used for other applications, for example for forming a diffraction pattern or diffraction grating on a SiGe layer. Such a diffraction grating may comprise elevated features such as for example lines. These elevated features may be formed by selective SiGe deposition. First a dielectric layer may

be deposited on the SiGe layer. This dielectric layer is then patterned, thereby selectively removing the dielectric layer in the regions where additional SiGe is to be deposited for forming the elevated features. Patterning the dielectric layer may be done by using methods known by a person skilled in the art, for example
5 by means of a litho step followed by dry or wet etching of the dielectric layer. In a next step a layer of doped SiGe may be deposited selectively. By tuning the successive deposition and etch steps of the selective SiGe deposition process as described above, deposition of SiGe only on the exposed SiGe surface may be obtained and deposition on the dielectric layer may be prevented. In this way a
10 patterned SiGe layer can be deposited with a well controlled thickness, thereby forming a structure comprising raised areas forming the elevated features where the dielectric layer has been removed and comprising recessed areas where the dielectric layer is present. An additional advantage of this method for forming a diffraction grating is that both surfaces (i.e. the surface in the raised areas and
15 the surface in the recessed areas) of the grating can be polished to obtain high reflectivity. A first polishing step can be done before forming the grating to smoothen the surface in the recessed areas of the grating. A second polishing step can be done after grating formation to smoothen the surface in the raised areas of the grating.

20 Experiments utilising the selective deposition of doped SiGe layers have been carried out. The alternating SiGe deposition steps and etching steps were performed at 420°C on an Applied Materials Centura PECVD platform, on wafers with a SiGe top layer and on wafers with an oxide top layer. After wafer temperature stabilization, a first LPCVD deposition of B-doped SiGe was done at
25 a pressure of 4 Torr, with 15 sccm SiH₄, 166 sccm GeH₄ (10% in H₂) and 40 sccm B₂H₆ (1% in H₂). The deposition time was 50 seconds. After this first LPCVD deposition step, an H₂ RF plasma treatment was done for 120 seconds with an RF power of 50 W. Next the deposition step and the plasma treatment were repeated with the same process conditions as above. In total five SiGe
30 deposition steps and four plasma treatment steps were done. The same experiment was repeated for longer SiGe deposition times (5 x 100 seconds, 5 x 150 seconds and 5 x 200 seconds). The results of these experiments are shown in Figure 4 for deposition on an oxide layer (♦) and for deposition on a SiGe layer (■). From these results it can be concluded that the thickness of the B-doped

SiGe layer on a SiGe layer is substantially larger than the thickness of the B-doped SiGe layer on an oxide layer. The difference in thickness is about 140 nm for a 5 x 100 seconds SiGe deposition, about 255 nm for a 5 x 150 seconds SiGe deposition and about 266 nm for a 5 x 200 seconds SiGe deposition. This difference is substantially higher as compared with a B doped SiGe deposition without intermediate plasma treatment steps: it was shown that in this case the difference in thickness between a B-doped SiGe layer grown on a SiGe layer and a B-doped SiGe layer grown on an oxide layer is about 80 nm.

In a second set of experiments, the effect of the duration of the H₂ plasma treatment steps was investigated. After wafer temperature stabilization, a first LPCVD deposition of B-doped SiGe was done at a pressure of 4 Torr, with 15 sccm SiH₄, 166 sccm GeH₄ (10% in H₂) and 40 sccm B₂H₆ (1% in H₂). The deposition time was 200 seconds. After this first LPCVD deposition step, an H₂ RF plasma treatment was done for 60 seconds with an RF power of 50 W. Next the deposition step and the plasma treatment were repeated with the same process conditions. In total five SiGe deposition steps and four plasma treatment steps were done. The same experiment was repeated with longer H₂ plasma treatment times (4 x 120 seconds and 4 x 180 seconds). From the results shown in Figure 5 (for deposition on an oxide layer (♦) and for deposition on a SiGe layer (■)) it can be concluded that longer plasma treatment times result in less deposition on an oxide layer. The selectivity, i.e. the difference in thickness of the B-doped SiGe layer on an underlying SiGe layer versus an underlying oxide layer slightly increases with increasing plasma treatment time: from about 180 nm for 4 x 60 seconds plasma treatment to about 280 nm for 4 x 180 seconds plasma treatment.

Trench refilling experiments have been done. Figure 6 shows a SEM photograph of a structure after partial refilling of the trenches with a boron-doped SiGe layer using the non-selective approach (without H₂ plasma treatments). The trench refilling was performed by depositing an LPCVD SiGe layer at 450°C for 420 seconds, with 15 sccm SiH₄, 166 sccm GeH₄, and 40 sccm B₂H₆. As can be seen in Figure 6, good sidewall coverage is obtained, so that the thickness of the layer deposited on the sidewalls has a good uniformity along the height of the sidewall. From Figure 6 it can furthermore be concluded that SiGe is also deposited on the oxide layers, e.g. at the bottom of the trenches. Figure 7 and

Figure 8 show respectively the top part and the bottom part of the structure of Figure 6. Figures 7 and 8 show that the layer deposited on the top surface (thickness ~ 170 nm) is somewhat thicker than the layer deposited on the trench bottom (thickness ~ 130-150 nm). This difference in thickness between the layer deposited on the top surface and the layer deposited at the trench bottom is not a problem for the process, because the etching steps can be tuned to make sure that both top and bottom layers are removed in a subsequent step. In the example shown, the thickness of the layer on the sidewalls is about 150 to 160 nm.

Two sets of experiments have been done related to removing the SiGe layer from horizontal surfaces (e.g. the top surface and the trench bottom) by means of DRIE etching. Only one passivation/etch cycle was performed. In the first experiment (Figures 9-11) the passivation time was 5 seconds, and for the second experiment (Figure 12-14) a passivation time of 6 seconds was used.

The difference in passivation time effectively corresponds to a difference in the thickness of the protective layer on the trench sidewalls. The etch time was 7 seconds in both cases.

Figure 9, Figure 10 and Figure 11 are SEM photographs showing respectively the whole trench, the top region of the trench and the bottom region of the trench for the first experiment (with 5 seconds passivation). Comparing the thickness of the SiGe layer in these figures with the thickness before etching (Figures 6-8), it may be concluded that for the DRIE etch parameters used, about 40nm of SiGe has been removed from the sidewalls and about 80 nm of SiGe has been removed from the top layer and from the bottom layer. In the example shown, the final trench width achieved is about 206 nm.

Figure 12, Figure 13 and Figure 14 are SEM photographs showing respectively the whole trench, the top region of the trench and the bottom region of the trench for the second experiment (with 6 seconds passivation). It can be seen that in this case almost no material is removed from the sidewalls, and about 60 nm of SiGe is removed from the top layer and from the bottom layer. In the example shown, the final trench width achieved is about 170 nm.

From these two experiments it can be concluded that the parameters used for the DRIE etching have a significant impact on the difference in etch rate on vertical and horizontal planes, and thus on the final trench width. It can

furthermore be concluded that it is an advantage to use longer passivation times, to form a better protection of the sidewalls. The passivation/etch cycles may be repeated a number of times, until the SiGe layer at the bottom of the trench is completely removed.

5 According to other embodiments of the present invention an alternative method of selective deposition is to add hydrogen during deposition, e.g. adding H₂ to doped SiGe such as boron doped SiGe. The effect of H₂ on the incubation time of the deposition of CVD SiGe has not been previously documented. Tests on thick PECVD SiGe deposition indicated that adding H₂ to the process
10 improved the within-wafer thickness uniformity. When the effect of adding H₂ on the CVD SiGe process was evaluated there was no measurable deposition on thermal oxide after 300secs (no added weight). Adding H₂ during CVD SiGe deposition the deposited layer was thicker on SiGe than on thermal oxide. Tests have been carried out in a CVD chamber at 480°C, spacing 500mils, pressure
15 4Torr, SiH₄ supplied at 15sccm, GeH₄ at 166sccm (10% in H₂) and B₂H₆ at 40sccm (1% in H₂). There is already ~190sccm of H₂ in the reference process as it is the carrier gas in the GeH₄ and B₂H₆ bottles. The H₂ flows according to an embodiment of the present invention are introduced in a separate H₂ line, so the total H₂ flow is in excess of 190sccm.

20 Accordingly, methods of the present invention include deposition selectively of CVD SiGe on substrates with the shortest incubation times such as SiGe and SiC. The maximum selectivity of deposition between thermal oxide and SiGe is achieved with a H₂ flow of 800sccm however a range of 200 sccm to 1200 sccm is included within the scope of this invention, e.g. between 400 and
25 1000 sccm.

 This increased the selectivity from ~70nm on the reference process to up to 170nm in accordance with this embodiment of the present invention. Results are shown in Figs. 16 and 17. The selective deposition of SiGe on an oxide layer can be used when an SiGe layer, especially a doped SiGe layer is grown on the
30 trench sidewalls but not on the silicon oxide surfaces in the devices described above, i.e. not at the bottom of the trench and on the hard mask layer. Hence, there is no need to remove a doped layer at the bottom of the trench that could make short-circuits in the final structures.

 In accordance with any of the embodiments of the present invention, after

refilling of the trenches for forming narrow gaps, the MEMS structures may be released, thereby creating a free standing resonator.

The method may be performed at temperatures not exceeding 450°C. Therefore the method may be used for forming micromachined structures comprising narrow gaps on a substrate comprising electrical circuitry, e.g. on a substrate comprising at least one transistor, e.g. on a CMOS substrate, by post-processing without affecting the underlying circuitry. With post-processing is meant that the micromachined devices, e.g. MEMS devices, are formed on the substrate after the electrical circuitry has been provided. The micromachined devices may be electrically connected to the underlying electrical circuitry, e.g. CMOS circuitry.

For example, the method for MEMS post-processing as described in US 60/863,679 may be used, the entire disclosure of which is incorporated herein by reference. After CMOS processing, the CMOS substrate comprising metal contacts may be covered with a dielectric layer, e.g. intermetal dielectric layer. The dielectric layer may be planarized, e.g. by means of CMP, and it may be covered with a protective layer, e.g. SiC layer. Vias may then be etched through the protective layer and the dielectric layer, e.g. vias may be etched where metal contacts of the underlying electrical circuitry are located. The vias may then be filled with plugs, e.g. metal plugs, for forming electrical connections to the underlying electrical circuitry, e.g. CMOS circuitry, through the dielectric layer and the protective layer. In a next step MEMS electrodes may be formed on top of the protective layer, and a MEMS sacrificial layer, e.g. silicon oxide layer, may be deposited and planarized. Openings may then be made through the sacrificial layer, e.g. to form contacts to the MEMS electrodes and/or for forming anchors for the MEMS structures, e.g. MEMS resonators to be manufactured. After this the MEMS structural layer and the sacrificial hard mask layer may be deposited and patterned as described above, followed by trench formation and trench narrowing. The sacrificial layer and the sacrificial hard mask layer may then be removed, thereby creating a free standing resonator anchored to the substrate and electrically connected to the underlying electrical circuitry, e.g. CMOS circuitry.

The method for forming micromachined structures comprising narrow gaps, e.g. MEMS resonators comprising narrow transduction gaps between a

resonating structure and the corresponding electrodes, may be combined with a capping process or a zero-level packaging process for the micromachined devices, e.g. resonators. An example of a process flow for such a capping process is shown in Figure 15. After forming the relatively wide trenches in the layer of structural material as described above, and before partially refilling the trenches, a sacrificial silicon oxide layer is deposited over the entire structure (Figure 15.1). This oxide deposition step may be followed by a planarization step, e.g. a CMP planarization step. After local etching of the sacrificial silicon oxide layer (Figure 15.2), a cap layer, e.g. a SiGe cap layer may be deposited (Figure 15.3). In a next step, illustrated in Figure 15.4, narrow openings may be etched in the cap layer using any suitable technique known by a person skilled in the art, the width of the openings being smaller than the width of the trenches in the underlying structural layer. The underlying MEMS structure may then be released and the sacrificial silicon oxide layer may be removed through the openings in the cap layer (Figure 15.5). Then a layer, e.g. a layer of undoped SiGe, may be deposited by means of a conformal deposition technique, such as for example an LPCVD technique (Figure 15.6). This undoped SiGe layer may be deposited on the sidewalls of the trenches underlying the SiGe cap layer, thereby narrowing the trenches and forming narrow gaps, e.g. between the resonating structure and the corresponding electrodes of the underlying resonator. During the same deposition step, this undoped SiGe layer may also be deposited on the sidewalls of the openings in the SiGe cap layer. As the openings in the cap layer are narrower than the trenches in the underlying structural layer, the cap layer may be sealed before the gap between the resonating structure and the corresponding electrodes is closed. The remaining gap width is thus determined by the difference between the initial trench width and the width of the openings in the cap layer, and thus can be accurately controlled by this self-limiting process. Alternatively, instead of depositing a layer of undoped SiGe for closing the openings in the cap layer and for narrowing the underlying trenches, a doped SiGe layer may be selectively deposited by alternating deposition and etching steps.

Amended Claims:

1. A method for manufacturing a micromachined or MEMS structure having at least one narrow gap between a first structural element and a second structural element, the method comprising:
- 5 depositing a first layer of a structural material on a substrate;
forming at least one trench in the first layer of structural material, the at least one trench being arranged for defining the first structural element and the second structural element; and
- 10 depositing a second layer for partially refilling and narrowing the at least one trench, thereby forming the at least one narrow gap.
2. The method of claim 1, wherein the second layer is of structural material.
- 15 3. The method of claim 1 or 2 further comprising: forming a dielectric layer on the substrate before depositing the first layer of structural material.
4. The method of any previous claim, wherein depositing of the second layer is by means of a conformal deposition technique.
- 20 5. The method of claim 4, wherein the deposition method is LPCVD (Low Pressure Chemical Vapor Deposition).
6. The method of any previous claim wherein the at least one trench is formed with sidewalls that form a substantially right angle with an average surface plane of the substrate.
- 25 7. The method of any previous claim wherein the at least one trench is formed extending through the first layer of structural material.
- 30 8. The method of any previous claim, wherein the structural material is silicon germanium.
9. The method of any previous claim wherein the at least one gap is formed

narrower than 400 nm, optionally narrower than 200 nm.

10. The method of any previous claim wherein depositing the second comprises depositing a layer of doped silicon germanium.

5

11. The method of any of the previous claims wherein the deposition of the second layer selectively forms more of the second layer on the at least one trench sidewalls rather than on the bottom of the trench.

10

12. The method of claim 11, wherein the deposition of the second layer is carried out with a flow of hydrogen.

13. The method of claim 12, wherein the flow of hydrogen is between 200 and 1200 sccm, optionally 400 and 1000 sccm.

15

14. The method according to any of the claims 1 to 9, wherein the depositing the second layer comprises depositing a layer of undoped silicon germanium.

20

15. The method of any previous claim further comprising removing the second layer of structural material from the bottom of the at least one trench.

16. The method of any previous claim wherein depositing the second layer of structural material comprises a plurality of alternating deposition steps and etching steps.

25

17. The method of any of the previous claims performed at temperatures not exceeding 450°C.

30

18. A method for forming a sealed cap or zero-level package over a structure comprising narrow gaps made according to any of the previous claims, comprising:

after forming the at least one trench and before depositing the second layer of structural material, depositing a sacrificial layer; depositing a cap layer over the sacrificial layer; and forming a plurality of openings in the cap layer, the width of

the plurality of openings being smaller than the width of the at least one trench.

19. The method of claim 18, the cap layer being formed from the structural material.

5

20. The method of claim 18 or 19, wherein after forming the plurality of openings in the cap layer, the underlying MEMS structure is released, at the same time removing the sacrificial layer.

10

21. The method of claim 20, further comprising depositing a second layer of undoped structural material or a second layer of doped structural material by alternating deposition steps and etching steps, thereby refilling and narrowing the at least one trench and closing the plurality of openings in the cap layer.

15

22. A MEMS device manufacturable according to any of the claims 1 to 21.

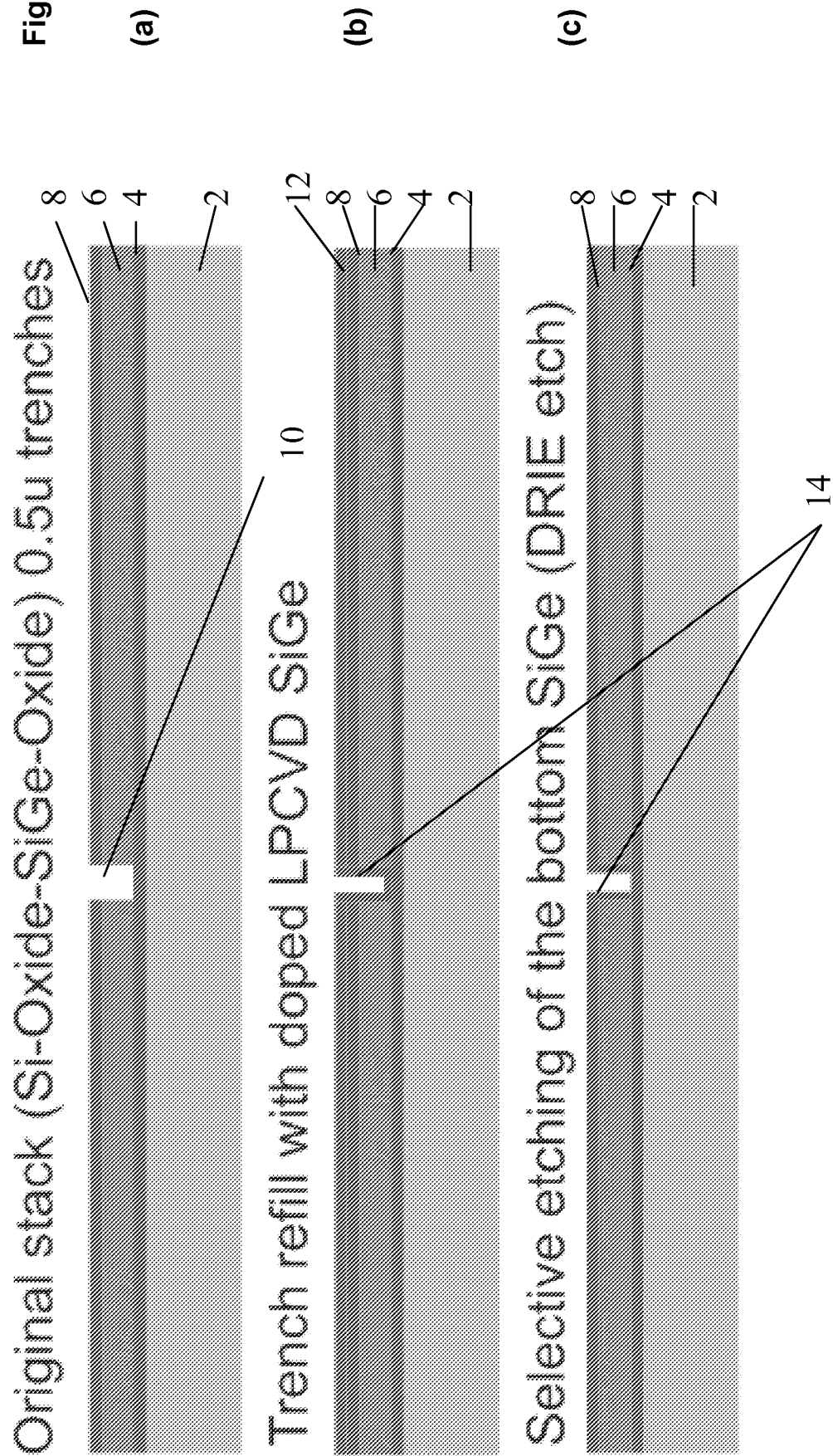
23. The MEMS device of claim 22, the device being a resonator structure, wherein the at least one narrow gap is a transduction gap between a resonating element and a corresponding electrode.

20

24. The MEMS device of claim 23, wherein the device is a capacitive MEMS resonator.

25. Use of a hydrogen flow to modulate the selective deposition of SiGe.

Figure 1



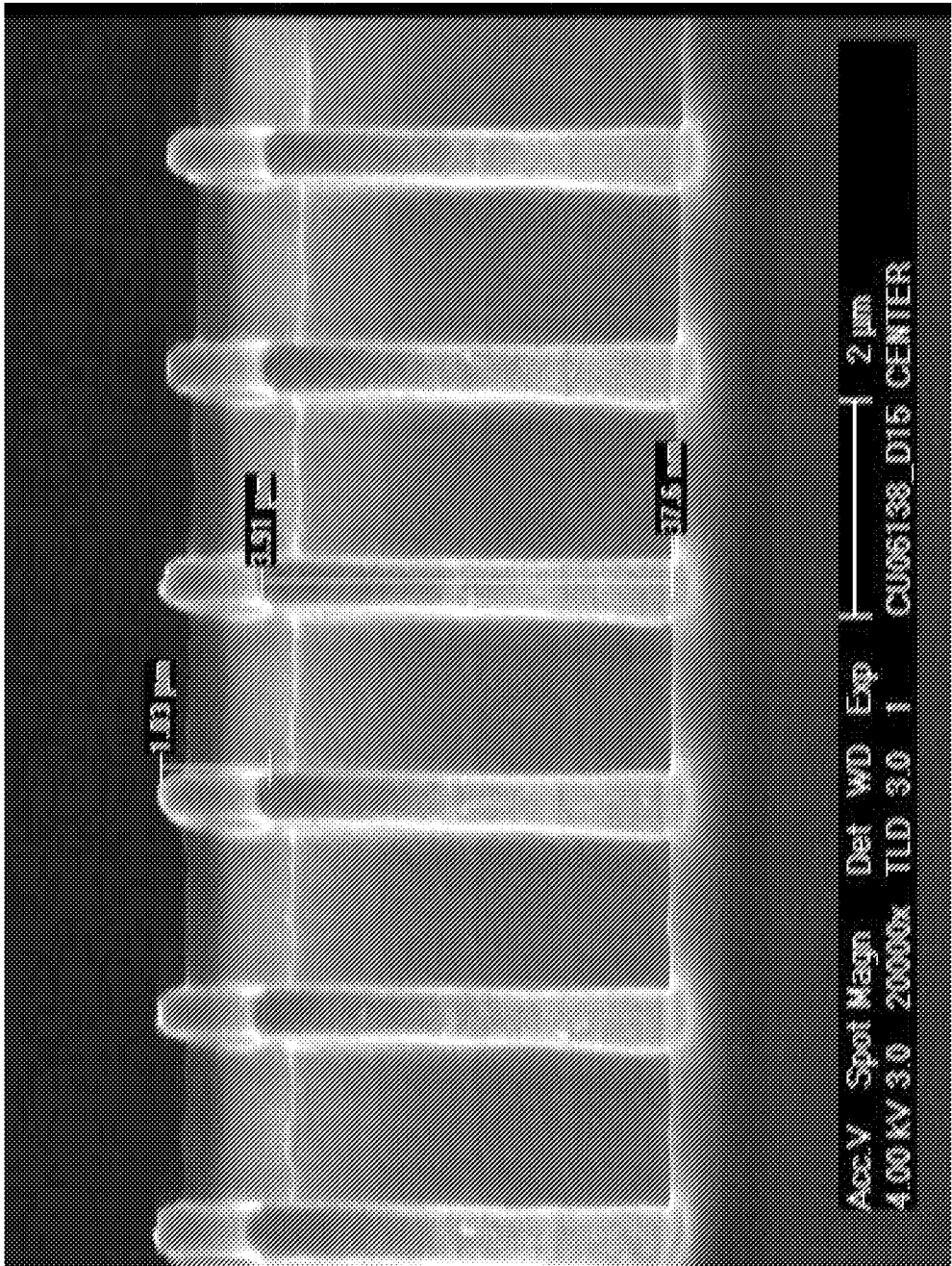
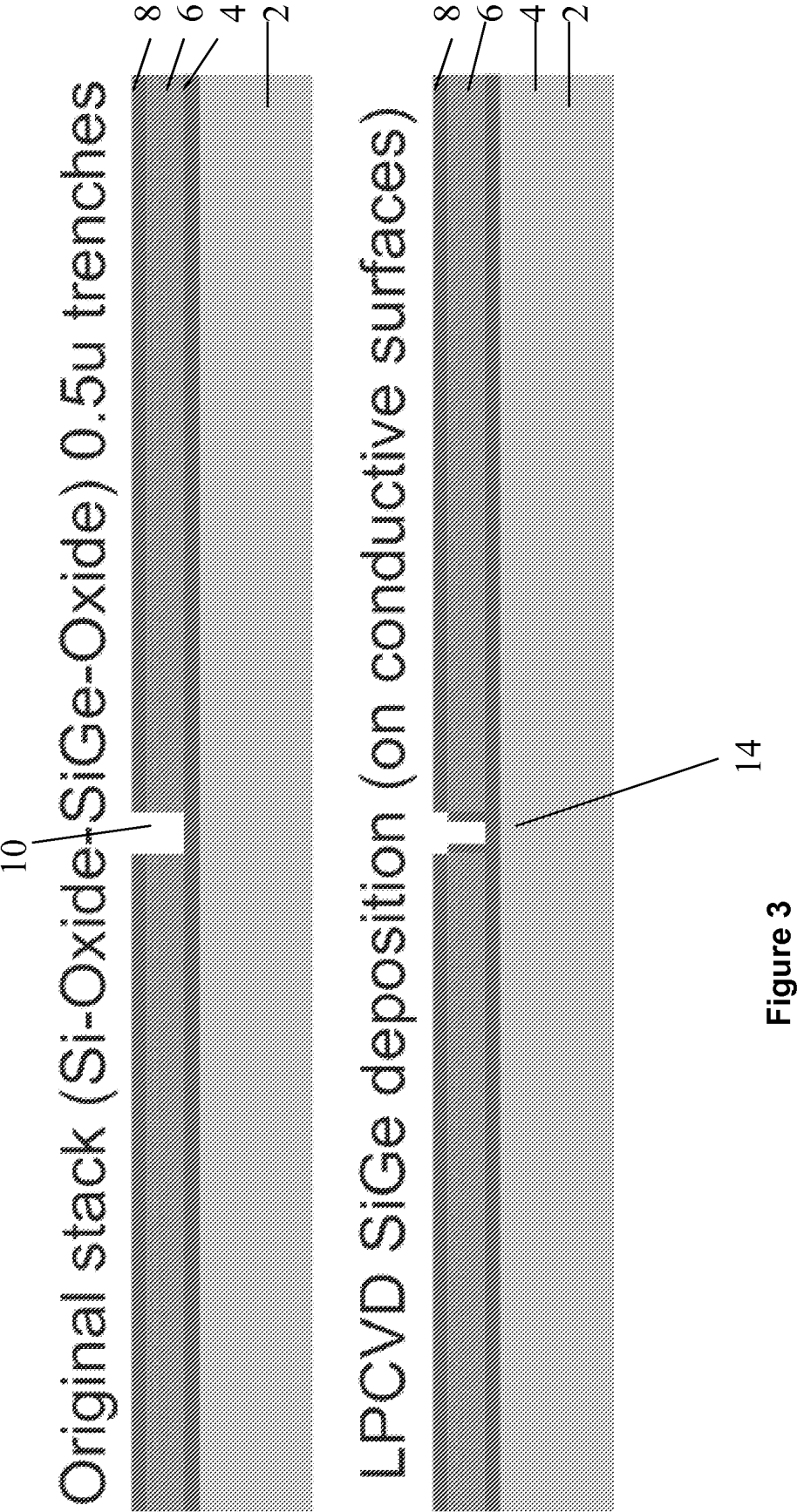


Figure 2



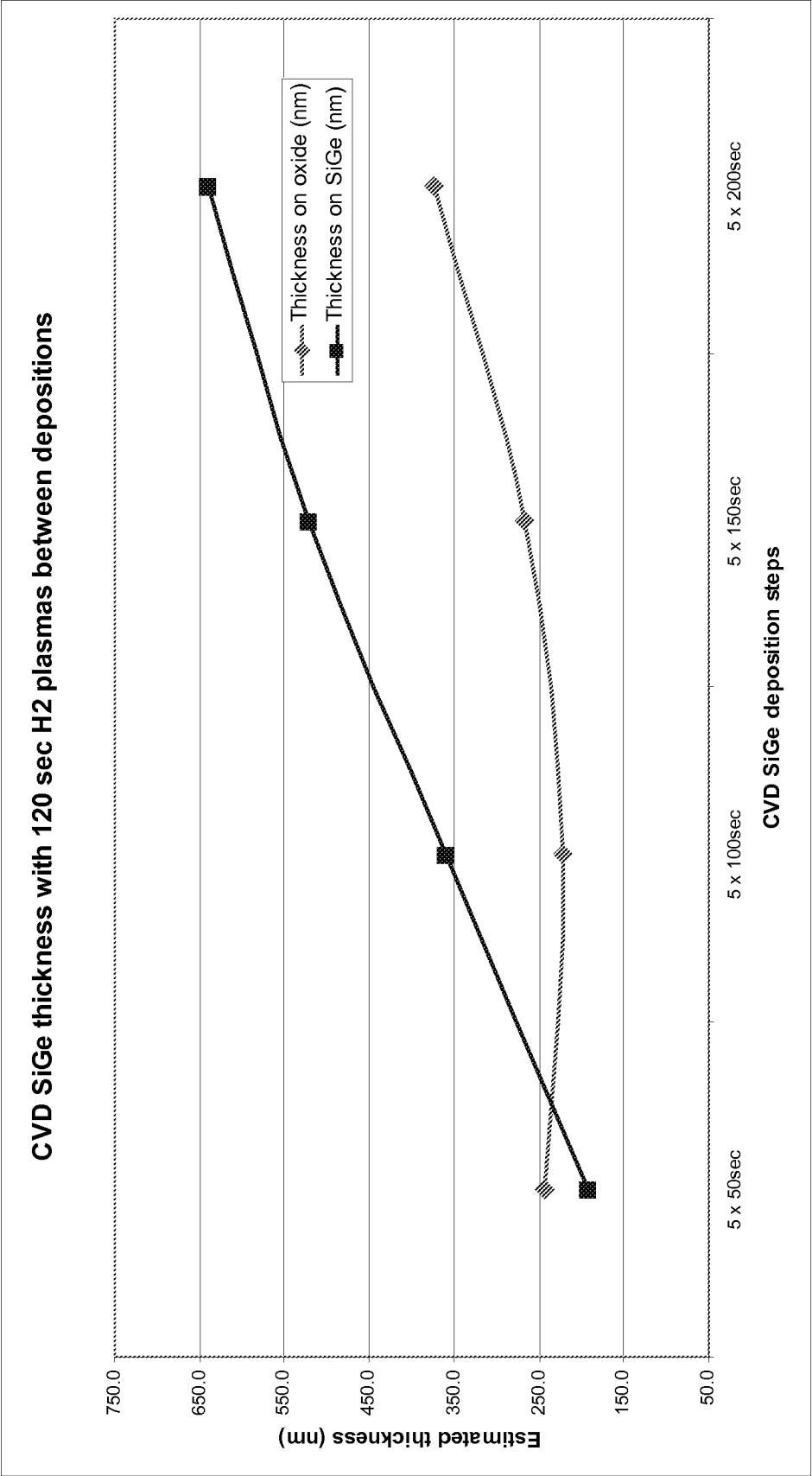


Figure 4

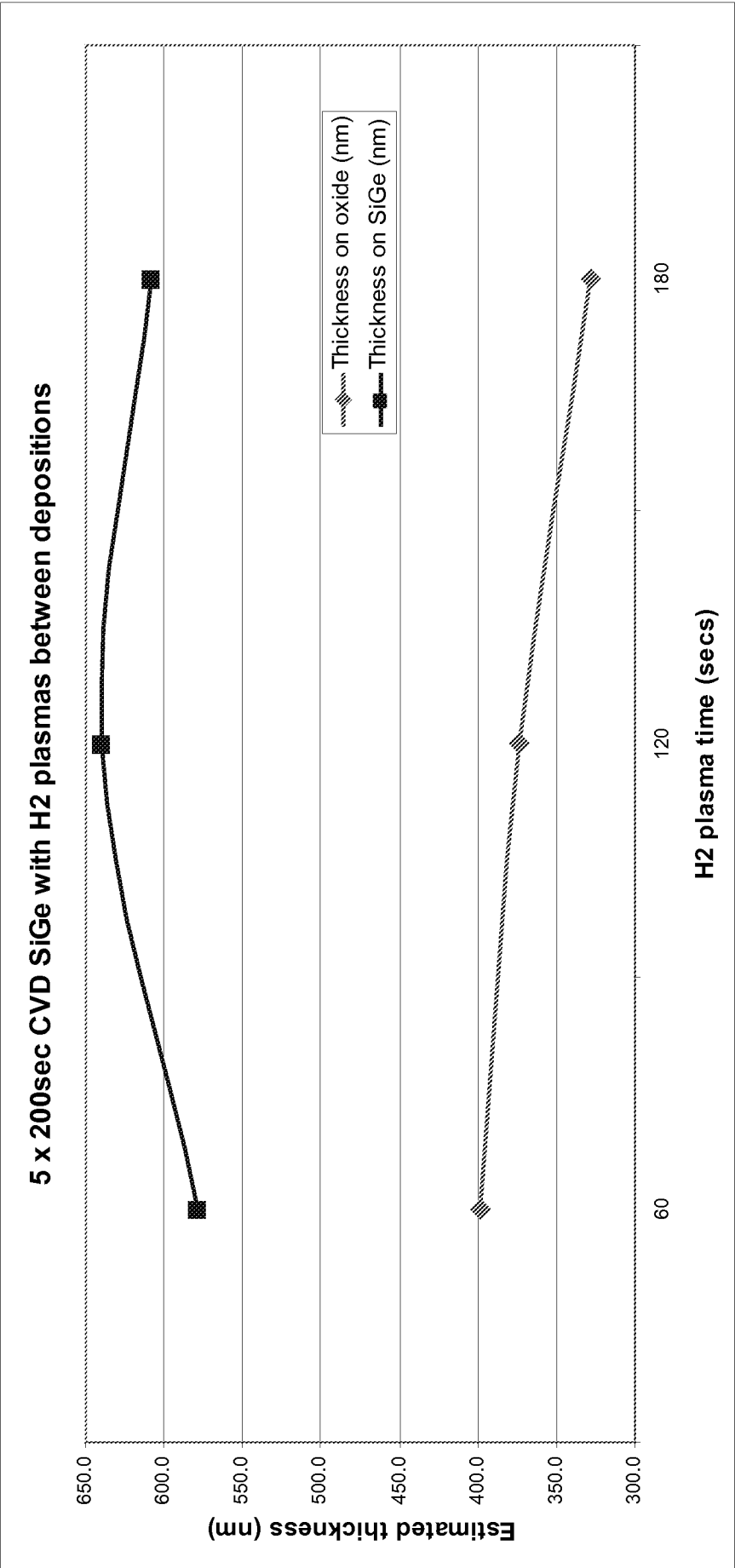
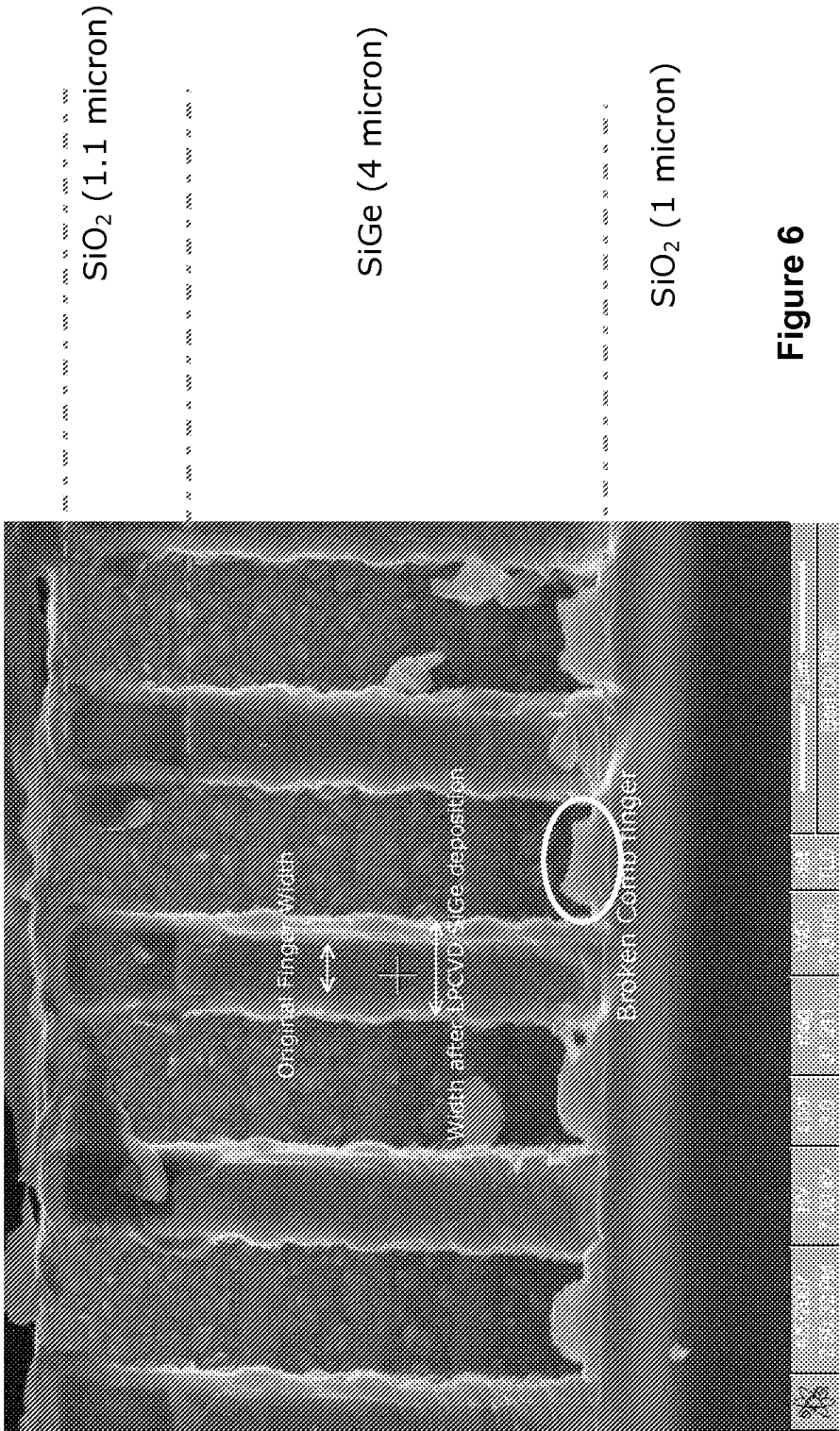


Figure 5



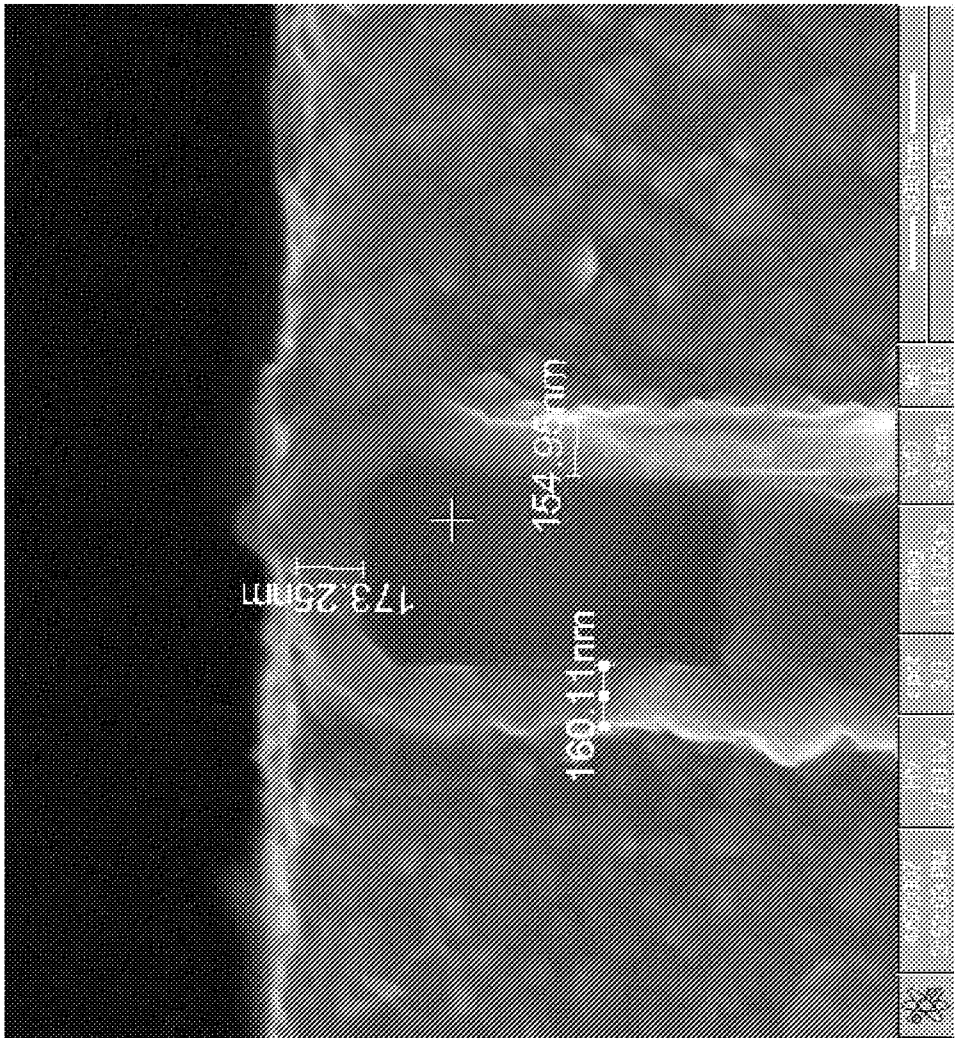


Figure 7

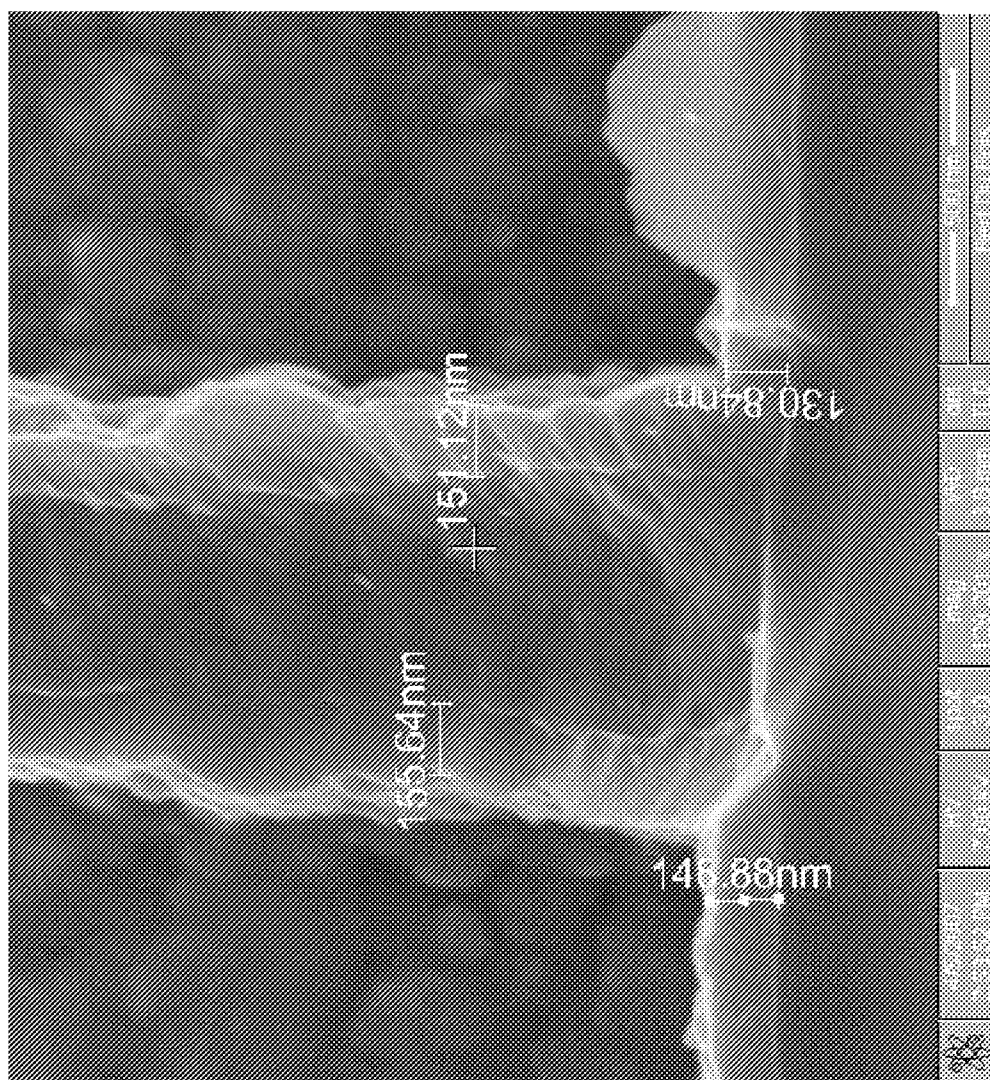


Figure 8

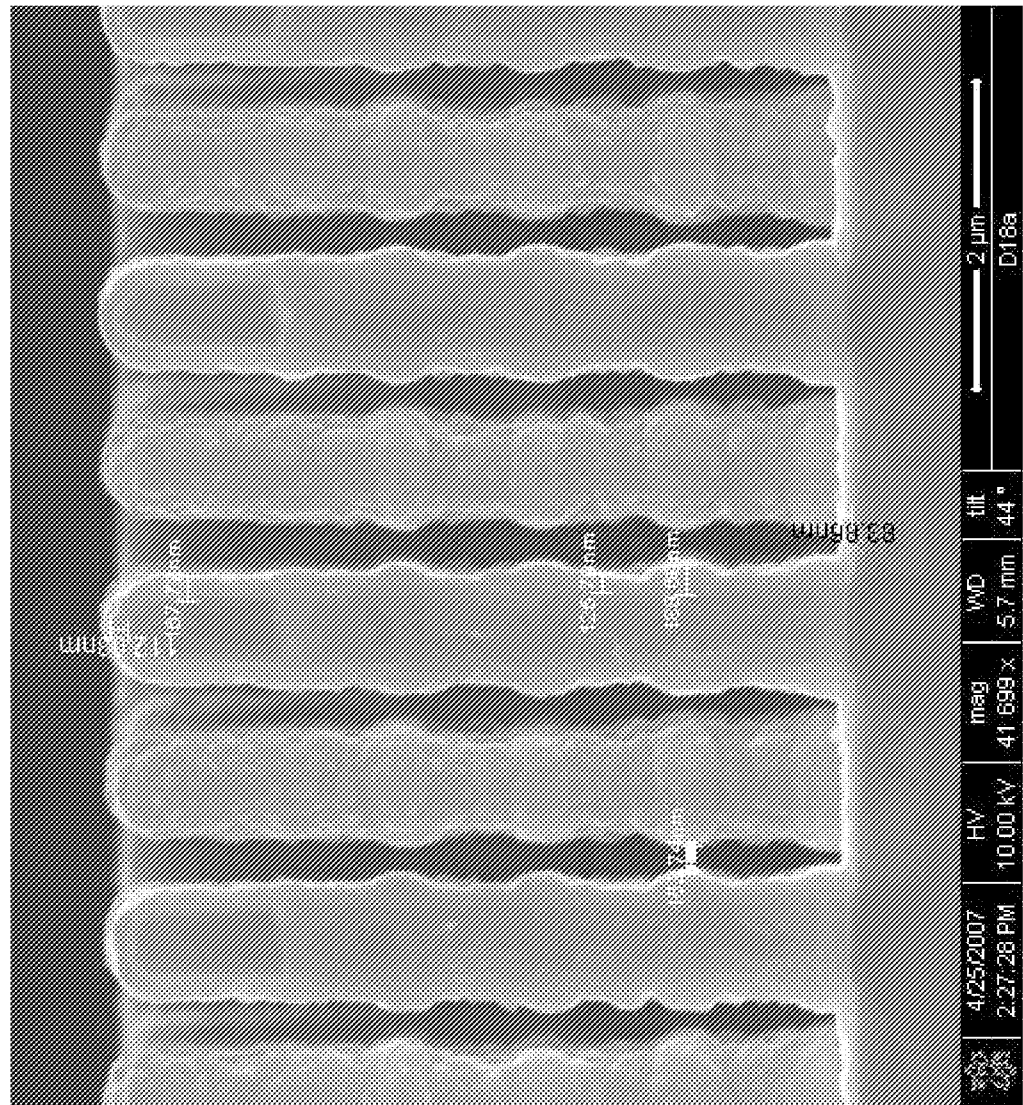


Figure 9

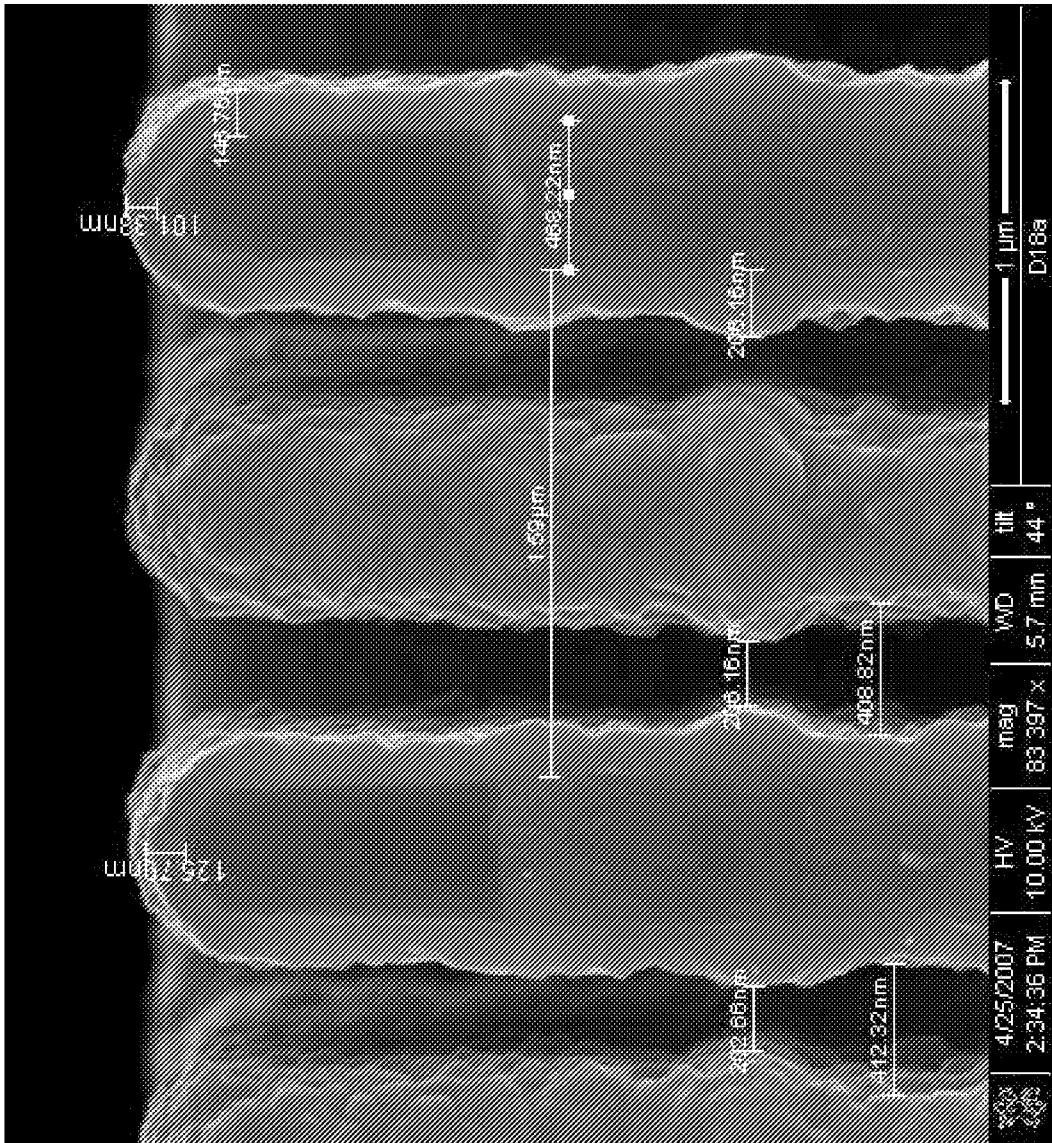
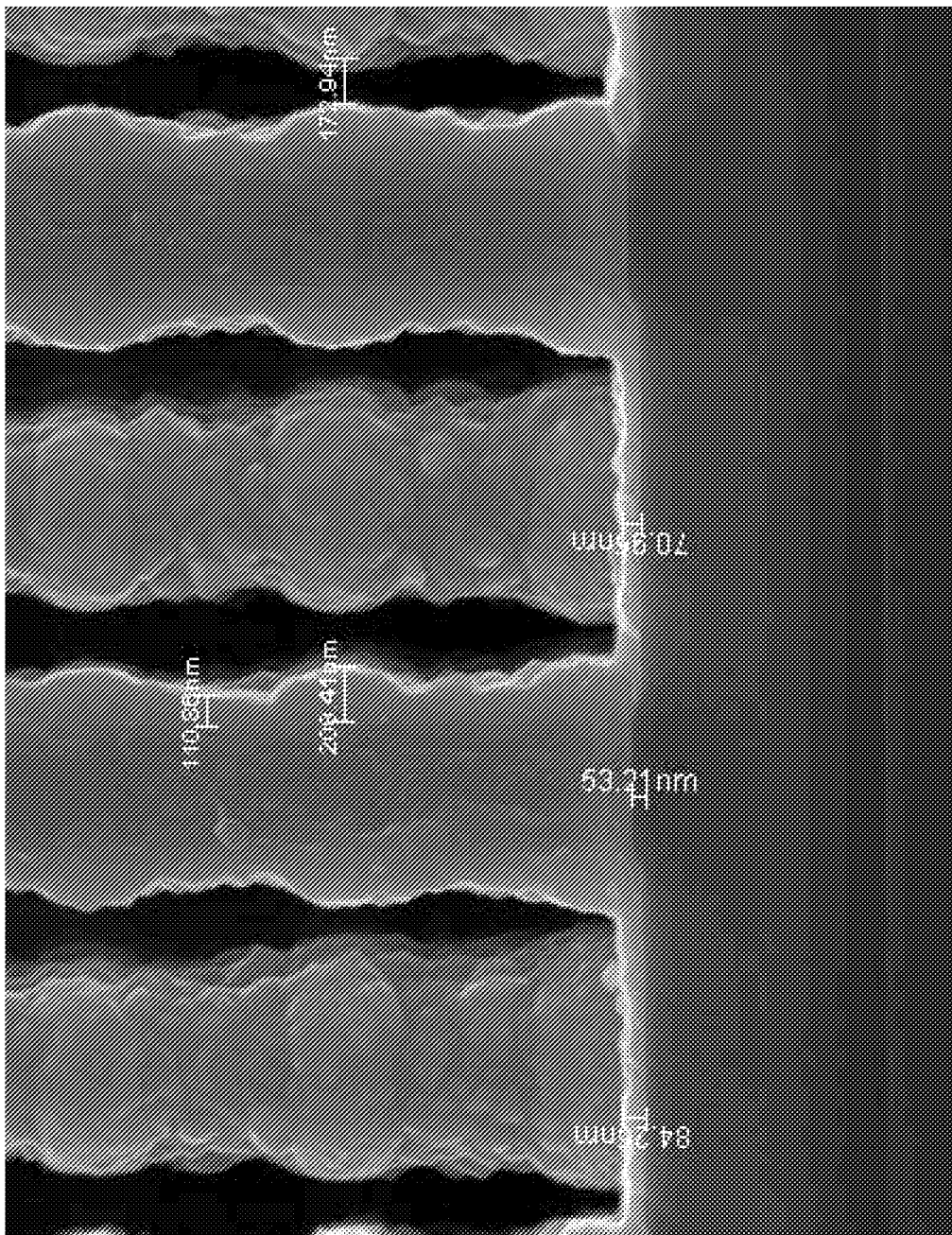


Figure 10

Figure 11



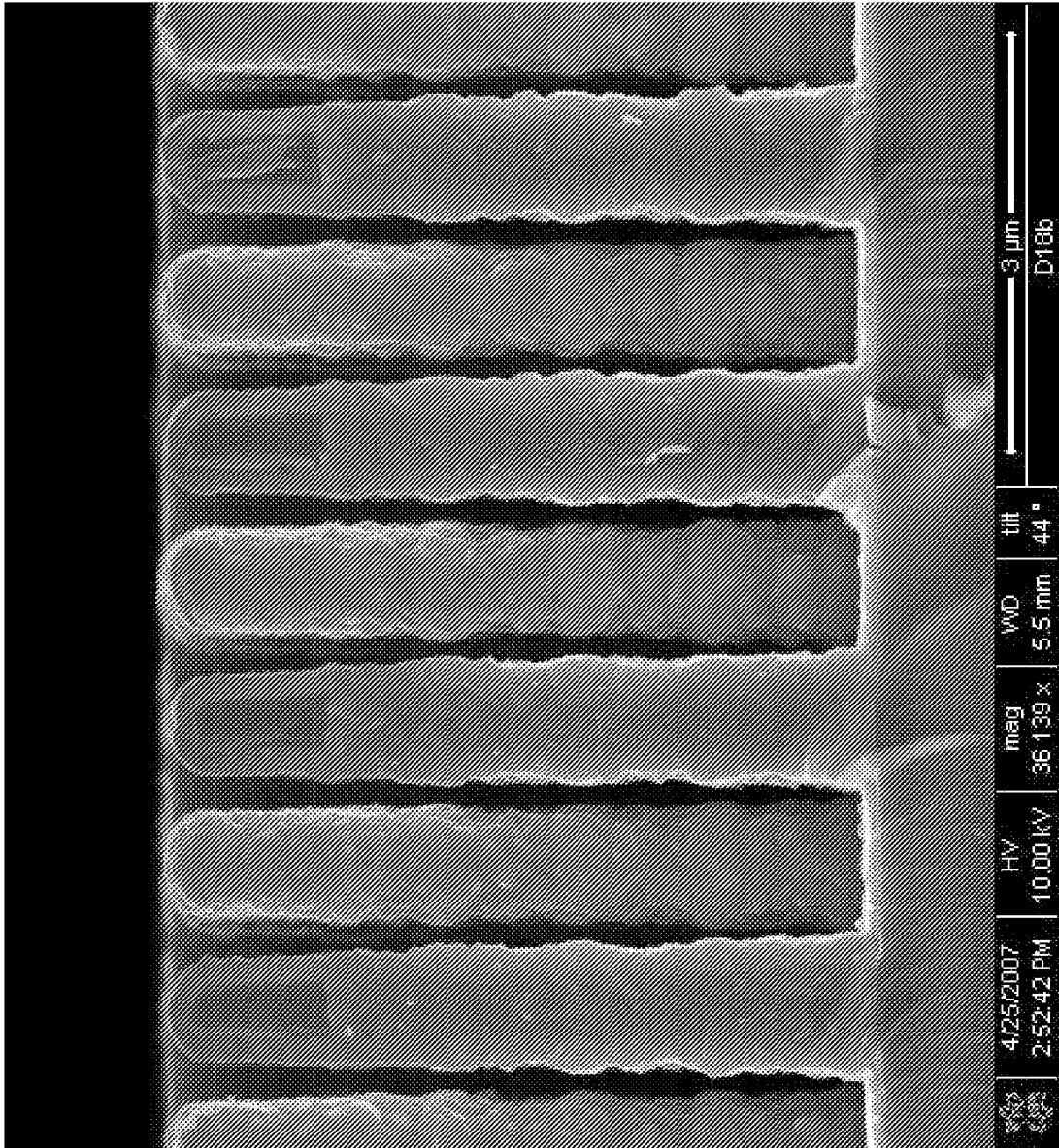
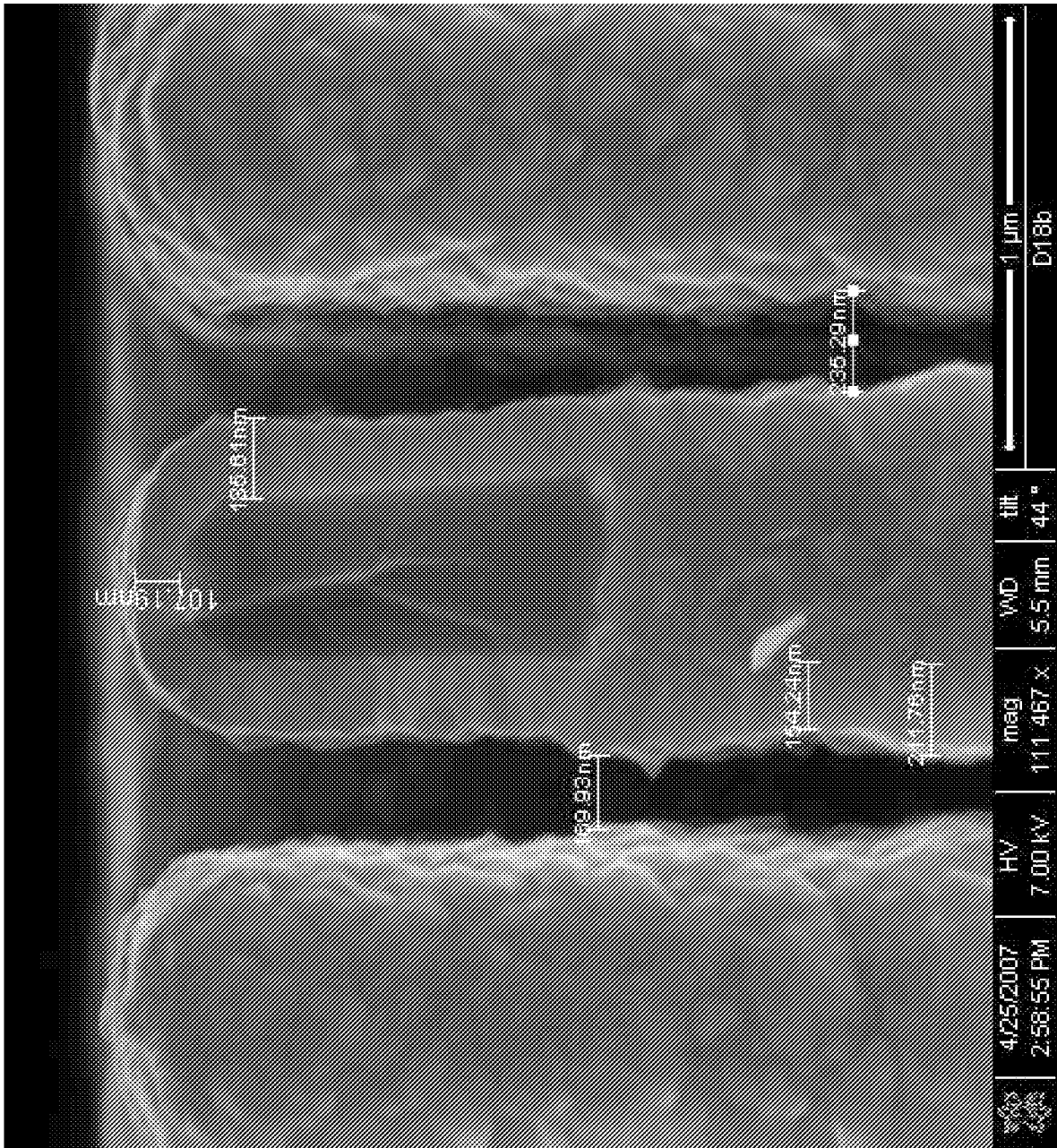


Figure 12

Figure 13



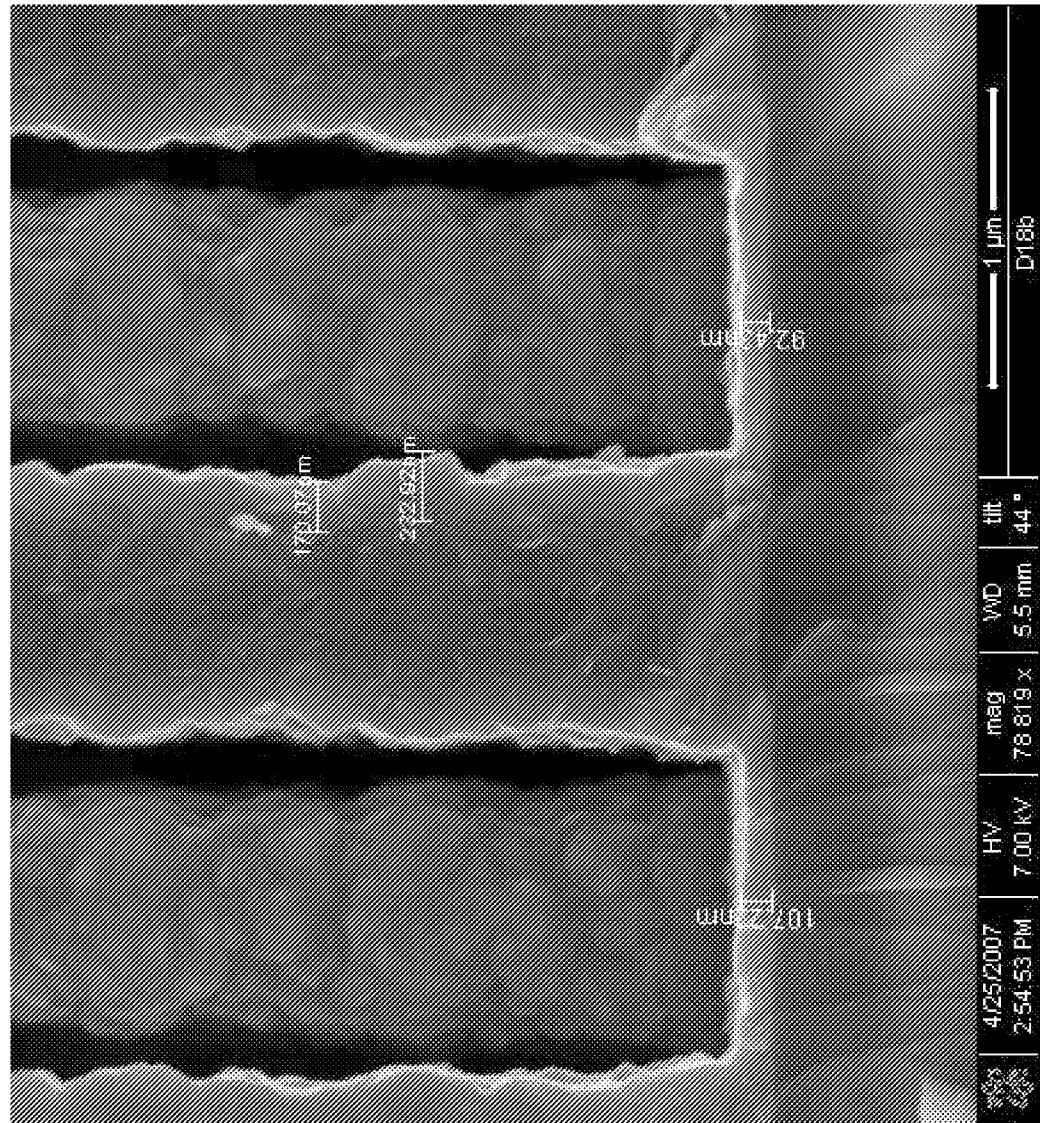


Figure 14

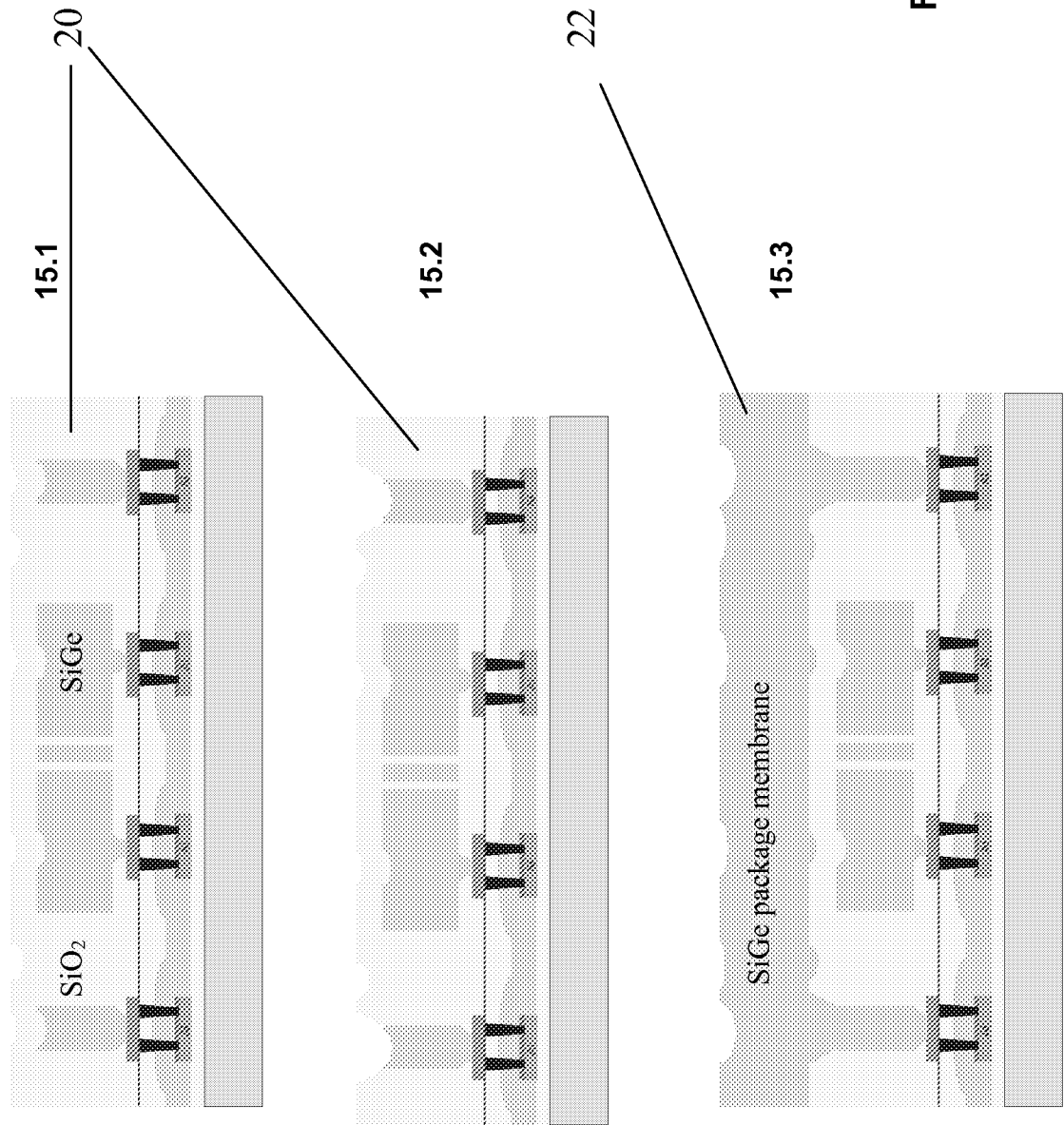


Figure 15

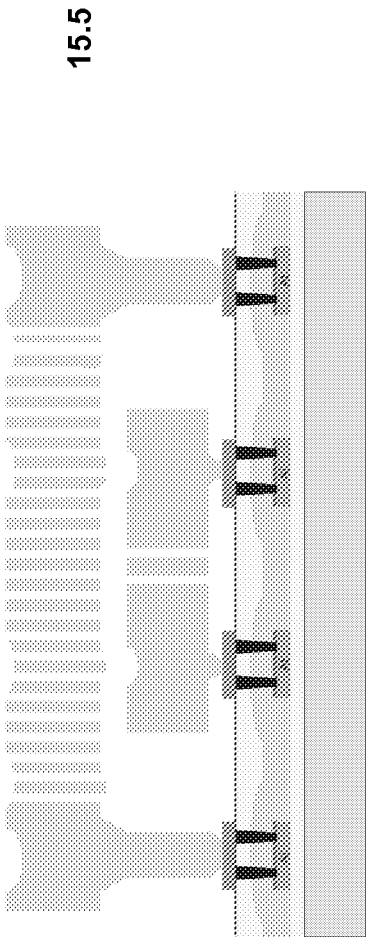
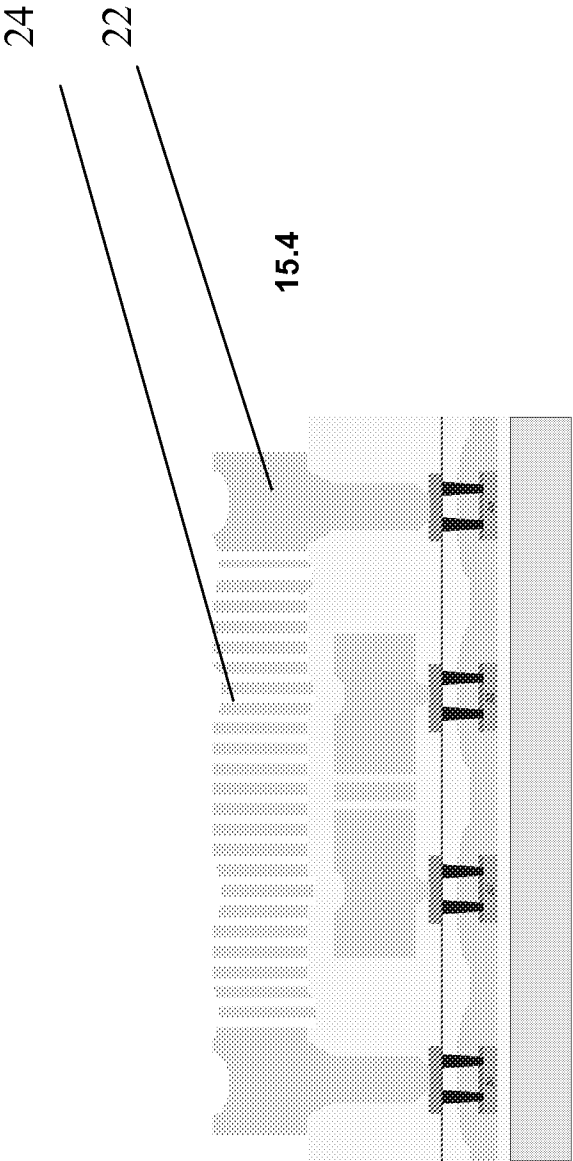


Figure 15 (cont)

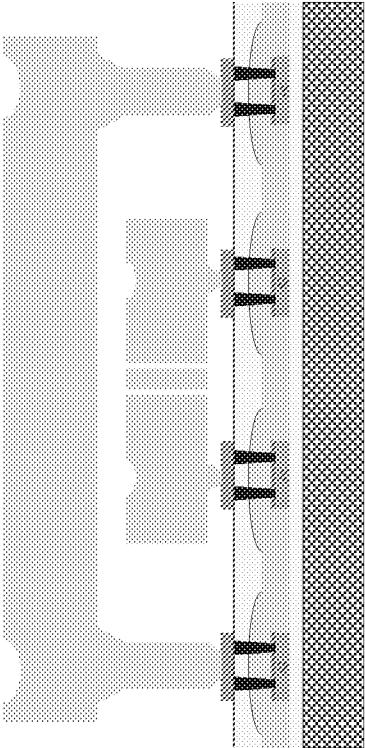


Figure 15 (cont)

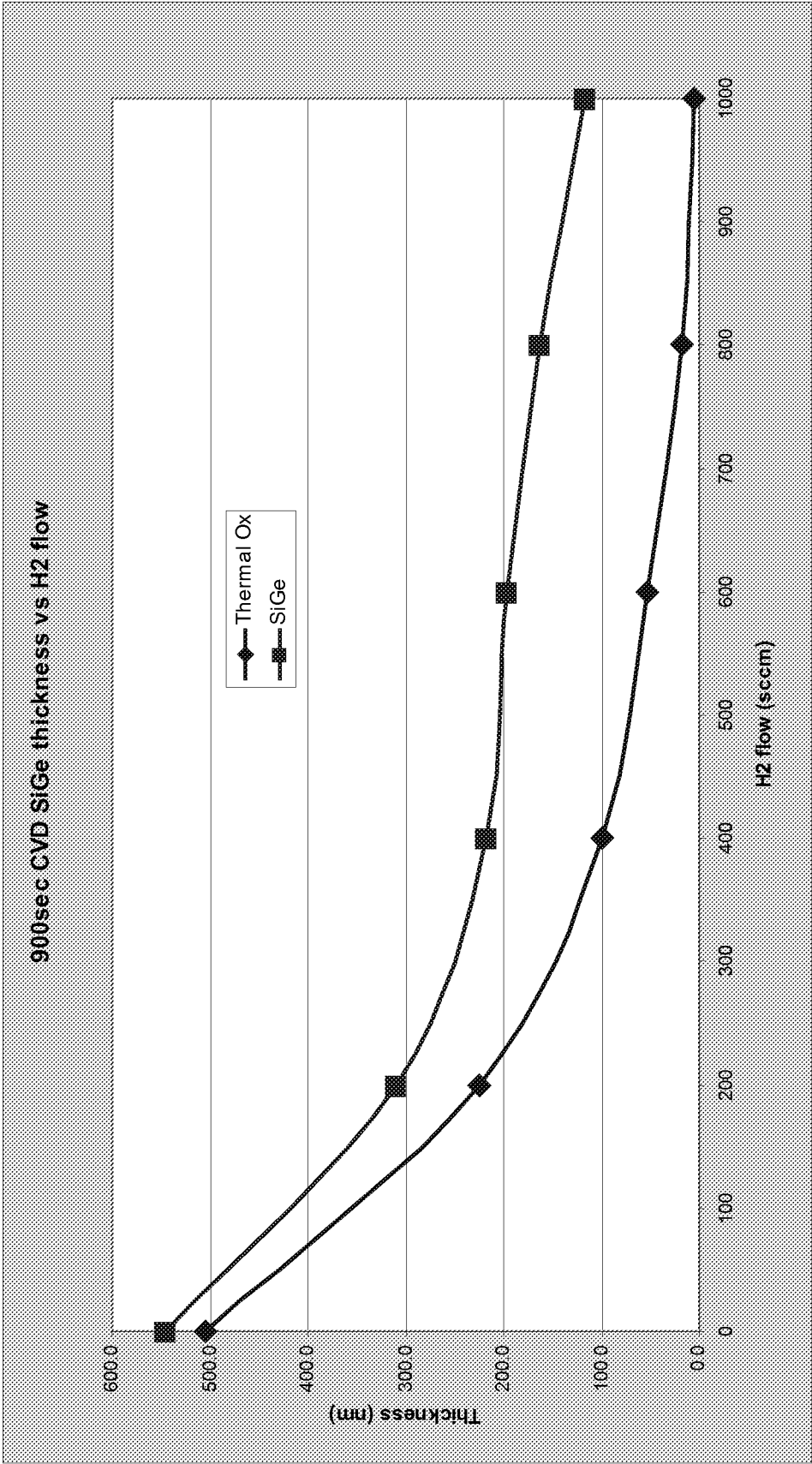


Figure 16

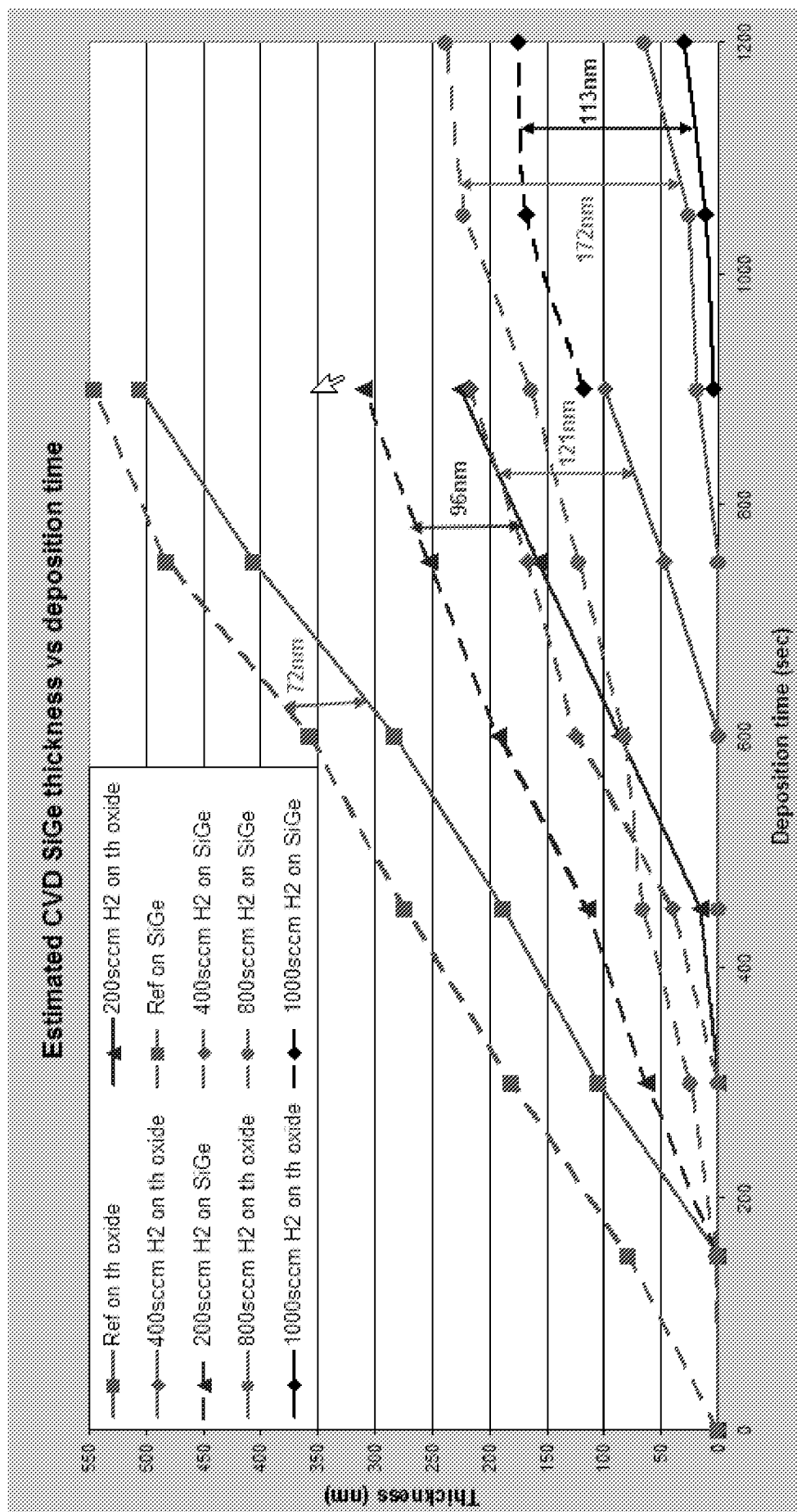


Figure 17