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- (71) **Applicant:** MARVELL WORLD TRADE LTD.
[BB/BB]; L'horizon, Gunsite Road, Brittons Hill, St. Michael, BB14027 (BB).
- (72) **Inventors; and**
- (73) **Applicants :** LIU, Chenglin [US/US]; 1182 Adams Court, San Jose, CA 95132 (US). LIAO, Sheng, C. [—/US]; 559 Crystalberry Terrace, San Jose, CA 95129 (US). LIOU, Shiann-Ming [US/US]; 2187 Anthony Drive, Campbell, CA 95008 (US).
- (74) **Agents:** WICHNER, Brian, Donald et al.; Lee & Hayes, PLLC, 601 W. Riverside Ave, Suite 1400, Spokane, WA 99201 (US).
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(54) **Title:** DUAL ROW QUAD FLAT NO-LEAD SEMICONDUCTOR PACKAGE

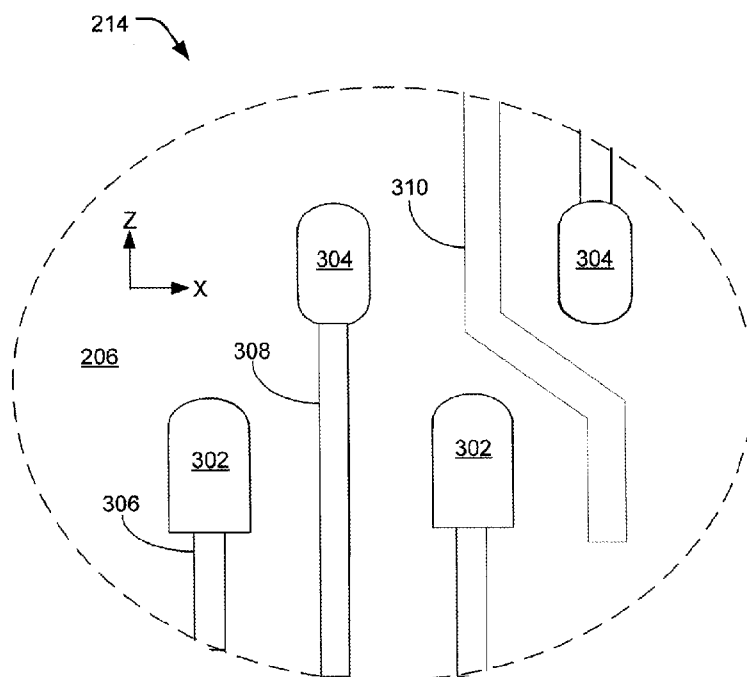


FIG. 3

(57) **Abstract:** Some of the embodiments of the present disclosure provide a Quad Flat No-Lead package comprising: an outer row of outer peripheral leads disposed on an outer periphery of a bottom surface of the Quad Flat No-Lead package; and an inner row of inner peripheral leads disposed on an inner periphery of the bottom surface of the Quad Flat No-Lead package, wherein each of the inner peripheral leads has a substantially rectangular shape, and wherein the substantially rectangular shape has two rounded corners adjacent to the outer row of outer peripheral leads.



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DUAL ROW QUAD FLAT NO-LEAD SEMICONDUCTOR PACKAGE**Cross Reference to Related Applications**

[0001] This disclosure claims priority to U.S. Patent Application No. 14/023,259, filed September 10, 2013, which claims priority to U.S. Provisional Patent Application No. 61/700,136, filed on September 12, 2012, which are incorporated herein by reference.

Technical Field

[0002] Embodiments of the present disclosure relate to chip packaging technology for semiconductor integrated circuits and more particularly, to Quad Flat No-Lead (QFN) packages.

Background

[0003] Unless otherwise indicated herein, the approaches described in this section are not prior art to the claims in the present disclosure and are not admitted to be prior art by inclusion in this section.

[0004] The rapidly growing portable electronics markets, e.g. cellular phones, laptop computers, and personal digital assistants (PDAs), are integral facets of modern life and each are operated by an integrated circuit (IC) with strict packaging demands. ICs have unique attributes which have significant impacts on manufacturing integration, in that they must be generally small, lightweight, rich in functionality, and they must be produced in high volumes at relatively low cost. For example, there is a demand for IC packages that are particularly well suited for use in devices that are small in size, such as small hand-held devices.

[0005] To meet such demand, manufacturers integrate increasingly more circuit functions, shrinking device features, and increasing speeds. As an extension of the IC industry, the electronics packaging industry is faced with similar technological and market dynamics. From a packaging perspective, smaller form factors, requirements for more input/output signals, and power management are major technology drivers. Sophisticated new products of all types are being developed, while barriers are continually being reached with conventional IC packages and processes.

Summary

[0006] In various embodiments, the present disclosure provides a Quad Flat No-Lead package comprising: an outer row of outer peripheral leads disposed on an outer periphery of a bottom surface of the Quad Flat No-Lead package; and an inner row of inner peripheral leads disposed on an inner periphery of the bottom surface of the Quad Flat No-Lead package, wherein each of the inner peripheral leads has a substantially rectangular shape, and wherein the substantially rectangular shape has two rounded corners adjacent to the outer row of outer peripheral leads.

[0007] In other embodiments, the present disclosure provides an integrated circuit package comprising: a Dual Row Quad Flat No-Lead package having a top surface and a bottom surface, wherein the bottom surface of the Dual Row Quad Flat No-Lead package includes (i) an outer row of outer peripheral leads disposed on an outer periphery of the bottom surface of the Dual Row Quad Flat No-Lead package and (ii) an inner row of inner peripheral leads disposed on an inner periphery of the bottom surface of the Quad Flat No-Lead package, wherein each of the

inner peripheral leads has a substantially rectangular shape, and wherein the substantially rectangular shape has two rounded corners adjacent to the outer row of outer peripheral leads; and a printed circuit board electrically connected to the bottom surface of the Dual Row Quad Flat No-Lead package.

Brief Description of the Drawings

[0008] In the following detailed description, reference is made to the accompanying drawings which form a part hereof wherein like numerals designate like parts throughout, and in which is shown by way of embodiments that illustrate principles of the present disclosure. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense, and the scope of embodiments in accordance with the present disclosure is defined by the appended claims and their equivalents.

[0009] FIG. 1 is a bottom view of a Dual Row Quad Flat No-Lead package, according to some embodiments.

[0010] FIG. 2 is a side view of an integrated circuit package, according to some embodiments.

[0011] FIG. 3 is a schematic diagram of a printed circuit board pin land pattern, according to some embodiments.

[0012] FIG. 4 is top view of a Dual Row Quad Flat No-Lead package, according to some embodiments.

[0013] FIG. 5 is a close-up view of a top corner of a Dual Row Quad Flat No-Lead package, according to various embodiments.

[0014] FIG. 6 is a bottom view of a Dual Row Quad Flat No-Lead package, according to some embodiments.

[0015] FIG. 7 is a top view of a Dual Row Quad Flat No-Lead package, according to some embodiments.

[0016] FIG. 8 is a bottom view of a Dual Row Quad Flat No-Lead package, according to other embodiments.

[0017] FIG. 9 is a top view of a Dual Row Quad Flat No-Lead package, according to other embodiments.

Detailed Description

[0018] In various embodiments, a quad flat no-lead (QFN) integrated circuit (IC) package comprises an IC die (e.g., IC chip) mounted on a die paddle, which in turn is attached to a metal leadframe. The metal leadframe is wire bonded during a wire bonding process to connect input/output (I/O) pads of the IC die to external lands of the QFN IC package. In some implementations, a leadframe assembly, including attached QFN IC packages, is over-molded in plastic. A singulation process subsequently partitions the IC packages and corresponding portions of the leadframe into individual IC packages. Resulting IC packages are square or rectangular and include external package leads for connecting the individual IC packages to a printed circuit board (PCB). These external package leads are flush (e.g., flat) with the leadframe and disposed around a bottom perimeter of the package. Dual Row QFN (DRQFN) IC packages include a second bottom perimeter of external package leads. A die paddle is flush with the top surface and the bottom surface of the leadframe.

[0019] The QFN IC package can be soldered onto a PCB by soldering the die paddle located on the bottom of the QFN IC package to the PCB. Conductive traces on the PCB are routed to individual leads of the QFN IC package. The conductive traces can terminate at pin lands, which correspond to external package leads of the QFN IC package. The conductive traces are electrically connected (via pin lands) by soldering to make the electrical connections between the IC lands and other elements mounted on the PCB. The die paddle can comprise thermally conductive material to function as a heat spreader or heat sink device. The die paddle can also provide a stable ground for the QFN IC package by using down bonds or an electrically

conductive die attach material to provide an electrical ground path from the QFN IC package to the PCB.

[0020] Though a QFN IC package is small, light, and has a low profile, the size of a QFN IC package generally depends on the number of lands that are in the QFN IC package and the size of the IC die. For example, QFN IC packages can have a dozen lands or as many as 148 or more lands.

[0021] In some embodiments, a DRQFN IC package includes an inner row of leads having a rounded outline so as to increase lead-to-lead separation from adjacent outer row leads. Such a separation is increased over the case where both inner row leads and outer row leads have a square outline. Increasing lead-to-lead separation provides a number of benefits, such as providing clearance for routing conductive traces between PCB lands for adjacent outer and inner row leads.

[0022] FIG. 1 is a bottom view of a DRQFN package 100, according to some embodiments. Hereinafter, for convenience, a DRQFN package is referred to as a “QFN” package, whether or not the package has a dual row of leads or a single row of leads. QFN package 100 includes an outer row of outer peripheral leads 102 disposed on an outer periphery of a bottom surface of QFN package 100. In some implementations, the outer periphery coincides with an edge 104 of QFN package 100.

[0023] QFN package 100 also includes an inner row of inner peripheral leads 106 disposed on an inner periphery of the bottom surface of QFN package 100, wherein each of the inner peripheral leads has a substantially rectangular shape having two rounded corners adjacent to the outer row of outer peripheral leads. In the particular implementation of FIG. 1, inner

peripheral leads 106 and outer peripheral leads 102 are labeled by numbers 108, though such numbering is not to impose any limits to claimed subject matter. For example, outer peripheral leads 102 labeled “1” and “148” are adjacent to one of four corners 112 of QFN package 100.

[0024] QFN package 100 also includes a die paddle 110 located inside the inner row of inner peripheral leads 106 on the bottom surface of QFN package 100. Die paddle 110 can be used for electrical grounding or for a power source for an IC die that can be attached to QFN package 100.

[0025] Region 114 is shown in greater detail in the bottom of FIG. 1. Outer row of outer peripheral leads 102 is disposed on an edge 104 of QFN package 100. Accordingly, edges 116 of outer peripheral leads 102 coincide with edge 104 of QFN package 100. Inner peripheral leads 106 have a rounded outline 118 at least partially defined by a radius of curvature labeled “R” in FIG. 1. Each of inner peripheral leads 106 has a width 120 measured in a direction parallel to a nearest edge 104 of the bottom surface of QFN package 100. For example, width 120 can be about 0.25 millimeters. However, this and other values set forth in embodiments herein can widely vary depending, at least in part, on the number of leads included in QFN package 100. In some implementations, two rounded corners 122 of the substantially rectangular shape of each inner peripheral lead 106 are rounded with a radius of curvature R that is equal to about half (e.g., give or take 20% or so) the width 120 of each of the inner peripheral leads 106. Claimed subject matter, however, is not limited to such a curvature, and inner peripheral leads 106 can be rounded in any of a number of fashions or values. The two corners opposite corners 122 can also be rounded. Inner peripheral leads 106 may achieve such a rounded outline during

fabrication of QFN package 106. For example, masking and etching processes can involve patterns that include rounded outlines.

[0026] Rounded outlines of inner peripheral leads 106 allow for an increase in separation 124 from outer peripheral leads 102, compared to the case where inner peripheral leads 106 have a square outline. In some implementations, inner peripheral leads 106 having a square outline can have the same increase in separation as inner peripheral leads 106 having the rounded outline. In this case, however, the surface area of inner peripheral leads 106 would be relatively small, thereby undesirably reducing conductivity of inner peripheral leads 106.

[0027] Increased separation 124 and a separation distance 126 between adjacent inner peripheral leads 106 can allow for greater clearance for routing conductive traces between adjacent inner peripheral leads 106 (e.g., as dictated, at least in part, by separation distance 126) or between adjacent inner peripheral leads 106 and outer peripheral leads 102 (e.g., as dictated, at least in part, by separation 124). In some particular implementations, separation distance 126 can range from about 0.25 millimeters to about 0.4 millimeters, though this range can widely vary depending, at least in part, on the number of leads included in QFN package 100.

[0028] In some embodiments, QFN package 100 includes individual outer peripheral leads 102 that are about (e.g., give or take 20% or so) equidistant from two nearest inner peripheral leads 106. In other words, separation 124 between an inner peripheral lead 106 and either of two adjacent outer peripheral leads 102 is about the same. In some implementations, separation 124 is about 0.3 millimeters, though claimed subject matter is not limited in this respect. In other implementations, a distance between two adjacent outer peripheral leads

102 is about equal to the width of the inner peripheral leads. Moreover, this distance may be about equal to separation distance 126.

[0029] FIG. 2 is a side view of an IC package 200, according to some embodiments. IC package 200 may comprise a QFN IC package including a leadframe 202, a module or IC die 204, and a PCB 206. As described above, leadframe 202 can include a die paddle (e.g., die paddle 110, shown in FIG. 1) to which IC die 204 is mechanically and/or electrically connected (e.g., by solder) at interface 208. For example, such electrical connection can be a ground or power supply for IC die 204. Referring to orthogonal directional axes X, Y, and Z (where Z is out of the page), interface 208 lies in the X-Z plane. Electrical vias (not shown) can be used to electrically connect circuitry at interface 208 with circuitry at interface 210. Such vias conduct electrical signals in the Y-direction. PCB 206 can be electrically connected to a bottom surface of leadframe 202 at interface 210. A surface 212 of PCB 206 includes circuitry comprising conductive traces, which are shown in detail for region 214 in FIG. 3.

[0030] FIG. 3 is a schematic diagram of a pin land pattern for a portion of PCB 206, according to some embodiments. Outer pin lands 302 correspond to outer peripheral leads (e.g., 102, in FIG. 1) of leadframe 202 at interface 210. Such correspondence means that, for example, an outer pin land 302 is aligned to be electrically connected (e.g., soldered) to a corresponding outer peripheral lead. Similarly, inner pin lands 304 correspond to inner peripheral leads (e.g., 106, in FIG. 1) of leadframe 202 at interface 210. Such correspondence means that, for example, an inner pin land 304 is aligned to be electrically connected (e.g., soldered) to a corresponding inner peripheral lead.

[0031] A few example conductive traces are shown. Conductive trace 306 carries electrical signals between outer pin land 302 and leadframe 202 (and thus to/from IC die 204) or between other portions of PCB 206. Conductive trace 308 carries electrical signals between inner pin land 304 and leadframe 202 (and thus to/from IC die 204) or between other portions of PCB 206. Conductive trace 310 carries electrical signals between one portion of PCB 206 and other portions of PCB 206. An area of PCB 206 surrounding conductive traces (e.g., 306, 308, 301, etc.), outer pin lands 302, and inner pin lands 304 can be covered with a solder mask material. Solder mask (e.g., solder stop mask or solder resist) can comprise a thin lacquer-like layer of polymer applied to conductive traces of a PCB for protection against oxidation and to prevent solder bridges from forming between closely spaced solder pads or pin lands. A solder bridge is an unintended electrical connection between two conductors by means of a small blob of solder.

[0032] An increased separation (e.g., due to rounding corners of inner peripheral leads on leadframe 202) between outer peripheral leads (e.g., 102, in FIG. 1) and inner peripheral leads (e.g., 106, in FIG. 1) results in a corresponding increased separation between outer pin land 302 and inner pin land 304. Such increased separation allows conductive trace 310 to be routed between outer pin land 302 and inner pin land 304 with sufficient physical clearance to avoid an electrical short between conductive trace 310 and outer pin land 302 and/or inner pin land 304. Such increased separation also can lead to improved fabrication yields whether or not conductive traces are routed between outer pin lands 302 and inner pin lands 304. This is because increased separation tends to reduce probability of occurrence of undesirable solder

bridges between outer pin lands 302 and inner pin lands 304 during fabrication. In some implementations, conductive traces 306, 308, and 310 may have a width of about 100 microns.

[0033] FIG. 4 is top view of a QFN package 400, according to some embodiments. A top surface of QFN package 400 includes outer pads 402, inner pads 404, die paddle 406, and tie-bars 408 that mechanically and/or electrically secure and connect die paddle 406 to the leadframe of QFN package 400. The top surface of QFN package 400 also includes conductive traces 410 and a plurality of conductive contacts 412 between die paddle 406 and conductive traces 410. Conductive contacts 412 are electrically connected to particular conductive traces 410.

[0034] FIG. 5 is a close-up view of a region 414 of QFN package 400, which includes a corner 504 of QFN package 400, according to various embodiments. Outer pads 402 and inner pads 404 are labeled with number labels 502. Outer pads 402 having the labels “20” and “21” are adjacent to a corner 504 of QFN package 400. Accordingly, these outer pads 402 (and other pads 402 that are adjacent to the other three corners 504 of QFN package 400) are electrically connected to tie-bar 408. Remaining outer pads 402 and inner pads 404 are selectively connected to conductive traces 410. Arrow 506 indicates the direction toward die paddle 406. Connecting pads that are adjacent to corners 504 (e.g., such as those labeled 20 and 21) can be beneficial by increasing mechanical strength of QFN package 400, compared to unconnected pads. Another benefit is that such connections can provide increased solder joint strength (which can increase fabrication reliability).

[0035] In some embodiments, outer pads 402 individually correspond to outer peripheral leads (e.g., outer peripheral leads 102, shown in FIG. 1) on the bottom of QFN package 400, and

inner pads 404 individually correspond to inner peripheral leads (e.g., inner peripheral leads 106) also on the bottom of QFN package 400. Outer pads 402 are electrically connected to the outer peripheral leads by outer vias, and inner pads 404 are electrically connected to the inner peripheral leads by inner vias. In some implementation, corner pads of outer pads 402 that are adjacent to corners 504 of QFN package 400 are electrically interconnected with one another. For example, all the corner pads of outer pads 402 can be electrically connected to a power source or a ground. In some implementations, outer pads 402 (e.g., pads labeled 20 and 21 in FIG. 5) provide electrical grounding to die paddle 406.

[0036] FIG. 6 is a bottom view of a QFN package 600, according to some embodiments. QFN package 600 includes an outer row of outer peripheral leads 602 disposed on an outer periphery of a bottom surface of QFN package 600. QFN package 600 also includes an inner row of inner peripheral leads 604 disposed on an inner periphery of the bottom surface of QFN package 600. QFN package 600 also includes a die paddle 606 located inside the inner row of inner peripheral leads 604 on the bottom surface of QFN package 600. A plurality of conductive contacts 608 are disposed between die paddle 606 and inner peripheral leads 604. Conductive contacts 608 are electrically connected to conductors on a top surface of QFN package 600 by vias. Conductive contacts 608 comprise a plurality of conductive pads.

[0037] FIG. 7 is a top view of QFN package 600, according to some embodiments. Conductive contacts 608 shown in FIG. 6 are connected by vias (not shown) to conductive contacts 702. For example, three conductive contacts 610 shown in FIG. 6 are connected by vias to conductive contacts 704. In some implementations, more than one conductive contact can be electrically interconnected with one another as a group. For example, conductive

contacts 702 are interconnected to one another within conducting bar 706, which in turn can be connected to any of the conductive traces 708 on the top surface of QFN package 600. Top surface of QFN package 600 includes outer pads 710, inner pads 712, die paddle 714, and tie-bars 716 that mechanically and/or electrically secure and connect die paddle 714 to the leadframe of QFN package 600. Conducting bar 706 can improve power integrity and electrical performance by reducing PCB trace length, compared to a QFN package that lacks a conducting bar. In some implementations, an individual conductive contact (e.g., 608 or 704) can have a design that is the same or similar to outer pads 710 and inner pads 712, which can allow for improved SMT (surface mount technology) process design and fabrication yield rate.

[0038] FIG. 8 is a bottom view of a QFN package 800, according to some embodiments. QFN package 800 includes an outer row of outer peripheral leads 802 disposed on an outer periphery of a bottom surface of QFN package 800. QFN package 800 also includes an inner row of inner peripheral leads 804 disposed on an inner periphery of the bottom surface of QFN package 800. QFN package 800 also includes a die paddle 806 located inside the inner row of inner peripheral leads 804 on the bottom surface of QFN package 800. A plurality of conductive contacts 808 are disposed between die paddle 806 and inner peripheral leads 804. Conductive contacts 808 are electrically connected to conductors on a top surface of QFN package 800 by vias. Conductive contacts 808 comprise a plurality of conductive pads.

[0039] FIG. 9 is a top view of QFN package 800, according to some embodiments. Conductive contacts 808 shown in FIG. 8 are connected by vias (not shown) to conductive contacts 902. For example, conductive contact 810 shown in FIG. 8 is connected by vias to conductive contacts 904. In some implementations, conductive contacts 902 comprise strips

instead of pads. For example, conductive contacts 902 comprise strips within conducting bar 906, which in turn can be connected to any of the conductive traces 908 on the top surface of QFN package 800. Top surface of QFN package 900 includes outer pads 908, inner pads 910, die paddle 912, and tie-bars 714 that mechanically and/or electrically secure and connect die paddle 912 to the leadframe of QFN package 900. Embodiments shown in FIGS. 6 and 7 are similar to embodiments shown in FIGS. 8 and 9, except that conductive contacts 608 in the former embodiments comprise pads, while conductive contacts 808 in the latter embodiments comprise strips.

[0040] As used herein, the term “module” or “block” may refer to, be part of, or include an Application Specific Integrated Circuit (ASIC), an electronic circuit, a processor (shared, dedicated, or group) and/or memory (shared, dedicated, or group) that execute one or more software or firmware programs, a combinational logic circuit, and/or other suitable components that provide the described functionality.

[0041] The description incorporates use of the phrases “in an embodiment,” or “in various embodiments,” which may each refer to one or more of the same or different embodiments. Furthermore, the terms “comprising,” “including,” “having,” and the like, as used with respect to embodiments of the present disclosure, are synonymous.

[0042] Various operations may have been described as multiple discrete actions or operations in turn, in a manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations may not be performed in the order of presentation. Operations described may be performed in a different

order than the described embodiment. Various additional operations may be performed and/or described operations may be omitted in additional embodiments.

[0043] Although specific embodiments have been illustrated and described herein, it is noted that a wide variety of alternate and/or equivalent implementations may be substituted for the specific embodiment shown and described without departing from the scope of the present disclosure. The present disclosure covers all methods, apparatus, and articles of manufacture fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents. This application is intended to cover any adaptations or variations of the embodiment disclosed herein. Therefore, it is manifested and intended that the present disclosure be limited only by the claims and the equivalents thereof.

Claims

What is claimed is:

1. A Quad Flat No-Lead package comprising:

an outer row of outer peripheral leads disposed on an outer periphery of a bottom surface of the Quad Flat No-Lead package; and

an inner row of inner peripheral leads disposed on an inner periphery of the bottom surface of the Quad Flat No-Lead package,

wherein each of the inner peripheral leads has a substantially rectangular shape, and

wherein the substantially rectangular shape has two rounded corners adjacent to the outer row of outer peripheral leads.
2. The Quad Flat No-Lead package of claim 1, wherein:

each of the inner peripheral leads has a width in a direction parallel to a nearest edge of the bottom surface of the Quad Flat No-Lead package; and

the two rounded corners of the substantially rectangular shape are rounded with a radius of curvature equal to about half the width of each of the inner peripheral leads.
3. The Quad Flat No-Lead package of claim 1, wherein:

individual outer peripheral leads of the outer peripheral leads are about equidistant from two nearest inner peripheral leads of the inner peripheral leads.

4. The Quad Flat No-Lead package of claim 3, wherein:
a separation distance between the individual outer peripheral leads and the two nearest inner peripheral leads is about 0.3 millimeters.
5. The Quad Flat No-Lead package of claim 2, wherein:
a distance between two adjacent outer peripheral leads of the outer peripheral leads is about equal to the width of the inner peripheral leads.
6. The Quad Flat No-Lead package of claim 1, further comprising:
a die paddle located inside the inner periphery on the bottom surface of the Quad Flat No-Lead package; and
a plurality of conductive contacts between the die paddle and the inner periphery of the bottom surface of the Quad Flat No-Lead package, wherein the conductive contacts are electrically connected to conductors on a top surface of the Quad Flat No-Lead package by vias.
7. The Quad Flat No-Lead package of claim 6, wherein the plurality of conductive contacts comprises a plurality of conductive pads.
8. The Quad Flat No-Lead package of claim 6, wherein the plurality of conductive contacts comprises a plurality of conductive strips.

9. The Quad Flat No-Lead package of claim 1, further comprising:

a top surface including (i) outer pads individually corresponding to the outer peripheral leads of the Quad Flat No-Lead package and (ii) inner pads individually corresponding to the inner peripheral leads of the Quad Flat No-Lead package, wherein

the outer pads include corner pads that are adjacent to corners of the Quad Flat No-Lead package,

the outer pads are electrically connected to the outer peripheral leads by outer vias,

the inner pads are electrically connected to the inner peripheral leads by inner vias, and

the corner pads that are adjacent to the corners of the Quad Flat No-Lead package are electrically interconnected with one another.

10. The Quad Flat No-Lead package of claim 9, wherein all the corner pads are electrically connected to a power source or to a ground.

11. The Quad Flat No-Lead package of claim 9, further comprising:

a die paddle located inside the inner periphery of the bottom surface of the Quad Flat No-Lead package, wherein all the corner pads are electrically connected to the die paddle.

12. An integrated circuit package comprising:

a Dual Row Quad Flat No-Lead package having a top surface and a bottom surface, wherein the bottom surface of the Dual Row Quad Flat No-Lead package includes (i) an outer row of outer peripheral leads disposed on an outer periphery of the bottom surface of the Dual Row Quad Flat No-Lead package and (ii) an inner row of inner peripheral leads disposed on an inner periphery of the bottom surface of the Quad Flat No-Lead package, wherein each of the inner peripheral leads has a substantially rectangular shape, and wherein the substantially rectangular shape has two rounded corners adjacent to the outer row of outer peripheral leads; and

a printed circuit board electrically connected to the bottom surface of the Dual Row Quad Flat No-Lead package.

13. The integrated circuit package of claim 12, wherein

the printed circuit board includes (i) outer land pads individually corresponding to the outer peripheral leads of the Dual Row Quad Flat No-Lead package and (ii) inner land pads individually corresponding to the inner peripheral leads of the Dual Row Quad Flat No-Lead package,

the outer land pads are electrically connected to the outer peripheral leads and the inner land pads are electrically connected to the inner peripheral leads, and

one or more conductive traces on the printed circuit board follow a path between two adjacent inner land pads.

14. The integrated circuit package of claim 13, wherein the one or more conductive traces on the printed circuit board follow a path between an outer land pad and an adjacent inner land pad.

15. The integrated circuit package of claim 12, wherein:
each of the inner peripheral leads has a width in a direction parallel to a nearest edge of the bottom surface of the Dual Row Quad Flat No-Lead package; and
the two rounded corners of the substantially rectangular shape are rounded with a radius of curvature equal to about half the width of each of the inner peripheral leads.

16. The integrated circuit package of claim 12, further comprising:
a die paddle located inside the inner periphery of the bottom surface of the Quad Flat No-Lead package; and
a plurality of conductive contacts between the die paddle and the inner periphery of the bottom surface of the Quad Flat No-Lead package, wherein the conductive contacts are electrically connected to conductors on a top surface of the Quad Flat No-Lead package by vias.

17. The integrated circuit package of claim 16, wherein the plurality of conductive contacts comprises a plurality of conductive pads.

18. The integrated circuit package of claim 16, wherein the plurality of conductive contacts comprises a plurality of conductive strips.

19. The integrated circuit package of claim 12, further comprising:

a top surface including (i) outer pads individually corresponding to the outer peripheral leads of the Quad Flat No-Lead package and (ii) inner pads individually corresponding to the inner peripheral leads of the Quad Flat No-Lead package, wherein

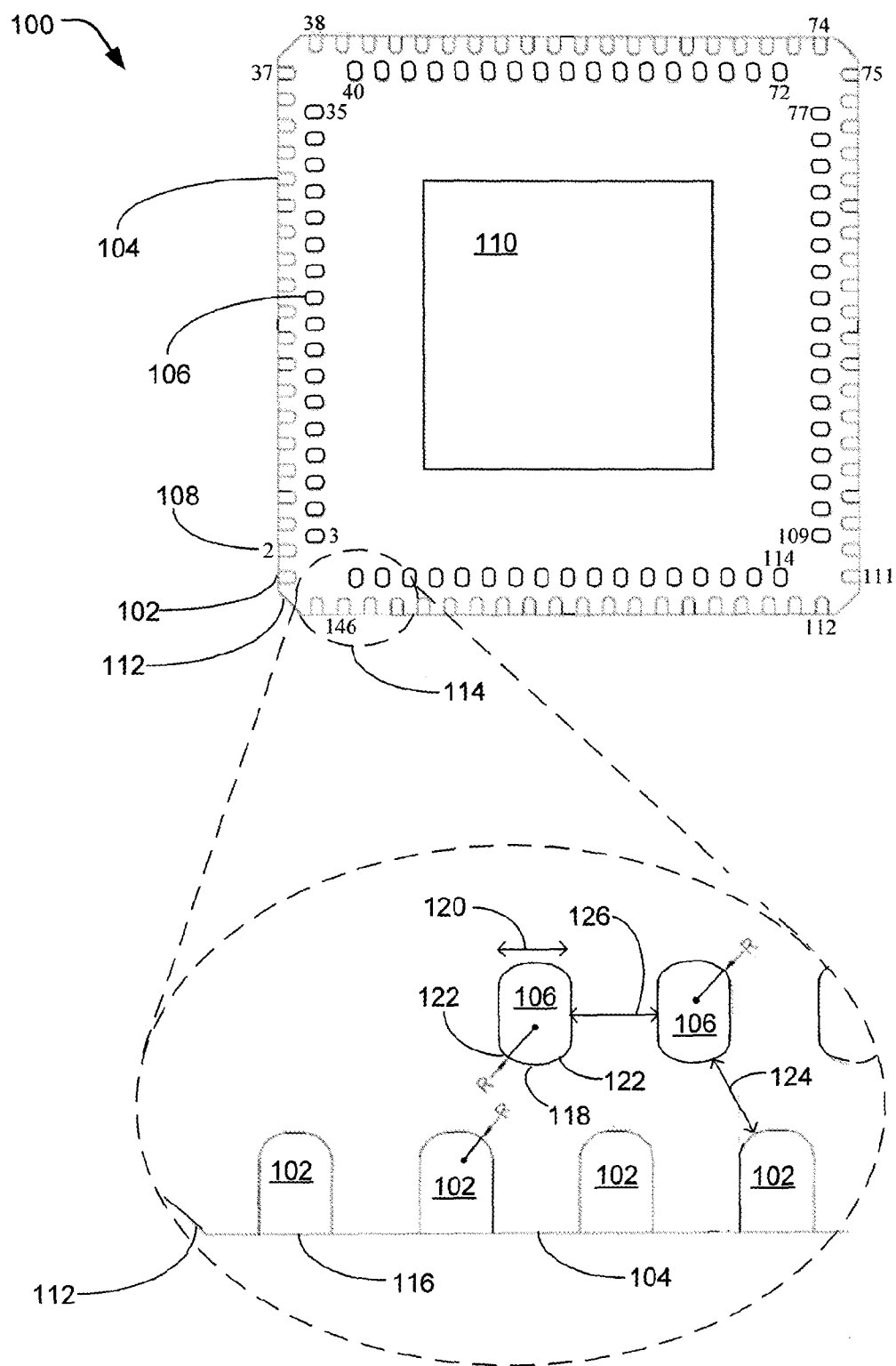
the outer pads include corner pads that are adjacent to corners of the Quad Flat No-Lead package,

the outer pads are electrically connected to the outer peripheral leads by outer vias,

the inner pads are electrically connected to the inner peripheral leads by inner vias, and

the corner pads that are adjacent to the corners of the Quad Flat No-Lead package are electrically interconnected with one another.

20. The integrated circuit package of claim 19, wherein all the corner pads are electrically connected to a power source or a ground.



2/5

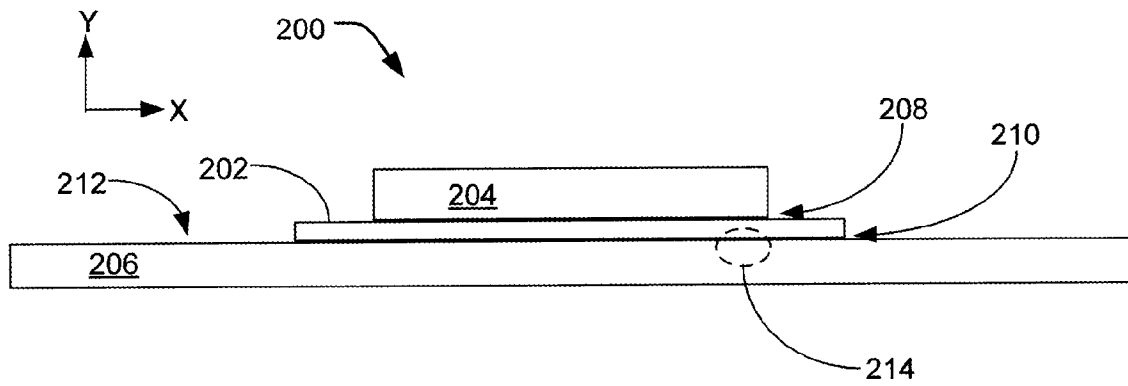


FIG. 2

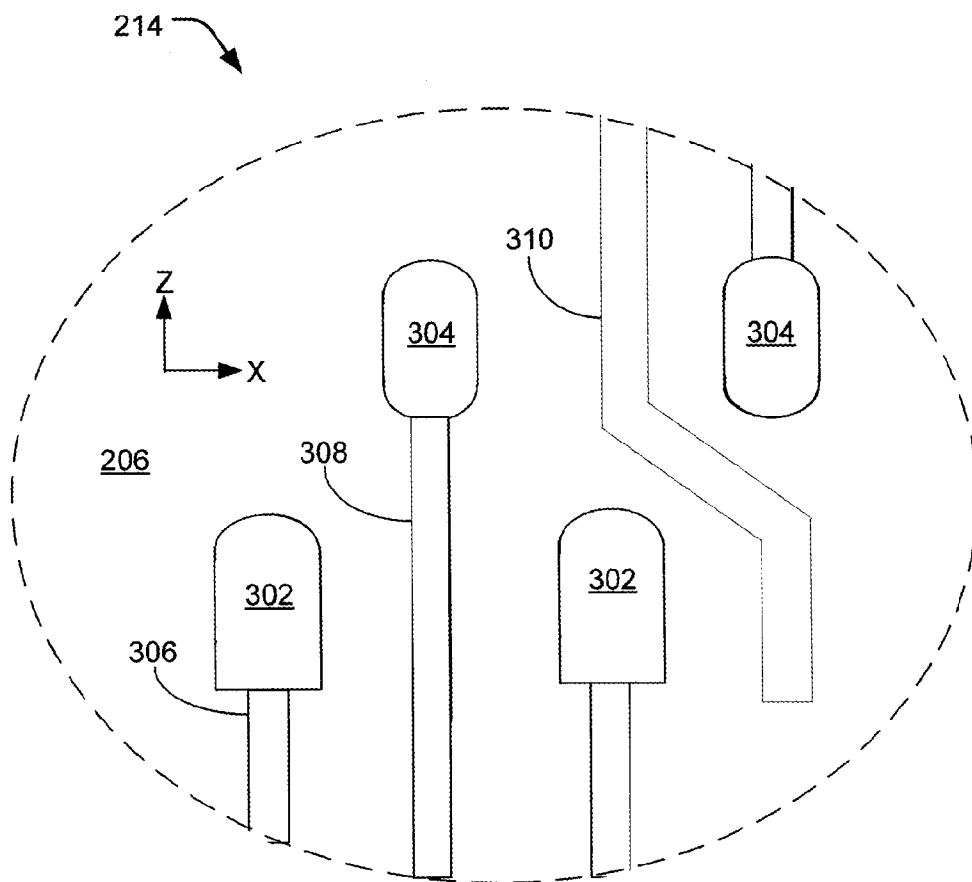


FIG. 3

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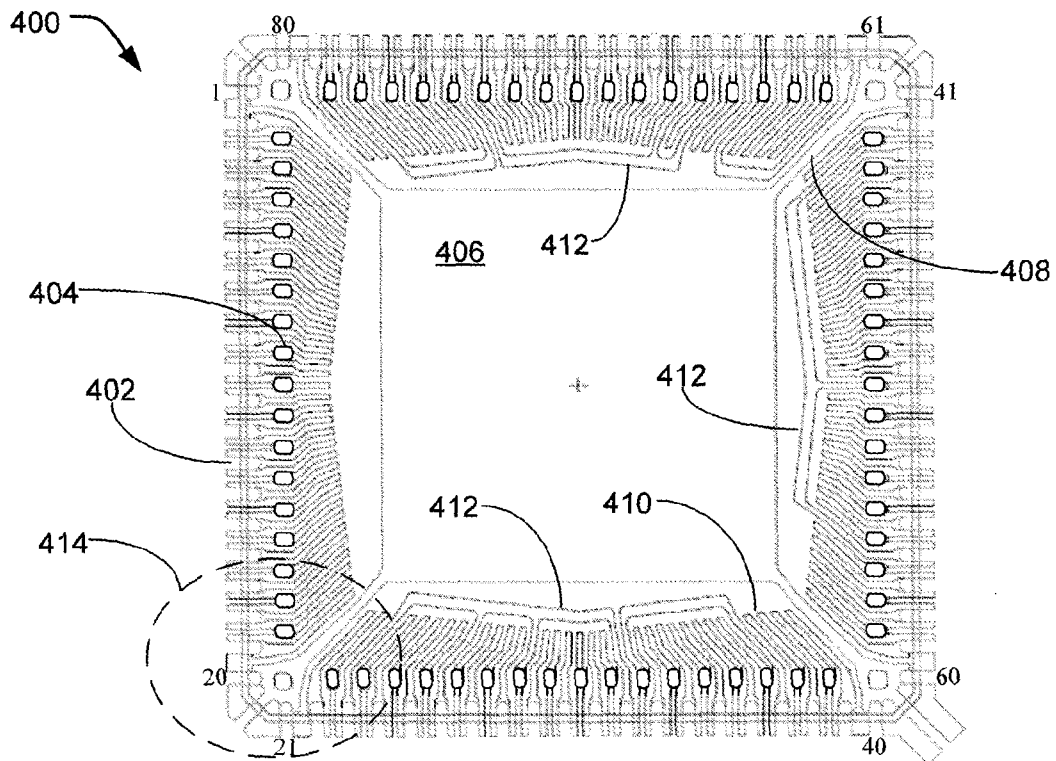


FIG. 4

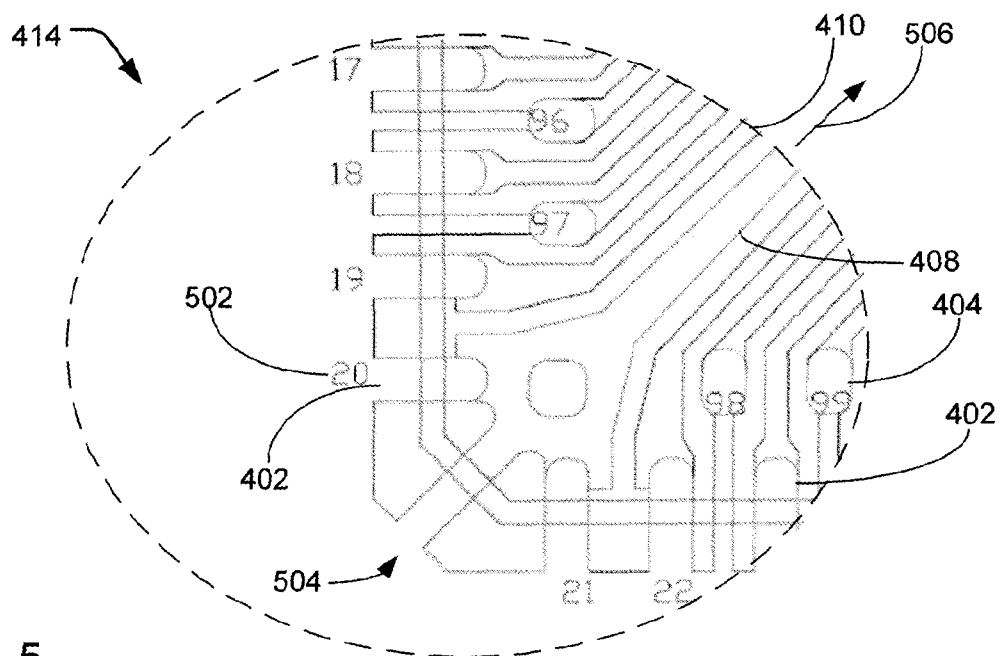


FIG. 5

4/5

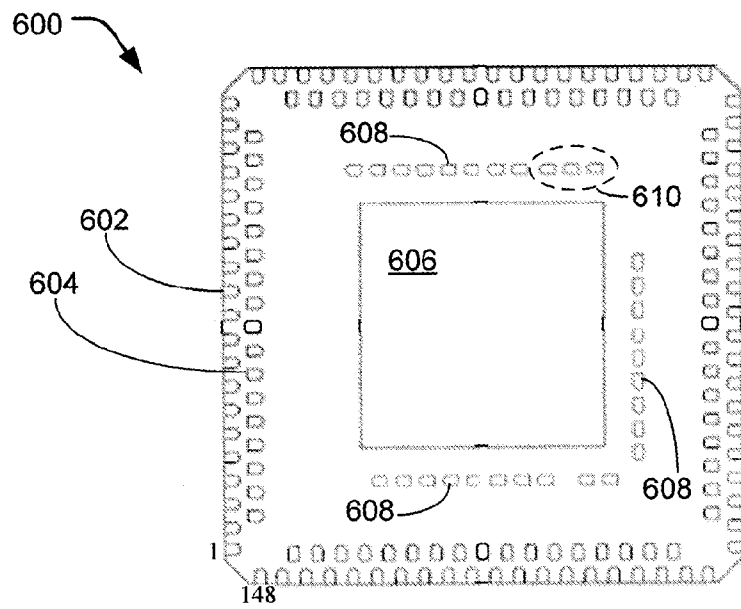


FIG. 6

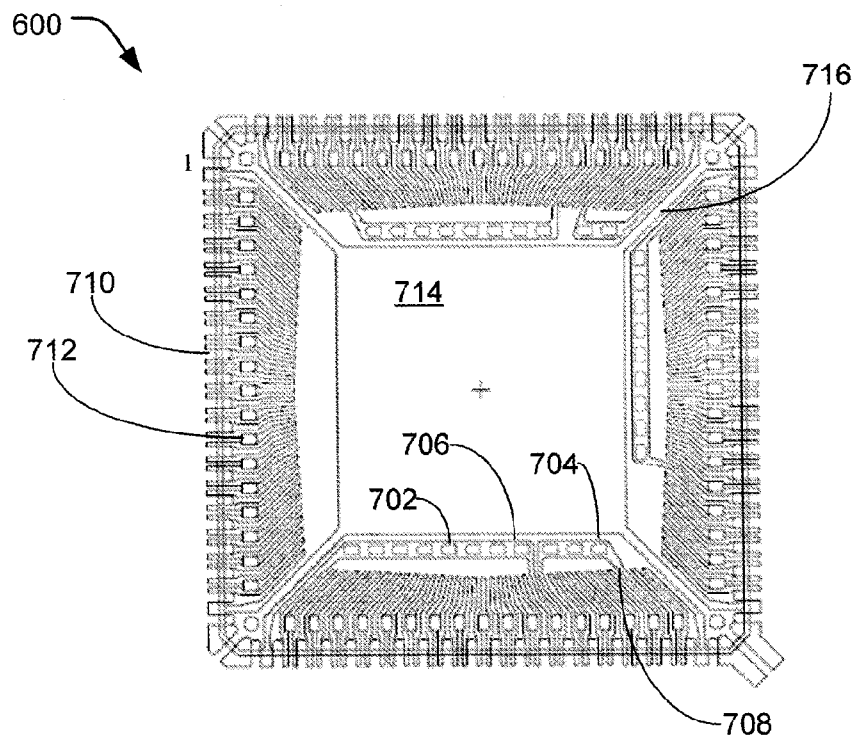


FIG. 7

5/5

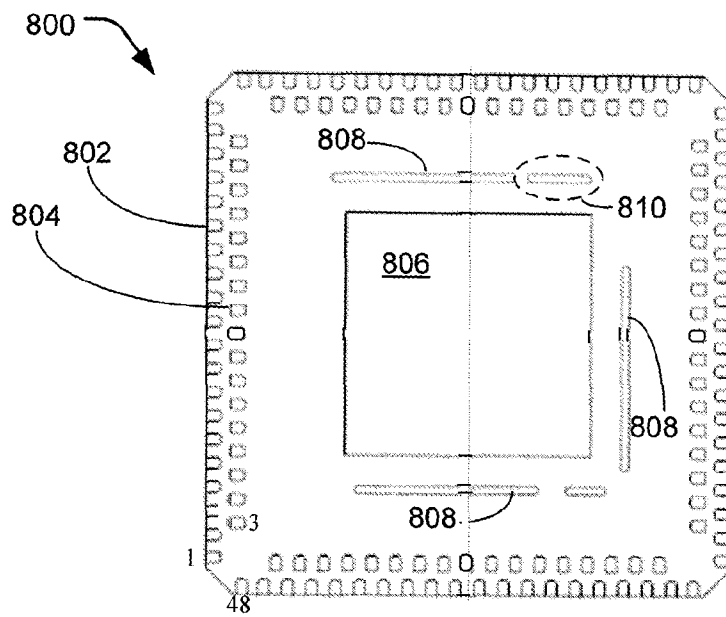


FIG. 8

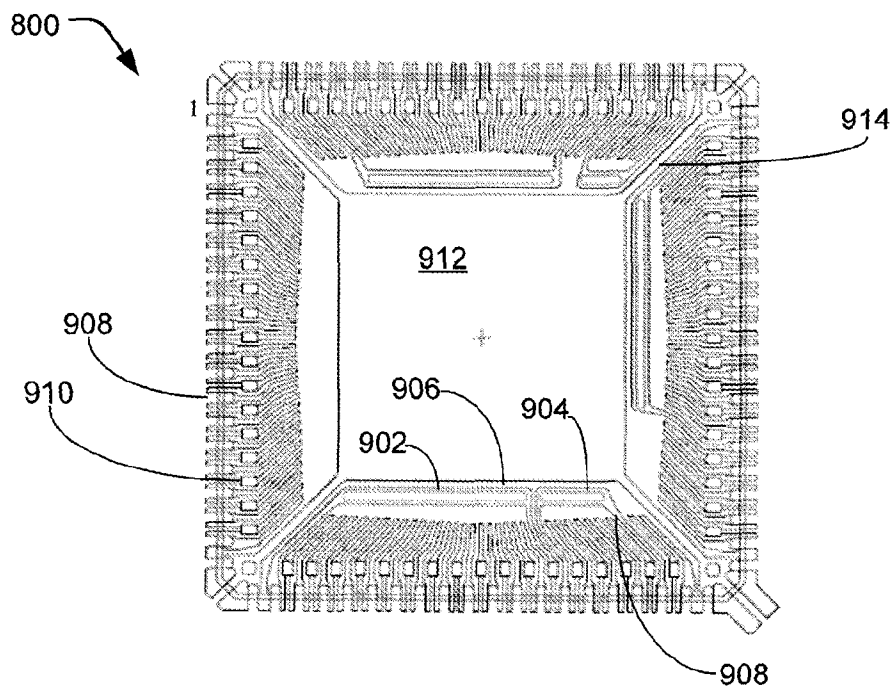


FIG. 9

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/059262

A. CLASSIFICATION OF SUBJECT MATTER INV. H01L23/495 ADD. H01L23/31		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) H01L		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-Internal		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2003/178723 A1 (ITO FUJIO [JP] ET AL) 25 September 2003 (2003-09-25) paragraphs [0055] - [0061], [0085], [0086], [0097]; figures 2,3 -----	1-5, 12-15
X	US 2003/168719 A1 (CHENG MAN HON [HK] ET AL) 11 September 2003 (2003-09-11) paragraphs [0033], [0034], [0036], [0038]; figures 6,9,10 -----	1-3,6-8, 11-18
X	US 2005/248041 A1 (KUAH TENG H [SG] ET AL) 10 November 2005 (2005-11-10) paragraphs [0021] - [0023]; figures 1,2 -----	1,3,5,12
X	US 2012/146203 A1 (CAMACHO ZIGMUND RAMIREZ [SG] ET AL) 14 June 2012 (2012-06-14) paragraphs [0035] - [0047]; figures 1,2 ----- -/--	1,12
☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents : "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 2 December 2013	Date of mailing of the international search report 13/12/2013	
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Zeisler, Peter	

INTERNATIONAL SEARCH REPORT

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
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